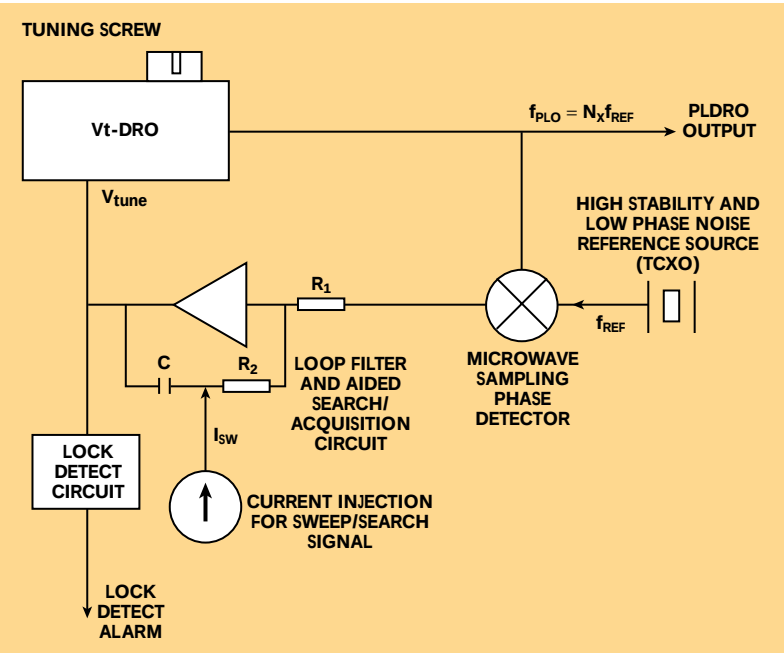
UNDERSTANDING PHASE-LOCKED DRO DESIGN ASPECTS

Phase-locked dielectric resonator oscillators (DRO) are essential components in high frequency microwave links where phase noise is a crucial parameter. The main advantage of a phase-locked DRO (PLDRO) source over an ordinary synthesizer is its phase noise characteristic. This is due to the voltage-tuned DRO's (Vt-DRO) high quality factor tank circuit (a dielectric resonator) on one hand, and direct locking to a high frequency reference harmonic by means of a microwave sampling phase detector (SPD) on the other. In this way, the noise floor contribution of prescalers and frequency dividers used in an ordinary synthesized frequency generator is avoided within the loop band. In addition, the free-running phase noise characteristic of the Vt-DRO gives the advantage of low phase noise performance outside the loop bandwidth at high offset frequencies. This characteristic is most evident with GaAsFET DROs, where the free-running phase noise spectrum rolls off at a –30 dB per decade rate. Furthermore, the possibility of wideband phase locking of the Vt-DRO provides good short-term stability (for instance, low microphonicity) for this frequency source. However, unlike a standard synthesizer, a PLDRO requires a special frequency acquisition and locking technique for correct and reliable operation. In this article, phase noise considerations, a loop optimization procedure and a specific acquisition technique for PLDROs are explained.

Fig. 1 The PLDRO block diagram concept.



ACQUISITION CIRCUIT REQUIREMENTS

Sweeping Range Considerations

Frequency acquisition can be accomplished by sweeping the Vt-DRO, as shown in the block diagram in ***Figure 1***. The SPD driven by the reference signal generates a comb-like spectrum. At the instant the Vt-DRO frequency coincides with the reference signal's desired harmonic, the loop will acquire a stable lock and will remained locked as long as the search signal is not too fast or large. The

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frequency spacing between each comb harmonic is equal to the temperature-compensated crystal oscillator's (TCXO) frequency as defined in

$$f(n) = f(TCXO) \bullet n \bullet \delta(n - N) \quad (1)$$

$$f(TCXO) = f(TCXO) \bullet \{n \bullet \delta(n - N) - [(n - 1) \bullet \delta([n - 1] - [N - 1])\} \quad (2)$$

Hence, to prevent false lock on an undesired comb harmonic, the tuning range Δf of the Vt-DRO should satisfy the condition

$$\Delta f < 2 \bullet f(TCXO) \quad (3)$$

For a symmetrical search, the optimum V_{tune} value of the Vt-DRO (that is, the value at which the desired phase-locked oscillator frequency is reached) should be half of the control voltage swing range (for instance, 1/2 V_{cc}, where V_{cc} is the supply voltage to the active loop filter). This value can be easily obtained by mechanically tuning the Vt-DRO tuning screw. In the same way, the search signal voltage should be properly offset (through a suitable bias voltage at the acquisition and lock circuitry) by a value equal to the same optimum V_{tune}. It is also important to use a sufficiently high frequency reference signal so that the sweep can be made wide enough to cover the temperature drifts of the Vt-DRO.

Frequency Acquisition

The sweep can be applied as an up-down ramp voltage directly to the Vt-DRO tuning input. For a perfect second-order loop with active integrator, a constant current I_{sw} is inserted to create a triangle sweep voltage with switching polarities. Such a triangle sweep signal is due to tracking considerations.

The steady-state phase error $\theta_e = \theta_i - \theta_o$ after all transient effects have terminated ($t \to \infty$) is given by

$$\theta_e(s) = \frac{s\theta_i(s)}{s + K_V K_d H(s)} \quad (4)$$

where

K_V = Vt-DRO modulation sensitivity (in radians/second per volt)

K_d = sampling phase detector output sensitivity (in volts per radian)

$H(s)$ = loop filter transfer function

In the case of a second-order PLL with an active loop filter, $H(s)$ is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1 + s\tau_1}{s\tau_2} \quad (5)$$

where

$$\tau_1 = R_1 C \quad (6)$$

$$\tau_2 = R_2 C \quad (7)$$

Substituting these expressions into Equation 4 and using the LaPlace final value theorem produces

$$\theta_e(s) = \frac{s^2\theta_i(s)}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (8)$$

where the natural loop frequency ω_n and the loop damping factor ξ are given by

$$\omega_n = \sqrt{\frac{K_V K_d}{\tau_1}} \quad (9)$$

$$\xi = \frac{\omega_n \tau_2}{2} \quad (10)$$

Now suppose that the input frequency is linearly changing with time at the rate of $\Delta\dot{\omega}$ rad/sec^2 such that

$$\theta_i = \int\int \omega dt \Rightarrow \theta_i(t) = \frac{1}{2}\Delta\dot{\omega}t^2 \quad (11)$$

Hence, $\theta(s)$ is given by the relevant LaPlace transform

$$\theta_i(s) = \frac{\Delta\dot{\omega}}{s^3} \quad (12)$$

Substituting Equation 12 into Equation 8 using the final value theorem yields the steady-state phase error accumulated during a linear frequency sweep

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s \frac{s^2 \frac{\Delta\dot{\omega}}{s^3}}{s^2 + 2\xi\omega_n s + \omega_n^2} \Rightarrow \theta_e(t) = \frac{\Delta\dot{\omega}}{\omega_n^2}\text{rad} \quad (13)$$

(also called dynamic tracking error). Such input behavior might arise from accelerated motion between a transmitter and receiver, Doppler frequency shift or frequency sweep modulation, which is the case here.

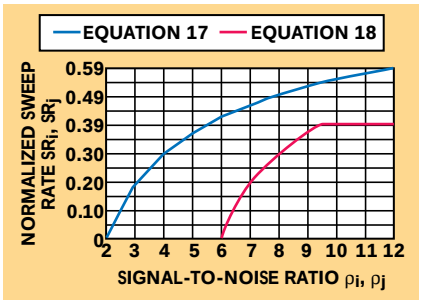


Fig. 2 Normalized sweep rate as a function of SNR_L.

For a sinusoidal characteristic phase detector, this expression is

$$\sin\theta_e = \frac{\Delta\dot{\omega}}{\omega_n^2} \quad (14)$$

Note that the sinus function cannot exceed ±1. Thus, the maximum permitted sweep rate limit is given by

$$\Delta\dot{\omega} = \omega_n^2 \Rightarrow \Delta\dot{\omega} < \omega_n^2 \quad (15)$$

However, this condition is not satisfactory; Viterbi discovered that acquisition is not certain even if the loop is noise free, and there is a possibility for acquisition only if

$$\Delta\dot{\omega} < \frac{\omega_n^2}{2}$$

Otherwise, it will not be locked.

Frazier and Page provided empirical data that indicate the sweep rate should satisfy a particular condition for acquisition in the presence of noise. Gardner's experience added some changes, resulting in

$$\Delta\dot{\omega} < \frac{1}{2}\omega_n^2\left[\frac{1 - 2}{\sqrt{SNR_L}}\right] \quad (16)$$

In this case, $0.707 \le \xi \le 1$ and the loop signal-to-noise ratio (SNR_L) is less than 6 dB.

Two other experimental formulas were suggested by Frazier and Page.

$$\left.\frac{\Delta\dot{\omega}}{\omega_N^2}\right|_{90\%} \approx 1 - \sqrt{\frac{2}{\rho}} \quad \forall \quad \xi > 0.707 \quad (17)$$

for 90 percent acquisition probability, while ρ represents SNR_L. In most cases, a probability of 0.9 is too low. For a better design where $E(B_L T_S) = 10^4$ cycle slips, the normalized sweep rate is given by

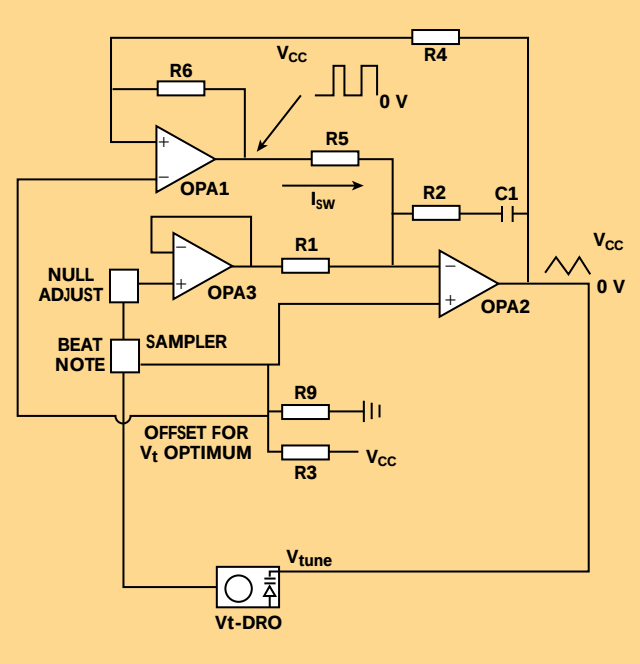


Fig. 3 The aided search/acquisition circuit.

$$\frac{\dot{\Delta\omega}}{\omega_n^2} = \left\{1 - \left(\frac{2}{\rho - 4}\right)^{1/2} \quad 6 < \rho < 9.5 \;\middle|\; 0.4 \quad \rho > 9.5\right\} \qquad (18)$$

Figure 2 shows the normalized sweeping rate as a function of loop SNR_L.

Sweeping and Locking

The PLDRO search and locking circuit, shown in ***Figure 3***, consists of two feedback paths: a negative feedback path, which is the locking circuit (OPA2-loop filter OPA3 high input impedance buffer), and a sweeping circuit for aided acquisition as the positive feedback (OPA1-Schmitt trigger comparator, OPA2-integrator). A better understanding of this circuit is possible by referring to it as a triangle wave generator circuit. Hence, the second-order loop design formulas together with the triangle generator design formulas are applicable.

Suppose that in the moment $t_0 = 0$ the output of OPA1 is V_{cc} while OPA1 is in its positive saturation (OPA1 is a comparator). Hence, the current to the invert input of OPA2 is

$$I_{SW} = \frac{V_{CC} - V_{offset}}{R_5} \qquad (19)$$

(This offset voltage has several names and meanings, for example, $V_{offset} = V_{tune\text{-}locking} = V_{bias}$.)

The constant positive current in Equation 19 will cause a negative-going liner voltage ramp at the output of OPA2 due to the charge of C_1. At that time (using superposition) the voltage at the noninverting input of the comparator OPA1 is given by

$$V(t)_{OPA1+} = \frac{V_{CC}R_4}{R_6 + R_4} + \frac{V_O(t)_{OPA2}R_6}{R_6 + R_4} \qquad (20)$$

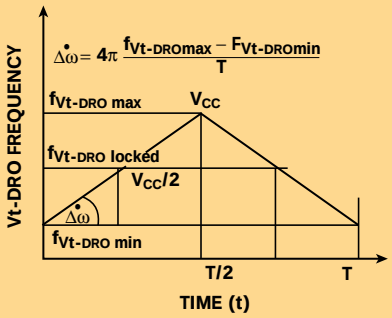


Fig. 4 The triangle sweep signal.

where

$V_o(t)_{OPA2}$ = the output voltage from OPA2 at a given time t

When, during the negative-going ramp of OPA2, the voltage $V(t)_{OPA1+}$ at the comparator noninverting input becomes smaller than V_{ref} at the comparator OPA1 inverting input, its output switches to 0 V. At that moment the current to the inverting input of the integrator OPA2 becomes

$$I_{SW} = \frac{-V_{offset}}{R_5} \qquad (21)$$

Since V_{offset} was chosen to be 1/2 V_{cc}, the current changes its sign and the capacitor C is discharged. When the voltage $V(t)_{OPA1+}$ reaches a higher value than V_{ref}, the charge of C_1 will begin and vice versa. ***Figure 4*** shows the triangle sweep signal generated by this circuit. The sweep rate $\dot{\Delta\omega}$ is defined by the triangle signal slope. Thus, the triangle frequency is one-half the sweep rate.

The next objective is to calculate the sweep frequency from the circuit parameters. The current I_{SW} through R_5 is equal to the charging current of C_1 and is related to the voltage $V_c(t)$ across the capacitor C_1 by

$$\frac{V_{CC} - V_{offset}}{R_5} = -\frac{dV_{C1}(t)}{dt}C_1 \qquad (22)$$

On the other hand,

$$V_{offset} - \frac{dV_{C1}(t)}{dt}C_1R_2 - V_{C1}(t) = V_O(t)_{OPA2} \qquad (23)$$

Since V_{CC} and V_{offset} are constants, the charge is linear as already observed. Substituting Equation 22 into Equation 23 and deriving it by t yields, as expected,

$$\frac{dV_O(t)_{OPA2}}{dt} = -\frac{dV_{C1}}{dt} \qquad (24)$$

Hence, the charging equation (after substituting Equation 24 into Equation 22 and integrating the result) is

$$V_O(t)_{OPA2} = \frac{V_{CC} - V_{offset}}{R_5C_1}\int_{t_0}^{t_1} dt \qquad (25)$$

The result is a linear ramp that creates the triangle wave described by

$$V_O(t)_{OPA2} = \frac{1}{R_5C_1}\left(V_{CC} - V_{offset}\right)\left(t_1 - t_0\right) + V_0(0) \quad (26)$$

To calculate T/2, which is half of the triangle duration, there is a need to calculate the charging time until the voltage at the noninverting input of the comparator OPA1 reaches the reference voltage value applied at the inverting input of the same operational amplifier. This equation is expressed as

$$V(t)_{OPA1-} = V_{ref} = \frac{V_{CC}R_4}{R_6 + R_4} + \frac{V_O(t)_{OPA2}R_6}{R_6 + R_4} \quad (27)$$

Thus,

$$V_O(t)_{OPA2} = \frac{R_6 + R_4}{R_6}\left(V_{ref} - \frac{V_{CC}R_4}{R_6 + R_4}\right) \quad (28)$$

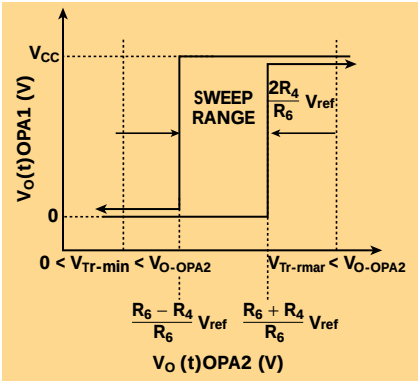


Fig. 5 The OPA1 comparator's hysteresis.

Combining Equation 26 with Equation 28 and writing the expression $(t_1 - t_0)$ as ΔT and assuming $V_O(0) = 0$ results in

$$\Delta T = \left(V_{ref} - \frac{V_{CC}R_4}{R_6 + R_4}\right) \bullet \left(\frac{R_6 + R_4}{R_6}\right)\frac{R_5C_1}{V_{CC} - V_{ref}} \quad (29)$$

Therefore, the triangle frequency is given by

$$f = \frac{1}{2\Delta T} \quad (30)$$

Bearing in mind that optimum V_{tune} for locking is $V_{CC}/2$ and that $V_{ref} = V_{CC}/2$ since a symmetrical sweep is required, Equation 29 can be simplified so the triangle frequency is given by

$$f = \frac{R_6}{2\left(R_6 - R_4\right)R_5C_1} \quad (31)$$

In some cases the sweep circuit may not operate due to improper design of the comparator's OPA1 hysteresys. The hysteresis plot, generated using superposition calculation, is shown in ***Figure 5***.

When the loop is locked the signal voltage coming from the sampling phase detector is at its maximum value. The current through R_4 is higher than the current through R_5 and, hence, the negative feedback becomes dominant. However, when the loop is out of lock, the sampler output voltage drops. The current through R_5 generated by the Schmitt trigger OPA1 becomes dominant and a new search triangle signal begins until the loop acquires lock. When the loop is locked the negative feedback becomes dominant, the positive feedback path is suppressed and the triangle sweep wave is stopped. This description demonstrates how a control system automatically operates its positive feedback to bring the system to a stable point where the negative feedback suppresses the positive feedback, stabilizing the system.

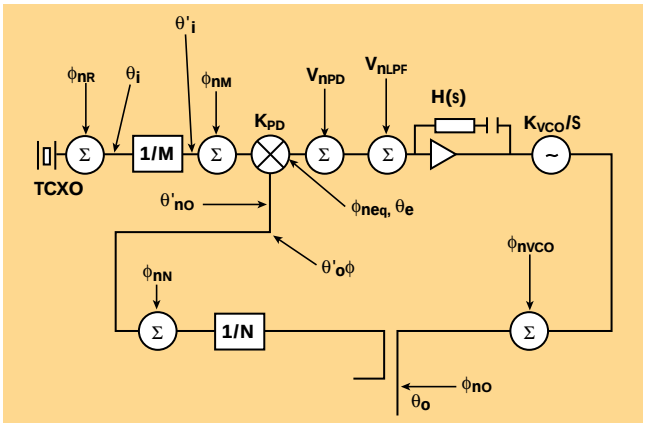


Fig. 6 Noise generators within a synthesizer.

PHASE NOISE

Phase noise at the output of a phase-locked loop (PLL) can be calculated as a root mean square summation of all the noise generators' variances. The noise generators considered here are the phase detector, VCO prescalers and dividers (if any), loop filter (operational amplifier), reference dividers or step recovery diode (SRD) that drive the microwave sampler in the case of PLDROs, VCOs and TCXOs.

The noise contributions injected into a PLL are shown in ***Figure 6***. For convenience, these noise term variances (rms values) in V/√Hz have been indicated as

ϕ_{nR} = reference TCXO phase noise
ϕ_{nM} = reference divider or SRD phase noise
ϕ_{nO} = total output phase noise
ϕ_{nN} = emitter-coupled logic (ECL) divider phase noise
ϕ_{NVCO} = VCO phase noise variance
V_{nD} = phase detector phase noise
V_{nLPF} = loop amplifier phase noise

The objective now is to determine the phase noise transmission function for each noise generator. Using control theory notation, the applicable noise equations are

$$\phi_{ni} = \frac{\phi_{nR}}{M} + \phi_{nM} \quad (32)$$

$$\phi_{neq} = \left(\phi_{ni} - \phi'_{nO}\right)K_{PD} \quad (33)$$

$$\left[\left(\phi_{neq} + V_{PD} + V_{nLPF}\right)H(s)\right]\frac{K_{VCO}}{s} + \phi_{nVCO} = \phi_{nO} \quad (34)$$

$$\phi'_{nO} = \frac{\phi_{nO}}{N} + \phi_{nN} \quad (35)$$

where

K_{VCO} = Vt-DRO modulation sensitivity (in radians/second per volt)
K_{PD} = phase detector or sampling phase detector output sensitivity (in volts per radian)
H(s) = loop filter transfer function
N = prescaler (and VCO frequency divider) ratio
M = reference divider ratio

After some manipulations, the expression becomes

$$\phi_{nO} = \left\{\left\{\left[\left(\frac{\phi_{nR}}{M} + \phi_{nM}\right) - \left(\frac{\phi_{nO}}{N} + \phi_{nN}\right)\right] \bullet K_{PD} + V_{nPD} + V_{nLPF}\right\} H(s)\right\} \bullet \frac{K_{VCO}}{s} + \phi_{nVCO} \quad (36)$$

Rearranging the variables in a way that ϕ_{nO} is the subject of the formula, the PLL phase noise at its output becomes

$$\phi_{nO} = \left[\frac{\phi_{nR}}{M} + \phi_{nM} - \phi_{nN}\right] \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} + \left[V_{nPD} + V_{nLPF}\right] \bullet \frac{\left[\frac{H(s)K_{VCO}}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} + \phi_{nVCO} \frac{1}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \quad (37)$$

This result is interesting because it gives the transfer function for each noise generator within the loop referred to the output. Furthermore, it can be easily investigated for phase noise optimization.

Since each noise term is uncorrelated, the phase noise power spectral density may be obtained from Equation 37 by mean square addition of the individual sources. The first expression of this formula should be changed in sign from $\phi_{nM} - \phi_{nN}$ to $\phi_{nM} + \phi_{nN}$ since these variances are not correlated.

Reference Source Noise Contribution

The TCXO output phase noise contribution to the output phase noise is given by

$$\sigma_{nTCXO} = \frac{\phi_{nR}}{M} \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \quad (38)$$

Assuming that H(s) describes an active filter, using Equations 5, 6, 7, 9 and 10 transforms Equation 38 into

$$\sigma_{nTCXO} = \frac{\phi_{nR}}{M} \bullet \frac{2\xi\omega_n S + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (39)$$

Equation 39 shows that the reference source (TCXO) phase noise within the loop is multiplied by the closed-loop lowpass transmission function with a –20 dB per decade slope, and will be attenuated outside the loop. Hence, the closed-loop sharpness defines the amount of the TCXO phase noise that is enhanced outside the loop bandwidth. For this reason, the damping factor ξ of the loop has a significant impact on the phase noise characteristic outside the loop bandwidth. This same conclusion also holds for the reference dividers or SRD, prescalers, loop amplifier and phase detector.

Well inside the loop bandwidth (where the loop gain is high — $K_{PD}K_{VCO}H(s) \rightarrow \infty$), the output phase noise standard due to the TCXO can be approximated as

$$\sigma_{nTCXO} = \frac{N}{M}\phi_{nR} \quad (40)$$

where

N = divider and prescaler ratio
M = reference divider ratio

In the actual case of a PLDRO, N = 1 and M = $1/M_{SRD}$, where M_{SRD} is the order of the reference frequency harmonic at which the Vt-DRO is locked. Thus, for a PLDRO it holds that

$$\sigma_{nTCXO} = M_{SRD}\phi_{nR} \quad (41)$$

Frequency Divider Noise Contribution

The 1/N and 1/M frequency dividers' contribution to the output phase noise is given by a similar expression that is almost identical (lowpass filtering action), such that

$$\sigma_{nN} = \phi_{nN} \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \quad (42)$$

$$\sigma_{nM} = \phi_{nM} \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \quad (43)$$

Like before, when the loop gain is high, the frequency dividers' noise contributions at the loop output are given by

$$\sigma_{nN} = N\phi_{nN}$$
$$\sigma_{nM} = N\phi_{nM} \quad (44)$$

As already discussed, in the PLDRO, N = 1 and ϕNr = 0 (no VCO dividers are used). Thus, the noise term that remains is the SRD contribution $\sigma_{nM} = \phi_{nM}$. As a result, the PLDRO has the benefit of a lower noise floor within the loop compared to the usual PLLs.

Phase Detector Noise Contribution

By changing the notation of the phase detector expression in Equation 37, the phase detector noise contribution can be written as

$$\sigma_{nPD} = \frac{V_{nPD}}{K_{PD}} \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1 + \frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \quad (45)$$

Again, this expression is a lowpass function as seen previously. In the same way, inside the loop band (where the loop gain is high) the phase detector rms noise contribution at the PLL output is expressed as

$$\sigma_{nPD} = V_{nPD}\frac{N}{K_{PD}} \tag{46}$$

In the case of a PLDRO, N = 1 (no VCO divider is used) — another reason why the noise floor within the loop is much lower compared to a classical synthesizer. Additionally (both in a PLDRO and synthesizer), a higher phase detector gain will reduce the noise floor within the loop bandwidth. In the case of a PLDRO, a higher phase detector gain means that a higher beat note output is required from the microwave sampler. The disadvantage is that the sampler must be driven with a higher power signal at microwave frequencies. In an ordinary charge-pump synthesizer, this increase of phase detector gain will usually affect the level of spurious signals around the output carrier.

Loop Amplifier Noise Contribution

In the same manner, the loop amplifier noise contribution is expressed as

$$\sigma_{nLPF} = \frac{V_{nLPF}}{K_{PD}} \bullet \frac{\left[\frac{K_{PD}K_{VCO}H(s)}{s}\right]}{\left[1+\frac{K_{PD}K_{VCO}H(s)}{Ns}\right]} \tag{47}$$

As explained previously, inside the loop band (where the loop gain is high), the loop active filter rms noise contribution at the PLL output is given by

$$\sigma_{nLPF} = V_{nLPF}\frac{N}{K_{PD}} \tag{48}$$

Again, a high phase detector gain will improve the phase noise characteristic within the loop bandwidth.

VCO Phase Noise Contribution

The VCO phase noise transfer function is given by

$$\sigma_{nVCO} = \phi_{nVCO} \bullet \frac{1}{1+\frac{K_{PD}K_{VCO}H(s)}{Ns}} \tag{49}$$

Replacing H(s) as in Equation 5 produces

$$\sigma_{nVCO} = \phi_{nVCO}\frac{s^2}{s^2+2\xi\omega_n s+\omega_n^2} \tag{50}$$

This expression describes a highpass filter (HPF) characteristic with a 40 dB per decade slope, which means that the phase noise generated by the VCO (or Vt-DRO) is strongly attenuated within the loop limits. At higher offset frequencies (far from the carrier) where there is no more feedback action, the output phase noise becomes equal to the free-running phase noise of the VCO or Vt-DRO alone. Hence, the best phase noise limit of a synthesizer or PLDRO is defined by the free-running VCO or Vt-DRO phase noise characteristic.

General Considerations

It can be demonstrated that the optimum choice for the loop bandwidth (that is, the one that minimizes the output phase noise variance) is the frequency at which the phase noise of the free-running VCO coincides with the total noise floor coming from the reference and phase detector side. In the transition region close to the loop corner frequency, the output phase noise can become higher than the free-running VCO noise. In fact, since the HPF function is given by HPF(s) = 1 – LPF(s) where LPF(s) is the closed-loop transfer function, the optimization of in-band phase noise will affect the out-of-band phase noise and vice versa. For example, a sharp lowpass filter (LPF) function means a sharp HPF function and better suppression of the VCO or Vt-DRO noise inside the loop frequency limits. Of course, this condition will require a high damping factor ξ and higher overshoot of the transfer function with subsequent increase of the phase noise in that offset frequency range.

With the previously described method, each phase noise contribution can be calculated separately by using an appropriate CAD method. The total output phase noise then can be obtained using the root mean square notation:

$$\sigma = \sqrt{\sigma_{nPD}^2+\sigma_{nTCXO}^2+\sigma_{nN}^2+\sigma_{nM}^2+\sigma_{nVCO}^2+\sigma_{nLPF}^2} \tag{51}$$

This frequency-dependent function gives the overall phase noise spectrum log.

Since the noise generators' contributions are expressed in rms terms, each contribution X can be expressed in logarithmic units by calculating 20logX. For example, considering the phase detector noise expressed by Equation 46 yields

$$\sigma_{nPD} = 20\log V_{nP} + 20\log\frac{N}{K_{PD}} \tag{52}$$

In this manner, so-called single-sideband phase noise can be obtained in dBc/Hz just as it would be displayed by a spectrum analyzer. (Note that the parameter $20\log V_{nPD}$ should be given by the manufacturer of the device or can be evaluated.) The overall phase noise (PN) within the loop bandwidth or outside the loop bandwidth in dBc/Hz notation is given by

$$PN(dBc/Hz) = 20\log\sigma \tag{53}$$

LOOP FILTER AND ACQUISITION CIRCUIT OPTIMIZATION

Design Procedure

The loop filter is a second-order integrator with optimized ω_{3dB} to obtain good phase noise matching between the loop noise floor and free-running Vt-DRO phase noise. Following the PLDRO design steps, the ω_{3dB} of the loop (and the damping factor ξ) is defined considering phase noise requirements. Next, the SPD beat note peak-to-peak output voltage V_{BN} is measured (or determined from the data sheet) and K_{PD} of the SPD is calculated using

$$K_{PD} = \frac{V_{BN}}{2}$$

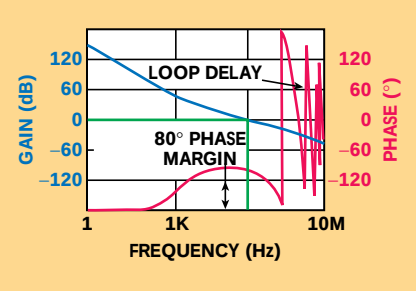
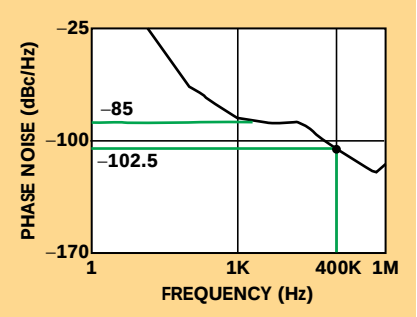


Fig. 7 Phase and gain margin.

Fig. 8 Phase noise simulation.



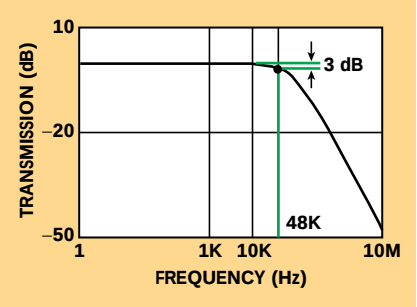
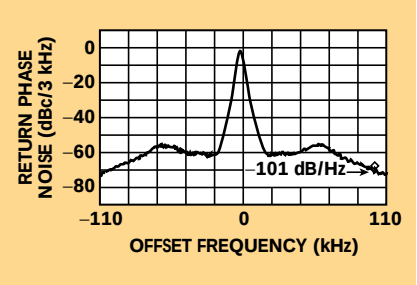


Fig. 9 The closed-loop transmission function.

Fig. 10 Phase noise at 11.3 GHz measured in a 3 kHz bandwidth.



Bear in mind that a high beat note voltage is required for good phase noise. The loop natural frequency ω then is calculated using

$$\omega_n = \frac{\omega_{3dB}}{\sqrt{2\xi^2 + 1 + \sqrt{\left(2\xi^2 + 1\right)^2 + 1}}}$$

Next, the Vt-DRO sweep range (SR) in Hertz is defined. The locking V_t must be optimized to be located at the middle of the sweep voltage swing range by using the tuning screw. This point is defined by the hysteresis of the OPA1 comparator. C_1 is selected and the remaining loop parameters are calculated using

$$\tau_1 = \frac{K_d K_V}{\omega_n^2}$$

$$\tau_2 = \frac{2\xi}{\omega_n}$$

$$R_1 = \frac{\tau_1}{C_1}$$

$$R_2 = \frac{\tau_2}{C_1}$$

The maximum allowable sweep rate is defined using Viterbi's condition

$$\dot{\Delta\omega} < \frac{\omega_n^2}{2}$$

More margin is added if needed. (For example,

$$\dot{\Delta\omega} = 0.1\frac{\omega_n^2}{2}$$

may be used.) The required triangle half-period T/2, expressed in seconds, is calculated using

$$\frac{T}{2} = \frac{2\pi \bullet SR}{\dot{\Delta\omega}}$$

where

SR = sweep range of the Vt-DRO (Hz)

Next, the OPA2 comparator feedback values are calculated and optimized for the required sweep time. Arbitrary initial values are selected for R_4 or R_6 and final values are calculated from the relation of the SR voltage swing V_{SR} defined by the comparator hysteresis limitations

$$V_{SR} = \frac{2R_4}{R_6} V_{ref} \quad \text{at} \quad V_{ref} = \frac{V_{CC}}{2}$$

Remembering that $V_{ref} = V_{CC}/2$, R_5 is calculated using

$$\Delta T = \frac{R_6 - R_4}{R_6} R_5 C_1$$

Finally, the current through R_5 is compared with the current through R_1 (beat $note_{max}$ is the peak voltage at the SPD output) to verify that the negative feedback can prevail over the positive feedback such that

$$\frac{V_{CC} - V_{ref}}{R_5} < \frac{beat\ \ note_{max}}{R_1}$$

$$V_{ref} = \frac{V_{CC} R_9}{R_3 + R_9}$$

If necessary, R_5 is increased in value to slow down the sweep rate.

Lock Indication Circuit

The lock indication circuit samples the output of the comparator amplifier or the tuning voltage V_{tune}. Whenever the loop is out of lock the square wave voltage will generate a 0 (low level). When the loop is locked the square wave stops and the output level is 1. However, the level indicating a correct lock can be 0 and then a 1 will indicate the unlocked state, depending on the system requirements. There are several ways to implement such a circuit. For example, a sample-and-hold circuit or an absolute value circuit, where the fluctuating voltage is detected, may be used.

MEASURED RESULTS

Three very low cost PLDROs were designed, built and tested at 9.5, 11.3 and 15.5 GHz. The reference frequency was 50 MHz. CAE optimization techniques were used to optimize the loop stability, phase noise and acquisition performance, showing good agreement with the measured results. The performance of a 11.3 GHz low cost PLDRO example for a local multipoint distribution system application is shown in ***Figures 7***, ***8***, ***9*** and ***10***.

CONCLUSION

When designing an aided search/acquisition PLDRO, the rise and fall times of the sweep signal are crucial parameters. A low frequency sweep signal with fast rise and fall times such as a square wave or exponential wave is not adequate because the sweep rate is much too fast and will be interpreted as a chirp modulation. The phase error θ_e transmission function of a PLL is an HPF so the fast transient interrupt will pass directly to the VCO output and the feedback path will not be able to track it. Dual-feedback circuits such as a classical Wien bridge are not recommended due to their temperature sensitivity. Finally, special consideration should be taken

when selecting the SPD to optimize phase noise performance.

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References

1. *Gardner Phaselock Techniques*, Second Edition, John Wiley and Sons, New York.
2. Heinrich Meyr and Gerd Ascheid, *Synchronization in Digital Communications*, Vol. 1, John Wiley and Sons, New York.
3. Alex Hodisan, Ziv Hellman and Avi Brillant, "Method Optimizes Performance of PLLs," *Microwaves & RF*, September 1994, pp. 87–96.
4. Alex Hodisan, Ziv Hellman and Avi Brillant, "CAE Software Predicts PLL Phase Noise," *Microwaves & RF*, November 1994, pp. 95–102.
5. V.F. Kroupa, "Noise Properties of PLL Systems," *IEEE Transactions on Communications*, October 1982, pp. 2244–2251.
6. Millman Halkias, *Integrated Electronics*, McGraw-Hill.



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