

2,5GHz/510MHz Prescaler with LMX2330

YO4HFU 05.01.2014

- **LMX2330 is Dual Frequency Synthesizer for RF**
- **It has an interesting option for amateurs: Output signals of Counters may be accessed from outside.**
- **LMX2330 contains 2 Phase Locked Loops: IF and RF.**
IF PLL – max. 510MHz
RF PLL – max. 2500MHz
- **Power Input: -10...+4dBm.**
Sensitivity is better (-15dBm) for 3V power supply.
- **Divided signal is available at pin FoLD (10).**
Both prescalers can't be accessed simultaneously!

For testing and registry calculation, I used Code Loader 4 from National Semiconductor.

Calculated values of the registers must be inserted into the source program written for PIC16F628A. Then the source code is compiled with MPLAB.

Some print screens with this software:

LMX2330

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup Registers Bits/Pins BurstMode **RF PLL** IF PLL

Reference Oscillator 10 MHz

R Counter 50

Phase Detector Frequency 200 kHz

N Counter 1000

Prescaler 32

Phase Detector Polarity +

Charge Pump Gain 4X

Charge Pump State Normal

To pin 10 FoLD

VCO 200 MHz

Similar settings for 510MHz input (only if used)

Set the division ratio (read datasheet to check if selected value is valid)
This value is a global factor of division (Prescaler & N Counter)

The other settings do not matter for this application.

LMX2330

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup Registers Bits/Pins BurstMode RF PLL IF PLL

For simplicity, this option is not used.

PLL

☐ IF_PWDN

☐ RF_PWDN

FoLD

RF N Counter

RF/IF Lock Detect

IF R Counter

IF N Counter

RF R Counter

RF N Counter

Fastlock

Test Mode

RF R Counter

Program Pins

☐ TRIGGER

Select your preferred Input: IF - pin 16, max. 510MHz
RF - pin 5, max. 2500MHz

Output of IF N Counter (510MHz) is selected to pin 10 FoLD

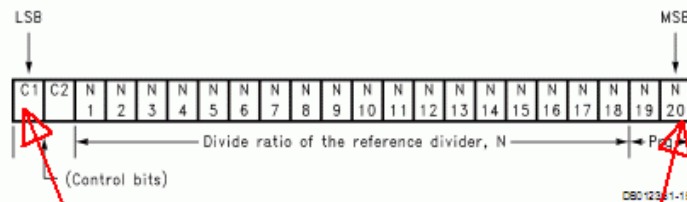
Output of RF N Counter (2,5GHz) is selected to pin 10 FoLD

Values of the registers:

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. For the IF N counter bits 5, 6, and 7 are don't care bits. The RF N counter does not have don't care bits.



7-BIT SWALLOW

RF

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup Registers Bits/Pins BurstMode RF PLL IF PLL

Export register values in hex to text file

LSB ->

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
IF_R	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	2	2
IF_N	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RF_R	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0
RF_N	1	1	0	0	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0

Hex Value

IF_R 0x07E 0320

IF_N 0x080 1811

RF_R 0x096 00CA

RF_N 0x000 3E23

MSB/LSB Display Switch

LMX2330

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup

Communication Mode

☐ USB ☒ LPT

LPT Port Setup

Port Address

☒ LPT1 ☐ LPT2 ☐ LPT3 ☐ Other 378

Reload Every 10 sec

Pin Configuration

LPT Connector

Clock Bit

☒ 1 ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 10 ☐ 11 ☐ 12 ☐ 14

Data Bit

☐ 1 ☒ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 10 ☐ 11 ☐ 12 ☐ 14

LE Bit

☐ 1 ☐ 2 ☐ 3 ☒ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 10 ☐ 11 ☐ 12 ☐ 14

TRIGGER

☐ 1 ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ 6 ☐ 7 ☐ 8 ☐ 10 ☐ 11 ☐ 12 ☒ 14

For tests can use a LPT PC control (without PIC16F628)

LMX2330 pinout

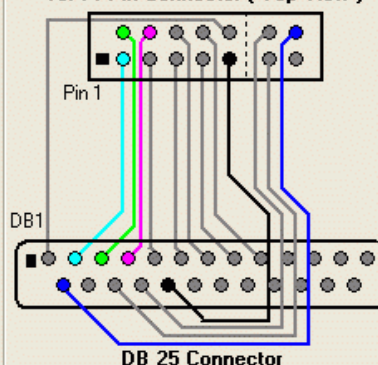
LPT Port Setup Diagram

☒ Clock pin 11 ☒ Other Pins

☒ Data pin 12 ☒ Ground

☒ LE (Latch Enable) pin 13 ☒ Address Conflict

10/14 Pin Connector (Top View)



Note 6: The I_{CPD} LOW current state = $1/4 \times I_{CPD}$ HIGH current.

Note 7: Activation of the IF PLL or RF PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_N inputs (to a high impedance state). The powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program mode is loaded, the part will go into powerdown mode when the charge pump reaches a TRI-STATE condition. The R counter functionality does not become disabled until both F and RF powerdown bits are activated. The MICROWIRE control register remains active and capable of loading and latching data during all of the powerdown modes.

TABLE 3. The F_o LD (Pin 10) Output Truth Table

RF R[19] (RF LD)	IF R[19] (IF LD)	RF R[20] (RF F_o)	IF R[20] (IF F_o)	F_o Output State
0	0	0	0	Disabled (Note 8)
0	1	0	0	IF Lock Detect (Note 9)
1	0	0	0	RF Lock Detect (Note 9)
1	1	0	0	RF/IF Lock Detect (Note 9)
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output

LMX2330

File Keyboard Controls Select Device Options Mode LPT/USB Help

Port Setup

Registers

Bits/Pins

BurstMode

RF PLL

IF PLL

Export register values in hex to text file

MSB -->

2 2 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

IF_R 0 1 1 1 1 0 0 0 0 0 0 0 1 1 0 0 1 0 0 0 0 0

IF_N 1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 0 0 0 1

RF_R 1 0 0 1 1 0 0 0 0 0 0 0 0 1 1 0 0 1 0 1 0

RF_N 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 1 0 0 0 1 1

Load

Load

Load

Load

Hex Value

IF_R 0x07E 0320

IF_N 0x080 1811

RF_R 0x096 00CA

RF_N 0x000 3E23