UPDATED DOCUMENTATION---MOuSeFET TRANSMITTERS

December 2018: Revision 8
Increased Harmonic Reduction-
Better PA Matching
Easy VFO Stabilization Adjustment

MOSFET Revision 8: 80 Meter, 40 Meter and 30 Meter Transmitters

Updated information, Improved Circuitry.
Original article was in December, 1986 QST by Mike Masterson WN2A (formerly KA2HZA).

Winner QST Cover Plaque Award,Dec 1986 Reprinted in QRP Classics,1990
QST Editor for this article originally was Paul Pagel, N1FB- (Credited with the term MOuSeFET)
Also, Chuck Hutchison K8CH,Former Technical Editor set up the ARRL Lab tests.

These transmitters have performed extremely well over the years, with no component failures or downtime since they were built in 1985. These have been used portable on camping and vacation trips, driving a variety of antennas often with less than perfect VSWR loads. They are intended to provide a clean keyed CW signal on 80,40 or 30 Meters, yielding approximately 20W from a single 13.8 volt supply.

UPDATED DOCUMENTATION---MOuSeFET TRANSMITTERS (Revision 8)

The original circuit worked fine, with many builders writing about their success. After the original article in QST, and the reprint in "QRP CLASSICS", builders and experimenters started to write me about:

- How easy it was to get up and running
- How tolerant it was of component variations -within reason.
- How much power they could obtain.
- Their various modifications to customize it for their own use
- The DX they were snagging with it

Generally great results with the A&A Engineering kits (~300 Kits Sold-out!)

But also: a few had problems getting power up to normal levels
It was determined that several causes could yield this result.
  Incorrect winding polarity of T1 (accompanied by high VFO feed-thru)
  Use of "substitute" transistors that have inadequate performance for gain ,etc
  Grounding paths too long (ex: Q5 emitter or Q6 source lead)
  Excessive lead lengths
  Tap location or winding errors for T2
The best way around these pitfalls is to get to know the RF construction practices found in these ARRL Publications:
1) The ARRL HANDBOOK-especially Construction Practices
2) Solid-State Design for the Radio Amateur. This is a landmark text as far as QRP/Homebrew is concerned. Very useful.
3) QRP CLASSICS,. Construction Practices chapter. Also numerous articles (such as mine and others) bring out some of the tips to home-brew construction.
4) Experimental Methods in RF Design.

Improvements:
The potentiometer for balancing the original doubler stage seemed bothersome, so on recommendation of Zack, KH6CP, I tried a balanced diode doubler. This is a much easier design to duplicate and obtain a clean signal, *provided* one winds T1 correctly and matches D6 & D7 for forward voltage. This being done, the cancellation of VFO "feedthru" is virtually automatic.
Also, a much better keying circuit developed, for better control of both keying edges. Key clicks were minimized by better wave shaping with Q4/Q7 circuit. Finally, in this revision, the use of thermistor/ varactor VFO temperature compensation brings significant VFO stability with a very simple circuit.

After the 80/40 and 30 Meter versions were built, (and re-built), I designed 20,17 and 10 meter VXO versions. The 20 meters runs 20W, 17 Meter runs 17 watts out and the 10 meter yields about 9 watts. Each has its own VXO (not VFO) and uses the IRF510 as Q6 with +13.8 volts supply. These (and the 80/40/30 meter) units have all been in service for years with no transistor failures, even after running them into high VSWR loads. For example, the WN2A/AK2F 10 Meter Beacon is based on an Oven-Controlled Crystal Oscillator (OCXO) MOuSeFET, on the air since March,1997.

Revised 11 Jan 2007: Deleted D5 and R4, changed to new D5 and D8 , better PA efficiency. For 30 Meters :Changed T1 Secondary From:10 Turns To: 8 Turns (Better Loading on FET Buffer, results in closer spot Frequency to TX Frequency, slightly greater power.
Revised 19 Jan 2013: Added additional filtering after Q3, Stabilized with R8, Added C15/R15 to reduce chirp during tune mode.

Rev 7; March 2015: Separated VFO and PA section's into <u>two (2) enclosures</u>.
Changed Zener D4 over to voltage regulator LM317
Added simple but effective Temperature Compensation Circuit.
Rev 8; November 2018: Low-Pass Filter added to PA Section to improve harmonic rejection.
Better PA Matching
Easy VFO Warm-Up Stabilization Procedure

These and more Revision 8 changes were made to address the need for a much more stable VFO, one that after a brief warm-up period would not appear to drift during a typical QSO. This was bought about by making the following modifications listed in APPENDIX A in addition to those made in Revision 6. This Revision 8 document bring all the changes together to a current design. Please note that several reference designators where changed and corrections made.

The author would like thank those who have build these transmitters and provided valuable feedback, particularity Rob Vijfschaft, PA3EQB. Also credit William Johnson, W0MS for his nice article “A Modified MouseFET Low Power Transmitter” in August, 2011 QST.

Mandatory Reading on VFO's is:

Crystal Sets to Sideband copyright 2010 Frank W. Harris Rev 10.

Better yet, download the whole book and read it end-to-end. Very well written.

CIRCUIT DESIGN DISCUSSION:

TRANSMITTER GENERAL NOTES:

MODES and POWER CONNECTIONS:

The transmitter has a few power supply connections whose functions should be clarified. I use the ubiquitous 9-pin D-miniature connectors for many applications. Here is the pin-out:

TABLE 1 J1 PIN-OUT:

J1 PIN NUMBER(S)	NAME	FUNCTION:
1,2	+ 13.8 T	Applies +13.8 VDC ,Transmit via T/R Relay . High current.
3	+ 13.8 A	Applies +13.8 VDC, Always. Low current
4,5	+24 T	Provision only. Not used on these transmitters.
6,7	GROUND	(RETURN)
8	KEY	Ground this pin to spot or transmit.
9	T/R	Grounded during transmit. Used to mute my receivers.

For the purposes of these transmitters, only +13.8 T, +13,8 A, KEY and GROUND are used.

VFO (Variable Frequency Oscillator) Assembly: Refer to Figure 1 for schematics.

Previously at revision 7, the 80 Meter VFO was changed over to the Clapp type. This has less to do with circuit performance than commonality. For all three bands, build up the VFO assembly first, starting with the Q1 and Q2 section, and install L1 *before* you stake it. Add or delete a turn to L1 windings to center C1A tuning range (3500-3600 kHz for example). Power up the VFO assembly and adjust L1 until C1B tuning range is centered at ~7000-7100 kHz for 40 Meters or ~10100-10150 kHz for 30 Meters.

Testing the VFO assembly is easier with an RF power meter connected to J5 and a simple RF voltage probe. With +13.8 V applied to J1-3, and J1-8 grounded, use the RF probe to check each node for RF voltage from Q1 thru Q3, while monitoring VFO board RF power output with the RF power meter. This helps find wiring faults and was very helpful in tuning C14 and C34. The selectivity of the double-tuned tank circuit is such that you may not detect RF power on the meter until you “sniff” with the RF voltage probe. The tuning of C14/C34 can be a bit critical, and one may need to find *slightly* different tap points on T2/T3 to get best results. Don’t vary tap point too much from that specified, or you may make Q3 unstable. R8 was added to aid Q3 stability. The VFO output power into the power meter has been measured (see Table 6). A slight retuning of C14/C34 may be done after integration with the PA board, since PA input impedance could be different from 50 ohms.

Revision 7 added R15 and C15. These components reduce the oscillator Q1 loading during standby (receive). This would normally not be important, if it was not for the VFO chirp during spotting. This was annoying, so R15/C15 forms a gate-leak circuit with Q2, reducing the loading. Now the chirp is not noticeable during spotting, and no chirp was noticed during normal transmit.

CW Keying was improved by re-arranging the keying circuit (Q7) and adding Q4. The issue with the previous circuit was control of the rise/fall times. With the previous circuit, the rise times were short compared to the long fall times, no matter what was done with the component values. This was caused by Q7 being an active pull-up, and the long discharge of C20, loaded by Q3. Transient simulation with QUCS demonstrated the inherent nature of this. So, an active pull-down (Q4) was added which allows rise and fall times to be adjusted independently. The values selected here are by no means fixed. The builder can elect to modify several values. Keep R9 fixed at 47 ohms, since that affects DC biasing of Q3. To increase both rise and fall times, increase C20. To increase fall time only, increase R16. To increase *only* rise time without changing fall time, increase C20 and decrease R16 proportionally.

PA (POWER AMP) Assembly:

The PA is largely unchanged from the original in 1986, other than the PA output network. The only significant change was to Q6 diode protection and a some Q6 output network changes. Based on results on the 10 and 17 meter VXO units I built, I changed from the Zener and resistor clamp to high-speed small signal diodes (D4 and D5). Less capacitive loading on Q6 gate drive and therefore slightly more output resulted. A QUCS simulation showed virtually no loading due to these diodes up to 30 MHz. Tuning with an RF voltage probe and RF power meter (connected to J2 output) is useful as it was with the VFO board, but the levels are much higher. Be sure your RF power meter can handle >25 watts or is preceded by adequate attenuation. Also, an RF probe can be damaged by high RF voltages in Q6's drain circuit! As noted before, a slight retuning of C14/C34 is optional after integration of VFO, PA and LPF (Low-Pass Filter) boards. Normally, just assemble the LPF and adjust L8 with a Dip Meter per Table 6. Then, if properly assembled, L8 should not need further adjustment. Use the measured RF power at J2 as the criteria.

OVERALL TRANSMITTER/ OTHER THOUGHTS:

RF output power will be a function of many factors, some of which we can control easily, others not so easy. I was able to obtain more power without sacrificing other performance goals just by raising the DC voltage from +12.0 to +13.8 VDC. This is been long pointed out by others, and MOSFET operation at +24 VDC can result in still better efficiency with modified circuit design. The builder may obtain results that differ from mine in Tables 7 and 8 for other reasons, such as layout and grounding differences. "Tight" grounding is required for the PA board due to high RF currents.

Components will affect the performance, especially the transistors in the RF path. To a large degree, the transistors in the RF path will determine how much RF power we will obtain. Each device from the first VFO stage (Q1) through the PA final (Q6) will affect the output. For the VFO, Q1 should have adequate transconductance, so that the VFO starts easily and has enough output to drive Q2. Q2 is used as a source-follower buffer, but still needs adequate transconductance to drive the diode multiplier. These diodes need to be matched for V_F within 2 millivolts or better so as to minimize VFO feed-through. That said, they should not have too high V_F, or doubler loss will be higher than necessary. The amplifier Q3 needs to have high gain at the output frequency, so sufficient Ft is required, but not so high as to become a stability issue. The parts specified work with an Ft of ~250 MHz, so don't use a microwave device here. The same advice goes for Q5, the PA Driver. This is a stage where too hot a device will cause problems. Since several of the devices specified for Q5 are metal can TO-39 parts, and may be in short supply now, the SMD devices in SOT-89 or SOT-223 type package, properly heatsunk in accordance with manufacturer's datasheet, potentially will provide an alternative. A brief search will show many such candidates. The PA stage (Q6) requires a power MOSFET with relatively low interelectrode capacitances and high transconductance, without resorting to more expensive RF MOSFETS. The IRF510 is (still) one of the better choices, even 25+ years after the original article. There are other choices that may be able to give us better gain/ output power especially up to the higher bands, but the IRF510 still works well, cost is low and is commonly available.

Finally, tuning is (often) critical to obtaining desired output power. As noted before, C14 and C34 tuning, and the tap adjustments on T2 and T3 determine VFO output level. Likewise the PA tuning is determined by tuning L3 inter-stage and for the PA output, L4 and L5. I generally find it is worth the time spent to premeasure the fixed capacitors with a simple C meter. Have the correct capacitance values in place on the board before attaching the inductors or transformers. Also, make sure you do not substitute the wrong type of ceramic capacitor (like a X7R or Z5U for an NPO or Silver-Mica, as specified), as you almost certainly will see performance suffer.

Revision 8, June 2018 LIST OF MATERIALS “MOuSeFET” Transmitters

TABLE 2: Parts Common to All Bands. Components leaded or SMT, unless noted.

REFERENCE DESIGNATORS	DESCRIPTION
C16,C17,C18,C19,C21,C22, C23,C24,C25,C26,C27,C28, C29,C33,C35,C36,C37	Capacitors, ceramic 0.1 uF, 25V min, X7R preferred or Z5U ceramic type. Leaded or SMD.
C30,C31,C32 C41,C42	Leaded capacitors, Ceramic 0.1 uF, 25V min, X7R or Z5U ceramic type. C30,C31,C32 locate at J1. C41 at J3; C42 at J4
C11	47uF, 16V electrolytic or tantalum
C15	Capacitor, ceramic NPO 50 pF, 25 V
C20	68 uF, 16 WV electrolytic or tantalum
C38,C39	6.8 uF , 35 WV electrolytic or tantalum
C40	330 pF NPO Chip or Leaded.
D1,D2,D3,D4,D5	1N4148,1N916 or MMBD914.D2&D2 matched for V_F < 2mV
D6	Zener, 16V. 1N5246 or equiv. SMD: MMBZ5246B
D7,D8,D9,D10	Varactor Diodes, Infineon BB505, BB535,BB555 or equal.
FB	2 T no. 28 enameled wire on FB-43-101 ferrite bead
J1	9-pin Male D-type connector, Amp 747904-2 or equiv.
J2,J5,J6	RCA Phono Jacks, Switchcraft 3501FPX
J3,J4	Banana Sockets, Red , Pomona 2854-2
Q1,Q2	2N5486, 2N4416A, MPF-102, MMBF5486, MMBF4416
Q3	2N3904, 2N2222, 2N2222A, MMBT2222A, MMBT3904
Q4	2N7000, 2N7002
Q5	80M: TN3053; 40M: 2N3053 ;30M:2N1711
Q6	80 M: IRF523, 40 M/30 M: IRF510
Q7	2N3906, 2N2907A; SMD MMBT2907A, MMBT3906
R1,R15	300 K or 330K
R4	200 ohms
R5	330 ohms
R6,R11	4.7 K
R7,R17	1100 ohms
R8,R9	47 ohms
R12,R16	100 ohms
R10,R18,R19	10 K
R13,R14	2.7 K
R20,R21	510K
RFC1,RFC2	100 uH RF chokes..API Develan 1025-68J or 1025-68K

RA	Trimmer Potentiometer, 10K, 20turn, BI TECH 66RW10K or equiv.
RB	Trimmer Potentiometer, 100K, 20turn, BI TECH 66RW100Kor equiv.
RT1	Thermistor, NTC, 3000 ohm. Vishay/Date 01C3001-5. SMD Possible Alt: Vishay-BC NTCLE300E3302SB. See Text.
U1	IC Regulator, LM317T, LM317LM, or equiv. Regulator for 8.2V
P1 (not on schematic)	9-pin Female D-type connector Amp 747905-2 for power cable.
P3,P4	Banana Plugs, Red Pomona 1825-2 . Wire these together with PVC Insulated AWG #18 or #20 10"long to make the Power Jumper.
P5,P6	RCA Phono Plugs, Shielding, Pomona 6881 or equal

TABLE 3 BAND DEPENDENT RESISTOR VALUES:

REFERENCE DESIGNATORS	80 METERS	40 METERS	30 METERS
R2	47 ohms	68 ohms	68 ohms
R3	33 ohms	33 ohms	51 ohms

TABLE 4 BAND DEPENDENT CAPACITOR VALUES:
Unless Noted ALL Capacitors are NPO Chip Ceramic.

REFERENCE DESIGNATORS	80 METERS	40 METERS	30 METERS
C1A	C1A: 8-48pF Air Variable	Not Used.	Not Used.
C1B	Not used	7~37 pF Air Variable	7~37 pF Air Variable
C2	2400 pF (2x 1200 pF)	990 pF or (3x330pF)	1000pF=(10x100pF)
C3	1200 pF	410 pF=(2x150pF) +(100 pF +10pF)	615 pF (6x100pF)+(3x5pF)
C4	200 pF	100 pF	100 pF
C5	133 pF (33+100pF)	100 pF	56 pF
C6	1000 pF	470 pF	330 pF
C7	1800 pF	1000 pF	400 pF
C8	2700 pF	1630 pF =(3x470)+220	1200 pF
C9	1100 pF	700 pF (7X100)	400 pF (4x100pF)
C10	33 pF	15 pF	10 pF
C12	247 pF (2x100 + 47pF)	100 pF	56 pF
C14,C34	5-60 pF Trimmer	5-60 pF Trimmer	5-60 pF Trimmer
C13	400pF=(4x100pF)	265 pF = (5x50pF) +(3x5pF)	330 pF= (6x50pF)+(2x15pF)

TABLE 5 BAND DEPENDENT INDUCTOR/TRANSFORMER VALUES: Inductance Values Approximate

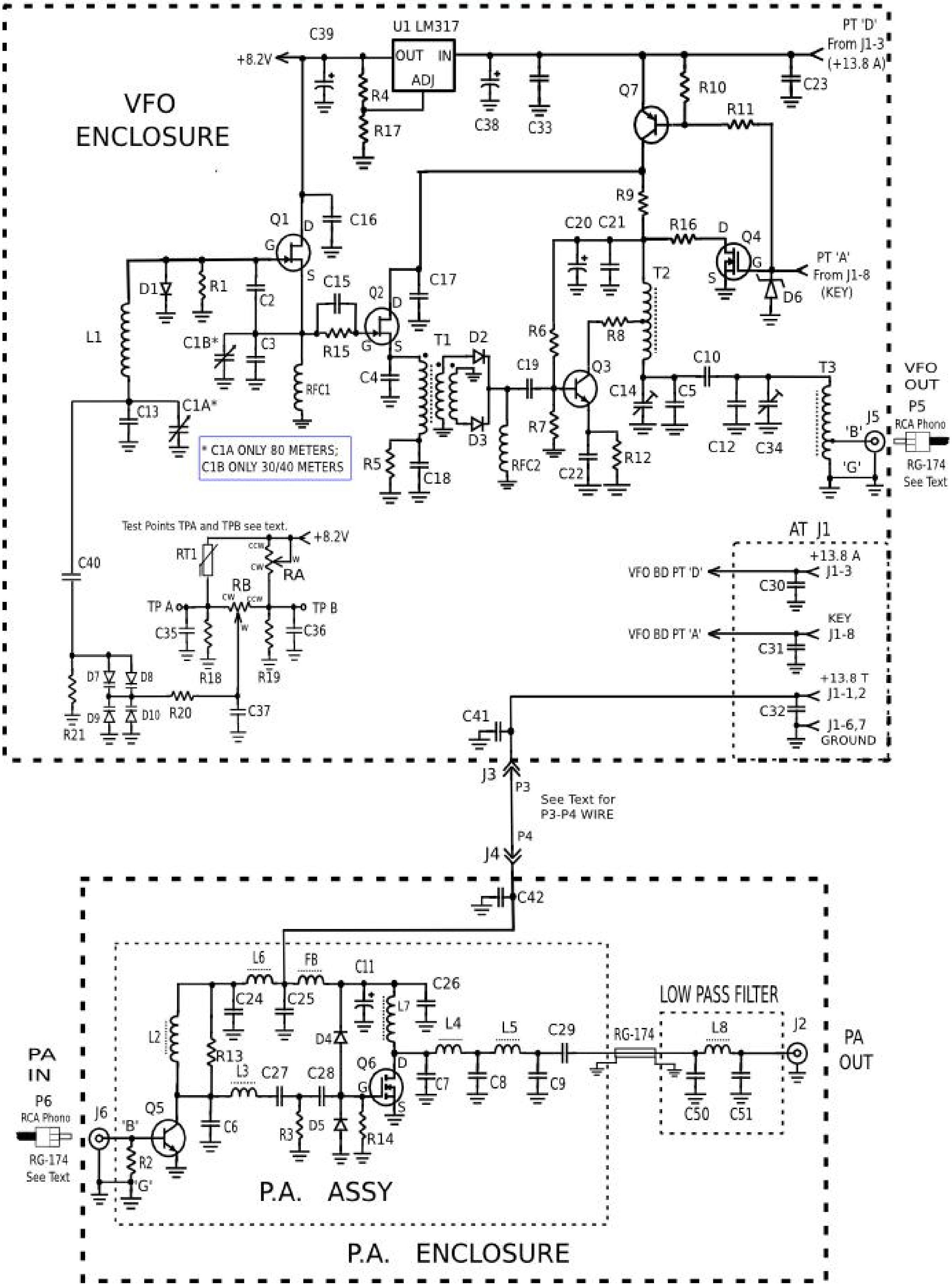
REFERENCE DESIGNATORS	80 METERS	40 METERS	30 METERS
L1 All Close Wound Coils	~31 uH Air Core Ceramic Form. 73T AWG#30, 0.5” Dia Form, ~0.85” Long	~14.5 uH 40T on 3/8 in dia AWG#36. Air Core Ceramic Form.	~5.5 uH 35T on 3/8 in dia Air Core Ceramic Form.
L2	14 T on FT37-61	9 T on FT37-61	9 T on FT37-61
L3	1.8uH, 17 T on T50-2	0.5uH, 13T on T50-6	0.5uH, 13 T on T50-6
L4	0.9uH, 15 T on T50-6	0.43uH, 10 T on T50-6	0.3uH, 7 T on T50-6
L5	2.8uH, 22 T on T50-2	1.2uH, 15 T on T50-2	0.9uH, 13 T on T50-6
L6	14T on FT37-61	10T on FT37-61	10T on FT37-61
L7	42 T on T50-6 ~ 7.1 uH	38 T on T50-6 ~ 5.5 uH	20T on T50-6 ~1.6 uH
T1	PRI: 18 T SEC: 11 T bifiliar FT50-61	PRI: 18 T SEC: 11 T bifiliar FT50-61	PRI: 12T SEC: 8 T bifiliar FT50-61
T2	10.14 uH, 45 T tap at 24 T from C21 end. T50-2	3.6 uH, 30 T tap at 8 T from C21 end. T50-6	2.4 uH, 24 T tap at 7 T from C21 end. T50-6
T3	6.4 uH, 36 T tap at 7 T from ground end. T50-2	3.6 uH, 30T tap at 4 T from ground end. T50-6	2.4 uH, 24T tap at 4 T from ground end. T50-6

TABLE 6 HARMONIC LOW-PASS FILTERS : New in MouSeFET Revison. 8

REFERENCE DESIGNATORS	80 METERS	40 METERS	30 METERS
L8	21 T T50-6 ~1776 nH	14T T50-6 ~890 nH	11 T T50-6 ~646 nH
C50,C51	1800 pF	910 pF	620 pF
F Resonate* [MHz]	3.98 MHz	7.91 MHz	11.25 MHz

* With no connections made to the Harmonic filter assembly, use a DIP meter to adjust L8 for the indicated resonate frequency.

FIGURE 1. **SCHEMATIC MOUSEFET REV 8**



VFO Board Assembly Drawings and Notes

Refer to Figures 2 and 3. The last page has suggested PCB patterns for VFO and PA boards.
A variety of assembly methods that can be used for both 80 meter and 30/40 meter versions. Whether one uses primarily SMT or leaded or some combination of each, the results have been found to be equivalent. I would encourage one to use SMT if possible, since it makes for a neater, less cluttered result. Note that if you do use SMT, avoid overheating these parts as termination dewetting also known as “leaching” can result. Also space the SMT capacitors (C2 on 80 Meter version and C13 on 30/40 meter version) away from the corner mounting screw. It could result in SMT capacitor cracking when installing the VFO Assembly Board. The PC board material is conventional FR-4 (G10) Epoxy Fiberglass, Single-sided (no back conductor!) ~0.060” thick. Single-sided Phenolic (FR-2) has also been used. The use of a double-sided board has been found to make for poor VFO stability if the ground plane is not removed under the VFO (Q1) and VFO Buffer (Q2) stages. Use PCB ~0.062” thick to control warpage. Elevate the VFO board above the metal housing with metal standoffs (4) so to preserve VFO stability.

PA Board Assembly Drawing and Notes

Refer to Figures 2 and 4.
As with the VFO Assembly Boards, one can use a combination of Leaded and SMT components on this board. The soldering issues are the same, but these PA boards have also been built successfully using SMT ceramic capacitors and resistors. In this case Double-Sided PCB, ~0.060 inch thick FR-4 (G10) or Phenolic FR-2 has been used. Use copper foil to supply low-inductance ground wrap-rounds from the ground plane to the top, around the board periphery. Q5 will need some kind of small heatsink, whereas it is best just to use a mica or Kapton insulator between Q6 and the metal housing. A *very* small amount of heatsink grease can be applied to both sides of the kapton insulator.

Integration

I prefer to keep the VFO and PA boards in separate shielded enclosures. The enclosures are interconnected with DC Power from J3 to J4 with approximately 10” (25mm) of PVC Insulated AWG #18 or #20 stranded wire assembled into P3 and P4. The VFO RF is supplied from
J5 to J6 with approximately 10” (25mm) RG-174/U 50 ohm coax and two RCA Phono Plugs P5,P6. Generally I operate the units without them contacting each other, just sitting separately in the operating position. I store them together as a stack, using duct tape or whatever is convenient.

Figure 2.

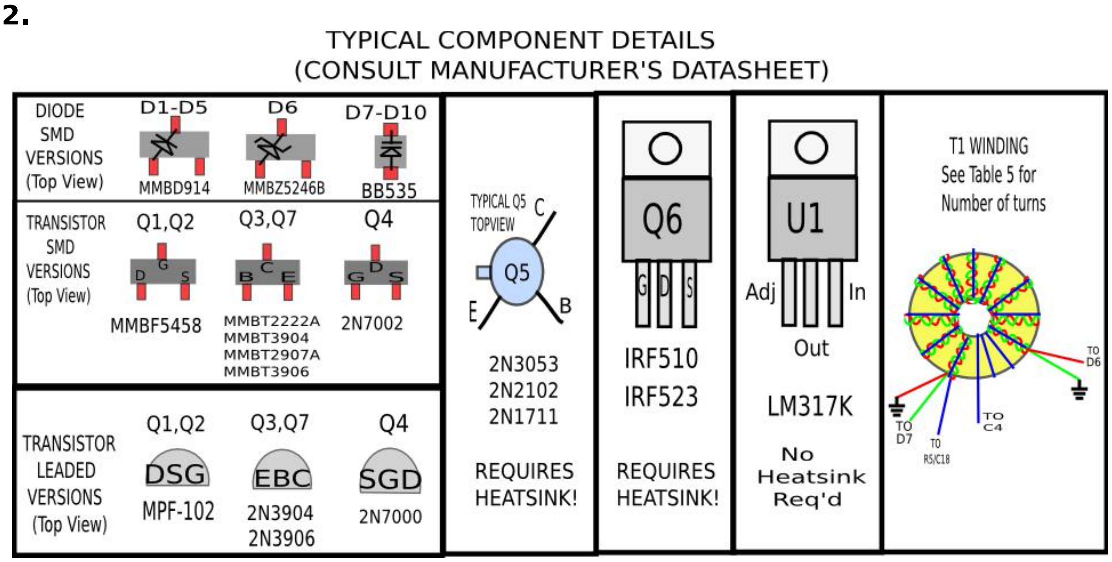
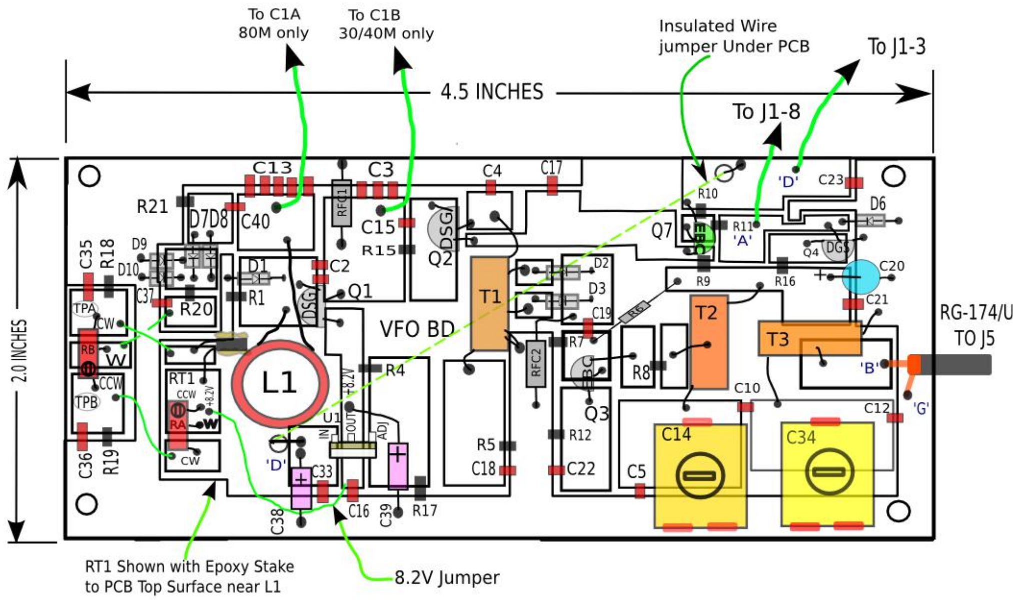


Figure 3 VFO Board Assembly Drawing. **(Scale to Dimensions Shown)**

PROPOSED REVISION 8 LAYOUT
w/ LEADED TRANSISTORS & DIODES
Components may vary from as shown here



PROPOSED REVISION 8 LAYOUT
W/ SMT TRANSISTORS & DIODES
Components may vary from as shown here

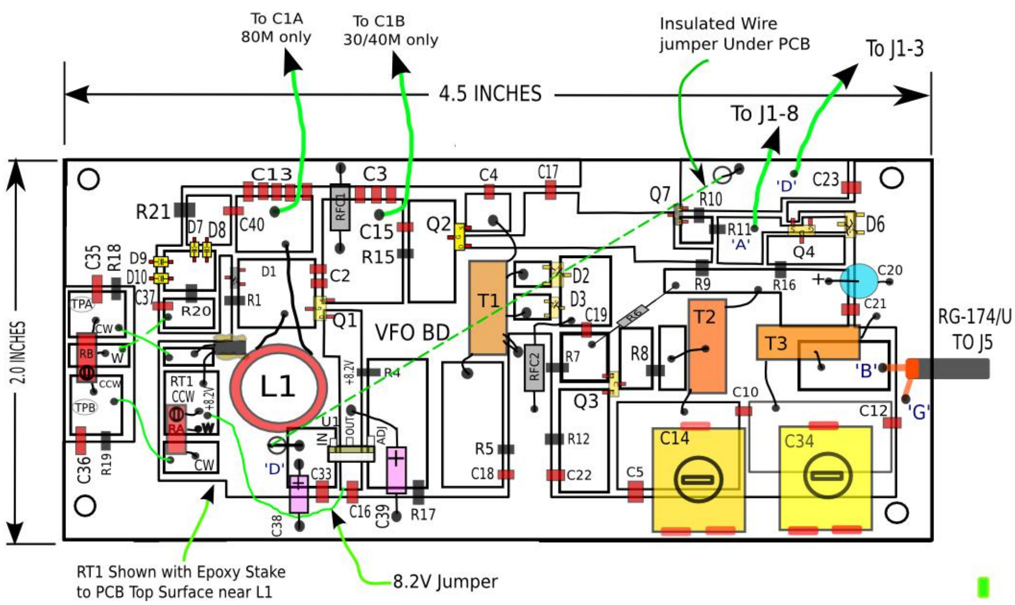


Fig 4. PA Assembly

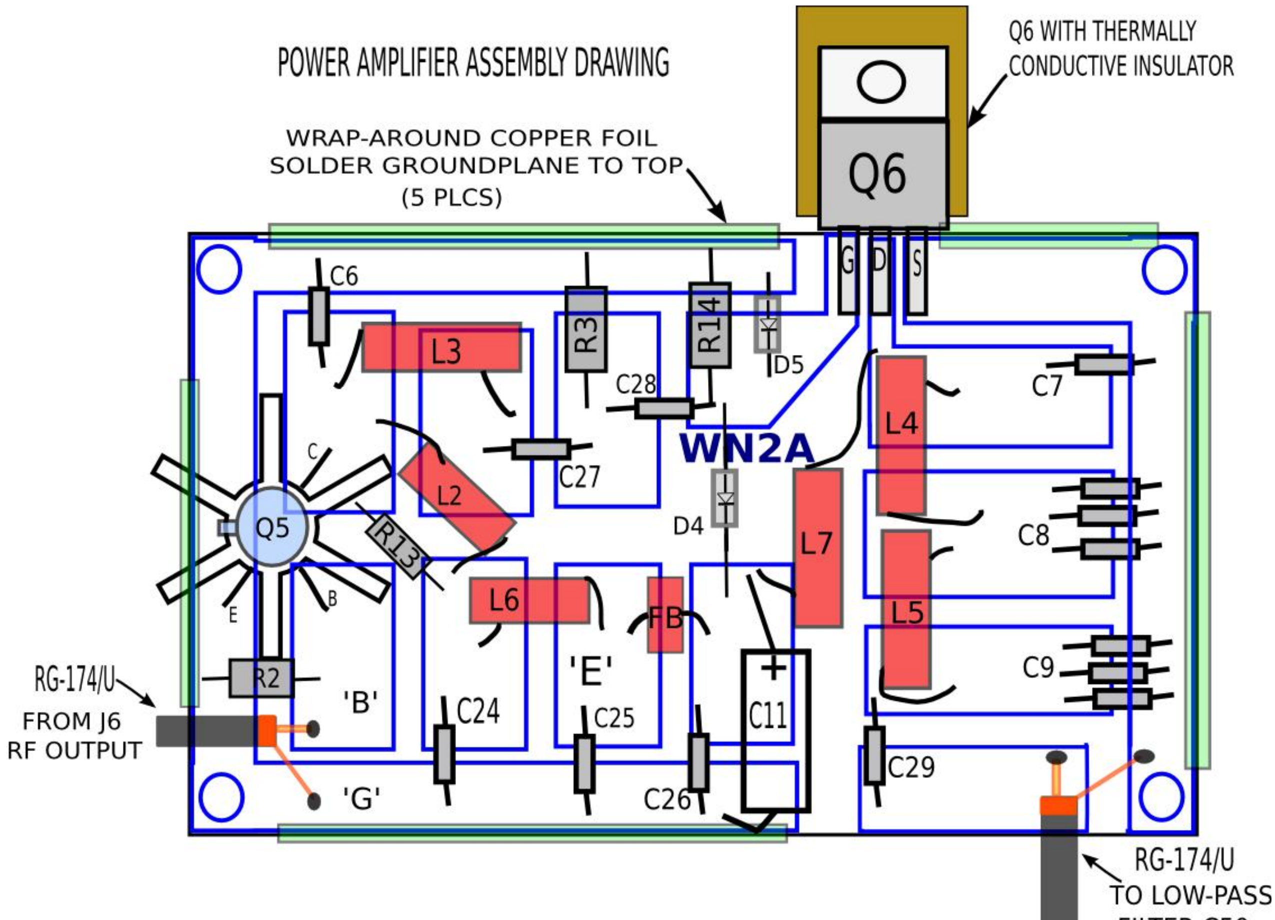


Fig 5.Low-Pass Filter Assembly

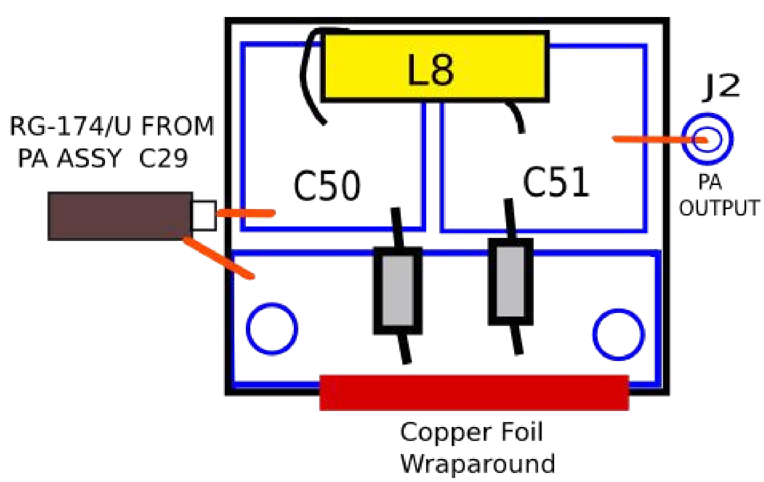


Figure 6. Photo of My 80 Meter VFO and PA Assemblies (For Reference Only).

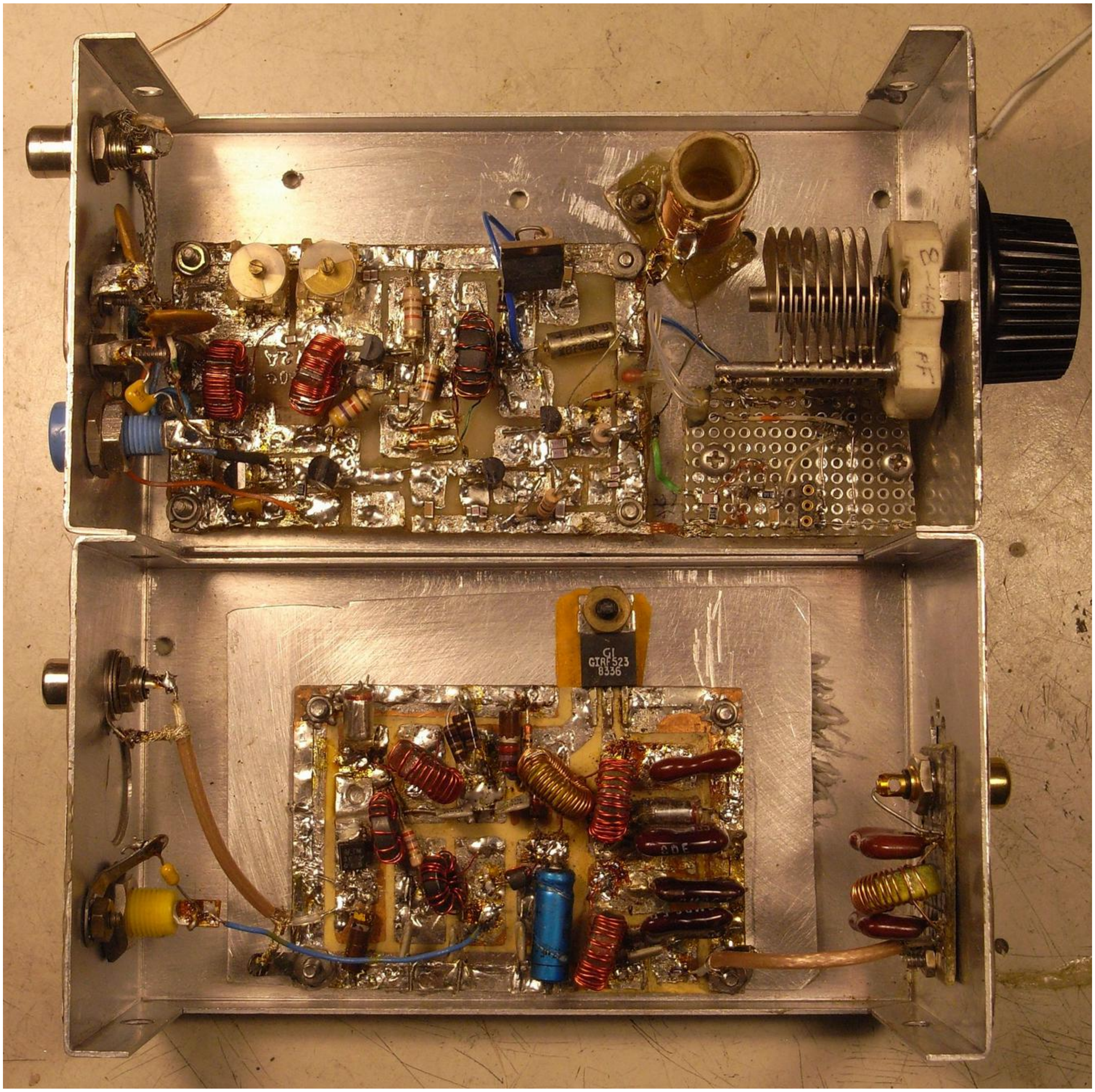


Figure 7. Photo of My 40 Meter VFO and PA Assemblies (For Reference Only).

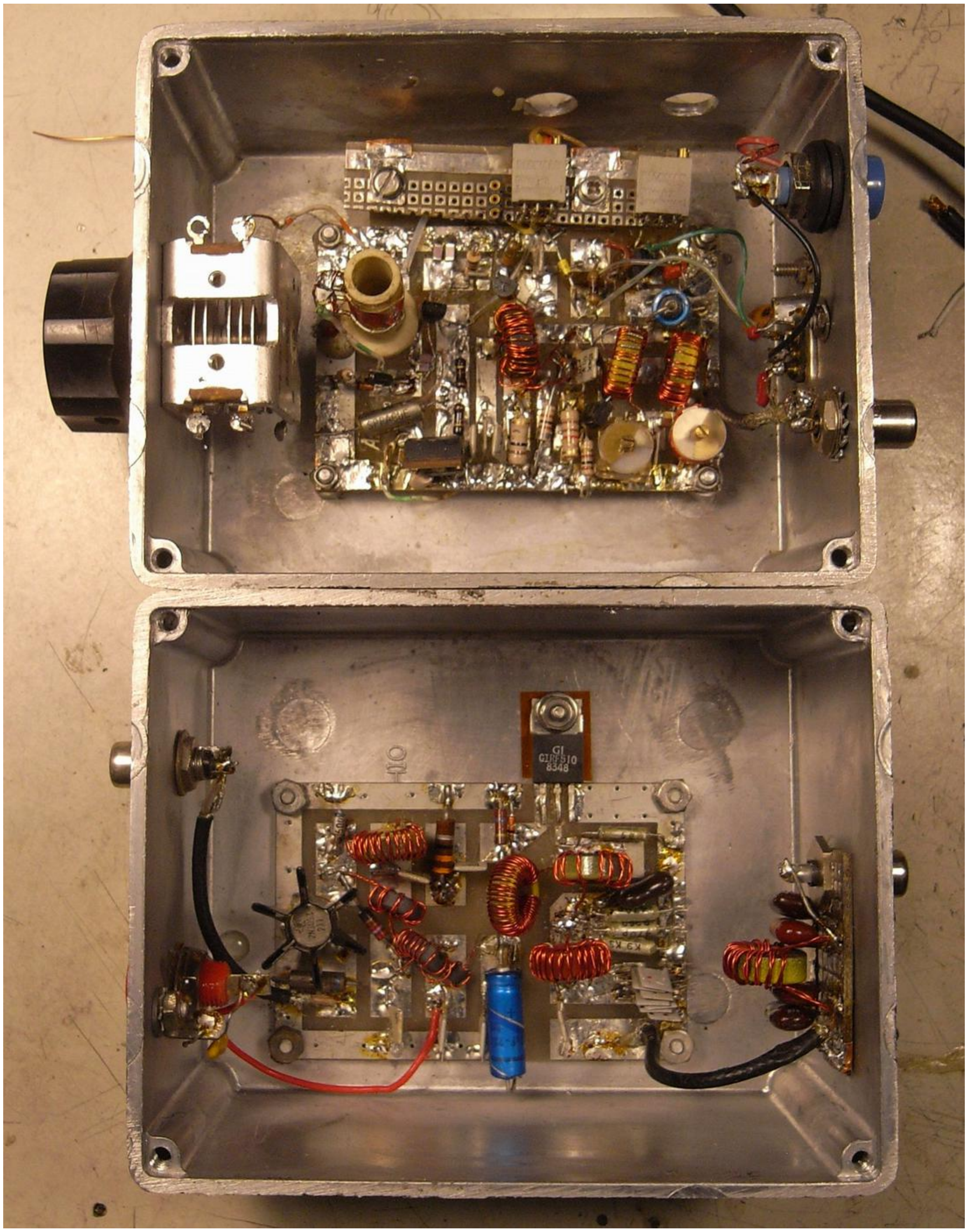


Figure 8. Photo of My 30 Meter VFO and PA Assemblies (For Reference Only).

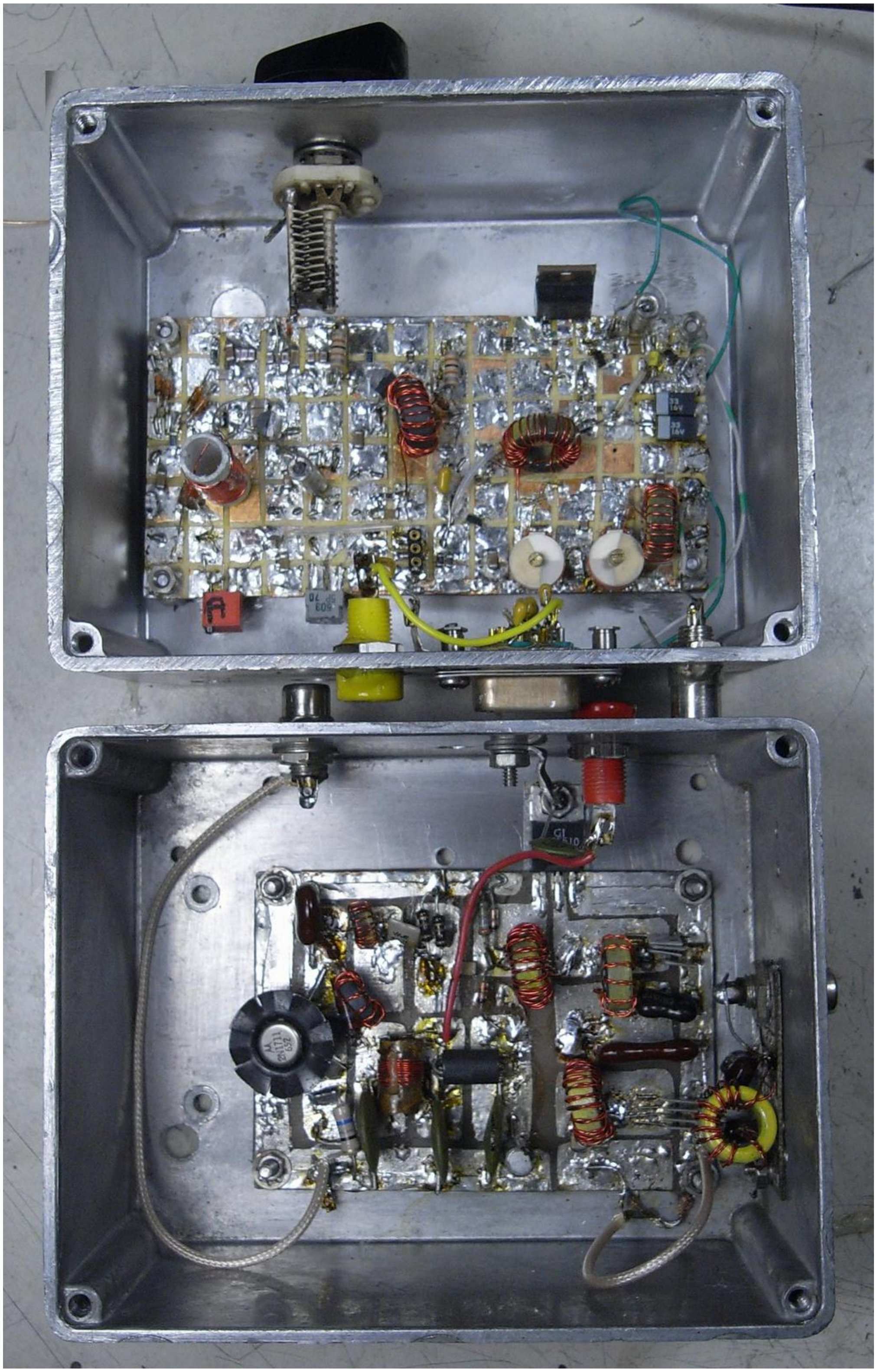


Table 7. Measurements on my Revision 8 Transmitters. These may or may not be “Typical”!

Operating Parameters: +13.8 VDC nominal supply. Note 1.

Transmitter Measurement (VFO + PA Board) at J2	80 meter	40 meter	30 meter
Power output [Watts]	22	22	19.4
Subharmonic (1/2 F) [dBc]	-55	-65	< -65
Second Harmonic (2F) [dBc]	<-65	<-65	<-65
Keying Waveform (attack [msec] /decay [msec])	3/3	2/2	3/3
DC Voltage measured at J4 [V]	13.33	13.33	13.33
PA Assembly Current (Transmit Key-down) [Amps]	3.04	3.06	2.61
PA Assembly DC Power [W]	40.5	40.7	34.8
PA Assembly Efficiency @ J4 input DC Power.	54.3%	53.9%	55.7%
RF Feedthru (+13.8T and +13,8A, applied Key-up). [dBc below Key-down] Note 2.	<-90	<-90	<-90

VFO Board Measurements, at Points B-E. No PA Unit.	80 meter	40 meter	30 meter
Power out (VFO Stage) [mW]	96	67.6	54
Subharmonic (1/2 F) [dBc]	-60	-60	-60
Second Harmonic (2F) [dBc]	-55	-56	-56
RF Feedthru (dBm)	<<-70	<<-70	<<-70

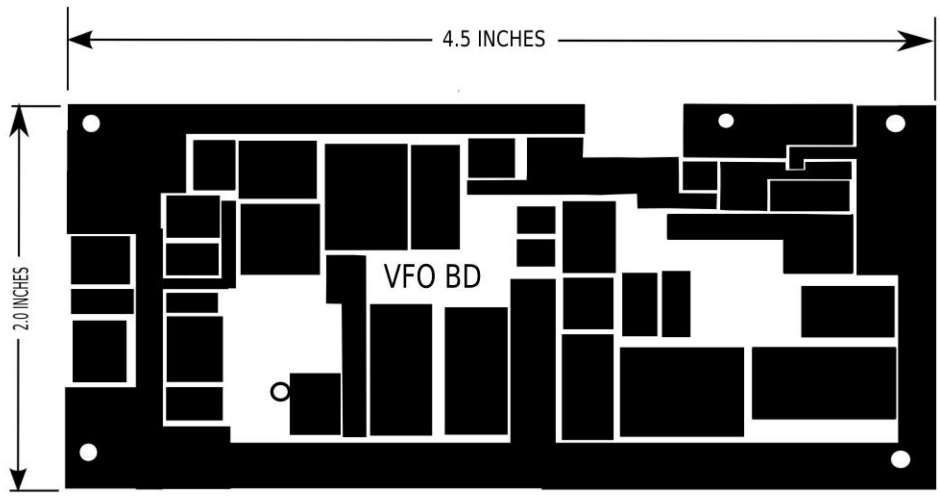
Note 1: Temperature ~ 20C (RT) . Test Equipment: HB=”HomeBrew”.
Spectrum Analyzer HP8558B/HP182T,
Oscilloscope Leader LBO-513A, HB 13.8VDC Supply. DVM:Simpson 461-2.
HB RF Power Meter

Note 2: RF Feedthru beyond limits of my measurement capability. Receiver tests suggest much less feedthru.

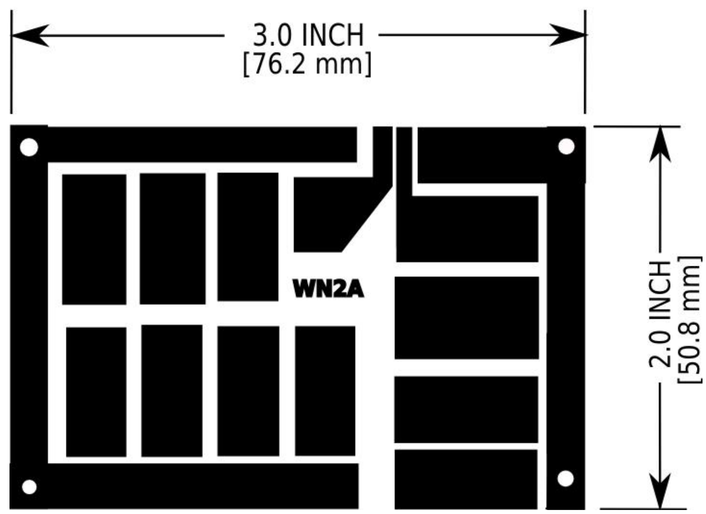
Table 8: Typical DC Voltages for Debugging. DVM: Simpson 461. +13.8A applied.

U1 Regulator voltage [V]	8.2	8.2	8.2
Q2-gate, Key Up, +13.8T off, through 100K resistor [V]	-1.8	-1.5	-1.2
R5/C18, Key Down, +13.8T off. [V]	1.75	1.68	1.18
R5/C18, Key Up, +13.8T applied [V]	1.68	1.67	1.18
R12/C22, Key Down [V]	1.83	1.63	1.76
C20/C21, Key Down [V]	12.8	12.26	12.67
C20/C21, Key Up [V]	0	0	0
Q6-Gate via 68K DMM Voltage Measurement. Key Down +13.8T Applied [V]	+5.7	+6.0	+5.7

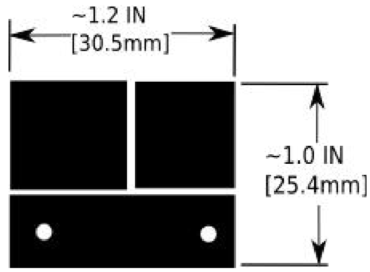
Figure 9: Suggested PCB Patterns



PA PCB



LPF PCB



REVISION 8 APPENDIX A: IMPROVED TEMPERATURE STABILITY:

The Revision 8 changes were made to address the need for a much more stable VFO, one that after a brief stabilization period would not appear to drift at least audibly during a typical QSO. This was bought about by making the following modifications in addition to those of revision 6:

Chapter 10 of Harris's work [1] is required reading. Let's place emphasis on several of his VFO Stabilization points with some my paraphrasing, and some of my additional points, etc:

1) Separate, thermally isolated enclosures for the VFO and PA boards. These functions were on separate PCB's anyway, it makes sense to protect the VFO components from the heat generated by the PA board.

2) Starting in Revision 7, I use only NPO Capacitors in VFO tuned circuitry. No need for Polystyrene or hard-to-get Negative-Temperature compensating capacitors. You may find some availability of these hard-to-get NTC's occasionally, but as others have noted the NP0 capacitors are much more readily obtainable from the distributors.

3) Air Core/Ceramic Form inductor at L1. Very light epoxy stake on L1. No inductors with powdered iron cores or ferrite. I did obtain good results with an Air Core/ Cardboard Form inductor. Supposedly, cardboard has a low mechanical TC. Light Epoxy Stake this type also.

4) Replace Zener D4 with LM317 (or better) regulator.

5) Single-Sided PCB for VFO (as was always the case).

6) Power buffer Q2 only when keyed for lower power dissipation and less self heating.

7) Seal all VFO Enclosures “Air Tight”.

8) Add simple Temperature Compensating circuit using Thermistor and Varactors. This circuit then provides the measured amount of TC required over the user's temperature range after it is calibrated..

9) Common VFO circuit for all bands. This has less to do with stabilization, just makes for commonality of design.

10) Revised schematics and BOM's as required. Re-assigned reference designators as required.

No specific layout information is given here, rather just the layout/construction guidelines. Most builders tend to make substitutes and improvise anyway. Use the provided photos as a guide, but do an appropriate layout for the components you are using. Some components were annotated for clarity, but a proper RF layout will result in cleaner looking construction and likely be a bit more mechanically and electrically stable than my specific construction.

VFO Temperature Compensation Process Steps/Detail:

Abstract: The MOSFET Transmitters for 80/40 and 30 meters from my QST December 1986 article had JFET VFO's, which for its time probably were as stable as needed for the type of CW operating then being done. After recently noting that VFO stability could be (and should be) improved over the original circuit, steps were taken to better the VFO temperature characteristics. Results were very good after evaluating and building three different methods, with the simplest (Thermistor-controlled Varactor) working most satisfactory. The circuit, procedure and test results of this method are documented here. Years later, JFET-based VFO's for HF use are still preferred now in 2015, owing to excellent phase-noise, excellent stability, and ease of use, and JFET availability..

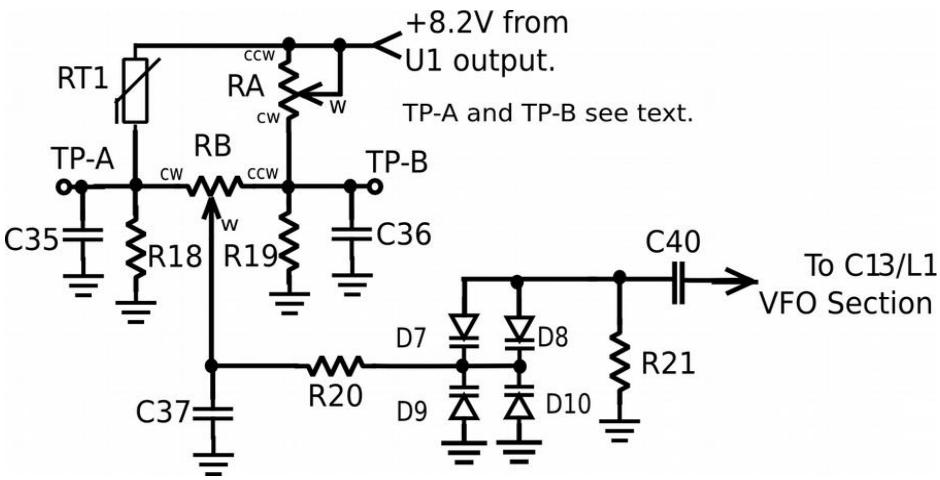
Methods: The original Three-Fine Mice Article was written to demonstrate that very inexpensive MOSFETS could be used to provide ~10-20 Watts of CW in the HF region. Not a lot of effort or thought was required to design the VFO section at that point. And after the QST article was published, the design of the PA section has been unchanged, other than diode protection for the PA final (Q7). Over time, The VFO section required modification for spectral purity, CW waveform shaping, and now Temperature Stability. The heating created within the PA section was identified as a major source of drift, sometimes causing the transmitted frequency to drift audibly during a QSO. This I deemed unacceptable. Hence, thermal isolation from the PA was effected by placing the VFO and PA in separate housings, with no openings. An LM317 regulator replaced the simple shunt Zener diode, providing much better voltage regulation. The VFO buffer (Q2) was only powered during the CW key-down, reducing the dissipation. No undesirable chirp was noted from the new Q2 arrangement.

With the Qucs Analysis of a Thermistor Bridge-Controlled Varactor circuit demonstrated (below) the feasibility of a simple temperature-compensation method. The tests done on the 80/40 and 30 meter VFO's demonstrated that all VFO's that I built with NPO capacitors and Air-Core/ Ceramic-Form VFO inductor (L1) had a negative temperature coefficient of frequency (TCF), mostly due to the positive-temperature coefficient of L1. Hence, only temperature compensation in one direction, appears to be necessary.

Chapter 10 of Harris's landmark work [1] is required reading. Let's place emphasis on several of his VFO Stabilization points with some my paraphrasing, and other interjection, etc:

1. Separate VFO and PA enclosures for thermal isolation, completely enclosed VFO section from air currents.
2. LM317 Regulator replacing the Zener. I you have a better precision 8.2V reference supply that can supply enough current, use it.
3. Changed 80 Meter VFO from Hartley to Clapp, just to have common schematic for the three bands. (not for any inherent performance change).
4. Reduced dissipation of the Q2 Buffer Stage to reduce heating.
5. NPO capacitors for all frequency determining capacitors in VFO. Multiple NPO capacitors in parallel to reduce self-heating drift.
6. Air-core Ceramic-Form inductor at L1. An Air-core, Cardboard-Form inductor was also constructed with approximately equal results. No powder-iron or ferrite cores used at L1.
7. Single-Sided PCB for the VFO section. Double-Sided PCB results in an additional source of drift, from the PCB capacitance.
8. Clean all Flux and residue from the VFO section. Apply alcohol with a Q-tip, then dry out the VFO thoroughly. See my Note 1 in “Discussion”.
9. The temperature-compensating circuit described herein was built and calibrated.

Schematic: Full schematic/part list found on MOSFET revision 8



Parts List: See Table 2 in MouSeFET Rev 7.

Construction Information:

No specific layout information is given here, rather just the layout/construction guidelines. Most builders tend to make substitutes and improvise anyway.

1. Attach/Epoxy Thermistor RT1 on the VFO board, nearest the frequency determining components, such as L1 and C13. Epoxy the thermistor onto the PCB and allow full cure. I used Cytec Conap Easypoxy K-20. I also use that epoxy as a very light stake on L1, forming several thin strings to bond L1 windings and reduce vibration problems.

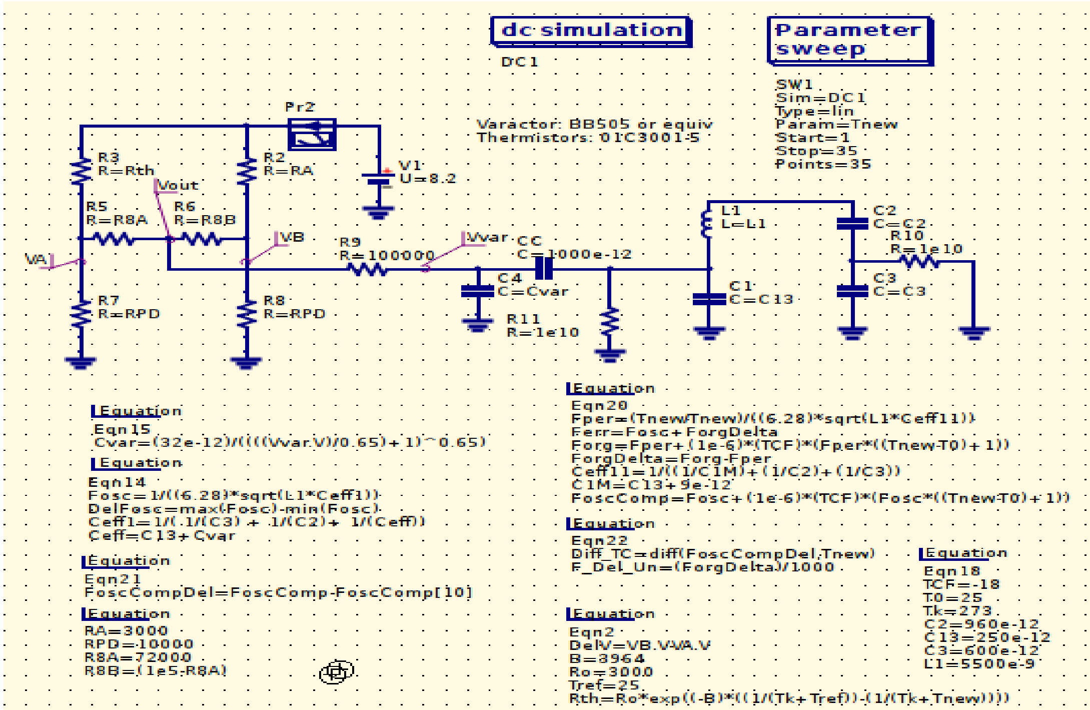
2. *Build up the VFO section fully and test before applying the temperature compensating procedure*. At Room Temperature Preset RA at room temperature such that the voltage across test points 'A' to 'B' is nulled with a DVM, and that the wiper(W) of RB is preset to the side closest to test point 'B', (usually CCW).. You should then set the frequency coverage set so that the bottom to top of desired VFO range is covered. This may mean using a different tuning capacitor (C1) to achieve desired coverage. This can be done by installing low-value NPO capacitors at C13, C2 and C3, depending on the frequency coverage desired.

The Math: Temperature in [K]; Voltage [V]; Resistance [Ω]; Capacitance[F]
Thermistor Characteristics: 01C3001-5 Dale/Vishay 3000[Ω] +/-5% @ 25°C (Tref). $B_{(25/75)}=3964$; $B_{(25/85)}=3974$

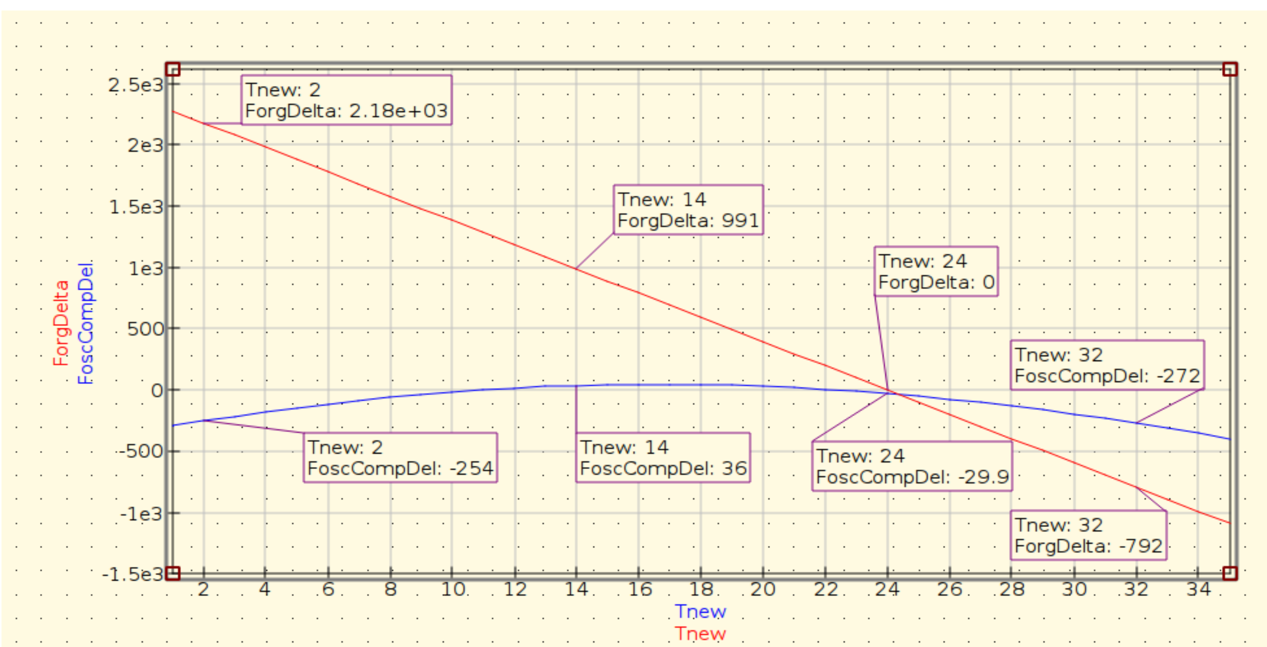
$R_{TH}=R_0*\exp((-B)*((1/273+T_{REF}))-((1/273+T_{NEW}))))$
$R_{TH}=3000*\exp((-3964)*((1/298[K]))-(1/(273[K]+T_{NEW}))))$ This may not be exact; an approximation.

Varactor Characteristics: Infineon BB505, Derived from datasheet and interpreted from its graphs.
C(V)= Capacitance as function of Voltage. C_0=ZeroVoltage Capacitance; Φ=Built in Potential;
V_R=Reverse Bias. $^{\mathbf{Y}}$**=** slope of the LogC vs. LogV curve
$C(V)=C_{0*}[1/[[V_R/\Phi]+1]]^{\mathbf{Y}} \cong C_{0*}[1/[[V_R/0.65]+1]]^{(0.65)} \cong 32e\text{-}12*[1/[[V_R/0.65]+1]]^{(0.65)}$

Qucs Analysis: Schematic and Qucs equations.



Simulation:



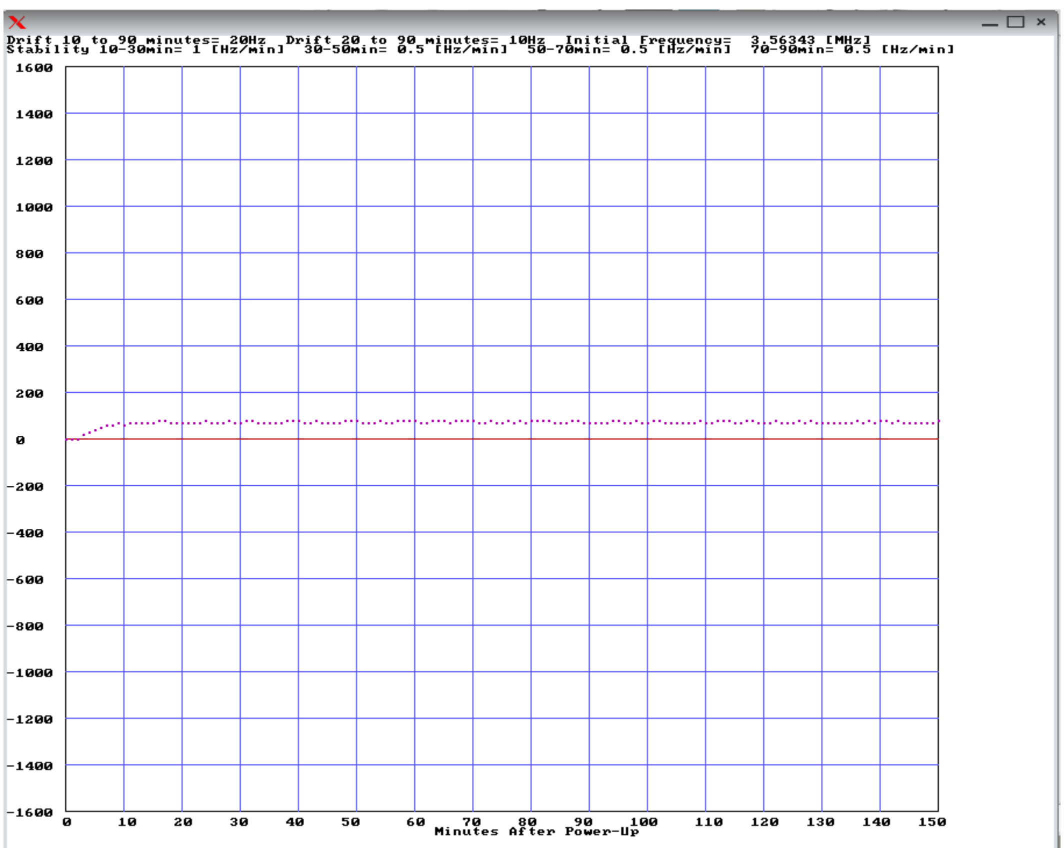
ForgeDelta (Red) is uncompensated frequency change vs. Temperature. FoscCompDel (Blue) is Temperature Compensated frequency change vs. Temperature. The potential for excellent Temperature Stability is evident.

Warm-Up Drift Compensation Method

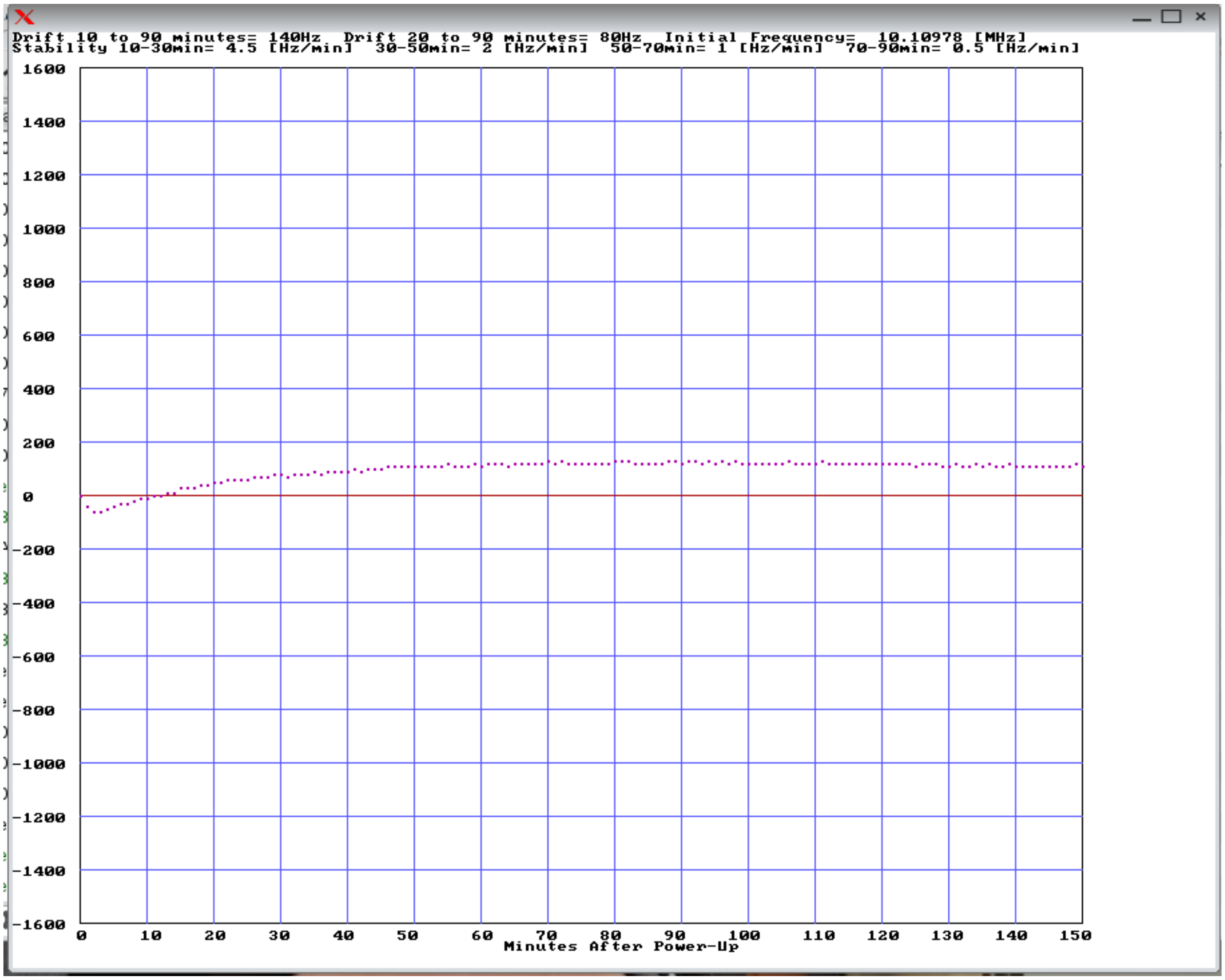
The advantage to this method is that it does not require any temperature chambers, but it may require several iterations until low warm-up drift is achieved. I have been using this method in place of the original “Chamber” method with very good results.

1) At Room Temp (~68 deg F or ~ 20deg C), set RB for full CCW such that the wiper (W) of RB is nearest to TP-B. Stabilize at ambient for 30 minutes..
2) Adjust RA for a DC null from points ‘A’ to ‘B’. Do not adjust RA after this step.
3) Turn off VFO power for 30 minutes. After 30 minutes turn VFO back on and observe warm-up drift, for the next 30-150 minutes. Record the frequency as it stabilizes.
4) Adjust RB to approx ½ CW and repeat profile for 90 minutes.
5) Repeat this procedure until the warm-up drift is minimized. This may take several iterations. Less than 20 Hz drift over 90 minutes after 20 min warm-up is feasible.
6) Small, careful adjustments in RB can result in better stability.
As stated, no temperature chambers required, but may need several iterations.

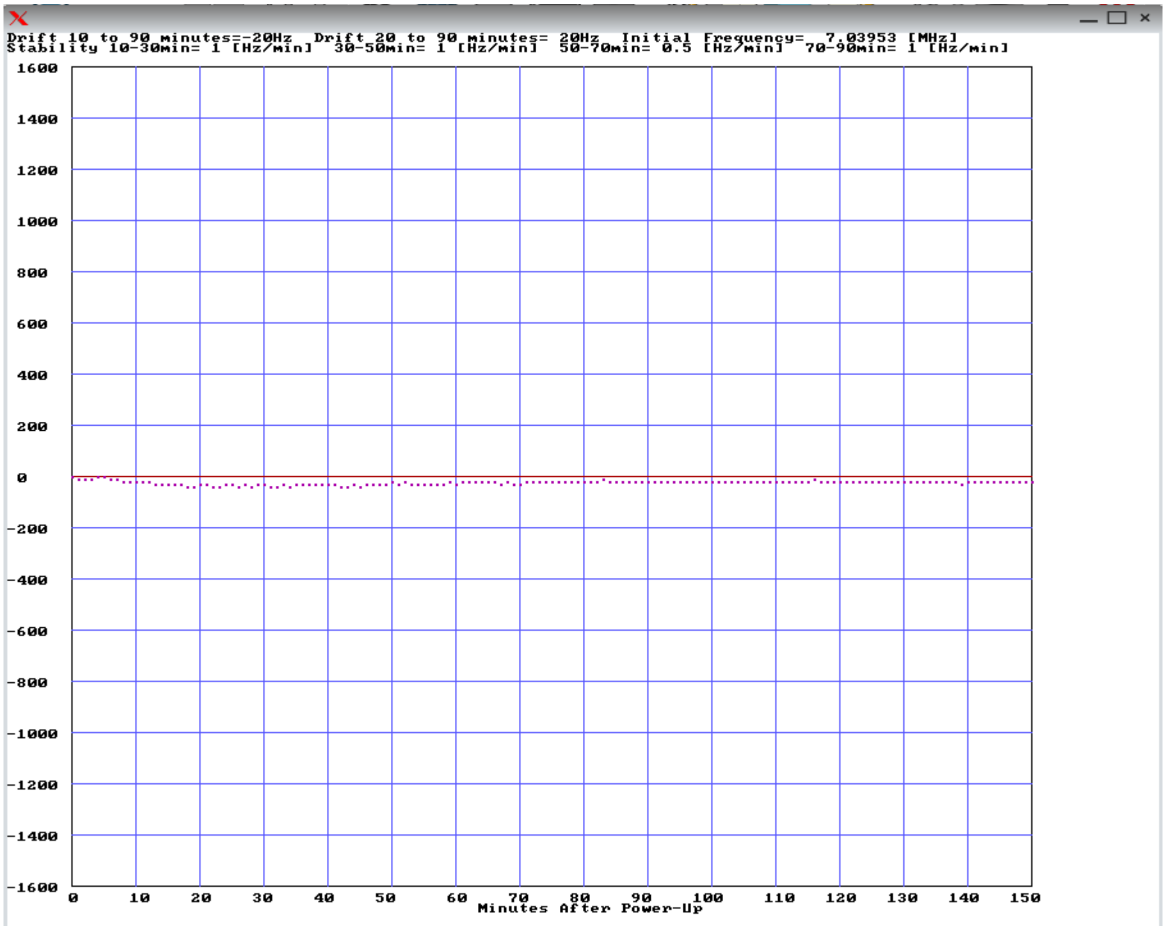
80 Meter Warm-Up Drift Results:



40 Meter Warm-Up Drift Results:



30 Meter Warm-Up Drift Results:



Discussion:
Paying attention to the Temperature Compensation process is as important as the actual construction process. Close attention to these details can pay off in better results.

1. During the VFO (and P.A.) build, I would cure epoxy and dry out flux solvent in my home's small furnace room which runs +27 to +33 C during the winter months. During summer months, placing the unit on an outdoor surface in sun worked fine. Just allow adequate time to thoroughly cure or dry.

References:
[1] Crystal Sets to Sideband copyright 2010 Frank W. Harris Rev 10.
[2] Varactor Equations: http://ricksturdivant.com/varactordiodemodeling/

Software Used in Revision 8:
LibreOffice 5.0.1.2 used for creating this document in .odt format and convert to .pdf
Inkscape 0.45.1
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