Recommended Assembly Methods for GaAs FET and HEMT Chip Form

In assembling the GaAs FET and HEMT chips onto the microstrip circuits, the following die attaching and wire bonding methods are recommended.

Precautions

1. The operation should be performed in a clean and dry environment.
2. A heater stage for die attaching, a wire bonder, tweezers and the operators should be grounded to avoid damage due to electrostatic discharge.
3. Careful attention must be paid in handling chips with tweezers because GaAs is more brittle than Si.

A. Die Attaching

1. Conditions

   Recommended die attaching conditions are as follows;

   (1) Solder : AuSn (80-20)
   (2) Die attaching atmosphere : N_2 gas
   (3) Operating temperature : 290 ± 10°C
   (4) Operating time : Less than one minute

2. Procedure

   (1) Keep the heater stage under the recommended conditions described in item 1.
   (2) Put the dielectric substrate or metals carriers of microstrip circuit on the heater stage.
   (3) Place and melt the As-Sn preform at the correct position where the die is mounted.
   (4) Press the die on the melted preform with a slight wedge and scrub several times to realize uniform adhesion as shown in Fig. 1.

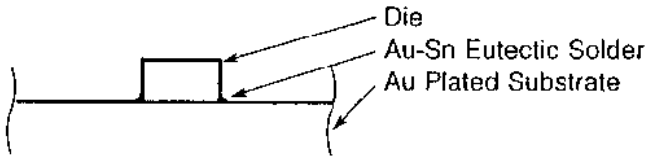


Fig. 1 Die bonding

B. Wire Bonding

1. Conditions

   Recommended wire bonding conditions are as follows;

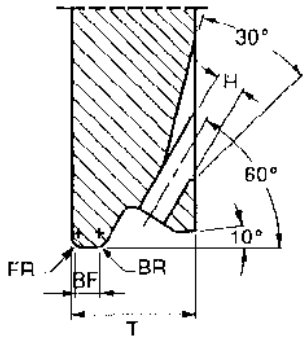
   (1) Stage temperature : 200 ± 10°C
   (2) Bonding weight : 147~176 mN
   (3) Pressure time : 0.5~1 sec.
   (4) Bonding wire : ø25 μm Au
   (5) Tip temperature : Room Temperature (Not heated)
   (6) Ultrasonic power
   Bonding pad side : Not applied (slight power can be applied)
   Substrate side : Not applied (very slight power can be applied)
   (7) Wire bonding atmosphere : N2 gas
   (8) Operating time : Less than 5 minutes

2. Recommended Bonding equipments

   (1) Bonding machine : West Bond Inc. (USA)
   Model 7400A equipped with Uti-Sonic-Power Supply, Model 10G
   (2) Work holder : Standard parts for Model 7400A
   (3) Temperature Controller : West Bond Inc. (USA), Model 1200A
   (4) Bonding wedge : Small Precision Tools Co. (USA),
   Model M60B-W-2007-S-F
   Wire feeding angle is 60 degree as shown in Fig. 2.
   H = 38 mm
   BR = 10 mm
   FR = 10 mm
   BF = 18 mm
   T = 203 mm

3. Procedure

   (1) Keep the bonding equipments under the recommended conditions described in item 1.
   (2) Put the substrate with FET die on the work holder.
   The substrate should be tightly fixed on the work holder.
   (3) Bond first to the substrate side.
   (4) Bond to the pad of the FET die side.
   (5) The following special two attentions should be paid in adjusting Model 7400A wire bonder.
   (a) Auto pull cut of the wire must be made in adequate timing in order to avoid the pad peeling.
   For example, good timing and bad timing, when auto pull cut, are shown in Fig.3 and Fig. 4 respectively.



H = 38 μm
BR = 10 μm
FR = 10 μm
BF = 18 μm
T = 203 μm

Fig. 3 Good timing example of auto pull cut.

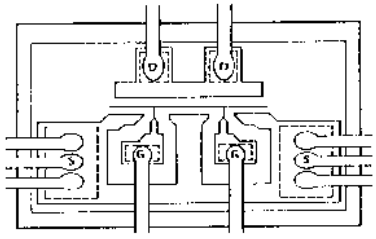
The wire on the pad is pulled in a condition where the wedge continues to pres the wire even after the wire is sufficiently smashed as shown in Fig. 3.

Fig. 4. Bad timing of auto pull cut.

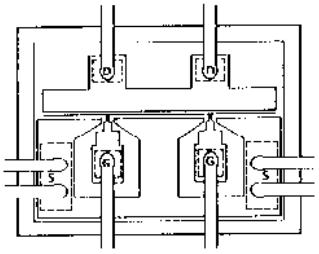
The wire on the pad is pulled after the wedge is slightly raised as shown in Fig. 4.

(b) Do not apply the ultrasonic power for the bonding to the pad. The ultrasonic power might be cause of the pad peeding. For the bonding to the substrate, the ultrasonic power, if possible, can be very slightly applied.

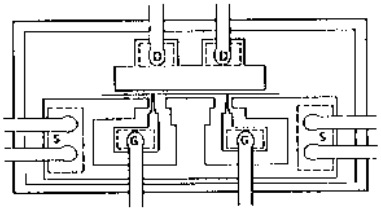
C. Bond-Wire Layout



JS8901/02/05/10/11 AS

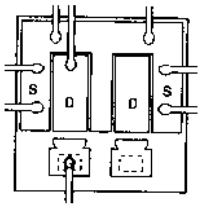


JS8818/18A/19-AS

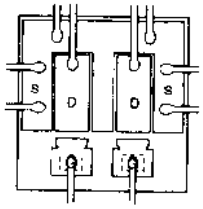


JS8830-AS

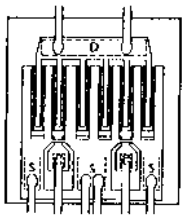
Bond-Wire Layout



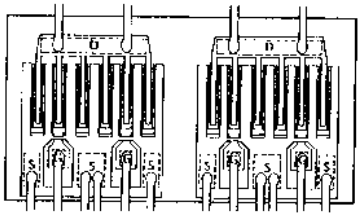
JS8834-AS



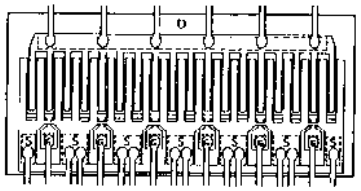
JS8835-AS



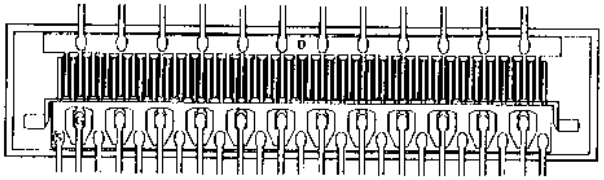
JS8836A-AS



JS8837A-AS

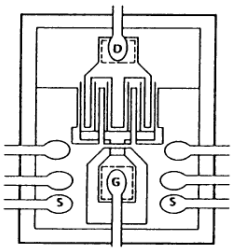


JS8838A-AS

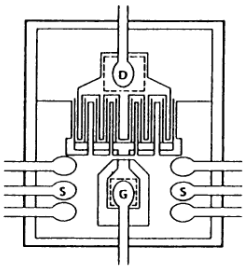


JS8820-AS

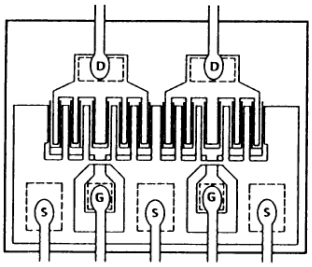
Bond-Wire Layout



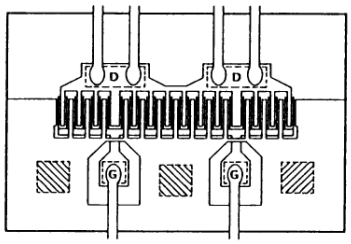
JS8850A-AS



JS8851-AS

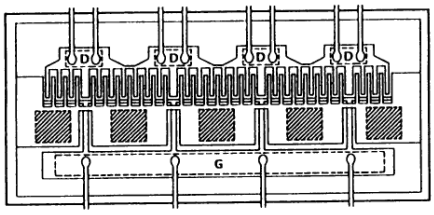


JS8852-AS

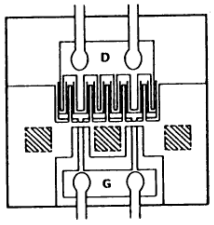


JS8853-AS

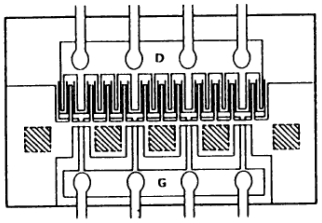
Bond-Wire Layout



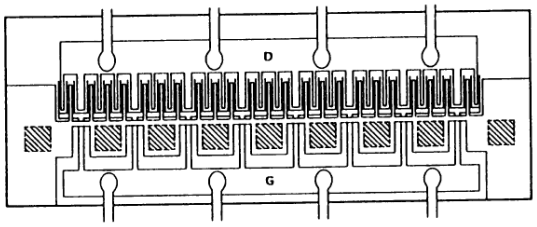
JS8855-AS



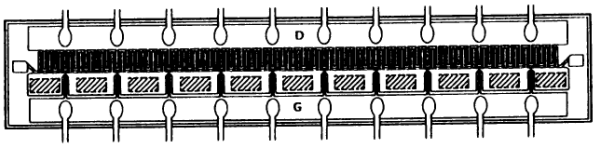
JS8892-AS



JS8893-AS



JS8894-AS



JS8856-AS

HANDLING AND OPERATING PRECAUTIONS

GaAs FET and HEMT devices should be carefully handled and operated in order to maintain the high reliability of these devices.

A. PRECAUTIONS AGAINST ELECTROSTATIC DISCHARGE

GaAs FET and HEMT devices are sensitive to electrostatic discharge. Recommended work station arrangement to protect devices from electrostatic discharge is shown in Fig. 1.

The working desk and chair should be placed on the conductive floor mat.

The working desk should be made of metal.

The conductive mat should be placed on the working desk.

And please use electrostatic precipitator (ion blower), so that the ionized air flows in the working area.

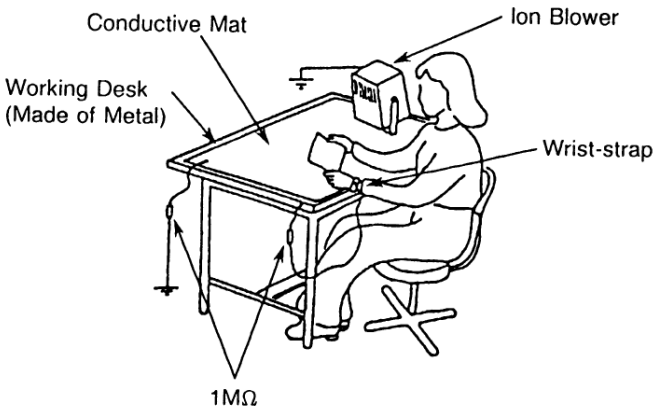


Fig. 1. Recommended Work Station Arrangement

The operator should not wear nylon gloves.
The working desk, conductive floor mat, ion blower and wrist-strap should be grounded.
In addition, assembly/test equipments should be grounded, too.
Do not touch the gate and the drain lead of the FETs.

B. STORING PRECAUTIONS

All devices should be stored in a clean, dust-free and dry environment. Especially, chip devices should be stored in dry nitrogen environment.

C. SCREW MOUNTING

The flange of the device should be attached using screws. Recommended torque is shown in Table 1.
Unless recommended torque is used, the package may be damaged or the channel temperature of the device may become exssecively high.

Table 1

Package Code	Recommended Torque	Maximum Torque
2-3H1B 2-3K1B 2-4J1B	0.08 N • m	0.10 N • m
2-7C1b 2-9C1B 2-9D2A 2-16G1B	0.25 N • m	0.30 N • m
2-11C1B 2-11D1B	0.45 N • m	0.50 N • m

D. Recommended Operating Conditions

We recommend the following conditions for reliable long life operation.
Recommended drain voltage (V_{DS}), gate current (I_{GS}), gate resistance (Rg) and channel temperature (Tch) are as follows:

Recommended Conditions

Product	VDS (V)	IGS (mA)	Rg (Ω)	Tch (°C)
Low Noise GaAs FETs	≦ 3.0	–	–	≦ 150
Low Noise HEMTs (JS8901/02/05/11-AS)	≦ 2.0			
Low Noise HEMTs (JS8910-AS)	≦ 1.5			≦ 125
Power GaAs FETs (except for JS8856/92/93/94-AS)	≦ 10.0	≦ R.O.C. Refer Table I-IV	≦ Recommended values Refer Table I-IV	≦ 150
Power GaAs FETs (JS8856-AS)	≦ 9.0			
Power GaAs FETs (JS8892/93/94-AS)	≦ 7.0			
Internally Matched Power GaAs FETs (L, C Band)	≦ 10.0			
Internally Matched Power GaAs FETs (X, Ku Band)	≦ 9.0			

Table I. Gate Current of Medium Power GaAs FETs under RF Operating Condition

Type No.	M.A.G.C.* (mA)	R.O.C.**		Recommended Rg Value (Ω)
		Forward (mA)	Reverse (mA)	
<GBAND>				
JS8834-AS	0.4	0.15	0.08	100
S8834	0.4	0.15	0.08	100
JS8835-AS	0.8	0.3	0.16	100
S8835	0.8	0.3	0.16	100
JS8836A-AS	2.4	0.9	0.5	100
S8836A/S8836B	2.4	0.9	0.5	100
JS8837A-AS	4.8	1.8	1.0	100
S8837A	4.8	1.8	1.0	100
JS8838A-AS	7.2	2.7	1.5	100
S8838A	7.2	7.7	1.5	100
JS8820-AS	15.0	5.0	3.0	100
<Ku-BAND>				
JS8850A-AS	1.3	0.3	0.12	100
S8850A	1.3	0.3	0.12	100
JS8851-AS	2.6	0.6	0.25	100
S8851	2.6	0.6	0.25	100
JS8853-AS	6.0	1.5	0.6	100
S8853	6.0	1.5	0.6	100
JS8855-AS	12.0	3.0	1.2	100
S8855	12.0	3.0	1.2	100
JS8856-AS	24.0	6.0	2.4	100
<K-BAND>				
JS8892-AS	1.1	0.25	0.1	100
JS8893-AS	2.2	0.5	0.2	100
JS8894-AS	4 4	1.0	0.4	100

* : Maximum Allowable Gate Current
** : Reasonable Operating Current

Table II. Gate Current of L, S-Band Non-Matched and Partially Matched Power GaAs FETs Under RF Operating Condition

Type No.	M.A.G.C.* (mA)	R.O.C.**		Recommended Rg Value (Ω)
		Forward (mA)	Reverse (mA)	
<L, S-BAND>				
TPM 1617-8	30	10	6	150
TPM1617-16	60	20	12	100
TNM 1800-7	25	9	6	120
TPM1818-14	55	18	11	60
TPM1818-30	105	35	21	30
TPM2323-14	55	18	11	60
TPM2323-30	105	35	21	30
TNM2600-7	25	9	6	120
TPM2626-14	55	18	11	60
TPM2626-30	105	35	21	30

* : Maximum Allowable Gate Current
** : Reasonable Operating Current

Table III. Gate Current of C-Band Internally Matched Power GaAs FETs Under RF Operating Condition

Type No.	M.A.G.C.* (mA)	R.O.C.**		Recommended Rg Value (Ω)
		Forward (mA)	Reverse (mA)	
<C-BAND>				
TIM3742-4/4L	15	5	3	150
TIM3742-8/-8L	30	10	6	150
TIM3742-16/-16L	60	20	12	100
TIM3742-30L	100	35	21	28
TIM4450-4/-4L	15	5	3	150
TIM4450-8/-8L	30	10	6	150
TIM4450-16/-16L	60	20	12	100
TIM4450-30L	100	35	21	28
TIM4951-4	15	5	3	150
TIM4951-8	30	10	6	150
TIM4951-16	60	20	12	100
TIM4951-30L	100	35	21	28
TIM5053-4	15	5	3	150
TIM5053-8	30	10	6	150
TIM5053-16/-16L	60	20	12	100
TIM5053-30L	100	35	21	28
TIM5359-4	15	5	3	150
TIM5359-8	30	10	6	150
TIM5359-16	60	20	12	100
TIM5359-30L	100	35	21	28
TIM5964-4/-4A/-4L/4SL	15	5	3	150
TIM5964-7L	25	8	5	150
TIM5964-8/-8A/-8L/8SL	30	10	6	150
TIM59ff4-14L	50	17	10	100
TIM5964-16/-16L/-16LA/ 16SL	60	20	12	100
TIM5964-30L	100	35	21	28
TIM6472-4/-4L/4SL	15	5	3	150
TIM6472-7L	25	8	5	150
TIM6472-8/-8L/8SL	30	10	6	150
TIM6472-14L	50	17	10	100
TlM6472-16/16L/16SL	60	20	12	100
TlM6472-30L	100	35	21	28
TIM7179-4	15	5	3	150
Tl M7179-7L	25	8	5	150
TIM7179-8/-8L	30	10	6	150
TIM7179-14L	50	17	10	100
TIM7179-16/-16L	60	20	12	100
TIM7785-4/4SL	15	5	3	150
TIM7785-7L	25	8	5	150

Type No.	M.A.G.C.* (mA)	R.O.C.**		Recommended Rg Value (Ω)
		Forward (mA)	Reverse (mA)	
TIM7785-8/-8L/8SL	30	10	6	150
TIM7785-14L	50	17	20	100
TIM7785-16/-16L/16SL	60	20	12	100
TIM7785-30L	100	35	21	28

* : Maximum Allowable Gate Current
** : Reasonable Operating Current

Table IV. Gate Current of X, Ku-Band Internally Matched Power GaAs FETs Under RF Operating Condition

Type No.	M.A.G.C.* (mA)	R.O.C.**		Recommended Rg Value (Ω)
		Forward (mA)	Reverse (mA)	
<X, Ku-BAND>				
TIM8596-2	24	6	2.4	150
TIM8596-4	48	12	4.8	150
TIM8596-8	96	24	9.6	150
TIMO910-2	24	6	2.4	150
TIMO9104	48	12	4.8	150
TIMO910-5	48	12	4.8	150
TIMO910-8	96	24	9.6	150
TIMO910-10	96	24	9.6	100
TIM1011-2/-2L	24	6	2.4	150
TIM1011-4/4L	48	12	4.8	150
TIM1011-5	48	12	4.8	150
TIM1011-8/-8L	96	24	9.6	150
TIM 1011-10/-10L	96	24	9.6	100
TIM 1011 -15	96	24	9.6	100
TIM1112-2	24	6	2.4	150
TIM1112-4	48	12	4.8	150
TIM1112-8	96	24	9.6	150
TIM1213-2	24	6	2.4	150
TIM 12134/-4L	48	12	4.8	150
TIM1213-8/-8L	96	24	9.6	150
TIM1213-10	96	24	9.6	100
TIM1414-2	24	6	2.4	150
TIM1414-4/4A	48	12	4.8	150
TIM 1414-5	48	12	4.8	150
TIM1414-8/-8L	96	24	9.6	150
TIM1414-10/-10A/-10L	96	24	9.6	100
TIM 1414-15	96	24	9.6	100
TIM1415-2	24	6	2.4	150
TIM1415-4	48	12	4.8	150
TIM 1415-8	96	24	9.6	150

* : Maximum Allowable Gate Current
** : Reasonable Operating Current

Channel temperature (Tch) is related to flange temperature ~Tf) as follows,

$$Tch = Tf + I_{DS} \times V_{DS} \times Rth\ (c\text{-}c)$$

where I_{DS} is drain current and Rth (c-c) is thermal resistance between channel and flange.
The flange temperature should be reduced as low as possible using heat sink block and/or blower.
The devices should be operated at RF operating conditions where input power is lower than that for obtaining output power at 1 dB gain compression.

E. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are the limits one should not exceed under any conditions and does not mean actual applicable bias condition.

F. RECOMMENDED BIASING PROCEDURE

Recommended biasing procedure is as follows:

(1) Slowly increase gate to source voltage (V_{GS}) from 0V to about - 2.5V.

(2) Gradually increase drain to source voltage (V_{DS}) form 0V to the recommended value.

(3) Adjust drain current (I_{DS}) approximately to the value shown in the inspection sheet by controlling VGS

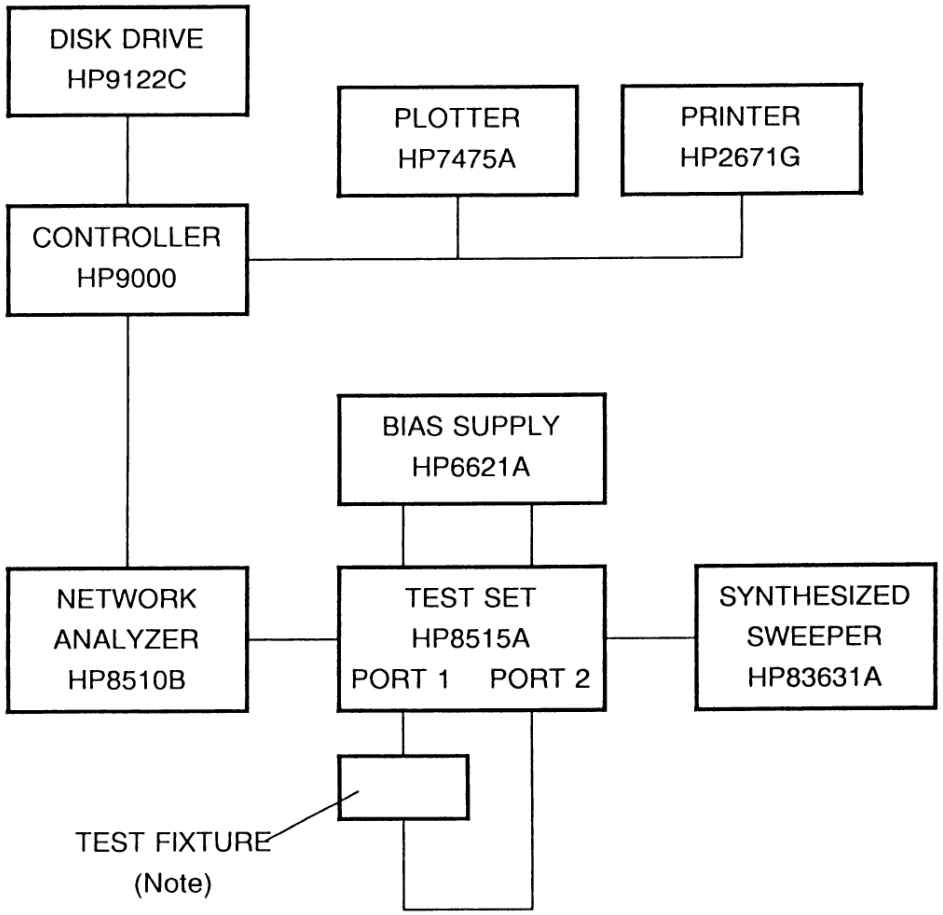
When turning off the bias, the reverse procedure should be performed.
Do not apply RF power to the devices until they are biased on. Turn off RF power before removing DC bias.

G. OTHERS

When the device is attached to amplifier case, thermal conductive grease and conductive sheet made of Indium and so forth should not be used.
They might cause degradation of the thermal resistance between package and amplifier case. They also cause might poor grounding of the source flanges.

Electrical Measurement

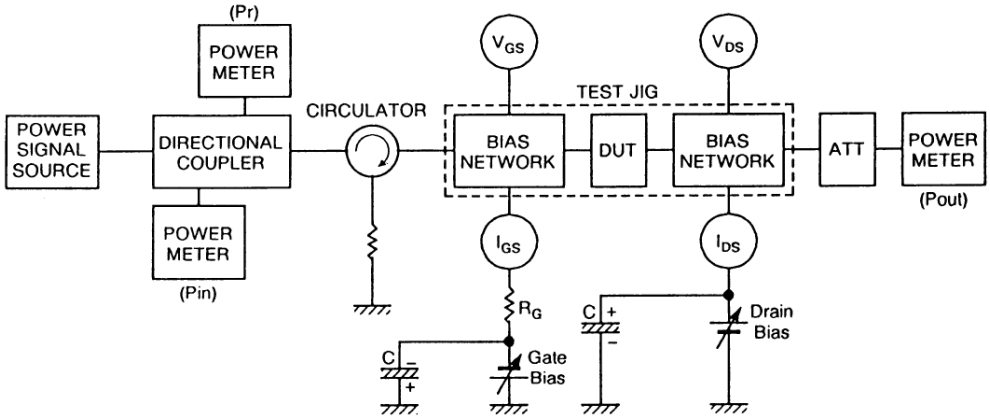
A. S-Parameter Measurement System Block Diagram



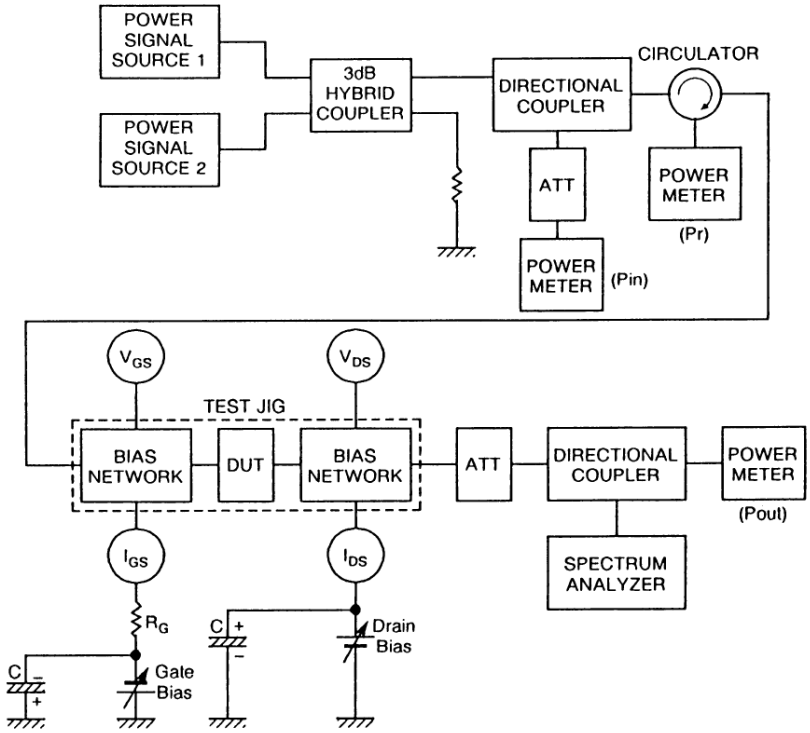
Note: USE TF-2000 MADE BY INTER-CONTINENTAL MICROWAVE.

Note: Use TF-2000 made by Inter-Contental Microwave

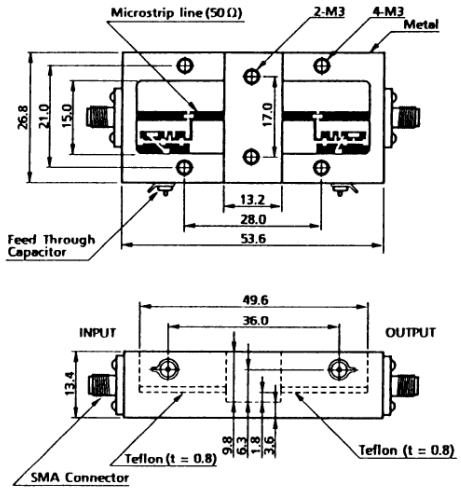
B. Po Test Block Diagram



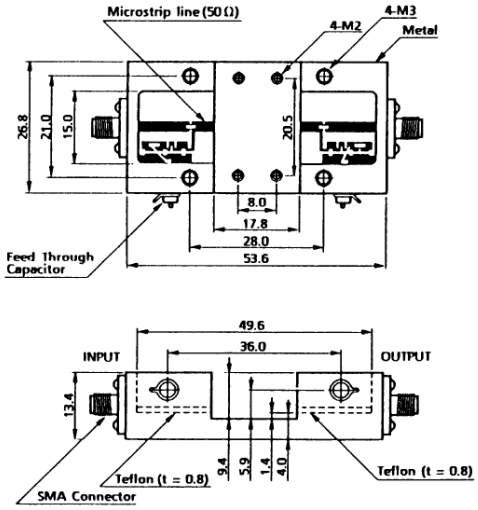
C. Outline of IM_3 & Power Test Block Diagram



D. Outline of Power Test JIG



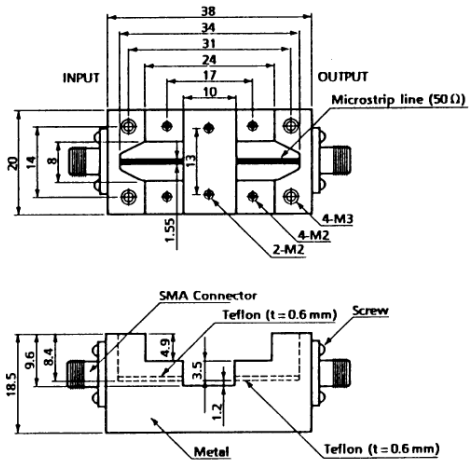
C-BAND
(4W, 7W, 8W)



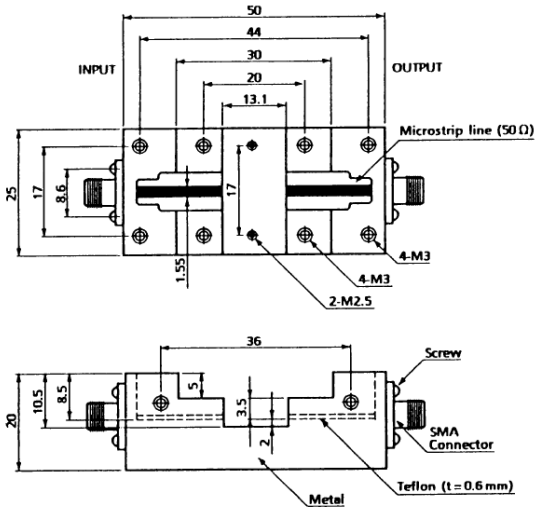
C-BAND
(14W, 16W)

(Unit in mm)

Outline of Power Test JIG



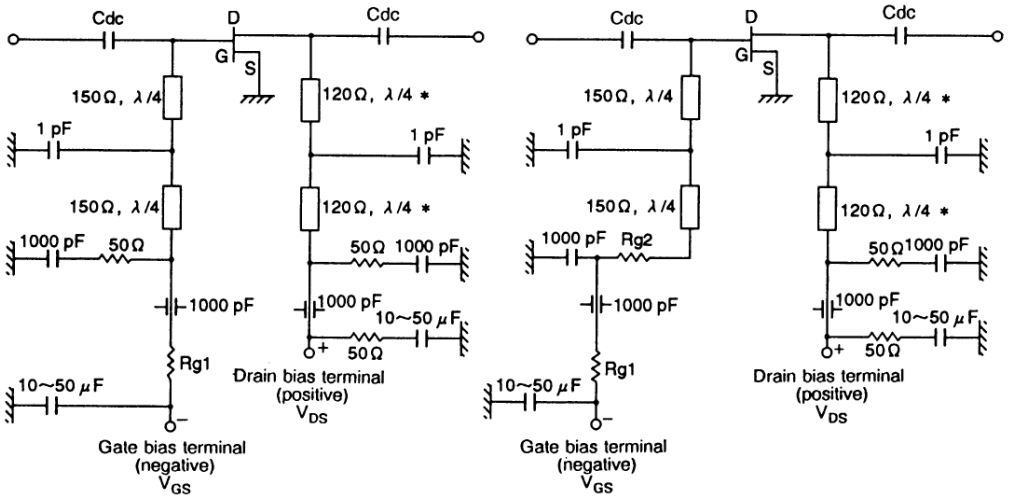
X, Ku-Band
(2W, 4W, 5W)



X, Ku-Band
(8W, 10W)

(Unit in mm)

E. Bias Circuits



Bias Circuit No. 1 **Bias Circuit No. 2**

CAUTION: The cross section of drain biasing line (*) should be made large enough to avoid its burning down.

Product		Cdc (pF)	Rg1 (Ω)	Rg2 (Ω)	Bias Circuit No.
L, S-Band	7W, 8W	10 ~ 15	120		1
	14W, 16W		60		
	30W		30		
C-Band	4W	1 ~ 2	100	50	2
	7W, 8W				
	14W, 16W		50		
	30W		10	18	
X, Ku-Band	2W, 4W, 5W		100	50	
	8W				
	10W, 15W		50		

F. METHOD FOR THERMAL RESISTANCE MEASUREMENT

The thermal resistance of GaAs FETs can be measured by using drain to source voltage (V_{DS}) pulse to produce varying voltages across the forward biased gate to source junction, as shown in Fig. A. The constant gate forward current (I_M) is chosen small enough not to cause the device heating excessively nor burn-out but of sufficient magnitude to ensure reliable readings of V_{GSF}.

When heating power (I_{DS} X V_{DS}) is applied to the FET during the time period T, the channel temperature increases and V_{GSF} decreases, due to the temperature characteristics of V_{GSF} shown in Fig. B. After a sufficient time to ensure that the channel temperature has stabilized at its new value, V_{DS} is quickly reduced to zero. If V_{GSF1} and V_{GSF2} are the values of V_{GSF} before and afler heating, the difference $\Delta V_{GSF} = V_{GSF1} - V_{GSF2}$ is related to the channel temperature increase (ΔTch) as follows;

$$\Delta V_{GSF} = Tch/K$$

where K is the temperature coefficient for V_{GSF} under constant I_M.

Using ΔTch determined by above equation, the thermal resistance Rth (c-c) between channel and flange of the FET is obtained as follows;

$$Rth\ (c\text{-}c) = \Delta Tch/(I_{DS} \times V_{DS}) = (K \times \Delta V_{GSF})/(I_{DS} \times V_{DS})\ (°C/W)$$

The thermal resistance value obtained by the above electrical measurement is calibrated by IR (Infra-Red) measurement results. Because IR measurement has better resolution than the above measurement technique.

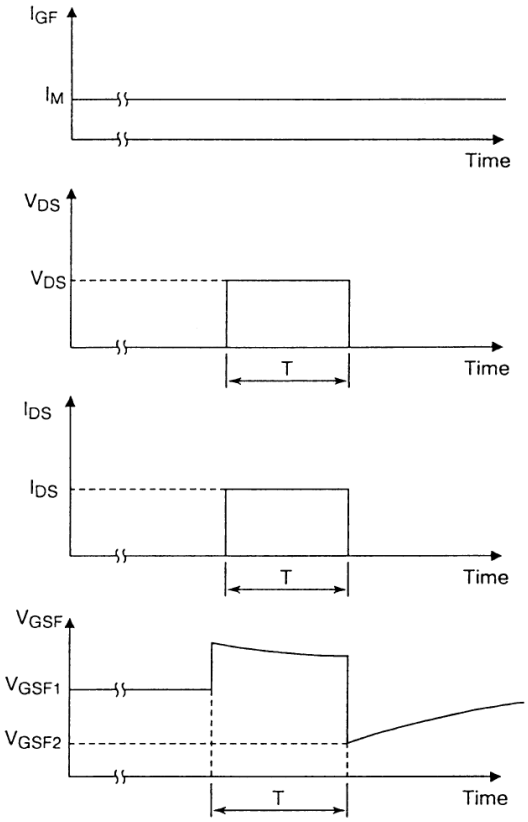


Fig. A. Timing Diagram

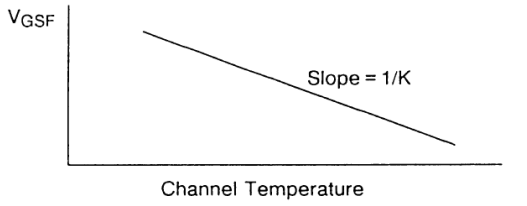
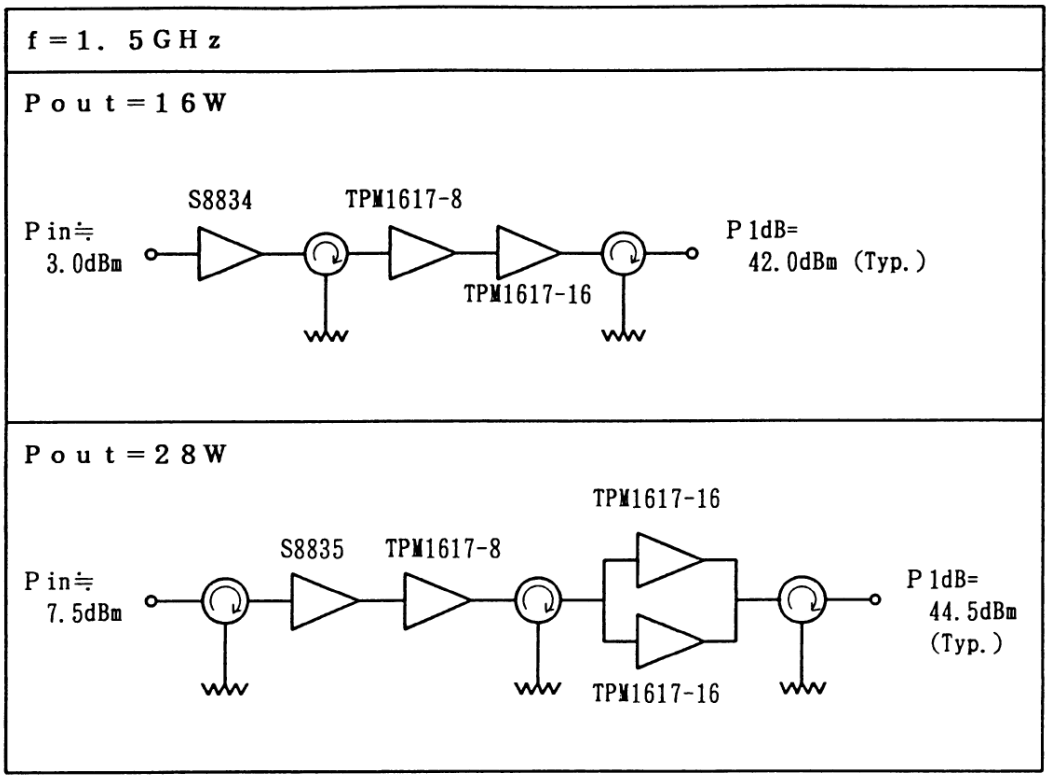


Fig. B. Forward Biased Gate to Source Voltage vs. Channel Temperature.

Recommended Line-Up

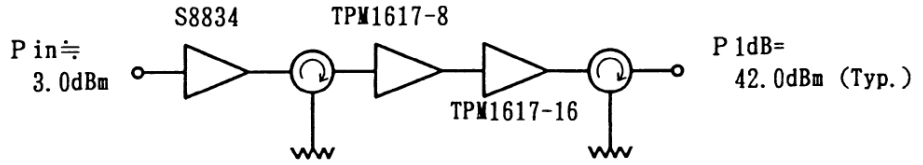
A. L-Band Line-Ups



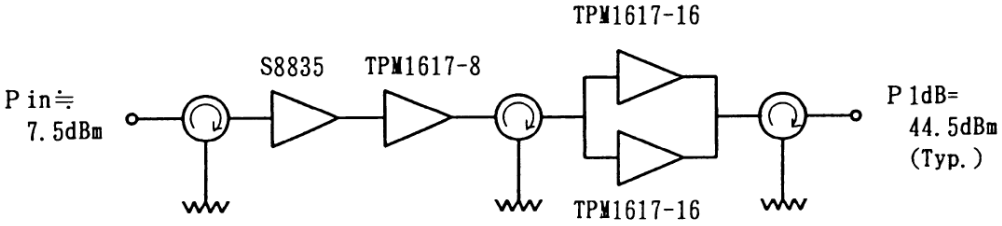
L-Band Line-Ups

f＝1．6～1．7GHz

Pout＝16W



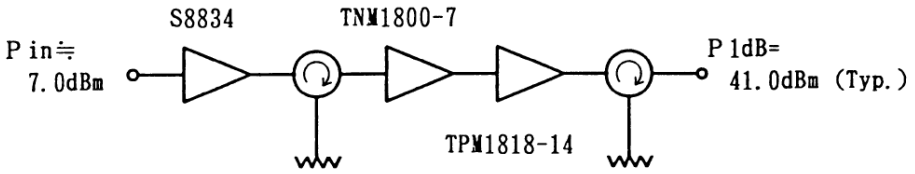
Pout＝28W



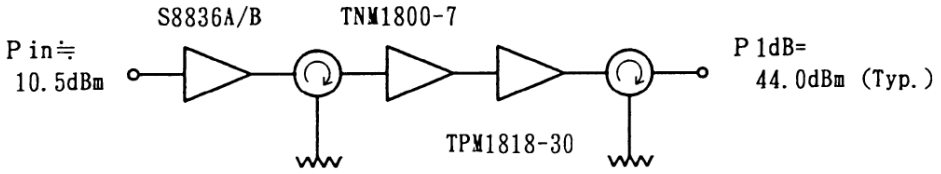
L-Band Line-Ups

f = 1. 8 GHz

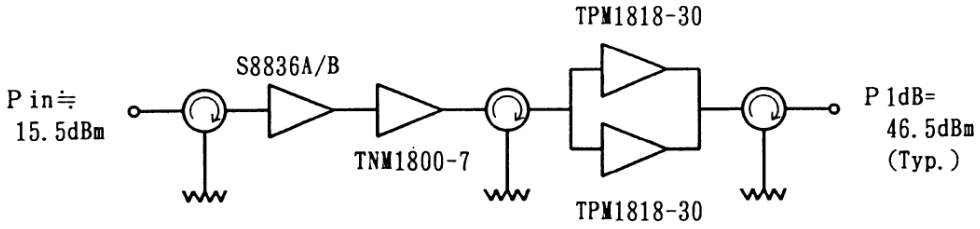
Pout = 12. 5W



Pout = 25W



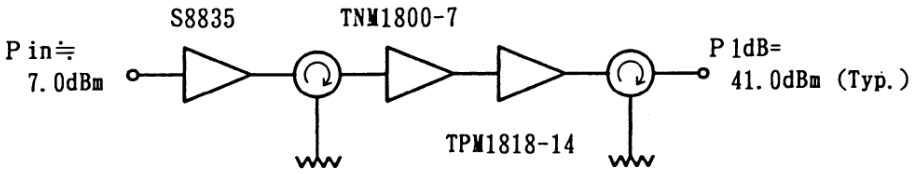
Pout = 44. 5W



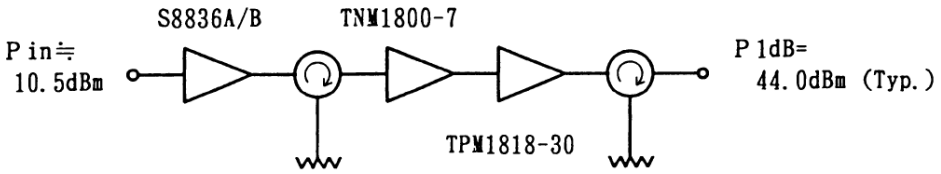
L-Band Line-Ups

f = 1. 9 GHz

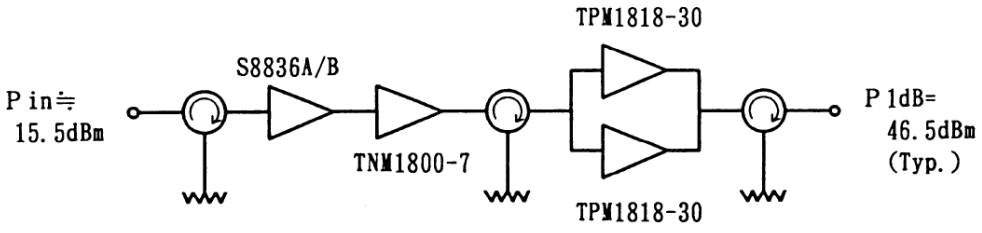
Pout = 12. 5W



Pout = 25W



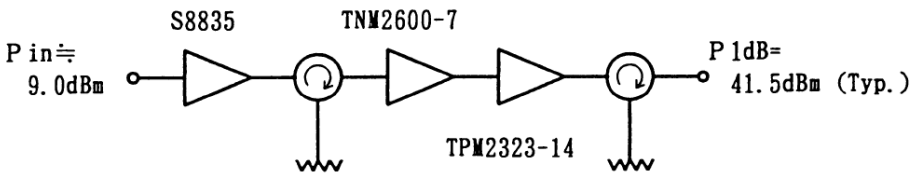
Pout = 44. 5W



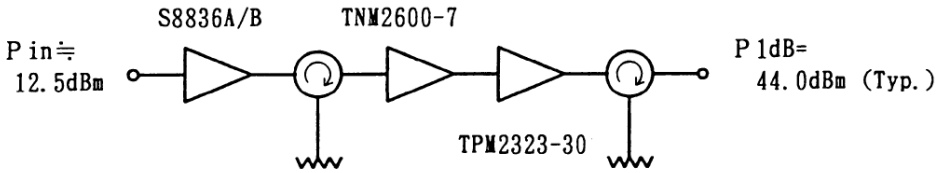
B. S-Band Line-Ups

f = 2. 3 GHz

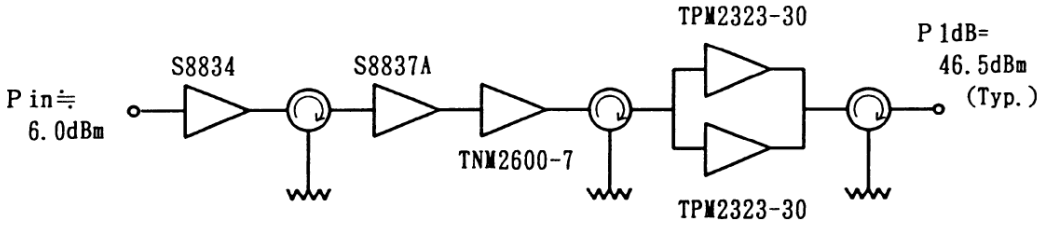
Pout = 14W



Pout = 25W



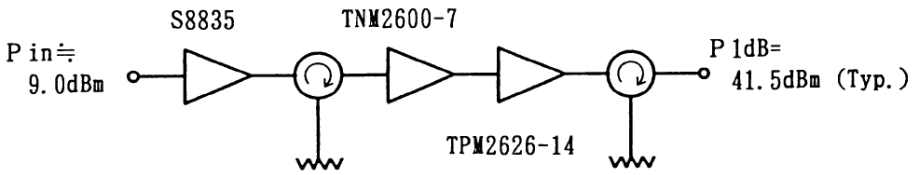
Pout = 44. 5W



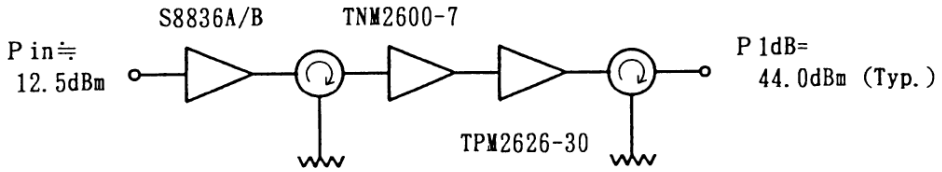
S-Band Line-Ups

f = 2. 6 GHz

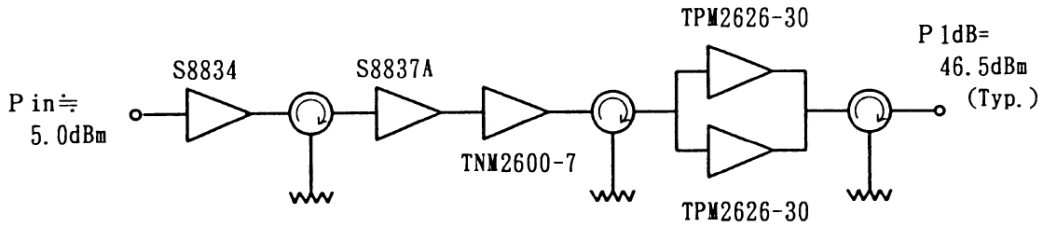
Pout = 14 W



Pout = 25 W



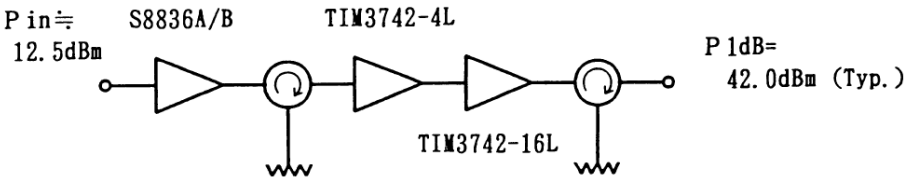
Pout = 44. 5 W



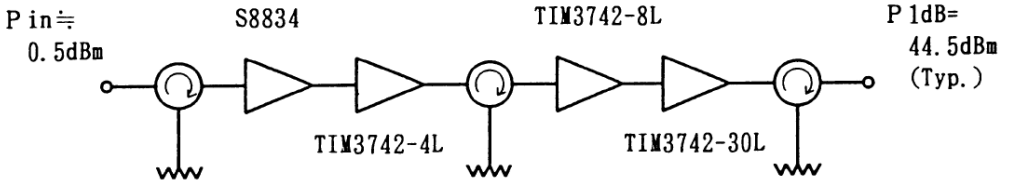
C. C-Band Line-Ups

f＝3．7～4．2GHz

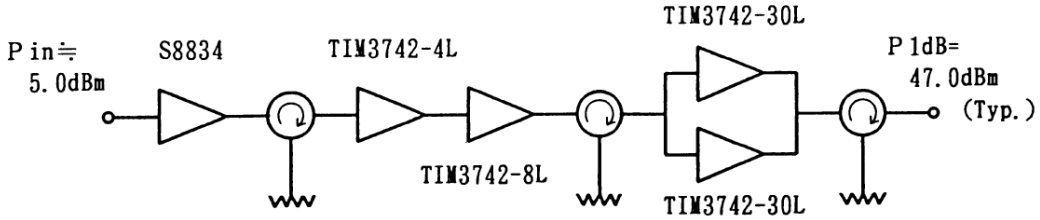
Pout＝16W



Pout＝28W



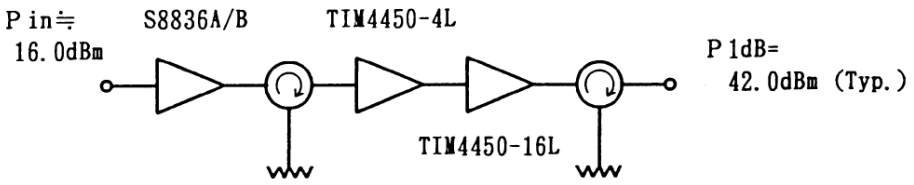
Pout＝50W



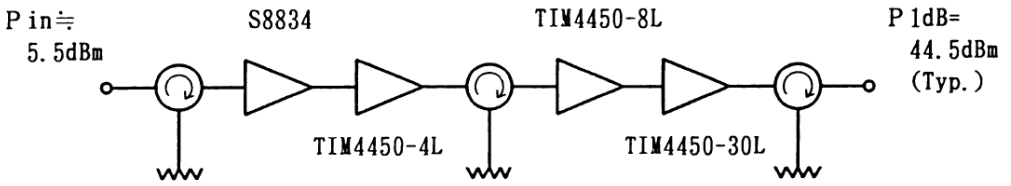
C-Band Line-Ups

f = 4. 4 ~ 5. 0 GHz

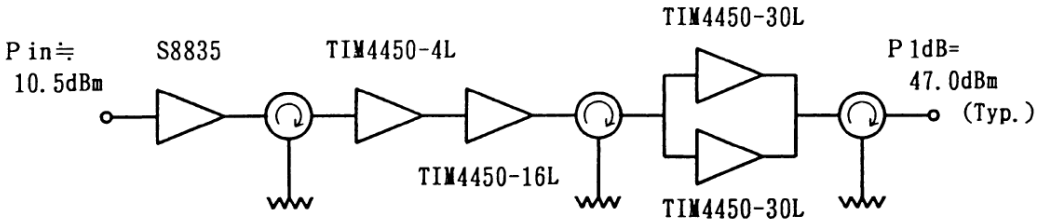
P o u t = 1 6 W



P o u t = 2 8 W



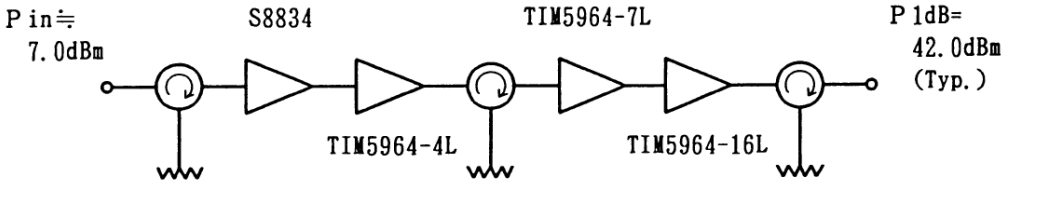
P o u t = 5 0 W



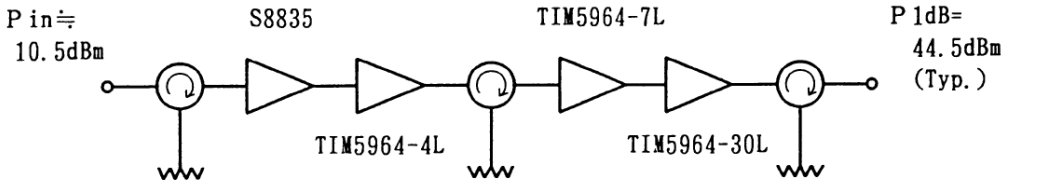
C-Band Line-Ups

f＝5．9～6．4GHz

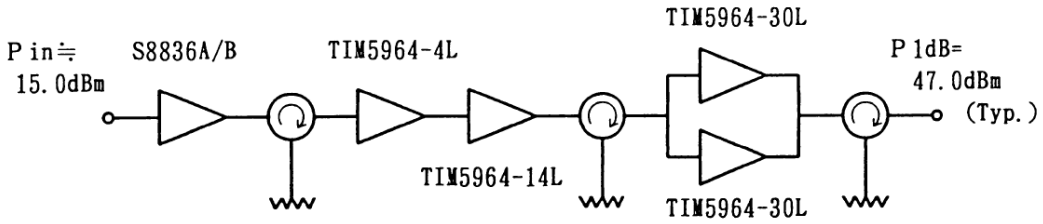
Pout＝16W



Pout＝28W



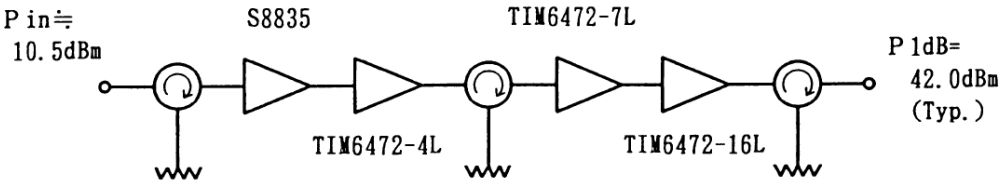
Pout＝50W



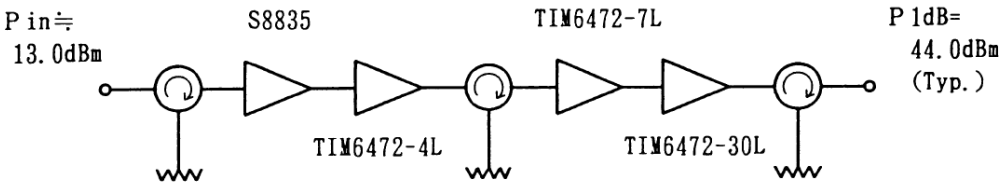
C-Band Line-Ups

f = 6. 4 ~ 7. 2 GHz

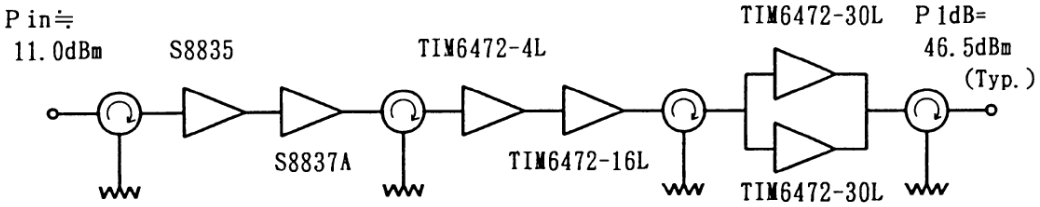
Pout = 16W



Pout = 25W



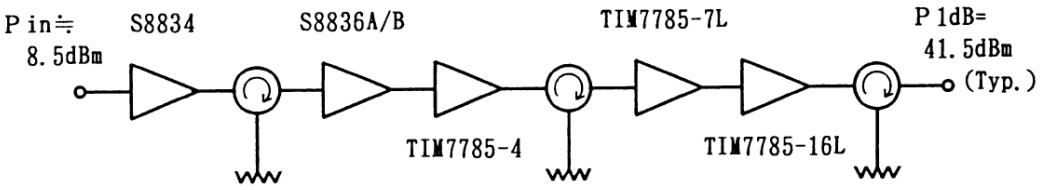
Pout = 45W



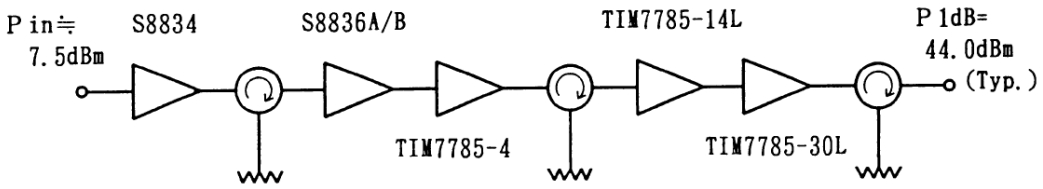
C-Band Line-Ups

f＝7．7～8．5GHz

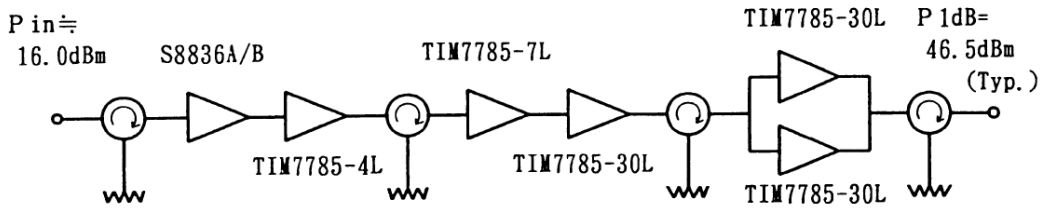
Pout＝14W



Pout＝25W



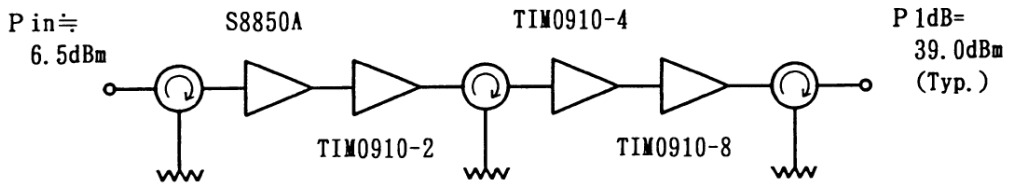
Pout＝45W



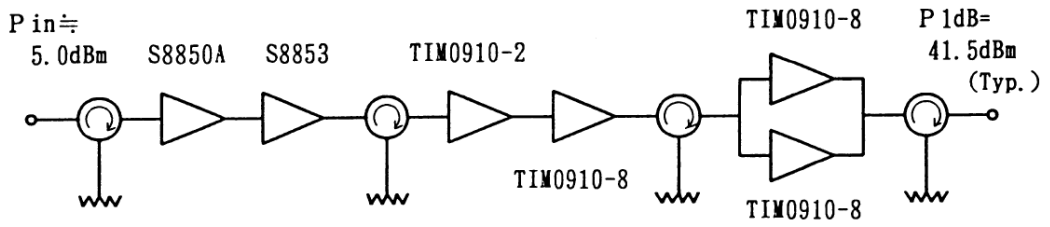
D. X-Band Line-Ups

f＝9．5～10．5GHz

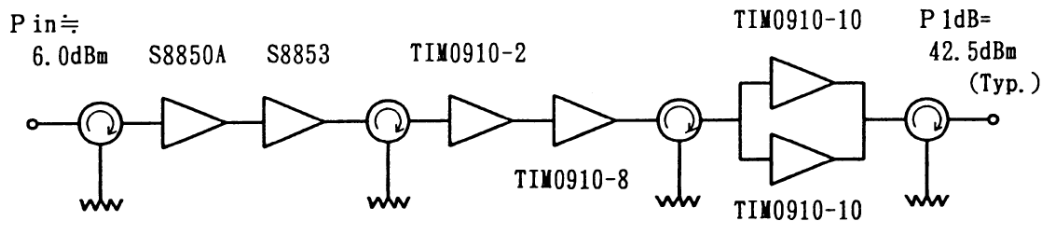
Pout＝8W



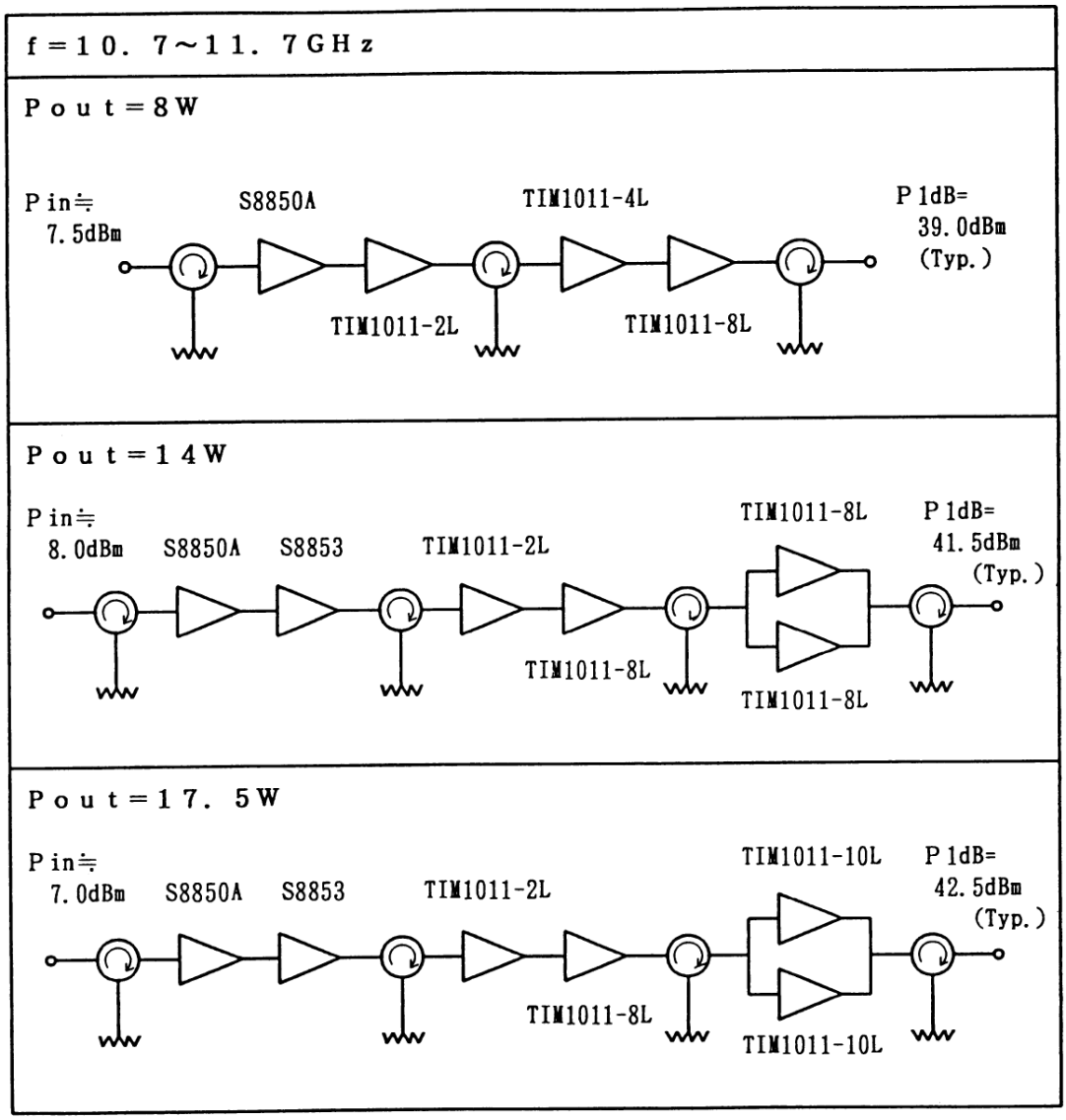
Pout＝14W



Pout＝17．5W



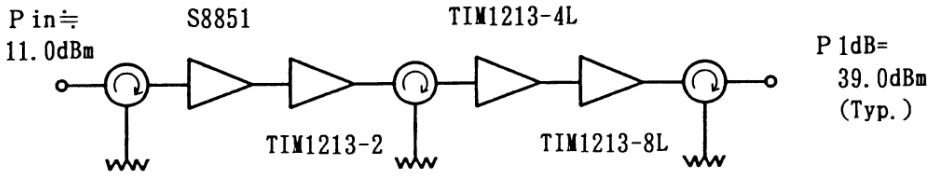
X-Band Line-Ups



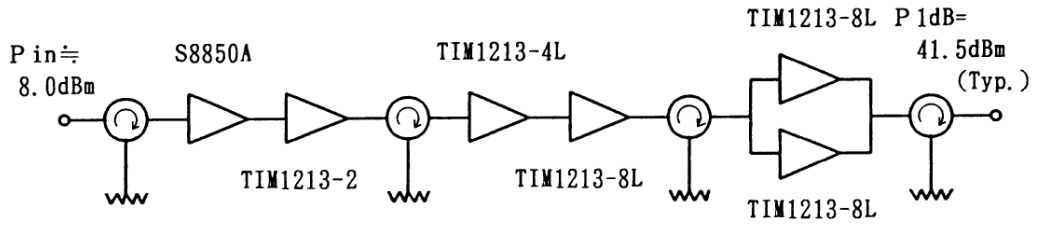
E. Ku-Band Line-Ups

f＝12．7～13．2GHz

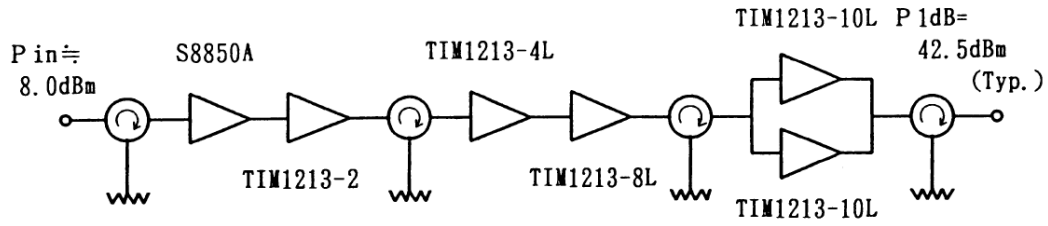
Pout＝8W



Pout＝14W



Pout＝17．5W



Ku-Band Line-Ups