

FMM5049VT

L,S-Band Power Amplifier MMIC

FEATURES

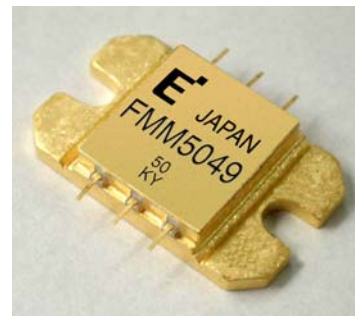
- High Output Power: Pout=41.0dBm (typ.)
- High Linear Gain: GL=33.0dB (typ.)
- Broad Band: 1.8~2.3GHz
- Hermetically sealed Package

DESCRIPTION

The FMM5049VT is a high-gain wide-band three-stage MMIC amplifier designed for PCS/PCN and W-CDMA application as a driver or output stage in the 1.8-2.3GHz band. The device is partially matched.

This product is uniquely suited for use in base station amplifiers as it offers high gain, long term reliability and ease of use.

Eudyna's stringent Quality Assurance Program assures the highest reliability and consistent performance.



RECOMMENDED OPERATING CONDITION (Case Temperature Tc=25°C)

Item	Symbol	Condition	Unit
DC Input Voltage	VDD1,2	10	V
DC Input Voltage	VGG	-5	V
Input Power	Pin	≤12	dBm

ELECTRICAL CHARACTERISTICS (Case Temperature Tc=25°C)

Item	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Output Power	Pout	VDD1,2 =10V VGG=-5.0V f=2.2GHz Pin=12dBm (Note 2)	39.0	41.0	-	dBm
Linear Gain (Note 1)	GL		30.0	33.0	-	dB
Total Drain Current	IDDt		-	4.0	-	A
Total Gate Current	IGG		-	70	-	mA
DC Input Current	IDD(DC)	Without RF	-	2.5	-	A

Note 1 : Pin < -6dBm

Note 2 : The RF parameters are measured with a tuned test fixture. (The tuning condition is on Page 6)

CASE STYLE: VT

ESD	Class I	200 ~ 499 V
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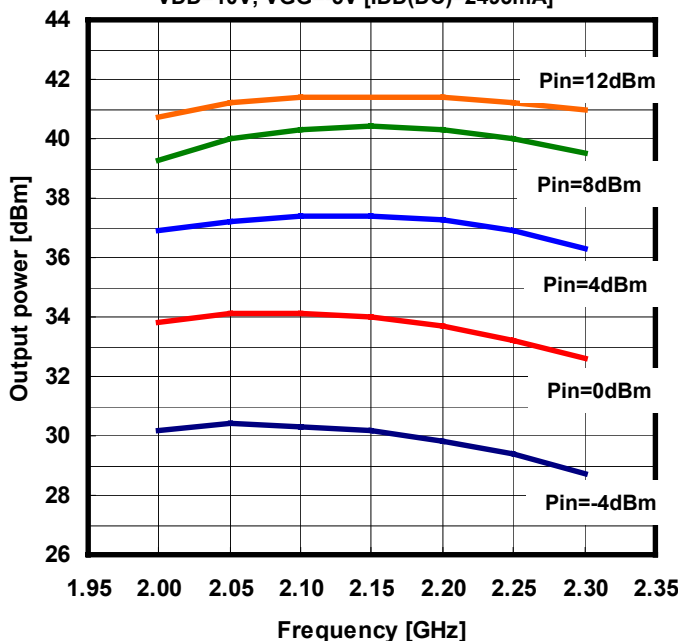
Note : Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5kΩ)

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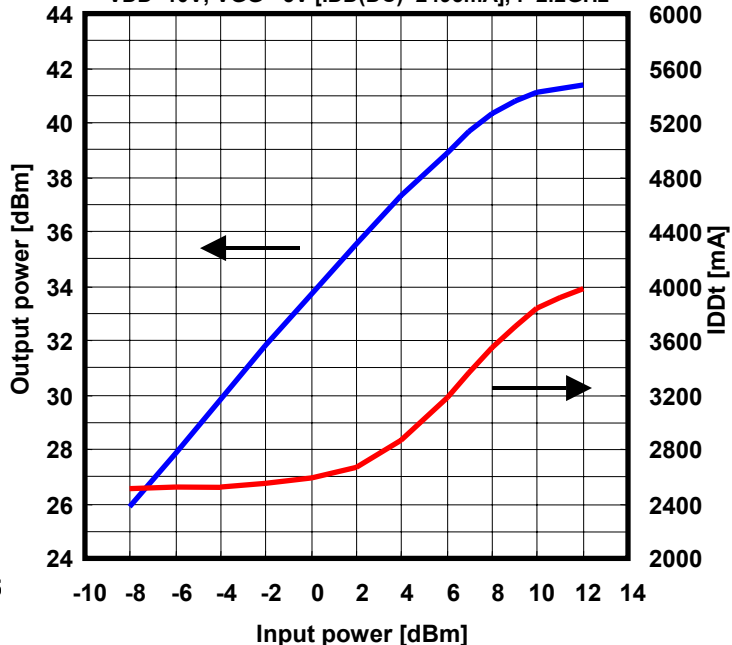
OUTPUT POWER vs. FREQUENCY

VDD=10V, VGG=-5V [IDD(DC)=2495mA]



OUTPUT POWER, IDDT vs. INPUT POWER

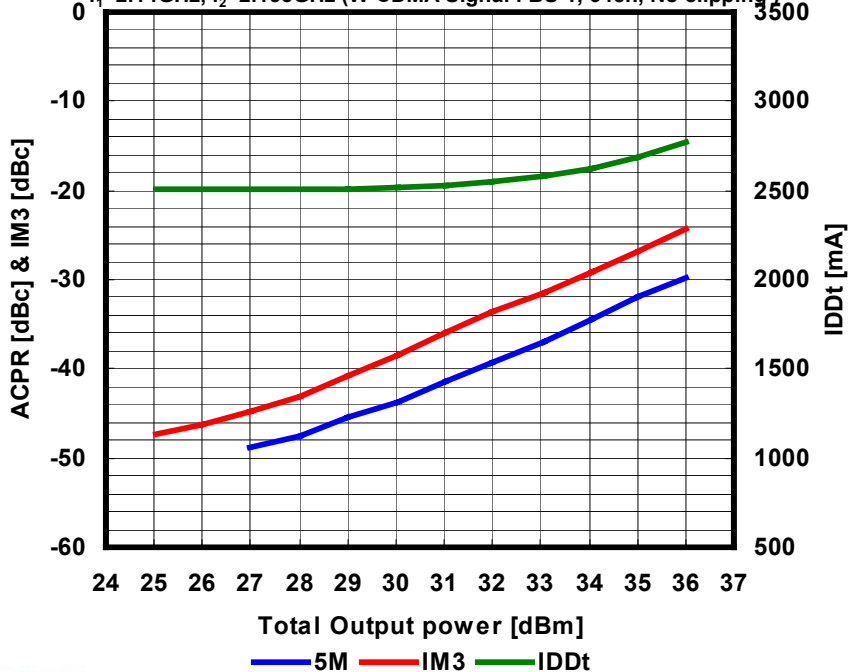
VDD=10V, VGG=-5V [IDD(DC)=2495mA], f=2.2GHz



ACPR, IM3 vs TOTAL OUTPUT POWER

VDD=10V, VGG=-5V [IDD(DC)=2495mA]

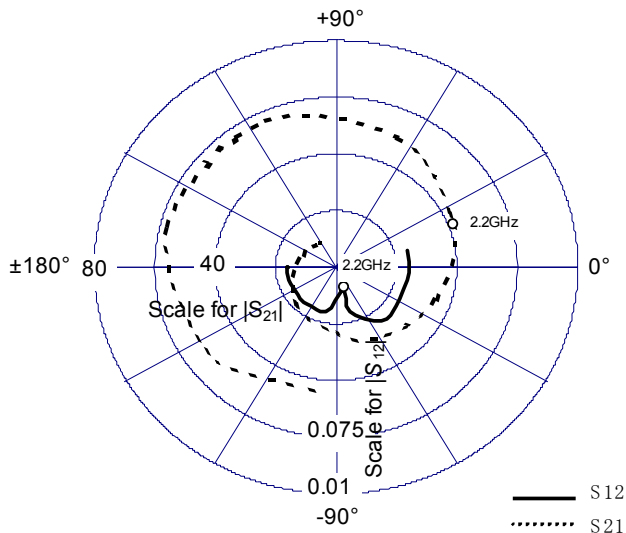
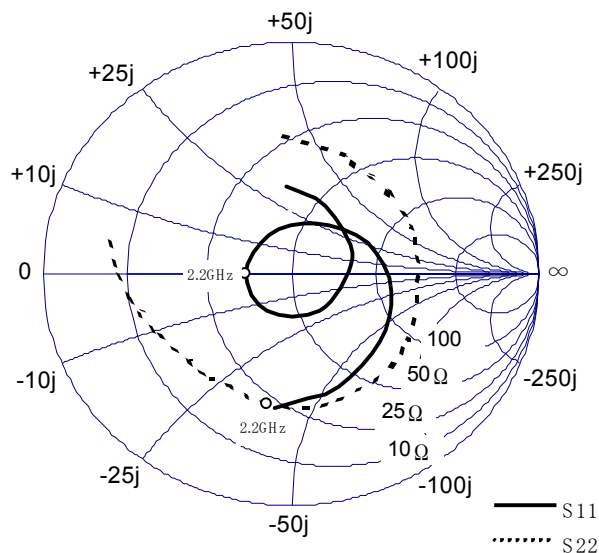
f₁=2.14GHz, f₂=2.155GHz (W-CDMA Signal : BS-1, 64ch, No clipping)



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■ S-PARAMETER



VDD1,2=10V, VGG=-5V

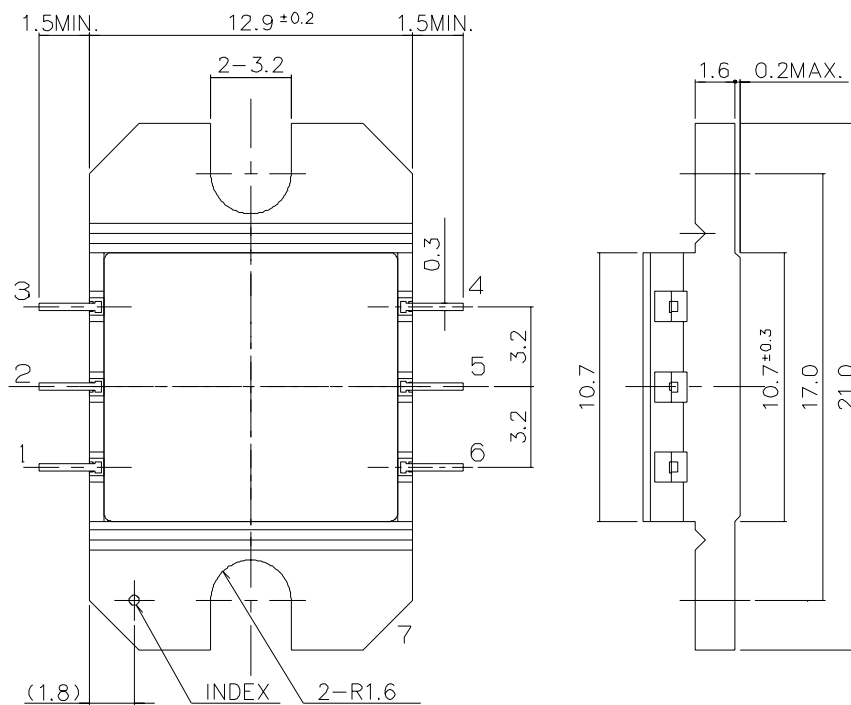
Freq [GHz]	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.7	0.37	92.6	44.40	-99.2	0.003	14.1	0.59	93.0
1.8	0.32	65.1	51.52	-144.4	0.003	-4.0	0.54	63.0
1.9	0.25	15.6	57.84	165.5	0.003	-34.5	0.52	17.2
2.0	0.20	-55.3	56.73	114.1	0.003	-51.8	0.56	-36.7
2.1	0.19	-121.9	49.89	65.6	0.002	-73.8	0.58	-75.4
2.2	0.18	179.1	41.99	21.2	0.001	-69.6	0.57	-99.7
2.3	0.19	118.2	35.14	-20.9	0.001	-78.6	0.54	-116.1
2.4	0.24	65.6	28.49	-62.0	0.001	-73.6	0.56	-128.5
2.5	0.34	23.9	22.19	-96.5	0.002	-102.5	0.57	-144.0
2.6	0.41	-11.00	19.01	-134.8	0.002	-125.7	0.60	-156.5
2.7	0.46	-39.60	14.90	-167.5	0.002	-136.7	0.66	-170.2
2.8	0.52	-68.20	11.45	155.9	0.002	-163.6	0.71	177.1
2.9	0.58	-96.60	9.73	122.1	0.002	179.7	0.75	167.1

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0.1

2.6

5.2 MAX.

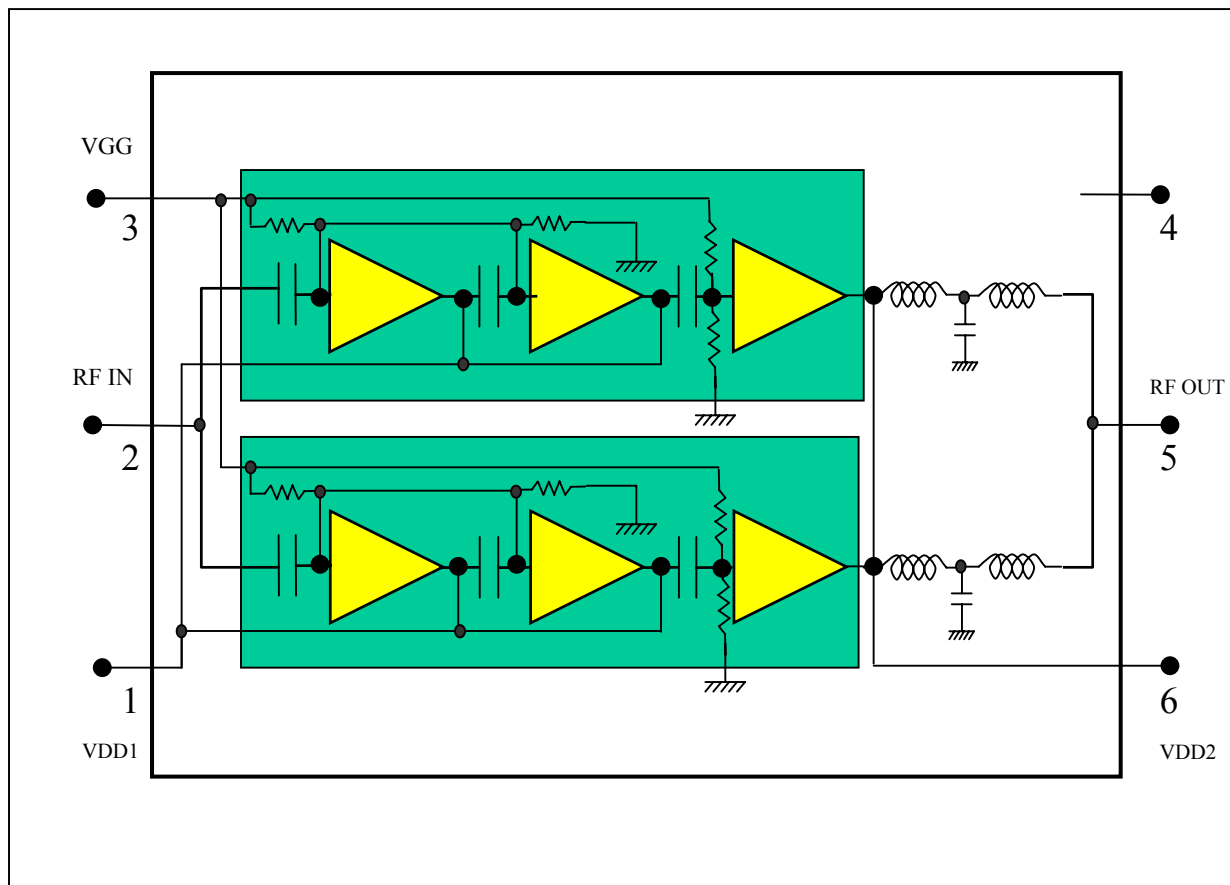


- 1.VDD1
2.RF in
3.VGG
4.NC
5.RF out
6.VDD2 (Unit : mm)
7.Source(GND) Tolerance : ± 0.15

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Internal Block Diagram



PIN ASSIGNMENT

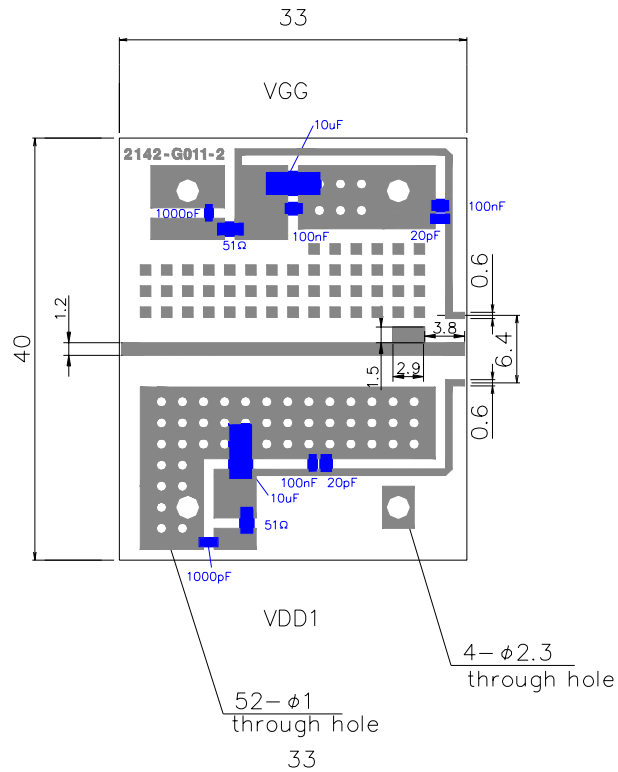
- 1 : VDD1
- 2 : RF in
- 3 : VGG
- 4 : N.C.
- 5 : RF out
- 6 : VDD2

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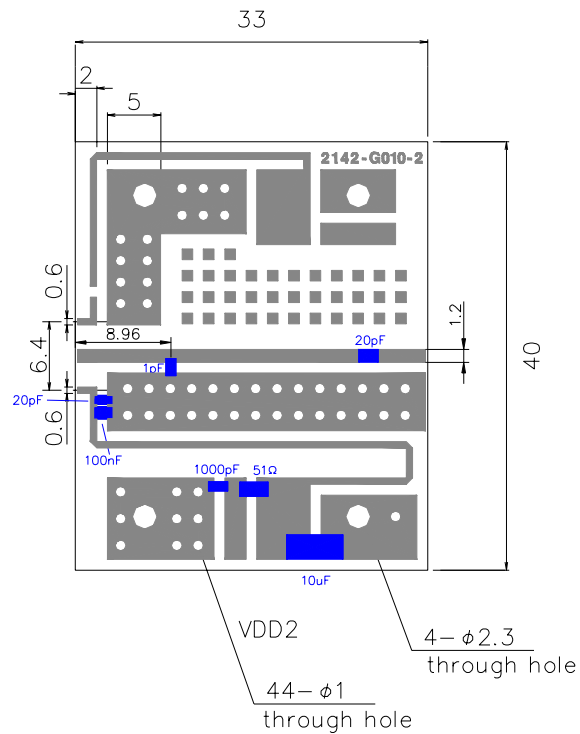
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Board Layout

<INPUT SIDE>



<OUTPUT SIDE>



εr=10.5 t=1.2mm

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