Abstract

“What is PSoC” is an application related review of programmable array systems, the system-on-chip, or PSoC.

The hardware and system requirements are explained, hand to hand with practical notes. Description of two examples of embedded wireless systems with digital data modulation follows the theory.

Keywords: PSoC, hardware, C language, wireless communication systems, Smart Power, Home Plug, Green Power, PLC.

I History

The industrial boom and dot com time during late 90’s was paved by major steps in technology and system architecture development. It usually starts with a smart idea. When somebody comes up with a new idea, others try to follow up. By my opinion, the market value of CDMA/GSM cell phones and associated Internet services influenced the R&D direction. The predicted downfall of wireless markets proved to be false. On the contrary, requirements for flexible, cheap, and performing chips with more features are shaking the industry. Design of mixed signal chips for wireless environment is always a challenge.

The wireless buzz, hum, and offsets in high resolution ADCs, DACs, audio amplifiers, and even loudspeakers focused the design to search for different system architecture and solutions. On the other hand, it pointed out the need for hardware verification platform for test and verification. Every simulation program is a very helpful tool for known problems. Sometimes we deal with the unknown.

Thinking about “who can program” the receive diversity switch, the Fractional-N synthesizer, and a call from a friend searching DSP related ideas brought my attention to PSoC chips from Cypress. After few years, I can tell it was worth of the effort.

II What is inside

There is nothing ready-to-work inside, except the downloader, internal RESET circuit, the band gap voltage reference, and the 25MHz clock source. The first generation of programmable array, the PSoC1™, was an 8-bit ASIC micro controller of Harvard architecture. The chip has a set of analog and digital ports for communication with the external world.

The digital I/O ports are configurable as inputs/outputs, open collector, or fast digital ports. The analog ports are high impedance inputs or outputs, used for DACs, ADCs, OP amps, or instrumentation amplifiers. The CPU is supported by up to 2K RAM memory, and proprietary technology FLASH memory space.

The device is a multi-purpose dynamically configurable system, programmable on the fly. What does it mean? If you need more gain from the amplifier, you ask for more gain. Then you drop the gain. It is not the class of single purpose dedicated chips, where you get stuck with 0.1k memory, and a single mixed signal functional block.

III How to use it

The tools required for first steps forward is a PC with USB1 port, single PCB board with
socket, four LEDs, the programming unit, and the programming GUI.

The programmable array’s blocks have to be configured, connected, and activated by software macros. The macros build each active block. The final properties of each functional block are later specified by custom software code; e.g. the sampling rate, auto-calibration, self-test, human interface, or LCD display communication. It is like the LEGO™ toy. The CPU clock speed can be set with a software shift-stick, up to 48 MHz. The low power mode employs 32 kHz oscillator.

IV Slow versus fast

Presently, there are three generations of the chip available:
- PSoC1 is ASIC controller of first generation.
- PSoC3 is 8051 version of the above. (Keil C51)
- PSoC5 (ARM RealView MDK)

The manual selection of building blocks offers many choices. Let’s mention few to get an idea:
- Timers
- Random sequence generator
- PWM, pulse width modulation
- Digital Comms
- Multiplexers
- Digital filters
- Counters
- DTMF dial
- Amplifiers
- DACs
- ADCs
- Infra red communication

With deeper and detailed knowledge of the internal structure, additional custom functional blocks can be created.

V Software support and compilers

The programming language is C or assembly. Both can be used at the same time. An important part of the software development package is basic set of libraries including floating point math, strings, and proprietary libraries. The “Strings” unit is traditionally the weakest part of C. Code from older projects is reusable. Rewriting software libraries from scratch is very time consuming. If you run a project, the engineering question stands: "how can I get from A to B, without wasting time"? Two compilers are supported. Just recently, a new embedded system C compiler from HI-TECH was released.

VI Power management

During operation, the unused blocks can be put asleep. External trigger can wake up particular block, or the whole device. There is also a section taking care of the program security. Particular memory sections can be encrypted. Specific software tasks can use the advantage of dedicated hardware multiplier.

The CPU clock has optional frequency multiplier by two, based on PLL (Phase Lock Loop). The minimized PLL loop filter spares the real estate space on the silicon chip. Sensitivity to RF EMI radiation was found, causing slight clock skew.

System power consumption from 5 Volt or 3.3 Volt power supply is really in the range of single digit mA, dependable on the selected clock speed.
From functional point of view, the device can bring major system improvements, replacing large portfolio of hardware state machines. It can run the laundry washing machine, it can supervise the brewing process, or provide data acquisition, signal processing, and data encryption. A desktop frequency counter burning few Watts of power can shrink to a handheld device with temperature controlled frequency standard. It is an interesting stand-alone engineering tool.

The PSoC was originally developed for wired communication, payment machines, and credit card readers. The industrial grade for high EMI immunity, reliability, and temperature range of -40C to +50C was implemented.

Demo and evaluation boards are available. Even the simplest board is quite helpful. It enables design verification and improvement implementation. The demo board is also very valuable for educational purpose. The theory behind proper analog grounding and PCB design is valid from microwave circuits to switched power supplies and embedded systems. You can see the difference. The CPU can crunch complex numbers and there is still some time left. An implementation of ADC converters helps to understand synchronous sampling and behavioral properties in noisy environments. The noise from AC wall outlet or the wideband noise from USB power supply is visible.

VII The RF communication device in example

A proprietary digital communication system with short latency of 100us for transmit and receive was developed with the PSoC controller. The base-band receive data packet was sampled, processed, and decrypted in real time. FEC helps. The output used a series communication port and a servo unit. Few wireless network based units shared the band and communicated with each other in dedicated time slots. Major focus was to performance, reliability, and wireless network intelligence. Later we added high-quality audio over the wireless for system verification. It is easier to find hardware and software glitches by listening to the CD player, than waiting for unknown failure to occur. All wireless systems have finite BER or PER (packet error rate). The inherent wireless BER is much higher than fiber optic BER. On the other hand, there are not many high-quality wireless audio systems where you don’t hear any dropouts. The work around lost data is quite interesting. Many factors are in the playground, including the way how humans process and perceive sound. We checked the insertion of man made random background noise. The time-critical tasks requiring extensive CPU machine time were implemented in hardware.

Selection of transceiver chipsets for 900 MHz and 2.4GHz bands is limited. There are chips dedicated for high frequency IF with SAW filter, and the nearly direct conversion radios with low frequency IF in the range of hundreds of kHz. The pure direct conversion chips are rare (WiFi). They suffer from phase noise directly converted to the base band, and the 1/f noise. Each type has its own pros and cons. By the modulation technique, we can tell there are radio chips dedicated for linear modulation (QAM) with I and Q. The second type is for FM modulation, using FSK, PSK, and clones. Price plays a major role. Performance of particular commercial radio chipsets was found unsatisfactory. We had the chance to check few types from different manufacturers. The topic is very wide, ready for separate paper. I would like to mention few areas to keep eye on: IF band pass filtering, RX blocking, reciprocal mixing in mixers, VCO close phase noise, PLL EMI immunity, data packet shaping and filtering, AGC, RSSI, RSSI ADCs speed, MAC and IP address, sleep mode, PA efficiency, PA architecture, T/R switch speed.

VIII The Green Power application

It is quite certain; the electrical power will be distributed with different price during the day, night, and season. There is a call for efficient communication, to remotely switch off
the overloading power loads. The power grid has finite capacity, and gets overloaded during summer. On the customer side, there is a requirement to read the instant price, instant power consumption, and to disconnect the unnecessary power loads on demand. Flow of the energy is expected to be a two-way road. The pricing will influence extensive use of electrical cars.

The power distribution companies use their own communication system. There is planned and expected another system on the top. The discussed frequency range is from one hundred kHz up to 30 MHz. The frequency spectrum and the communication protocol for NA continent is recommended by EPRI. We will know soon who the winner is. It can be WiFi, Home Plug, PLC, ZigBee, or a different protocol.

There was a request for flexible tool to measure and investigate the RF spectrum and signal propagation. Communication reliability and code robustness are the keywords industry wants to hear. The purpose is to evaluate the environment; help with communication setup, verification, trials, and troubleshooting.

A palm type of Spectrum Analyzer (SA) was developed. The input frequency range is from 100 kHz up to 48 MHz. An input attenuator limits the signal amplitude in single dB steps. The frequency marker reads the signal level. The whole frequency spectrum of interest can be seen in single shot on graphical display. The graphical screen amplitude range is over 90 dB, while the dynamic range remains above 100 dB. The detected RF signal can be further processed or sent to audio. The data output can be used for PER loop back measurement.

The SA can process ASK, FSK or PSK signal. Different zooming filters can be selected. Full mobile operation is enabled with standalone intelligent battery charger. The power consumption including display unit is 1.5 Watt from a 12 Volt power supply. Following picture demonstrates spectrum of a 10 MHz transistor oscillator under test. Public device availability is under consideration. The SA is a mixture of RF, mixed signal, digital, and PSoC technology.

IX Conclusion

The presented description of system on chip with examples gives an overview of the concept. The goal was an introduction focused to features and flexibility.

PSoC is an industrial tool, aiming shorter design to market cycle. It targets professional applications and university projects with limited budget, as well.

X References

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