



Third option, depending by the output coupling topology you chose, the Push-Push oscillator can operate only at fundamental frequency  $f_o$ , which is the topology used in the VFO circuit presented here.

In general, the Push-Push concept offers several advantages over single-ended designs:

In Push–Push oscillators a **high Loaded-Q** can be achieved (close to unloaded-Q) using practical element values. This happens because each active element is acting as a "**Q-Multiplier**" during the half of the RF cycle when it is not oscillating, and consequently the effective loaded-Q of the circuit is higher than in single-ended counterparts.

Increasing the Loaded-Q improves the **phase noise**, improves **long-term frequency stability** versus **temperature variations**, reduces **supply pushing**, and reduces **load pulling**.

When you build a free running Push-Push oscillator you can achieve **high short-term frequency stability**, which is important when the VFO is part of a homebrew QRP transceiver operating for example in a Field-Day contest.

The Push-Push principle is widely accepted as an approach to realize low phase-noise oscillators, with their phase noise behaviour achieved to be better than that of single-ended counterparts.

Phase noise in the circuit is reduced because of synchronization effects between the two oscillators. On the other hand (according to theory) coupling of two otherwise identical oscillators gives a phase noise reduction by a factor of 2, and briefly speaking this is due to the fact that the noise does not increase as strong as the signal, assuming uncorrelated noise sources in both oscillators. So the coupling effect in Push-Push oscillators provides an extra of 3dB phase-noise improvement.

Push-Push oscillator topology allows you to arrange the feedback elements in a way to effectively short-circuit the intrinsic noise sources and also the low-quality intrinsic transistor reactances.

Since the transistors are operated at half of the desired output frequency, the usable frequency range of the active devices can be extended, so you can get great frequency range; common is at least one octave.

Push-Push oscillators have high immunity against load-pull, and this happens because only the 2<sup>nd</sup> harmonic ( $2f_o$ ) output is located at a virtual ground node, so changes of the load affect the fundamental signal only indirectly.

An important situation when you build a homebrew HF transceiver is the level of the variable oscillator versus frequencies and bands. In the case of the Push-Push VFO its output signal is a composite signal and not the summation of the two oscillators, therefore you will get a more stable output level versus frequencies.

**The Push-Push VFO presented here operates only at fundamental frequency  $f_o$  using a transformer at the combined source output.**

The signal produced by two identical Clapp oscillators has equal frequencies but they are forced  $180^\circ$  out-of-phase by the connection of the transistor drains. As an innovation of the circuit, the source capacitors of the two oscillators use the same feedback capacitor (C1).

The signal at the common drains has a frequency of  $2f_o$ , but in our circuit this line is decoupled with capacitors to the ground, so the 2<sup>nd</sup> harmonic is rejected at that point.

The VFO use two J310 JFET's (Q1 and Q2) with a high  $I_{dss}$  (60mA) which is required for good output power and reducing the phase noise. The source resistors (220 ohms) serve the dual purpose of an approximate current source and stabilizing JFET's drain currents  $I_D$  below  $I_{dss}$ . Because they are placed on the output path of the oscillator the output noise is also reduced.

Drains currents flowing in the sources resistors biases the sources at a positive voltage relative to the gates, and in this way effectively reverse biasing the gates. Have to remember that the symmetry of the built circuit is important to get good performances, as frequency stability and phase noise.

For tuning the circuit uses a dual variable capacitor (Cv1 and Cv2). You have to ensure that the difference between Cv1 and Cv2 capacitances (during tuning) is in +/- 20% range. Greater circuit asymmetry increases the 2<sup>nd</sup> harmonic at the output (otherwise decoupled at the drains in this topology), and inherently degrades the frequency stability and phase noise.

The resonator inductor L1 was made on a ferrite toroid, and to get good performances this should have an unloaded-Q higher than 200.

The output transformer Tr1 was made on a ferrite toroid using bifilar wires for the two windings L2 and L3 (2x10uH), and separate winding for L4 (0.5uH). I tried to avoid using a trifilar winding for this transformer, minimizing the coupling between the main oscillator and the output buffer (Q3).

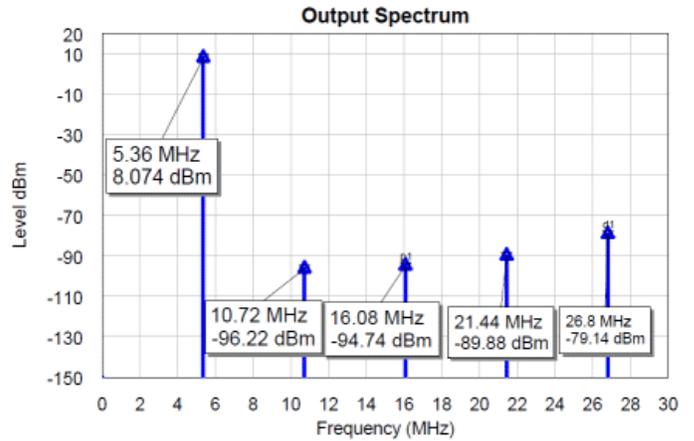
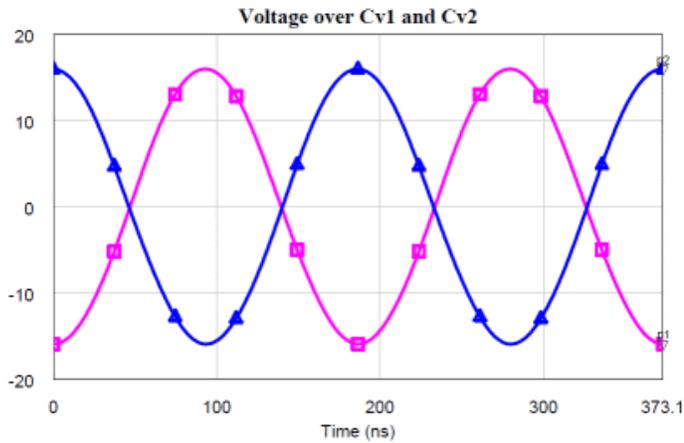
The output JFET buffer (Q3) use at the drain a 1:1 transformer followed by a steep Elliptical Low Pass Filter to cut all the remaining harmonics.

The VFO can operate up to 30 MHz and even up to 100 MHz, if you change in concordance the resonator values, the feedback capacitors, and of course the LPF values at the output.

Using JFETs in oscillators have some advantages compared to bipolar transistors (BJT) as follows:

- The noise contribution of the JFET is from the shot noise of the gate leakage current, the thermal noise of the channel resistance, and the frequency noise of the channel. These noise characteristics are generally lower than those found in BJT if the JFET is properly selected for the application. This is true as long as the JFET is biased, so that the drain-source voltage is greater than the pinch-off voltage.

- Unlike bipolar transistors, where noise characteristics vary directly with changes in the collector current ( $I_C$ ), similar characteristics in JFETs will vary only slightly as drain current ( $I_D$ ) is changed.
- The flicker-noise ( $1/f$ ) is negligible in JFETs, but it increases approximately 3dB per octave in BJTs starting below 100 Hz.
- In BJT the lowest noise is at low collector current ( $I_C$ ) when in JFET the lowest noise is at higher drain current ( $I_D$ ).



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