How to Characterize Surface-Mount RF devices

http://www.qsl.net/va3iul/

RF engineers rely on the vector network analyzer (VNA) to measure S-parameters of their RF components for characterization and subsequent design use. One problem in measurement is that these components are often meant for surface mounting and do not connect to the VNA directly. Simple PCB test fixtures are often fabricated to surface mount the device under test (DUT) for connection to the VNA, as shown in Figure 1. However, the test fixture itself introduces parasitics to the S-parameter measurements that must be removed in a process called de-embedding.

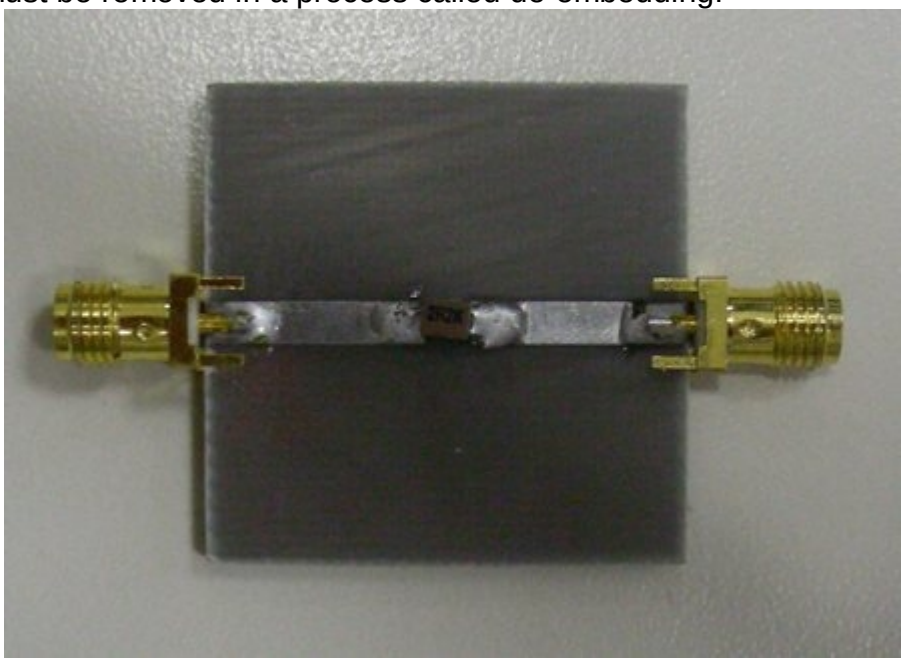


Figure 1

This article describes a practical de-embedding process that does not require developing an equivalent circuit model of the input and output feeds to the DUT. Nor does it require the input and output feeds to be symmetrical. You will need a simple linear simulator capable of manipulating S-parameters and S-Y-Z-matrix transformation.

Our example uses the Genesys Virtual Network Analyzer software from Agilent EEsof EDA, from which the screen shots were taken.

The De-Embedding Steps, Summarized

1.Build three PCB fixtures, with DUT, open, and short.
2.Measure S-parameters of the open, short, and DUT using your network analyzer.
3.Remove the series parasitics from both the embedded DUT and open fixtures by subtracting the Z-parameters of the short.
4. Remove the parallel parasitics from the embedded DUT by subtracting the Y-parameters of the open from previous step.
5. Obtain the actual DUT characteristics by converting Y- to S-parameters from step 4.

The steps are described in more detail in the following section. A fat low-impedance transmission line is used as the DUT to illustrate the before and after results of de-embedding.

Step 1: Build Three Fixtures with DUT, Open, and Short

Prepare for this de-embedding process by fabricating three test fixtures:

1. The PCB with DUT (shown in Figure 2).

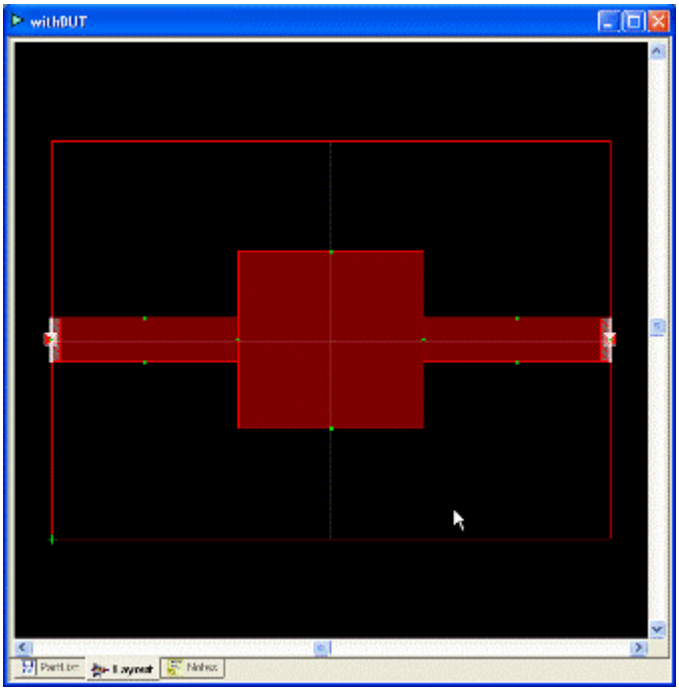


Figure 2

2. The open fixture is the PCB without the DUT mounted, leaving only the transmission lines connected to the input and output ports, as shown in Figure 3. This fixture contains both series and parallel parasitics.

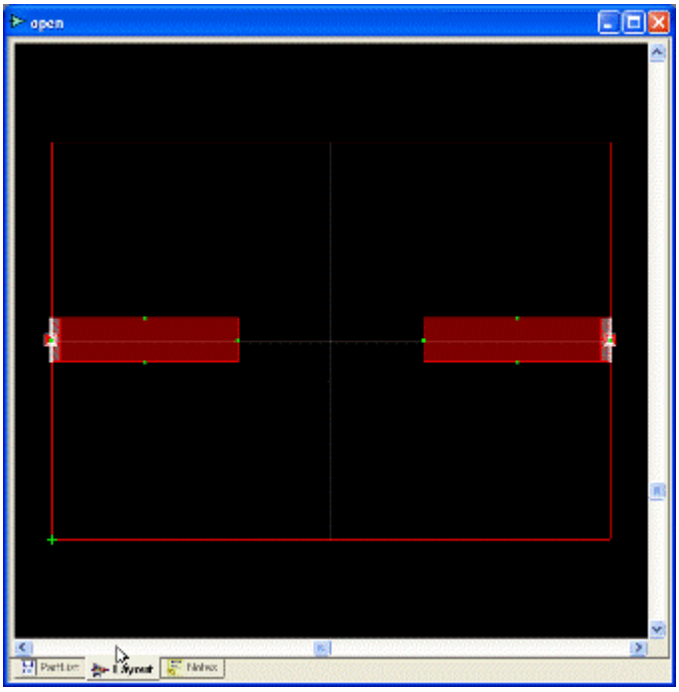


Figure 3

3. The short fixture is the open fixture shown in Figure 3 with the ends of the transmission lines to the DUT input and output reference planes shorted by a row of via holes to ground (shown in Figure 4). The grounded via holes short out the parallel parasitics to leave only the series parasitics.

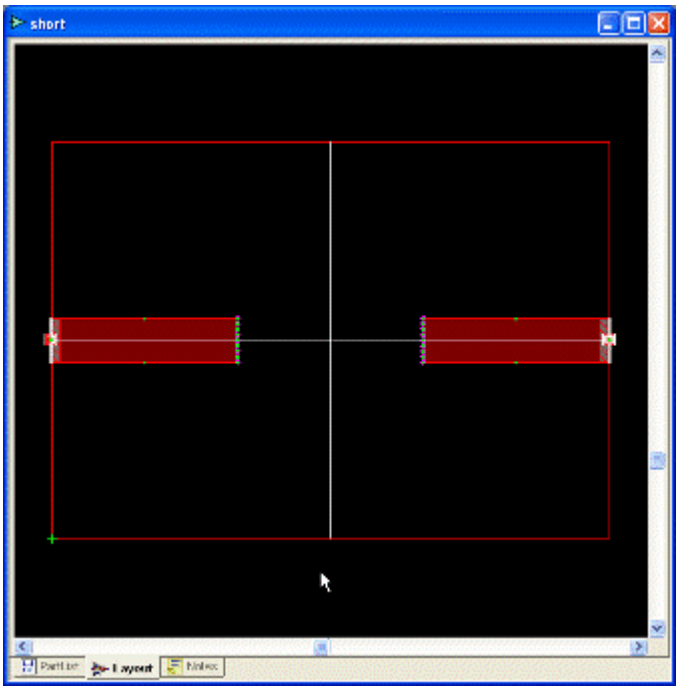


Figure 4

Step 2: Measure S-Parameter of Open, Short, and DUT

With the VNA properly calibrated, measure the S-parameters of the three fixtures and store the results as "Open_Data," "Short_Data," and "DUT_data." Verify the quality of the short and open measurements by displaying their S-parameters on the Smith chart.

Figure 5 shows the open fixture response. The S-parameters are located at the right open region of the Smith chart. It shows the parallel capacitive parasitics in the open fixture.

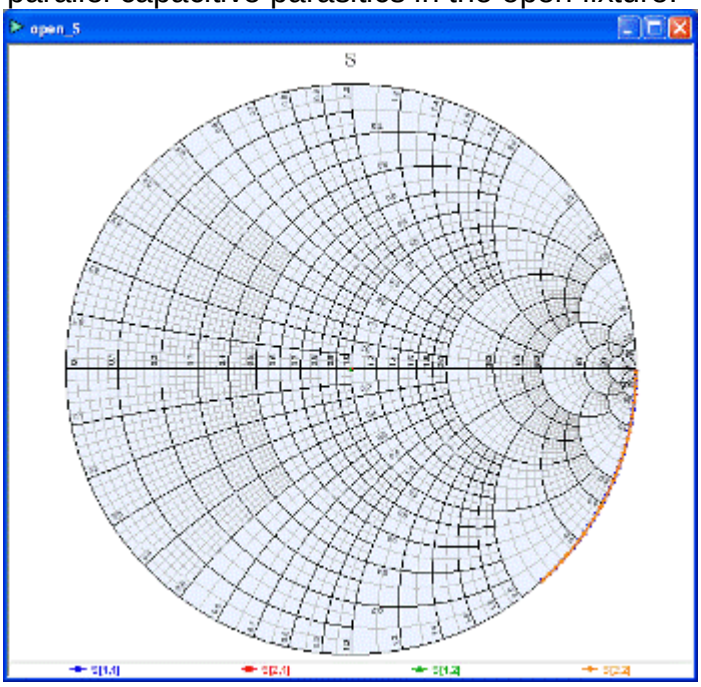


Figure 5

Figure 6 shows the short fixture response. The S-parameters are located at the left short region of the Smith chart with some series inductance, which look reasonable due to the via holes.

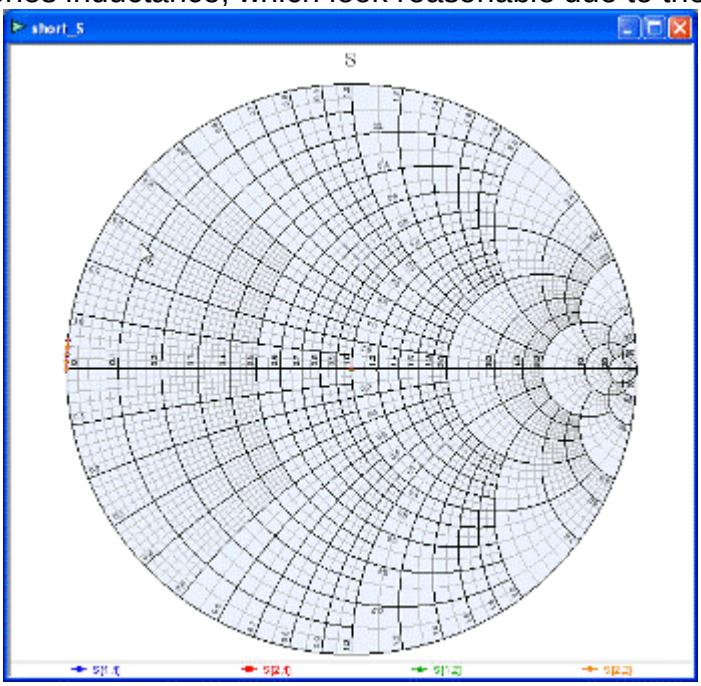


Figure 6

Figure 7 shows the DUT (a wide transmission line in this case) response before de-embedding.

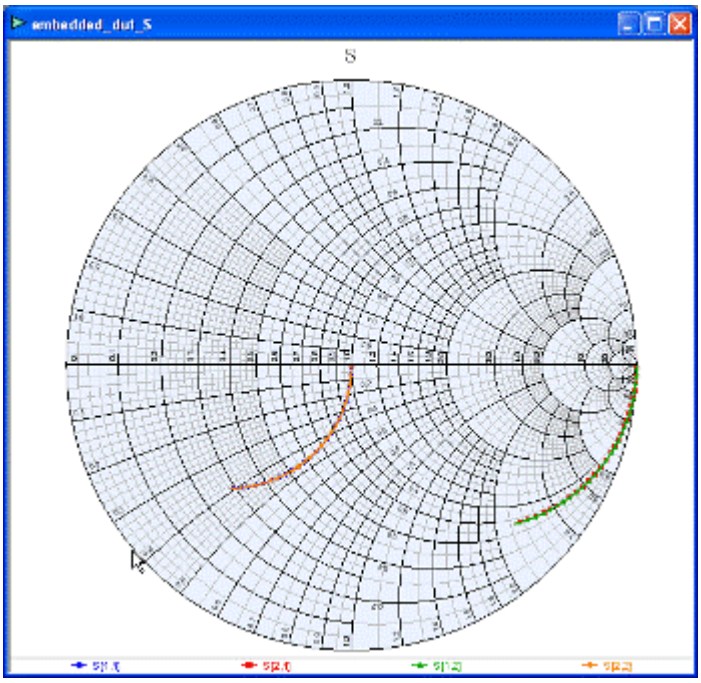


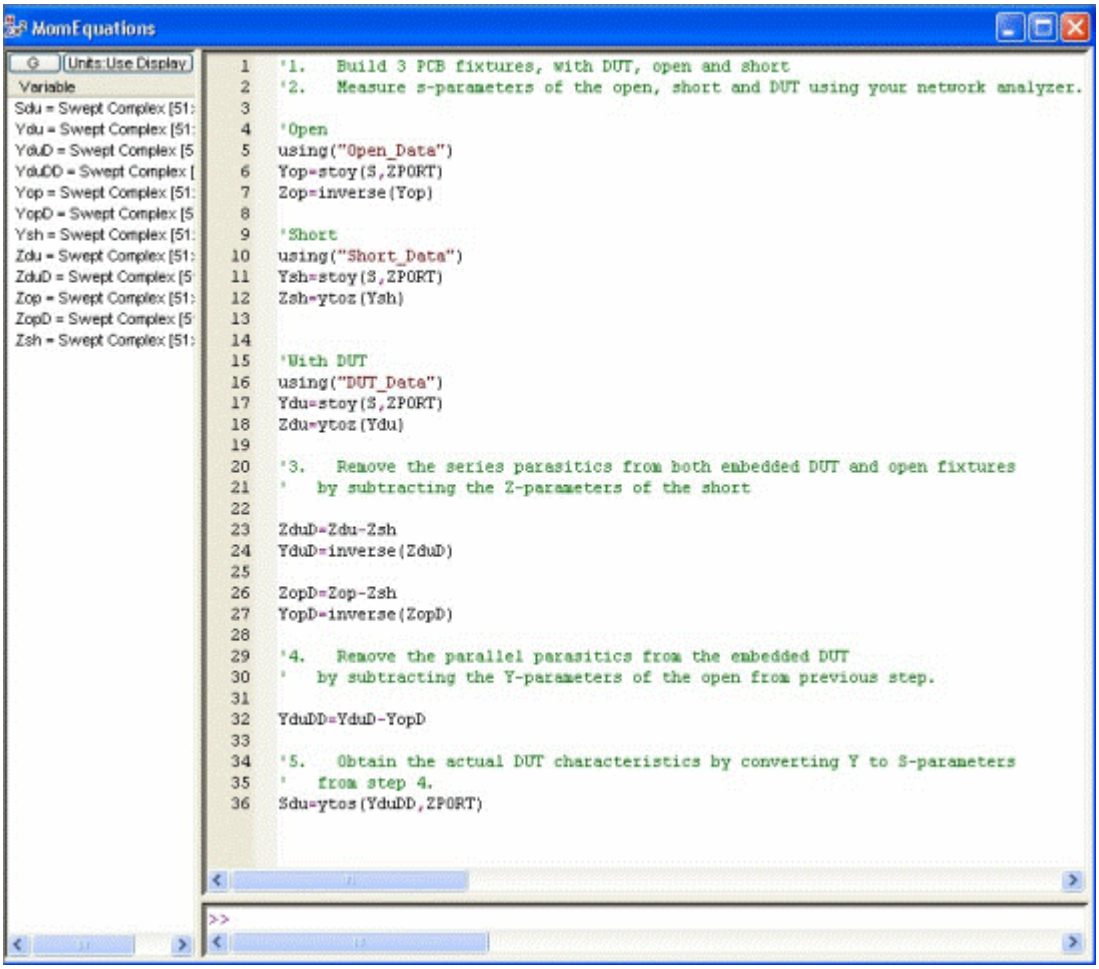
Figure 7

Step 3: Remove Series Parasitics of DUT and Open Fixtures by Subtracting the Z-Parameters of the Short

To remove the series parasitics, we subtract the series parasitics of the Short from both the DUT and Open fixtures. This is done through Z-parameter subtraction.

First, convert the measured "Open," "Short," and "DUT" S- to Z-parameters as shown in lines 7, 12 and 18 of the equation editor in the Genesys software (Shown in Figure 8). (You can perform the same matrix transformation math elsewhere.)

We are now ready for subtraction to remove the series parasitics from the "DUT" and "Open" measurements. This is shown in Figure 8, lines 23 and 26.



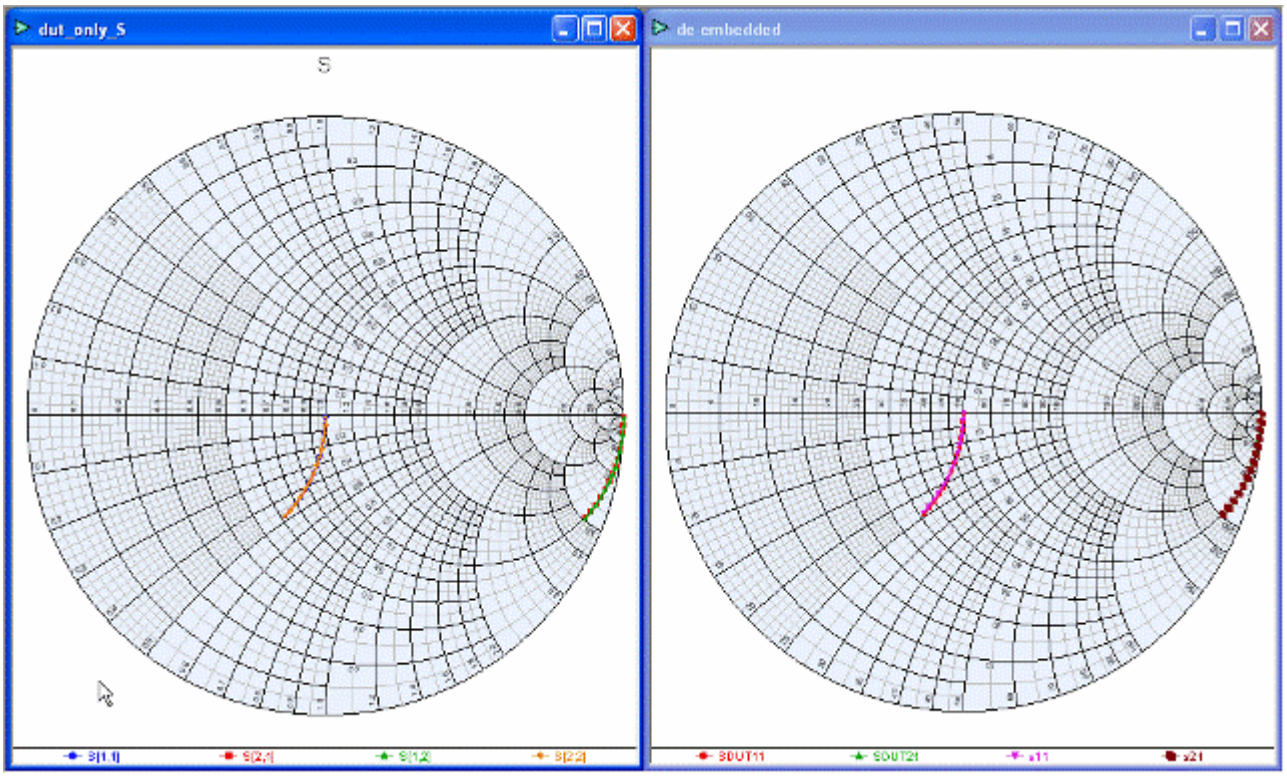
Step 4: Remove the Parallel Parasitics of DUT by Subtracting Y-Parameters of the Open from Step 3

Now prepare to remove the parallel parasitics by Y-parameter subtractions. Convert the resultant Z- to Y-parameters of the "DUT" and "OPEN" from step 3 as shown in lines 24 and 27 of Figure 8, respectively. Subtract the parallel parasitics represented by the Y-parameter of the "OPEN" from the DUT as shown in line 32 of Figure 8.

Step 5: Obtain Actual DUT Characteristics by Converting Y- to S-Parameters from Step 4

The final step in our de-embedding process is to convert the final Y-parameters of the DUT back to S-parameters, as shown in line 36 of Fig. 8.

To verify that these de-embedding steps work accurately, we compare the simulated DUT versus our de-embedded S-parameters from the above steps on the Smith charts shown in Figure 9.



We have verified the de-embedded results. Note that the resulting Smith chart aligns perfectly with the DUT-only simulation of the fat transmission line.

The de-embedding technique described and proven here is a practical approach that can be used to get good accuracy out of simple self-made test fixtures for components you solder onto PCB boards for VNA measurements. For good accuracy, keep the feed to the DUT as short as possible--preferably less than one-twentieth of a wavelength--on the substrate.

Agilent Technologies