A TWO–LOOP 10Hz STEP 40–70MHz SYNTHESIZER

By Luiz Amaral
PY1LL/AC2BR

INTRODUCTION

For HF radios (from 1 to 30MHz), the use of a local oscillator from 40 to 70MHz, with the first IF on 41MHz, is a well-accepted mode to get a reception almost images free.
Many times some conflicting design characteristics are fine frequency resolution, tune speed, low output noise, high spectral purity, low power and low price.
Most designs use many loops to get fine resolution. This article shows a method to overcome this difficulty, using only two loops.
The work is a more modern version of my former article presented in December 1989 Ham Radio review, with better characteristics due the existence, nowadays, of suitable components for the electronic demands.

THE ALGORITHM

Normally, unless we use special techniques, the synthesizer minimum frequency step, that is, its resolution, is equal to its reference frequency.
Figure 1 shows the block diagram of such a loop.

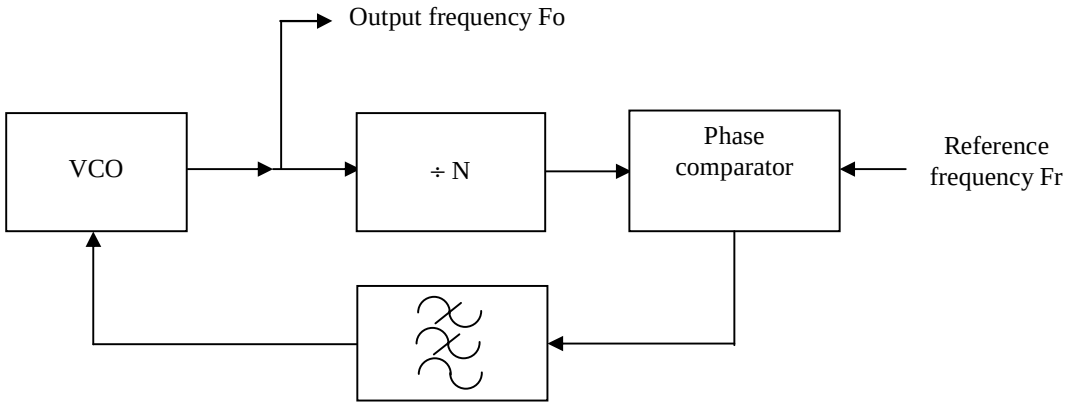

Figure 1

The output frequency **Fo** is given by:

Fo = N x Fr (I)

As we see in **(I)**, changing **N** to **N+1** or **N-1**, **Fo** increases or decreases by exactly **Fr**, that is, **Fr** is the resolution in this synthesis method.

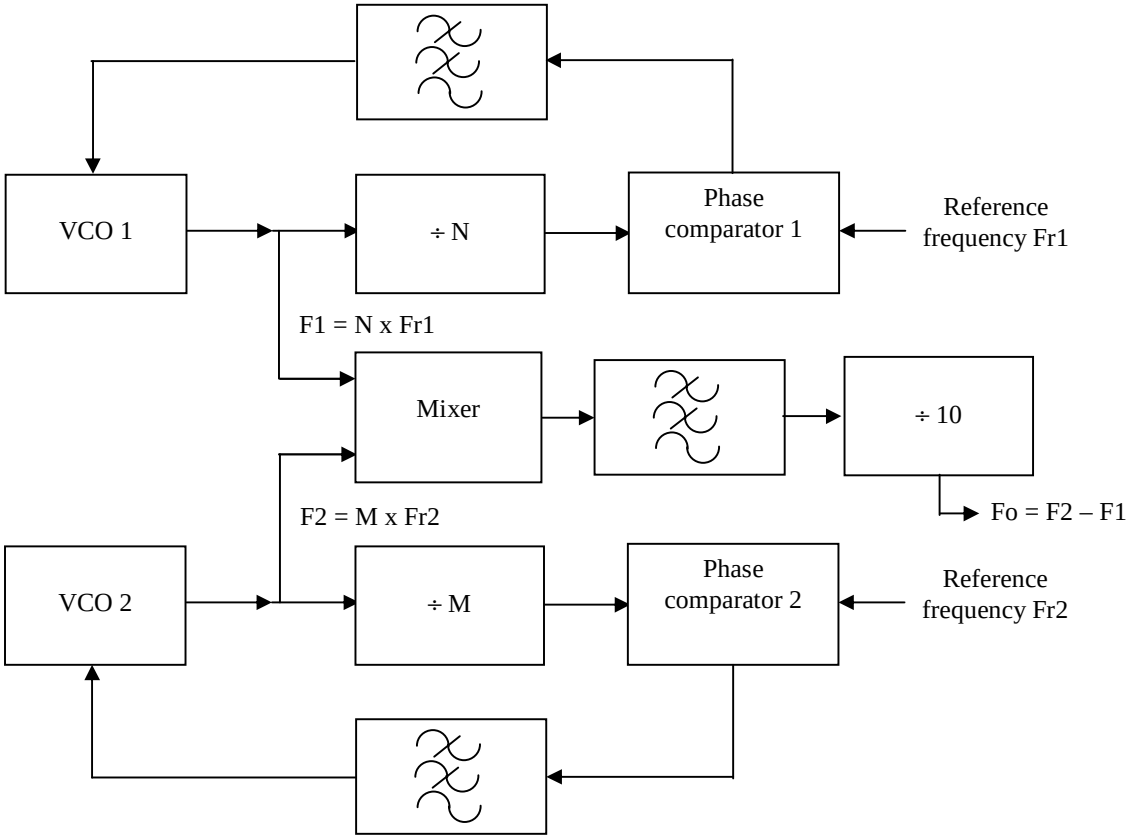

Figure 2

The block diagram of the new algorithm is showed in Figure 2. For getting short settling times and low output noise, it is necessary that we use reference frequencies substantially high. If we make Fr1 = 99.9kHz and Fr2 = 100kHz in Figure 2, we can rewrite equation **(1)** as:

Fo = [(M x 100 – N x 99.9) / 10] kHz = {[100 x M – (100 – 0.1) x N]} / 10 kHz

Fo = {[10 x (M – N) + 0.01 x N]} kHz (II)

We can verify that, by varying **N** by one, **Fo** changes by 0.01kHz that means, 10Hz, although loops reference frequencies are of the order of 100kHz!
For performing steps of 10, 100 or 1,000kHz, we change only **M**. To perform steps of 10, 100 and 1,000Hz (or some of their multiples), we must change **N** and **M** together, keeping the same value of **M – N**.

Deriving the Design Equations

One problem to synthesize from 40 to 70MHz is the rather high variation range: 30MHz for a 40MHz VCO. This, among other things, implies in a varactor with a capacitance variation of more than $(70/40)^2$, that is, Cmax/Cmin > 3.0625, remembering that Cmin and Cmax take into account the circuit stray capacitance, what worsens much things.
An advantage of the present method is that we may use VCO's in the high VHF part, for example, making the frequency band range a minor problem. We may suggest the M VCO operating from 1,600 to 2,000MHz and the N one from 1,200 to 1,300MHz, both simple loops.
Let's derive now the design equations for this system. We must remember that the output frequency is a decimal seven-digit number, for example, 47,936.42kHz.

Fo = 10,000 x B6 + 1,000 x B5 + 100 x B4 + 10 x B3 + B2 + 0.1 x B1 + 0.01 B0 (in kHz)

Alike:

N = N0 +10 x N1 + 100 x N2 + 1,000 x N3 = 10,000 x N4

M = M0 + 10 x M1 + 100 x M2 + 1,000 x M3 + 10,000 x M4

Carrying these last three expressions in **(II)**, one gets:

10,000 x B6 + 1,000 x B5 + 100 x B4 + 10 x B3 + B2 + 0.1 x B1 + 0.01 B0 = 10 x [M0 – N0 + 10 x (M1 – N1) + 100 x (M2 – N2) + 1,000 x (M3 – N3) + 10,000 x (M4 – N4)] + 0.01 x (N0 + 10 x N1 + 100 x N2 + 1,000 x N3 + 10,000 x N4)

By making equal all the corresponding terms, we have:

a) **M4 – N4 = 0**
b) **M3 – N3 = B6**
c) **M2 – N2 = B5**
d) **M1 – N1 + N4 = B4 (III)**
e) **M0 – N0 + N3 = B3**
f) **N2 = B2**
g) **N1 = B1**
h) **N0 = B0**

As the **Bi's** are given numbers, we have eight equations with 10 unknowns to determine the **Ni's** and the **Mi's**.
This gives us two degrees of freedom to choose the bands of **F1** and **F2**. As we have to establish values to two unknown parameters, we first choose **N4**. If this value and also that of **M4** are too high, we may have dividers problems that may fail and with more noise due the greater division factors. If, otherwise, **N4** and **M4** are too small, we will have problems to cover the entire band of the VCO's.
A good choice is **N4 = 1**.
The range of **F1** (loop N) is of the order of 100MHz because, to cover 99.9kHz (the maximum loop M alone) in 100Hz steps (after divided by 10 at the output), we have 1,000 channels with 99.9kHz of the reference frequency, that give us 100MHz. Therefore, the range of **F2** (loop M) is 100MHz + 300MHz (output range before the final division by 10) = 400MHz.
The other degree of freedom let us to fix the value of **N3**. Choosing the value 2 for it (it means that, with **N4 = 1**, for a 100MHz range, we have **F1** from 1,200 to 1,300MHz and, therefore, **F2** covers from 1,200 + 400 = 1,600MHz to 1,300 + 700 = 2,000MHz). Those frequencies are convenient for modern type 'two-modulus' and for the VCO's ranges.
Rewriting the expressions of **N** and **M** using the equations **(III)** and the values **N4 = 1** and **N3 = 2**, we write:

N = 10,000 x N4 + 1,000 x N3 + 100 x N2 + 10 x N1 + N0 or

N = 12,000 + 100 x B2 + 10 x B1 + B0 (IV)

M = 10,000 x M4 + 1,000 x M3 + 100 x M2 + 10 x M1 + M0 = 10,000 + 1,000 x (B6 + 2) + 100 x (B5 + B2) + 10 x (B4 – 1 + B1) + B3 – 2 + B0 or

M = 11,988 + 1,000 x B6 + 100 x (B5 + B2) + 10 x (B4 + B1) + B3 + B0 (V)

As the output covers from 40,000.00 to 69,999.99kHz, **B6** can be 4, 5 or 6. **B5, B4, B3, B2, B1** e **B0** can be any value from 0 to 9. Now it is possible to calculate the exact range of **N**, **M**, **F1** and **F2**:

a) Nmin: B2 = B1 = B0 = 0
From equation **(IV)**: **Nmin = 12,000** and **F1min = 99.9 x Nmin = 1,198,800kHz**

b) Nmax: B2 = B1 = B0 = 9

From equation **(IV): Nmax = 12,999** and **F1max = 99.9 x Nmax = 1,298,600.1kHz**

c) Mmin: B6 = 4; B5 = B4 = B3 = B2 = B1 = B0 = 0
From equation **(V)**: **Mmin = 15,988** and **F2min = 100 x Mmin = 1,598,800kHz**

d) Mmax: B6= 6; B5 = B4 = B3 = B2 = B1 = B0 = 9
From equation **(V): Mmax = 19,986** and **F2max = 10 x Mmax = 1,998,600kHz**

Let's suppose we want to synthesize an output of 56,721.98kHz. So, **B6 = 5**, **B5 = 6**, **B4 = 7**, **B3 = 2**, **B2 = 1, B1 = 9** and **B0 = 8**.
Using equations **(IV)** and **(V)**:

N = 12,000 + (100 x 1) + (10 x 9) + 8 = 12,198

M = 11,988 + (1,000 x 5) + [100 x (6 + 1)] + [10 x (7 + 9)] + (2 + 8) = 17,858

Thus **F1 = 99.9 x 12,198 = 1,218,580.2kHz** and **F2 = 100 x 17,858 = 1,785,800kHz**
All works because **Fo = (F2 – F1) / 10 = 56,721.98kHz**.
Obviously the algorithm showed here is better implemented with a microprocessor.
In practice, the dividers **N** and **M** of the commercial PLL IC's don't accept such high frequencies directly, but we can use the so-called 'two-modulus pre-scalers' that nowadays operate well in such frequencies.
So, **N** and **M** have to be written in the form they are used by such pre-scalers. Thus:

N = Np x Pn + An e **M = Mp x Pm + Am (VI)**

With **Np** and **Mp** being the value of the PLL's 'N', **Pn** and **Pm** the smaller values of the 'two-modulus pre-scalers' and **An** and **Am** the values of the PLL's 'A' dividers.
As the order of magnitude of both PLL's is the same, we may choose **Pn = Pm = P**.
For a frequency of 2GHz, a convenient value for **P** would be 128, as it would present to the PLL a frequency compatible with the nowadays technology.
So, using equation **(II)**, we write:

Fo = 10 x P x (Mp – Np) + 10 x (Am – An) + 0.01 x (P x Np + An) or with **P = 128**:

Fo = 1,280 x (Mp – Np) + 1.28 Np + 10 x Am – 9.99 x An (VII)

We can write the expressions for **Mp**, **Np**, **Am** and **Na,** using **(VI)**, with the division factors equal to **P**:

Mp = int (M / P)
Am = M – Mp x P (VIII)
Np = int (N / P)
An = N – Np x P

So, equations **(IV)**, **(V)** and **(VIII)** must be used for the determination, by the microprocessor, of the PLL's division factors values. It is, now, a mere software problem.

Conclusions

This article presents a method to synthesize frequencies from 40 to 70MHz with minimum steps of 10Hz, using only two loops. The output signal phase noise level results very low due the relatively high reference frequencies (≈ 100kHz) and with a final division by 10 that decreases the noise by more 20 dB. Clearly, to get the expected noise level, all good assembling techniques as short lines, rigorous DC signals filtering, good ground distribution techniques, well shielded VCO's and RF filters, high VCO's isolation from their loads, VCO's pre-tuning, etc, must be used as in any frequency synthesizer.
Indeed, it is shown more an algorithm than a circuit. The latter may be implemented with the suitable components already existent with modern technology.

It is presented also an example of the two loops frequencies compatible with components already in the market. Clearly, the evolution of the component technology, it is perfectly possible to adapt the algorithm to synthesizer designs with greater frequencies, with still more fine resolution and keeping the ‘two loops only’ simplicity.

References

Amaral, L. C. M, PY1LL and Mathias, C. A. C., A Two-Loop 10 Hz step 40 – 70 MHz Synthesizer, Ham Radio, January 1989.

All other references are listed in the above one.