AN969

Operation of the MC145159 PLL Frequency Synthesizer with Analog Phase Detector

INTRODUCTION

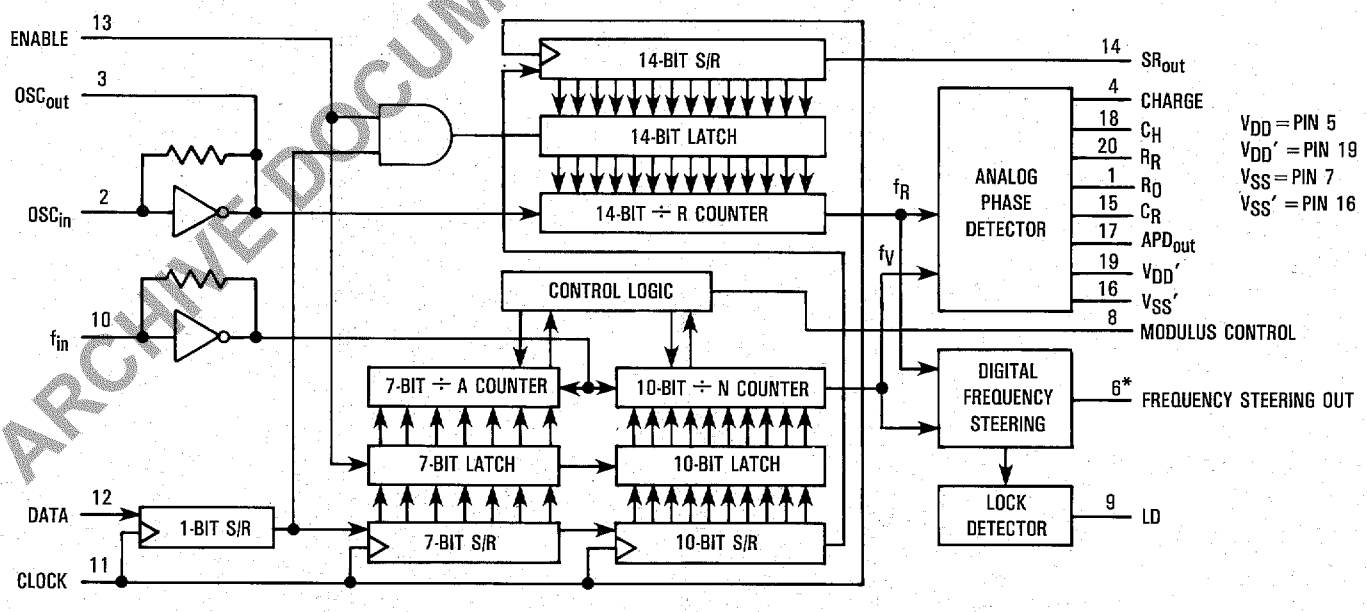
The MC145159 is a phase-locked loop frequency synthesizer with an analog, or more specifically a sample-and-hold, phase detector. The output of this phase detector (APD_{out}) is used as a fine error signal. The synthesizer also contains a digital frequency steering phase comparator for coarse adjustment of loop frequency, separate power supply pins for the analog phase detector, a lock detect output, and on-chip logic for control of a dual-modulus prescaler. (See Figure 1.)

Other features of the MC145159 are a 14-bit reference counter, as well as a 10-bit divide-by-N counter and a 7-bit divide-by-A counter. All three counters are programmed via a serial data stream which is compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs. The device also has on-chip circuitry to support an external crystal. OSC_{in} may also serve as an input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

With the features listed above, the MC145159 finds general purpose applications in such areas as 2-way radios, cellular radiotelephones, and avionics equipment.

As stated earlier, the MC145159 has a sample-and-hold phase detector. As opposed to standard digital phase comparators with fixed gain, the gain of the sample-and-hold phase comparator is programmable. Four external components, two resistors and two capacitors, help set the gain and drive levels of the phase detector. Higher gain is achievable with the MC145159 phase detector versus digital phase detectors.

Because a high degree of filtering compromises overall loop performance, phase detectors which provide an error signal that is as clean as possible prior to filtering are extremely advantageous. One obvious benefit of the sample-and-hold phase comparator is that its output is analog, and therefore already resembles the required control voltage necessary to drive the loop's voltage-controlled oscillator (VCO), thereby minimizing filtering requirements. Ideally, this control voltage is a perfectly clean signal with no undesired perturbations. Any of these disturbances cause unwanted modulation on the VCOs output signal. For high performance radio equipment, the sidebands resulting from this modulation must be very low. The analog output reduces VCO modulation sidebands and also allows for wider loop bandwidths than are normally possible with digital phase detector outputs.



*NOTE: Pin 6 is not and cannot be used as a digital phase detector output.

Figure 1. Logic Diagram

TRADITIONAL SAMPLE-AND-HOLD PHASE DETECTORS

Before examining the method by which the MC145159 performs a sample-and-hold function, the theory of operation of traditional sample-and-hold phase detectors will be reviewed.

The reference signal (divided-down OSC_{in} signal) and current source are used to establish the sawtooth voltage on the ramp capacitor, C_R. (See Figures 2 and 3.) C_R is charged by the current source and quickly discharged by a switch that is controlled by the reference signal. In this way, the period of the sawtooth voltage is equal to the period of the reference signal. The divided-down VCO signal is used to sample the sawtooth voltage by closing a sampling switch for a window of time and letting the hold capacitor, C_H, charge to the sampled voltage. Neglecting leakage current, the charge established on C_H at the end of the sample time remains constant until the next sample. If for some reason the VCO frequency begins to rise above the desired value, the phase of the sampling pulse falls back and sampling is done at a lower sawtooth voltage. This action, in effect, lowers the control voltage to slow down the VCO and keep the divided-down VCO frequency locked to the reference frequency. Likewise, if the VCO frequency falls below the desired value, the phase of the sampling pulse advances and sampling is done at a higher sawtooth voltage. This action raises the control voltage which speeds up the VCO to keep the divided-down VCO frequency locked to the reference frequency.

One serious side effect of this scheme is that an undesired ripple voltage occurs on C_H. This rippling is caused by the ramp waveform charging from level V_A to level V_B during the sample window. Upon opening of the sampling switch, C_H is charged to V_B and remains at V_B until the switch is closed again and voltage V_A is applied to the hold capacitor. Therefore, the hold capacitor is charged to V_B and discharged to V_A while in a locked condition. In effect, a ripple-free lock voltage cannot be established on C_H. The magnitude of this ripple is a function of the ramp charging slope, sample window time, and hold capacitor charge/discharge times.

To mask out the rippling effect, one solution is to follow C_H by a second sampling switch and hold capacitor combination along with the necessary control signals. However, this additional circuitry introduces more switching transients and consumes more chip and/or board space.

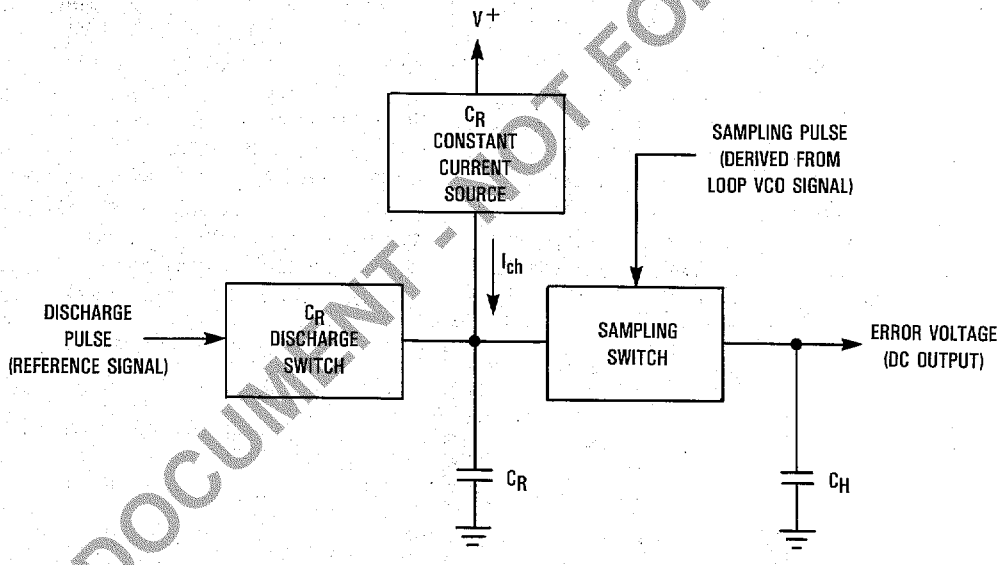


Figure 2. Traditional Sample-And-Hold Phase Detector Block Diagram

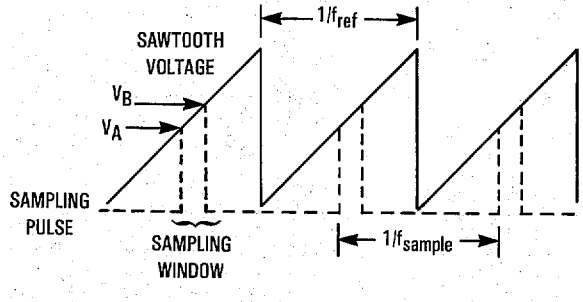


Figure 3. Traditional Sample-And-Hold Phase Detector Timing Diagram

OPERATION OF THE MC145159

THEORY

The MC145159 uses a new, patented design approach for sample-and-hold phase detectors called ramp clamping, which results in improved performance over the traditional approach. Ramp clamping minimizes the need for a second hold capacitor, and in most applications only one hold capacitor is needed. When the loop is in frequency lock, the rising edge of f_R (divided-down OSC_{in} signal) activates a constant current source to initiate charging of the ramp capacitor. (See Figures 4 and 5.) The slope of this ramp waveform is also known as the phase detector gain. The ramp voltage continues to build, at a rate determined by R_R, C_R, and V_{DD}', until the rising edge of f_V (divided-down VCO signal) terminates the charge signal, thereby establishing a constant voltage on C_R. After a predetermined delay (equal to two clock cycles of f_{in}) this ramp voltage is sampled onto the hold capacitor during a sample window lasting four periods of f_{in}. C_H is then isolated from C_R and, after a delay of two clock cycles of f_{in}, C_R is discharged. This cycle repeats every f_R period. The f_V edge relative to the f_R edge in time therefore determines how long the ramp charges before being clamped and sampled onto C_H. This establishes the hold voltage necessary to maintain loop lock. The voltage on C_H feeds an N-channel source follower, the output of which (APD_{out}) controls an external VCO.

When the loop is out of frequency lock, that is when f_R and f_V are not in a one-to-one relationship over a 2π window with respect to f_R, the Frequency Steering Output (FSO) becomes active. As a general rule, f_R and f_V must differ by 2% for the FSO to become active. However, as the reference frequency decreases, the frequency steering sensitivity increases. If the divided-down VCO frequency, f_V, is lower than the divided-down oscillator frequency, f_R, ($f_V < f_R$) then FSO pulses high. If $f_V > f_R$, then FSO pulses low. The FSO pulse width is approximately equal to the period of time between two f_V pulses if $f_V > f_R$, or two f_R pulses if $f_R > f_V$. FSOs repetition rate is equal to the difference frequency between f_R and f_V. When $f_V = f_R$ over a 2π window with respect to f_R, then the FSO remains in a high-impedance state and phase lock is maintained by the analog phase detector output. (See Figure 6.) By combining APD_{out} and FSO, the required low-noise VCO control voltage is provided by APD_{out} while the FSO provides a coarse error signal to achieve fast frequency lock.

The ramp clamp approach to phase detector design, which is implemented on the MC145159, offers significant advantages over the traditional method of sample-and-hold phase comparators. In traditional sample-and-hold detectors, ramp slewing during the sample window causes rippling on the hold capacitor. Therefore, a second hold capacitor and sampling switch may be needed. The ramp clamp technique however, alleviates the need for a second hold capacitor and all of its related circuitry. This becomes very significant in the production of monolithic integrated circuits due to the savings in chip area that result.

Another benefit of ramp clamping is that the ramp amplitude is not allowed to go beyond the value reached when sampling occurs. The traditional method permits the ramp capacitor to charge all the way up to the positive supply voltage value; in most cases well after sampling has occurred. This extends the ramp amplitude beyond that allowed with the ramp clamp approach. A lower ramp pulse results in less ripple in the output error signal caused by parasitic ramp feed-through. With ramp clamping, the ramp amplitude is limited to only that value necessary to keep the loop locked and, more importantly, it provides a constant voltage to the hold capacitor during the entire sample window.

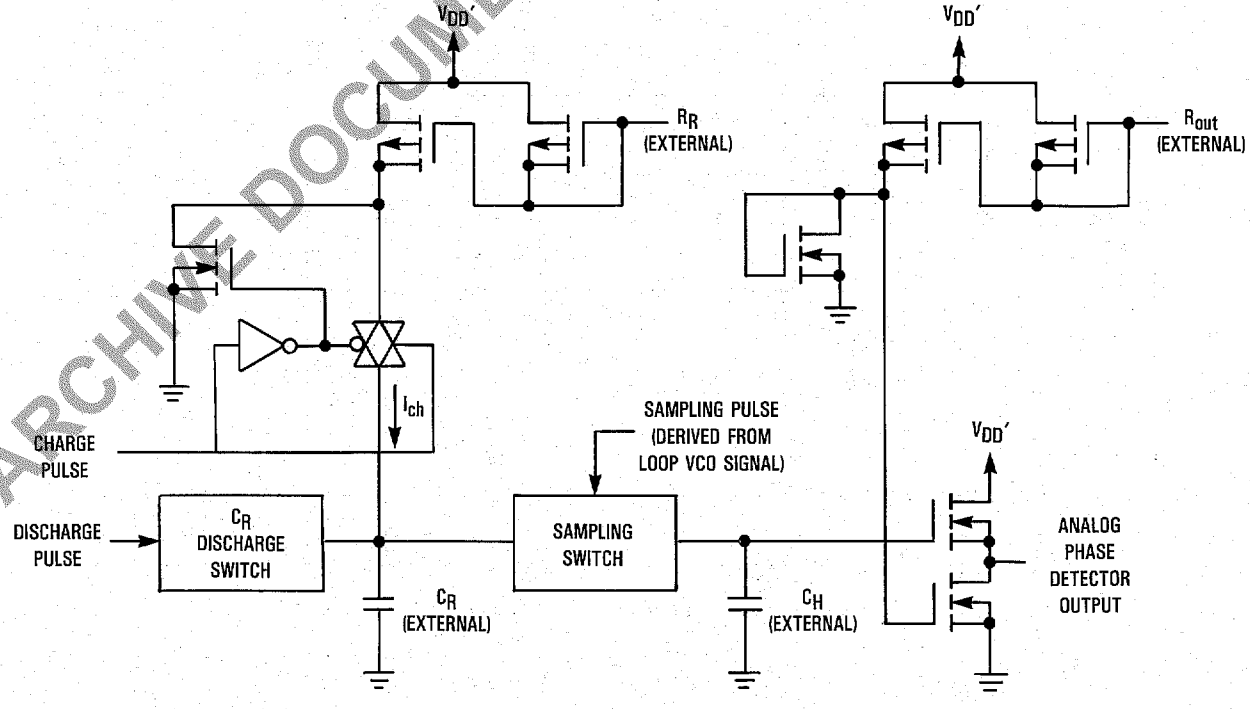


Figure 4. Analog Phase Detector Logic Detail

A word of caution exists for the analog phase detector power supply pins, V_{DD}' and V_{SS}'. These two pins are provided to help isolate the analog section from noise coming from the digital sections of this device and also noise from the surrounding circuitry. Ensure that V_{DD}' and V_{DD} are at the same voltage potential at all times. Likewise, V_{SS}' and V_{SS} must be at the same potential at all times. Otherwise, damage to the MC145159 may occur due to latch up.

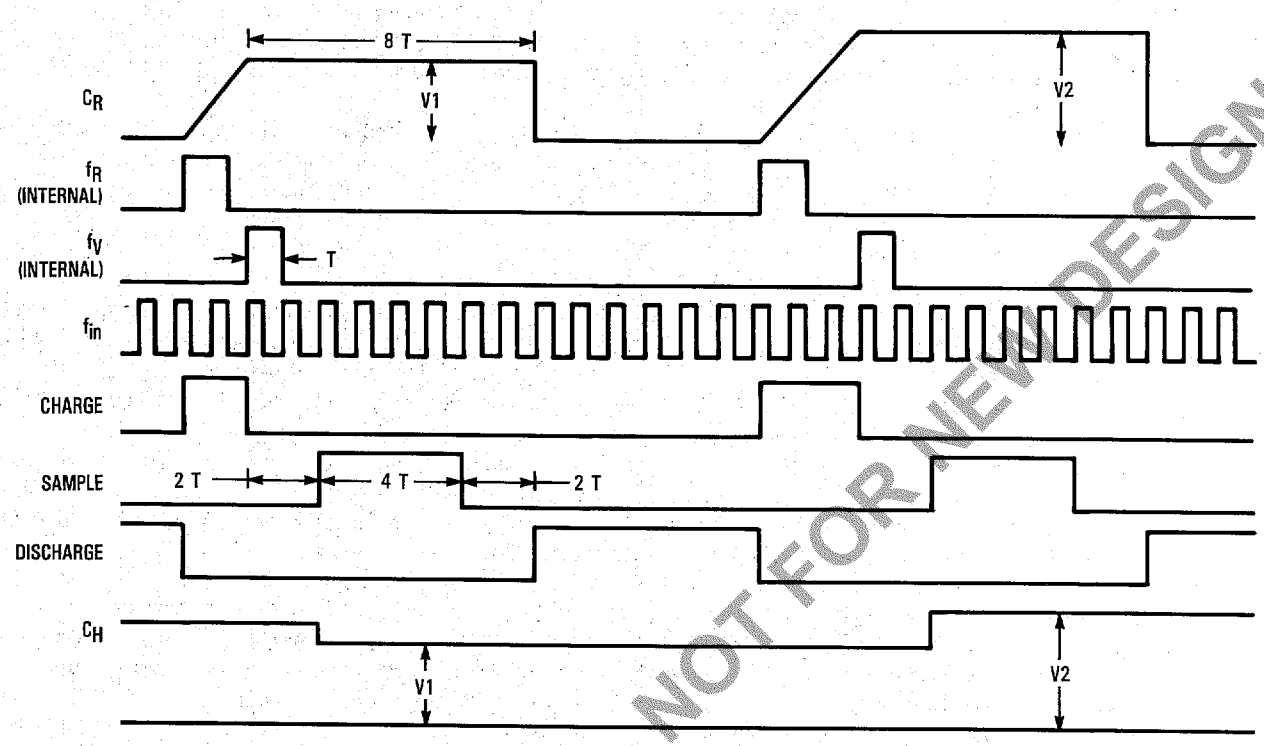
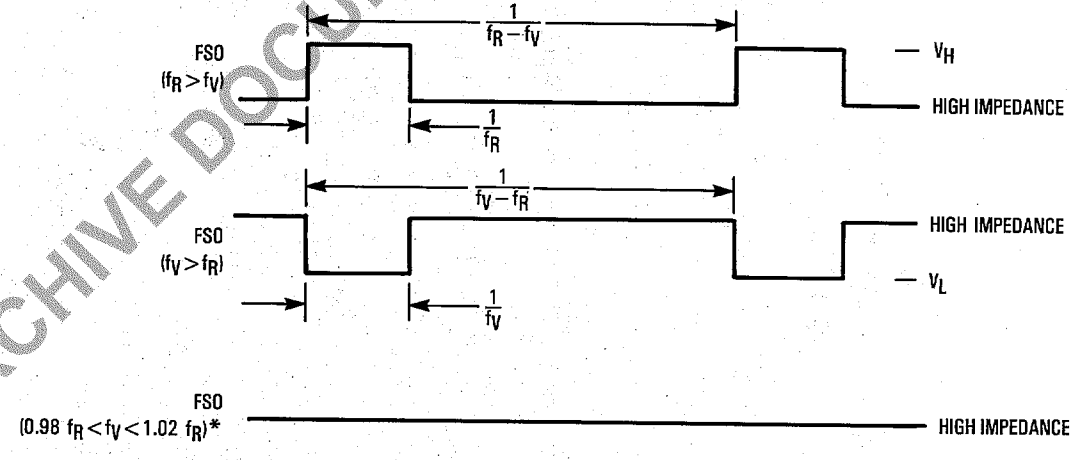


Figure 5. Analog Phase Detector Timing Diagram (N = 17)



NOTE: $f_R = \frac{f_{OSC}}{R}$, $f_V = \frac{f_{in}}{N}$. The R and N counter outputs are not externally available.

*The FSO sensitivity limits are not guarantees, but are design aids.

Figure 6. Frequency Steering Output Timing Diagram

PHASE DETECTOR GAIN

As stated earlier, the gain of the analog phase detector on the MC145159 is programmable. The gain is set by V_{DD}' and two external components; the ramp resistor, R_R, and the ramp capacitor, C_R. The user must therefore determine the optimal value of gain for his or her system.

To select the optimal gain for the phase detector, let us assume a PLL system with a reference frequency of 10 kHz. (See Figure 7a.) With this frequency going into the phase detector, consecutive f_R pulses occur 100 μs apart. Assuming that the Frequency Steering Out pin has already pulled the system into frequency lock and turned off, the Analog Phase Detector Output is in complete control. Therefore, the rising edges of f_R and f_V can be nearly 100 μs apart. Because f_R initiates the ramp waveform and f_V terminates the charging cycle, the ramp should be at most 100 μs, or 2π radians wide. Moreover, the ramp should be capable of charging from V_{SS}' to V_{DD}' during this time. The design equation for phase detector gain given in the data sheet is stated as:

$$K_\phi = \frac{I_{charge}}{2\pi f_R C_R} \quad [V/rad]$$

Substituting in for K_ϕ and f_R and selecting a value for C_R, one can solve for I_{charge}. From I_{charge}, the value of ramp resistance, R_R, is taken from Figure 8.

In this example, the gain of the phase detector is $V_{DD}'/2\pi$ [V/rad]. Larger values of gain can certainly be used. In fact, higher gain results in faster lock times. (See Figure 7b.) There is, however, an upper limit to the amount of gain selected. Higher gain is achieved by increasing V_{DD}' or reducing R_R or C_R (or some combination thereof). Increasing phase detector gain by reducing the size of the ramp capacitor leads to increased noise induced into the ramp, and consequently, hold capacitors.

On the other hand, too little gain results in the ramp capacitor taking slightly longer to reach the required error voltage level,

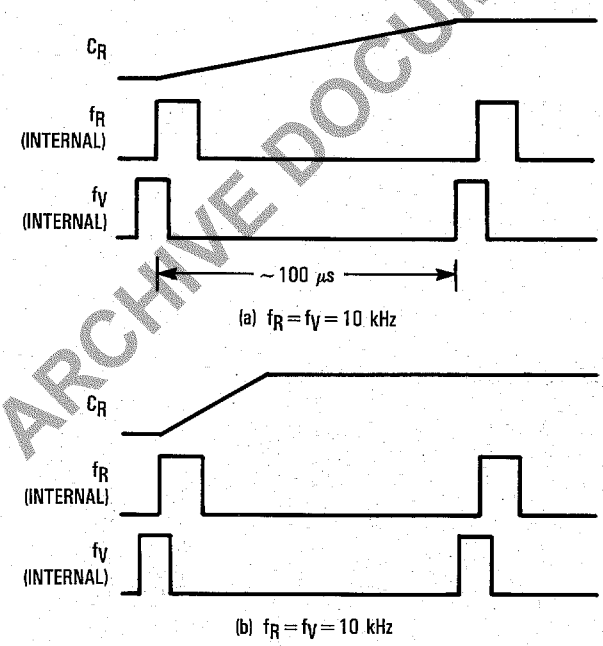


Figure 7. Determining the Gain of the Analog Phase Detector

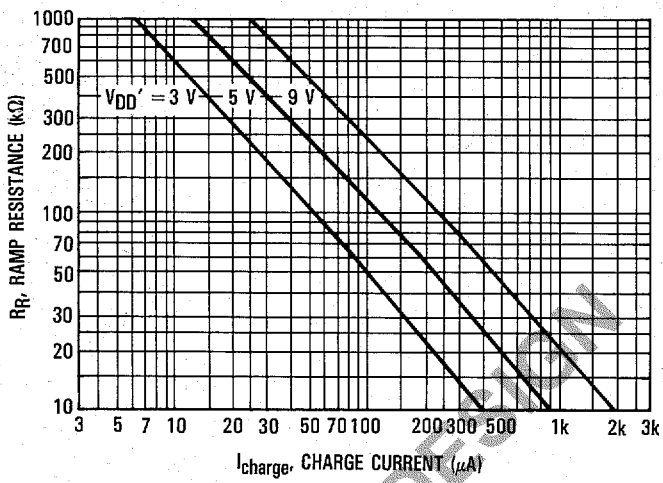


Figure 8. Charge Current versus Ramp Resistance

thereby widening the ramp waveform. This increased area under the curve represents more energy being transferred to the hold capacitor. The result is an increased potential to modulate the control voltage, yielding higher sidebands on the VCO output. Therefore, each system must be carefully analyzed and optimized for the gain/noise tradeoff.

The analog phase detector of the MC145159 can track changes in its input over a 2π range with respect to f_R. The digital frequency steering portion of the device produces error signals over a wide range of input frequency differences.

OUTPUT BIAS CURRENT RESISTOR

Included on the MC145159 is a pin dedicated for use with an external component, called the output bias current resistor. A resistor connected from this pin (R_O) to V_{SS}' biases the output N-channel transistor, thereby setting a current sink on the analog phase detector output. With larger values of output resistance, the analog output bias current decreases (See Figure 9.)

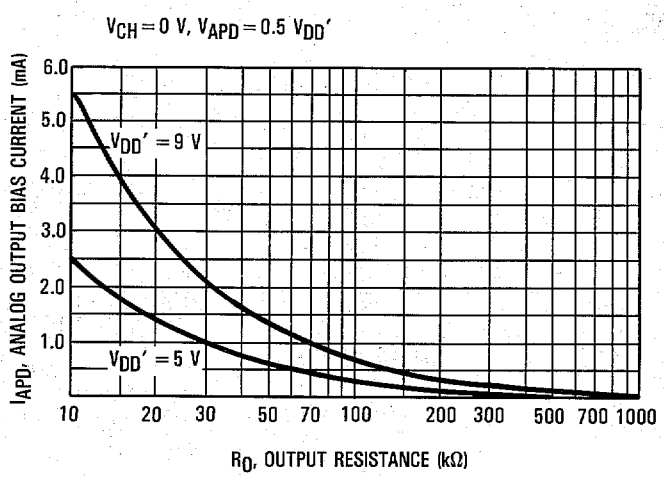


Figure 9. APD_{out} Bias Current versus Output Resistance

METHOD OF PROGRAMMING THE COUNTERS

The MC145159 contains three fully-programmable counters. The R, N, and A counters are programmed by a serial data bit stream. (See Figure 10.) Perusing the logic diagram of the device gives insight as to how the counters are loaded with data. (See Figure 1.)

First, the desired values for R, N, and A must be converted to binary form with the proper amount of bit positions. Note that the R counter is 14 bits long, the N counter 10 bits long, and the A counter 7 bits long. To load the data, the Enable pin must be taken low to isolate the counters from changes that occur in the shift registers. With Enable low, data is then loaded into the shift registers on the rising edge of the clock input. Care must be taken to ensure that Data, Clock, and Enable voltage levels and rise, fall, setup, hold, and recovery times are not violated. The divide-by-R word is loaded first with its most-significant bit as the first bit entered. The divide-by-N word follows immediately, again with its most-significant bit as the first bit entered. Next is word A, similarly with its most-significant bit entering first. The last bit of the string is the control bit. A logic one for the control bit allows all the counters to be loaded with shift register information when Enable is taken high. A logic zero entered as the control bit inhibits a reference counter latch load. Therefore, only the N and A counters are loaded when Enable is taken high.

Finally, after all the data is properly loaded into the shift registers and the control bit is at the desired logic state, Enable is taken high to program the counters. After satisfying the minimum input pulse width for Enable, that pin must then be taken low to isolate the counters from outside disturbances.

For example, suppose system requirements dictate that the R, N, and A counters be programmed with 40, 200, and 72, respectively. The steps to load the counters are outlined below.

R = 40 (14 bits)

0 0 0 0 0 0 0 0 1 0 1 0 0 0
MSB LSB

N = 200 (10 bits)

0 0 1 1 0 0 1 0 0 0
MSB LSB

A = 72 (7 bits)

1 0 0 1 0 0 0
MSB LSB

	Action	Comment
1.	Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters
2.	Shift in eight 0s	Start loading R word
3.	Shift in one 1	
4.	Shift in one 0	
5.	Shift in one 1	
6.	Shift in five 0s	R word entered; start loading N word
7.	Shift in two 1s	
8.	Shift in two 0s	
9.	Shift in one 1	
10.	Shift in three 0s	N word entered
11.	Shift in one 1	Start loading A word
12.	Shift in two 0s	
13.	Shift in one 1	
14.	Shift in three 0s	A word entered
15.	Shift in one 1	Control bit high
16.	Take Enable high ($>0.7\ V_{DD}$)	Load the three counters
17.	Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters

Now that the counters are loaded with the correct information and the system is working properly, changing the output frequency is desired. New values of N and A are chosen while keeping R the same. (R is only used in this case to set up the system resolution.) The same method can be used to program the N and A counters while simply ignoring the R counter. Take Enable low, shift in the appropriate binary data for N and A, shift in a control bit of logic zero to isolate the R counter form the Enable line, and pulse high the Enable input.

For example, suppose the new values for N and A are 178 and 13, respectively. The steps to load the counters are outlined below.

N = 178 (10 bits)

0 0 1 0 1 1 0 0 1 0
MSB LSB

A = 13 (7 bits)

0 0 0 1 1 0 1
MSB LSB

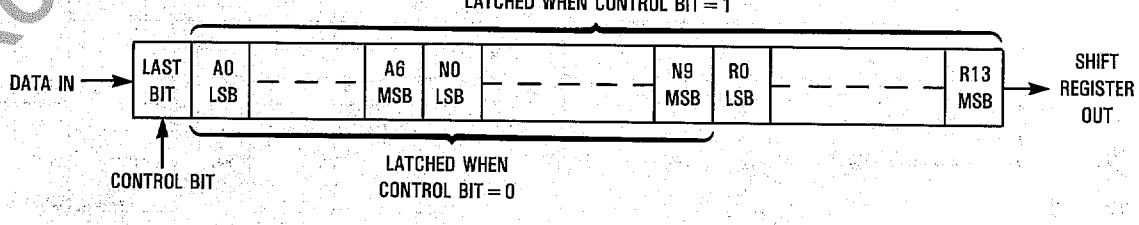


Figure 10. Data Entry Format

Action	Comment
1. Take Enable low	Isolate the counters
2. Shift in two 0s	Start loading N word
3. Shift in one 1	
4. Shift in one 0	
5. Shift in two 1s	
6. Shift in two 0s	
7. Shift in one 1	
8. Shift in four 0s	N word entered; start loading A word
9. Shift in two 1s	
10. Shift in one 0	
11. Shift in one 1	A word entered
12. Shift in one 0	Control bit low
13. Take Enable high	Load the two counters
14. Take Enable low	Isolate the counters

As is evident, the two prior routines are serial in nature. A microprocessor is therefore best suited to program the counters. Also, note that the counter outputs are not available on the MC145159 for checking correct counter operation. However, a shift register output, SR_{out}, is available. (See Figure 1.) Therefore, the same microprocessor that programs the counters can also be used to verify the contents of the shift registers to ensure that the correct data has been loaded. Enable must be held low while verifying shift register contents to avoid affecting the counters.

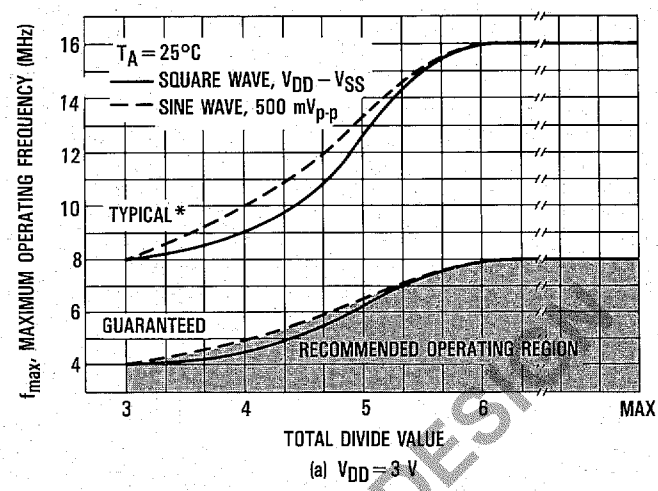
Although the MC145159 has on-chip logic for control of an external dual modulus prescaler, the device is capable of performing in a single modulus mode simply by leaving the modulus control output unconnected. In this case, the 10-bit divide-by-N counter performs the loop divide-by-N function. The A counter must still be loaded with data, but that data is a don't care. However, loading the A counter with all 0s is strongly recommended. In that way, the modulus control output is stuck high and cannot cause any possible interference by switching periodically.

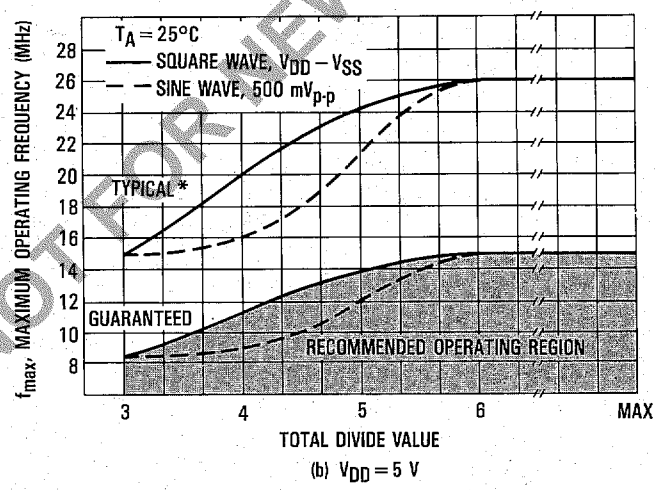
f_{in}, OSC_{in} LIMITS

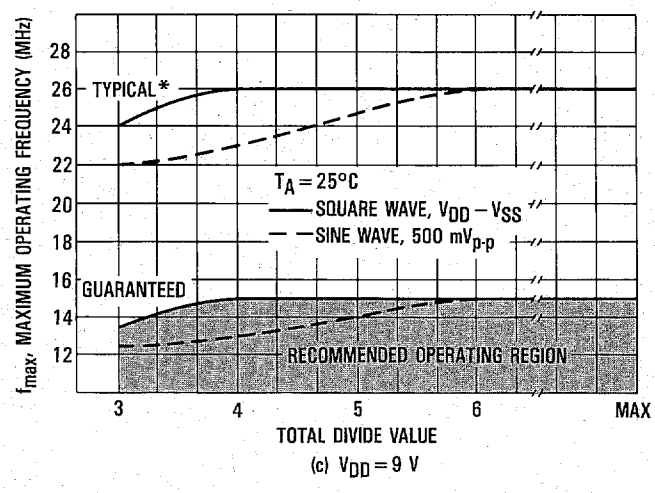
Although not stated on the data sheet, the f_{in} and OSC_{in} limits for the MC145159 are the same as for the rest of the silicon-gate MC1451XX family of frequency synthesizers. (See Figures 11 and 12.) One limit is 15 MHz for a supply voltage of 5 V and a divide value of six or greater for the N and R counters. For the time being, refer to these graphs for frequency limits.

The analog phase detector component values play a small role in determining the input frequency limits at the input to the phase detector. For high reference frequencies, a large value of I_{charge} is most likely required. Make certain that component values are in specified ranges. For best results, the following limits are recommended. (Low-leakage polystyrene or Mylar capacitors are recommended for C_R and C_H.)

$$1\ k\Omega \leq R_R \leq 1\ M\Omega$$
$$500\ pF \leq C_R \leq 0.1\ \mu F$$
$$10\ C_H \leq C_R$$
$$10\ k\Omega \leq R_O \leq 1\ M\Omega$$







*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

Figure 11. OSC_{in} and f_{in} Maximum Frequency versus Total Divide Value

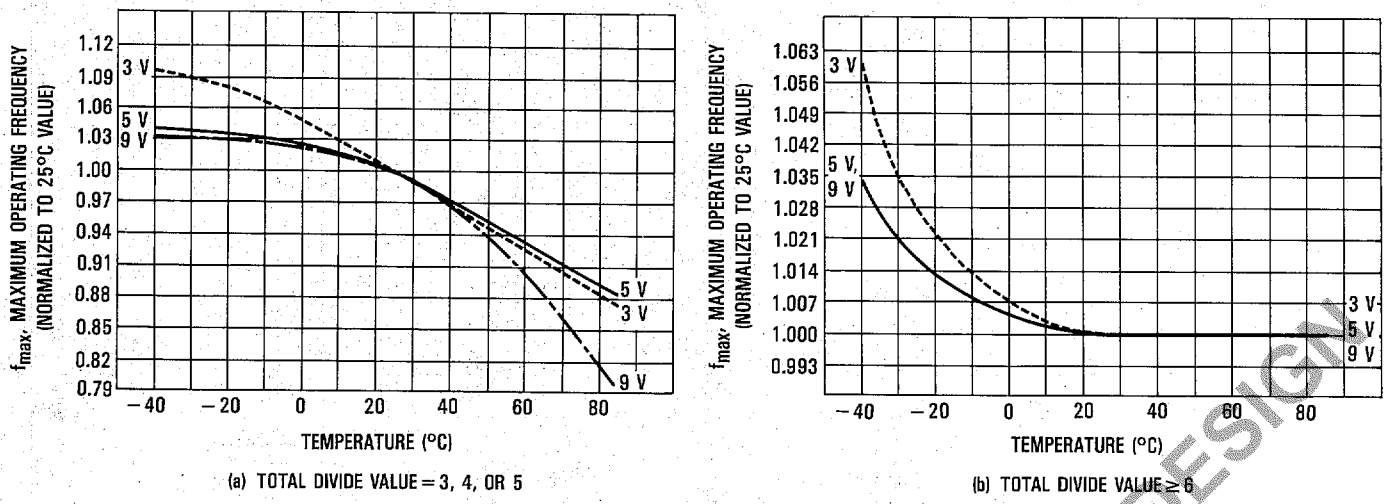


Figure 12. OSC_{in} and f_{in} Maximum Frequency versus Temperature for Sine and Square Wave Inputs

DUAL-MODULUS PRESCALING CONSTRAINTS

The MC145159 contains all the necessary logic for control of an external dual-modulus prescaler. Dual-modulus prescaling is a solution to some of the shortcomings associated with single-modulus prescaling. Inherent in the design of synthesizers using single-modulus prescaling is the fact that the value of the reference frequency into the phase detector is multiplied by the prescale value P, as well as by the counter value, N. (See Figure 13.) This results in a loss of system resolution because any unitary change of N results in the output frequency of the VCO changing by the reference frequency times P, which may be undesired.

Dual-modulus prescaling is a solution to this problem. It allows VCO step sizes equal to the value of the phase detector reference frequency to be obtained. This technique utilizes an additional A counter and a special prescaler which divides by any one of two values, depending upon the state of its control line. (See Figure 14.) In dual-modulus prescaling, the lower speed counters are uniquely configured. Special control logic is necessary to select the divide value, P or P+1, in the prescaler for the required amount of time.

The modulus control signal is low at the beginning of a count cycle, enabling the prescaler to divide by P+1, until the A counter has counted down to zero. At this time, modulus control goes high, enabling the prescaler to divide by P, until the N counter counts down the rest of the way to zero; N minus A additional counts.

$$N_{tot} = (P+1)A + P(N-A)$$

$$= NP + A$$

Modulus Control is then set back low, the counters preset to their respective programmed values, and the sequence is repeated.

This provides for a total programmable divide value of (N times P) + A. To have a range of total divide values in sequence, the A counter is programmed from zero through P−1 for a particular value N in the N counter. N is then incremented by 1 and the A counter is sequenced from zero to P−1 again.

Certain constraints apply when using dual-modulus prescaling: 1) N is greater than or equal to A always applies; 2) the value of P must be large enough so that the maximum frequency of the VCO divided by P must not exceed the frequency capability of the N and A counters; also, 3) P times the period of the maximum VCO frequency must be greater than the sum of the prop delay through the dual-modulus prescaler plus the prescaler setup or release time relative to its control signal plus the propagation delay of frequency in (f_{in}) to Modulus Control.

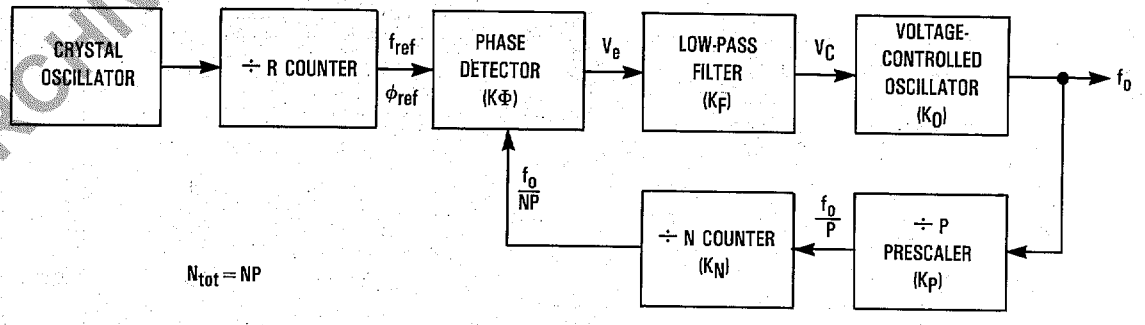


Figure 13. Single-Modulus Prescaling

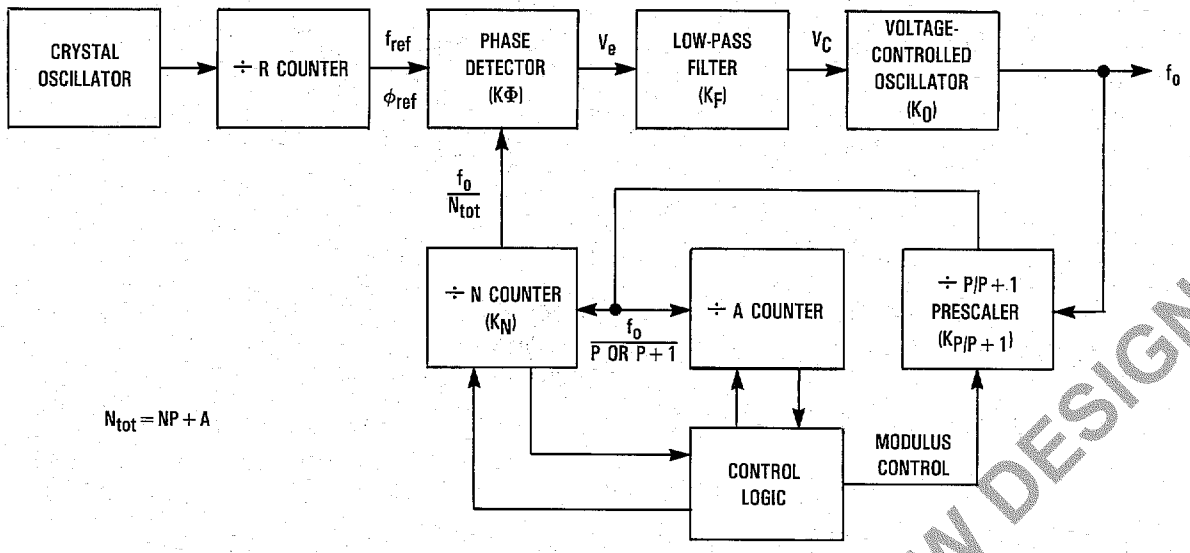


Figure 14. Dual-Modulus Prescaling

FREQUENCY SYNTHESIZER EXAMPLE

Suppose the MC145159 is to be used in a system which operates from 118.000 to 135.975 MHz in 25 kHz steps, i.e., aircraft communication transceivers. (See Figure 15.) A prescaler is needed to divide down the maximum VCO output frequency to a frequency that the MC145159 can handle (15 MHz maximum at $V_{DD} = 5$ V). A minimum prescale value of 10 is required. However, if a divide-by-10 single-modulus prescaler is used, the reference frequency would have to be adjusted to 2.5 kHz in order to maintain the 25 kHz step size. Therefore, dual-modulus prescaling is desired and the MC12016 divide-by-40/41 prescaler is selected due to an input frequency capability of 225 MHz and the ability to divide down the VCO frequency to well under 15 MHz.

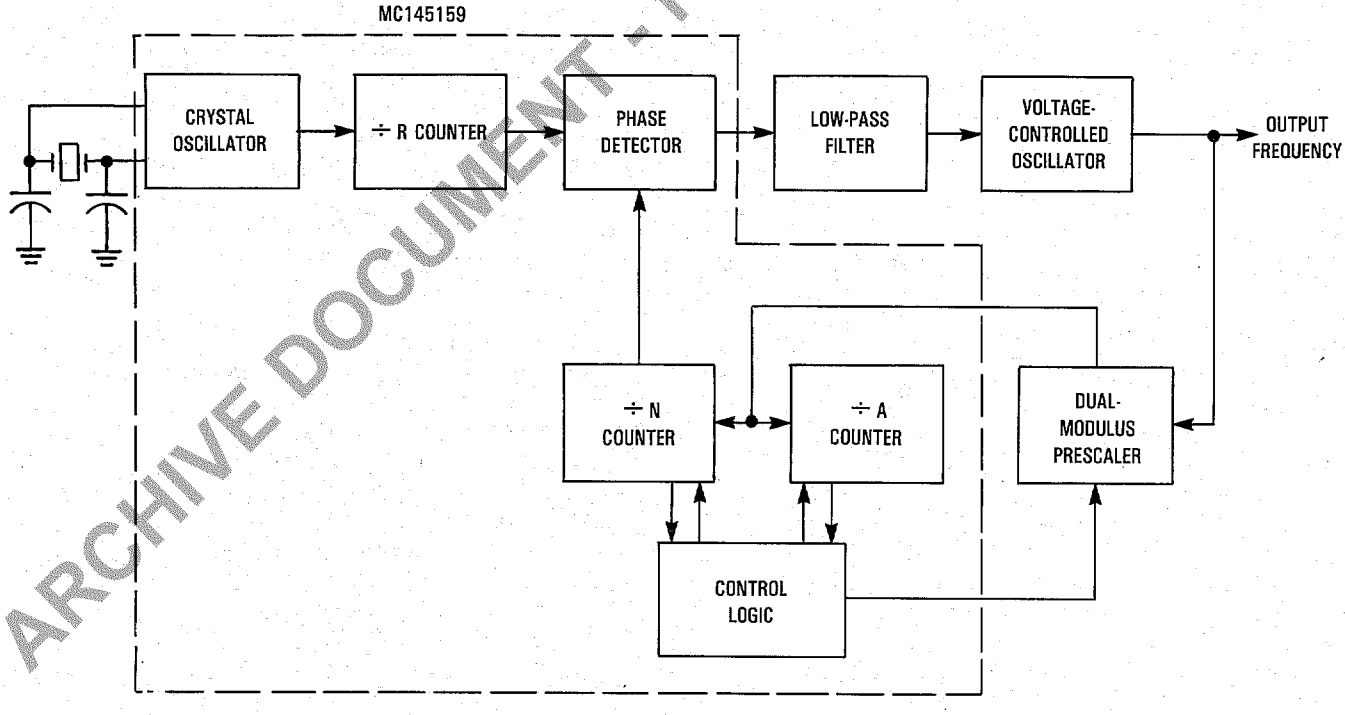


Figure 15. Typical System Application

With a reference frequency of 25 kHz, the N and A counters must be loaded with the proper values to achieve 118 to 135.975 MHz at the loop output. For example, at f_{max}:

$$N_{tot} = \frac{135.975\ MHz}{25\ kHz}$$

$$N_{tot} = 5{,}439$$

To arrive at programming values for N and A, use:

$$N_{tot} = NP + A$$

Substituting in, and for now, letting A = 0:

$$5{,}439 = N(40)$$

$$N = 135.975$$

Therefore, N = 135 is used. Now, A must be determined.

$$A = N_{tot} - NP$$

$$A = 5{,}439 - (135)(40)$$

$$A = 39$$

Similarly, at f_{min}:

$$N_{tot} = \frac{118\ MHz}{25\ kHz}$$

$$N_{tot} = 4{,}720$$

$$N_{tot} = NP + A$$

$$N = \frac{4{,}720}{40}$$

$$N = 118$$

Therefore N = 118 and A = 0.

A table can be built up showing the values of N and A and their corresponding loop output frequencies.

Table 1. Output Frequencies and Their Corresponding N and A Counter Values (f_{ref} = 25 kHz, P = 40)

Output Frequency (MHz)	N_{tot}	N	A
118.000	4,720	118	0
118.025	4,721	118	1
118.050	4,722	118	2
.	.	.	.
.	.	.	.
.	.	.	.
118.975	4,759	118	39*
119.000	4,760	119	0
119.025	4,761	119	1
.	.	.	.
.	.	.	.
.	.	.	.
135.950	5,438	135	38
135.975	5,439	135	39

*Note that because P = 40, the maximum value of A = 39.

In the example above, a 25 kHz reference frequency is used. This frequency is generally established at the reference input of the phase detector by an on-chip oscillator used with an external crystal. The R counter is programmed to divide down the crystal frequency to the required reference frequency, in this case 25 kHz. With the MC145159, the divide-by-R range is from 3 to 16,383. Therefore, the designer has many options in choosing the crystal frequency. One example is a 3.2 MHz crystal with a divide-by-R of 128 to yield a reference frequency of 25 kHz. Obviously, many other combinations are possible.

Now, a suitable gain must be chosen for the phase detector. With a 25 kHz reference frequency, successive f_R pulses occur 40 μs apart. For the first attempt, the ramp capacitor is chosen to charge up to V_{DD}' in one-eighth the time, or 5 μs. (The slope with which the ramp capacitor charges is the phase detector gain.) Therefore, the selected gain is 6.4 V/rad with a 5 V supply. Larger values of gain can be selected to speed up lock times; however, induced noise in the loop may be increased.

Values of phase detector components can now be determined using the equation for phase detector gain.

$$K_\phi = \frac{I_{charge}}{2\pi\, f_R\, C_R} \quad [V/rad]$$

letting C_R = 500 pF and solving for I_{charge} yields

$$I_{charge} = 500\ \mu A$$

Figure 8 shows that the graph for V_{DD} = 5 V crosses the 500 μA axis at R_R = 20 kΩ. With C_R = 500 pF, C_H is chosen to be 50 pF. Slightly larger values for hold capacitance may be required for noise considerations. Finally, the output resistor (R_O) can be any value between 10 kΩ and 1 MΩ, as long as the analog output bias current is compatible with the employed low-pass filter. (See Figure 9.)

A major concern in designs with the MC145159 is combining the analog phase detector output with the Frequency Steering Output properly. Three possible methods are shown in Figure 16. It should be noted that these three connection schemes are theoretical only and have not been tested in the lab. Methods of connecting these two outputs will be the subject of a forthcoming application note.

The low-pass filter and voltage-controlled oscillator must also be planned out carefully for optimal loop performance. For the MC145159, the loop filter can be combined with the connection scheme for the phase detector outputs. Further filtering may be necessary if dictated by the system requirements. In the previous example of aircraft communication transceivers, a VCO must be chosen for the loop. The Motorola MC1648 is a good choice due to an output frequency capability above the f_{max} constraint of 135.975 MHz. Consult the MC1648 data sheet for VCO design considerations.

With the loop all in place and powered up, the counters must be programmed for the synthesizer to tune to the desired channel. From Table 1, suppose 135.975 MHz is the VCO output frequency desired. The N counter should be programmed to 135 and the A counter to 39. Also, with a 3.2 MHz crystal and 25 kHz channel spacing, the R counter should be programmed to 128.

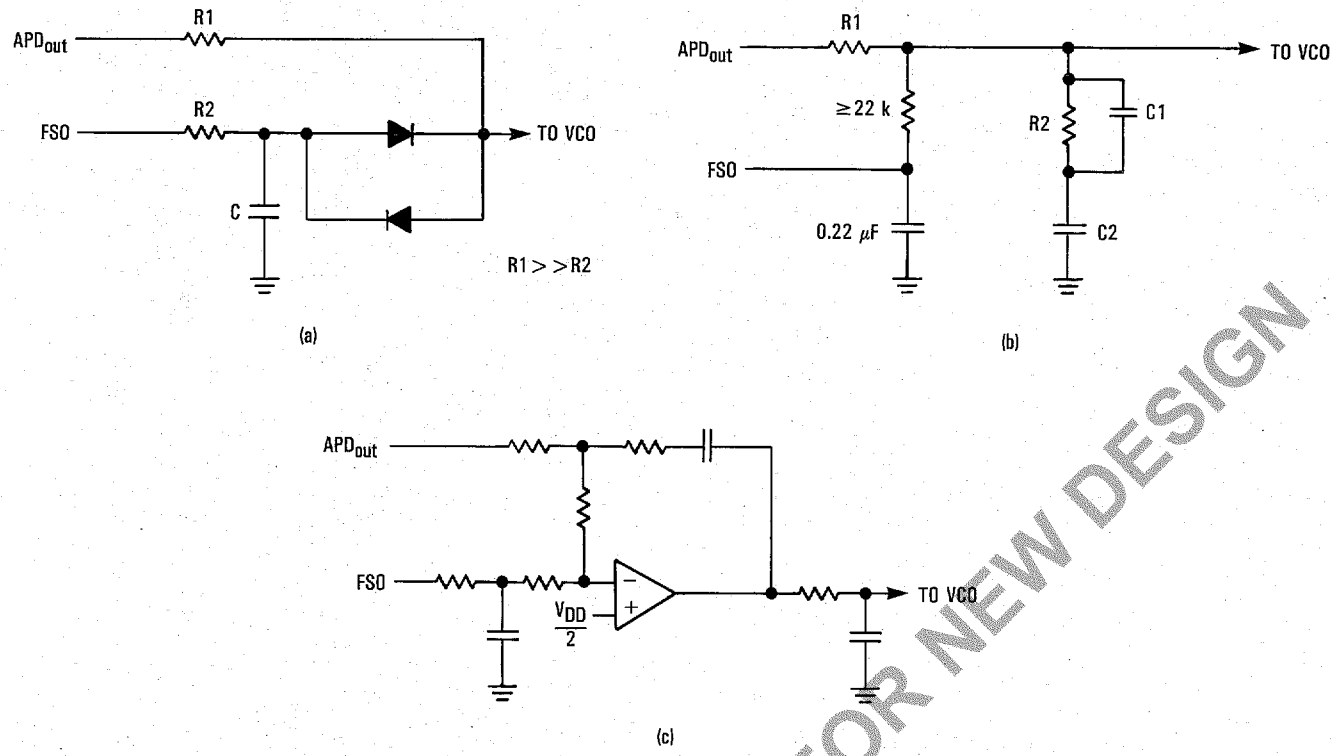


Figure 16. Possible Methods for Combining Analog Phase Detector Output and Frequency Steering Output

CONCLUSION

This application note discussed the open-loop characteristics of the MC145159 PLL frequency synthesizer with analog phase detector. The MC145159 uses an improved method over the traditional sample-and-hold technique while providing an alternative to digital phase detectors in frequency synthesis applications. The Frequency Steering Output together with the Analog Phase Detector Output combine to produce an error signal without the introduction of excessive noise. In fact, this phase detector scheme minimizes filtering requirements, reduces VCO modulation sidebands, and allows for wider loop bandwidths than are normally possible with digital phase detector outputs.

An additional application note is planned to cover the closed-loop application of the MC145159, especially the methods for combining the two phase detector outputs.

REFERENCES AND ACKNOWLEDGMENTS

1. *CMOS/NMOS Special Functions Data*, Motorola Inc.
2. Manassewitsch, Vadim, *Frequency Synthesizers—Theory and Design*, Wiley and Sons, 1980, pp. 401-407.
3. Sample and Hold Phase Detectors/Comparators, Motorola internal memo, signed by John Hatchett and Roy Jones, 10/3/79.
4. Sample and Hold Phase Detector Timing, Motorola internal memo, Andy Olesin and John Hatchett, 10/23/79.

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