



STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Circuit Examples for ISD1000A and ISD2500 Products

This chapter provides various applications of the ISD series of devices. Most can use the ISD1016A or ISD1020A, as required for the exact application. In many cases, the schematic shows an ISD1016A or the ISD2500 device in the socket.

SIMPLEST PLAYBACK ONLY

The circuit in the figure below represents the simplest playback-only implementation of an ISD1000A series device.

This schematic shows the minimum device count playback-only circuit. Change SW1 to the +5 volt "RUN" position and the contents of the ISD1000A will play one time, then stop. Because \overline{CE} is strapped LOW, set EOM bits will be ignored (though an EOM pulse will be output through the \overline{EOM} pin when a set EOM bit is encountered) and the device will play until it goes into overflow. A momentary change of SW1 to "STOP" then back to "RUN" will cause the contents of the ISD1000A to be played a second time.

VCC RUN STOP A0 VCCD Α1 16 **VCCA** A2 АЗ **VSSD** 13 Α4 VSSA A5 14 Α6 SP+ 15 Α7 SP-11 16Ω SPEAKER **AUX IN** ISD1016A Œ ANA IN 24 PD ANA OUT P/R **EOM** MIC REF 17 MIC **XCLK AGC**

Figure 1: Simplest Playback Only

SIMPLEST PLAYBACK/RECORD

The next circuit represents the simplest implementation of a record and playback non-addressed application. This circuit can use either an ISD1000A or ISD2500 device and is the same schematic found in the data sheets. To operate, start with chip enable HIGH. To record, change the Playback/Record switch to LOW, make sure the power-down switch is LOW, then change the chip enable switch to LOW. Record for the time period of the ISD device used. To playback, mo-

mentarily set the power-down switch to HIGH, then back to LOW, change the Playback/Record switch to HIGH, then pulse the chip enable switch LOW, then back HIGH. The previously recorded message will Playback. If the message did not totally fill the device, the power-down cycle is not required. If the chip enable switch is held LOW while in Playback, the entire contents of the device will play regardless of any EOM bits being set.

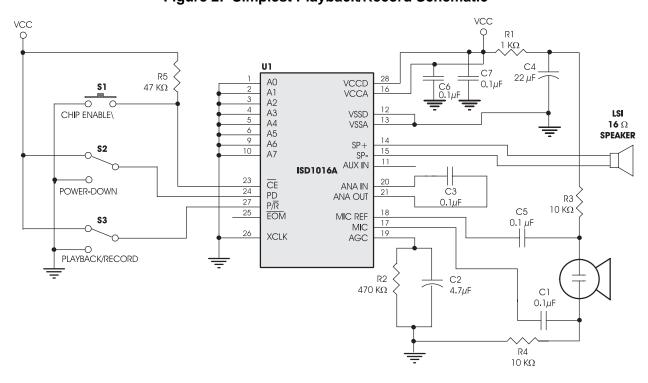


Figure 2: Simplest Playback/Record Schematic

PLAYBACK LOOPING

Many audio applications require repetitive play-back or looping on the same message for an extended time. The ISD1000A series of devices may be used to satisfy this requirement using either the built in Operational Mode or using a small amount of external logic. Both applications may be controlled by the Chip Enable pin so looping can be started and stopped or run continuously when power is applied.

PLAYBACK LOOPING USING OPERATIONAL MODE

Figure 3 shows that Operational Mode may be used to accomplish playback looping if the message starts at Address 0 (the beginning of the memory) and does not require the full 16 seconds of analog storage. Operational Mode may not be used if the starting address is not zero or the message completely fills the ISD1016A.

VCC VCC Α0 VCCD 2 Α1 VCCA 3 A2 4 VSSD А3 13 5 Α4 VSSA A5 9 14 Α6 SP+ 10 15 Α7 SP-11 $16~\Omega$ SPEAKER AUX IN ISD1016A 23 CE ANA IN 24 27 PD ANA OUT P/R EOM 18 MIC REF 17 MIC 26 **XCLK** 19 AGC

Figure 3: Operation Mode Playback Looping

NOTE: Circuit loops beginning at 000 and the message cannot reach 160 (end).

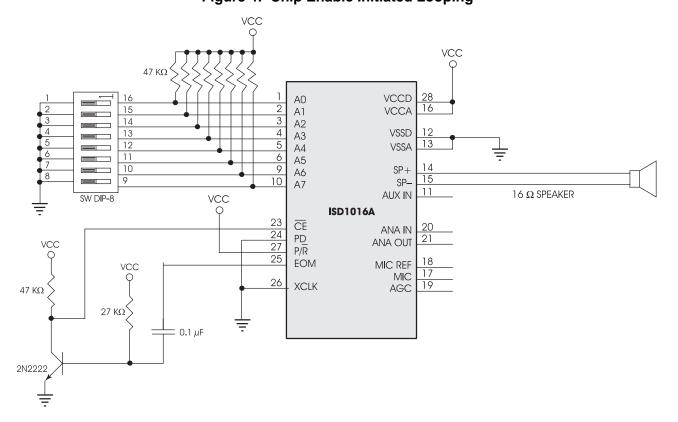


Figure 4: Chip Enable Initiated Looping

A message is first recorded into an ISD1016A with all the address bits tied LOW. This positions this message at the beginning of the ISD1016A's address space. Next, the device is put into Operational Mode by connecting Address bits A7 and A6 HIGH (+5 VDC). Bit A3 is also connected HIGH to enable continuous repeat. With PD LOW, P/ \overline{R} HIGH, and \overline{CE} held LOW, the beginning message in the ISD1016A will repeat. If \overline{CE} is taken back HIGH after a message has begun, the ISD1016A will complete the message, then stop. If \overline{CE} is strapped LOW, when power is applied, the message will repeat continuously.

CHIP ENABLE INITIATED LOOPING

Figure 4 shows a simple one transistor circuit that may be used to achieve playback looping using chip enable. This circuit may not be used if the ISD1000A series device is completely full.

The EOM pulse at the end of a message is differentiated to produce about a 15 ms positive going pulse into the CE pin. When this pulse falls, the address is loaded into the device by the DIP switch and a new Playback cycle starts at that address. Since the original message has continued to play during this pulse, the message is smoothly restarted without a break.

THREE MINUTE CASCADE USING THE ISD2560

The circuit illustrated in Figure 5 demonstrates a method of cascading three ISD2560 devices to obtain up to three minutes of storage.

The ISD2560 may be easily cascaded to increase the storage capacity of a system. Two methods are discussed in the following paragraphs. The first method shows three devices cascaded in a mode where a number of messages may be sequentially recorded starting at the beginning of memory. A message may be recorded across the boundary of two devices. The transition between the two devices will be transparent to the user. Message cueing, the AO Operational Mode

(fast forward) may then be used to rapidly access and playback any of the recorded messages. It is not necessary to know the exact address location of each message. Only the sequential message number need be known.

The second method shows how to directly address and record or playback a message at any point in the three devices' memory space. A message may be recorded or played back across the boundary of two devices. The transition between the two devices will again be transparent to the user.

In the two examples shown, three ISD2560s have been cascaded resulting in a total record/playback time of three minutes. Alternatively, ISD2575s or ISD2590s could be used to achieve 3 minutes 45 seconds, or 4 minutes 30 seconds, respectively.

In each example, U1, the first ISD2560 in the series, contains the microphone preamplifier and the speaker output for the entire system. This is in addition to having the first 60 seconds of analog memory. The remainder of the ICs being cascaded serve only as memory elements. The ANA OUT (microphone preamplifier output) pin of U1 is connected through blocking capacitors to the ANA IN of each of the three devices in the cascade. Additionally, the SP+ of U3 is fed back to U2's AUX IN pin and U2's SP+ is connected back to U1's AUX IN pin. Thus, the ANA IN pins are fed in parallel from U1's microphone preamplifier while the speaker outputs "daisy chain" back to U1's speaker amplifier.

SEQUENTIAL RECORD AND MESSAGE CUEING EXAMPLE

Operational Mode is used to set up the ISD2560 for proper cascade operation. The ISD2560 is placed into Operational Mode by connecting address bits A8 and A9 HIGH. The remainder of the Operational Mode bits are tied LOW except as follows:

 $_{0.1\,\mu \rm F}^{\rm C8}$ C7 1 µF C14 0.1 µF ÿΙ γ2 EOM C9 + |||• 2555 X X X X X X X X X 4082 Чμ -|||- \exists O VCC A7 KD ANA IN ANA OUT MIC REF AGC VSSD SP+ SP-AUX IN ISD2560 PLAYBACK/RECORD **S3** S1 CE PUSH BUTTON XOVEN A SET OF S POWER-DOWN 16Ω SPEAKER C3 1 µF C11 C11 μF HI tM1 Electret Microphone) C1 0.22 μF 0.1 µF R5 47 KΩ C2 4.7 μF ANA OUT
MIC REF
MIC AGC SP+ SP-AUX IN VSSD VSSA ISD2560 78 OI A0 (Message Cueing) R2 < 470 KΩ < C4 -220 µF \[\frac{1}{2} \\ \fr Цп.

Figure 5: 3-Minute Cascade Schematic

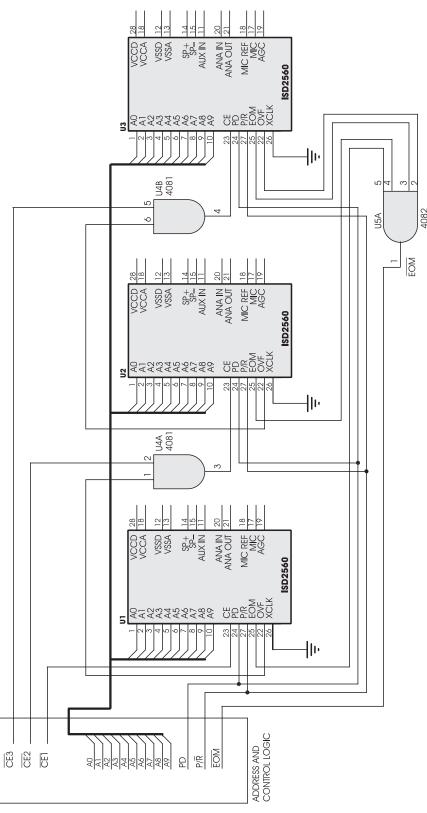


Figure 6: ISD2560 Cascade and Direct Addressing

- 1. All Record or Playback cycles must start with a power-down cycle.
- 2. Address lines should be applied T_{SET} before the falling CE and return to 0 after T_{HOLD} time. Address lines must then remain at 0 throughout a Record or Playback cycle.

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Bit A4 is HIGH to cause the Message Start Pointer (MSP) to *only* be reset when the system's mode is changed between Record and Playback. (Normally the MSP is initialized anytime the Chip Enable pin goes LOW.)

NOTE The MSP controls where the ISD2500 is going to begin to record or playback on the next operation. It is also initialized when the Power-Down Cycle is initiated.

The result of this configuration is that messages will be stacked sequentially during record across chip boundaries in a manner transparent to the user. Changing from Record to Playback resets the MSP back to the beginning of the first message in the series. The next Playback proceeds under control of chip enable.

Record Operation

To begin recording, place the Record/Playback switch in the record position and hold chip enable LOW for the duration of the recording. To record the second message, repeat the operation; recording will now begin at the end of the first message. Additional recordings may be placed sequentially into the cascaded devices until the memory is full. The OVF pulse out of the last memory may be used as a "memory full" indicator.

Playback Operation

To playback the first recorded messages, change the P/\overline{R} pin to a HIGH and pulse the \overline{CE} pin LOW. The first message will playback and stop at the set EOM bit. A second LOW \overline{CE} pulse will start playback of the second message. Each message may start or stop anywhere in the cascade memory. The AO Message Cueing Operational Mode may also be used to access messages anywhere in the cascade memory. This "fast forward" operation will transparently cross the boundary between two devices. AO Message Cueing is discussed in detail in the section on Operational Modes.

DIRECT ADDRESSING EXAMPLE

The second cascade circuit shows the added logic necessary for direct address of messages anywhere in the three devices' memories. Only a single 2 input AND gate is required for each chip cascade. For simplicity, the analog circuitry is left off this schematic.

To address any message, the user must know the starting address of the message and in which device it begins. For instance, a message might begin in device U2 at address 400, or 40 seconds into the memory. This message may run over into U3 with no problems. To start playback of this message, PD must be taken LOW and P/\overline{R} taken HIGH. The address 400 (decimal) must be placed on the address bus. This equates to 190 Hex.

Next the $\overline{\text{CE}}2$ line is taken LOW and playback begins. Playback will continue until a set EOM bit is found. The pulse will appear at the $\overline{\text{EOM}}$ output from U5A. Note that this will be a 12.5 ms pulse unless the message ends at overflow at U3. In this case, the $\overline{\text{EOM}}$ pulse will be approximately 6 μ s long.

PUSH BUTTON FOUR MEMORY RECORD/PLAYBACK

A version of the circuit shown in Figure 7 first appeared in December 1991 *QST Magazine*. It demonstrates how a single ISD1020A may be used to store up to four 5-second messages that may be individually retrieved using a single push button for each.

NOTE:

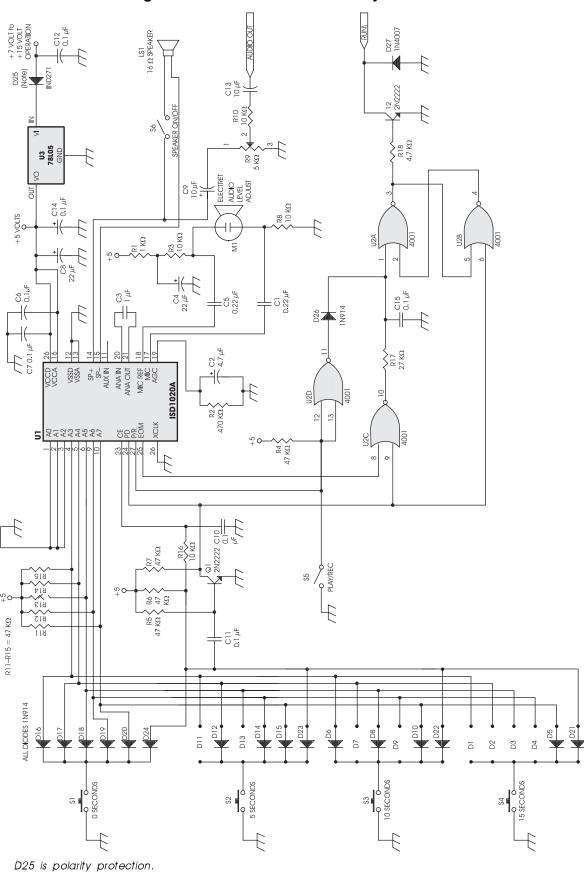


Figure 7: Push-Button Four Memory Schematic

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HOW THE CIRCUIT WORKS

The ISD1020A can be operated in several different modes. In this project, it operates in an "addressed" mode. The eight address pins of the device determine where the Record and Playback operations begin. The ISD1020A can be looked at as a miniature tape recorder. It has the ability to pre-position the Playback/Record head anywhere on this 20-second tape before we begin an operation. The device has 160 valid addresses, giving an address resolution of 0.125 seconds. This means eight address counts equal 1 second of record time.

To determine what address to give the device, we must first convert seconds into binary counts. A 1-second resolution is adequate for our purposes. Since eight counts equal 1 second and eight is an "even" binary multiple, we can ignore all the counts less than eight. We do this by strapping A0, A1 and A2 to ground and just programming the five remaining bits. Using push buttons and diodes, we can select any interval between 1 and 19 seconds for the start of record or playback.

As shown in Table 1, the four start message locations are 0 seconds (beginning of memory), 5 seconds, 10 seconds and 15 seconds. This defines four 5-second messages.

Table 1: Address Boundaries Example

Chart 1		Chart 2	
Monago	Addr Pins	Monaga	Addr Pins
Message Start Location	AAAAAAA 76543210	Message Start Location	AAAAAAA 76543210
Seconds		Seconds	
0	00000000	0	00000000
5	00101000	4	00100000
10	01010000	8	01000000
15	01111000	14	01110000

Table 1 shows the binary addressing for these intervals. The message start locations could have as easily been defined as 0 seconds, 4 seconds, 8 seconds, and 14 seconds giving two 4-second messages and two 6-second messages. Chart 2 shows this second set of intervals. You can experiment with the diode positions for various addresses but keep in mind that the highest message start address the ISD1020A will recognize is binary 10011111 or 159 decimal. Since A0, A1 and A2 are always at ground, the highest recognizable address is at the 19-second boundary or 10011000.

The Playback/Record function of the ISD1020A is determined by the P/\overline{R} pin (pin 27) of the device. Simply tie it LOW for Record and to +5 V for Playback.

The ISD1020A requires the Chip Enable pin (pin 23) to start HIGH, pulse LOW for Playback and stay at a LOW level during record. All the address and the Playback/Record inputs must be set up before the Chip Enable pin goes LOW. At the end of recording, returning the Chip Enable pin to a HIGH ends the recording and inserts an end of message bit into the ISD1020A's memory. When the Chip Enable pin is pulsed LOW when the Playback/Record pin is HIGH, the device will playback what is recorded until it encounters an end of message bit. It then stops Playback and waits for the next control input.

The one remaining input to the ISD1020A is the power-down or PD pin (pin 24). This pin controls the power requirements of the ISD1020A. When taken to +5 volts, the chip uses less than 10 microamps of current. The device must be powered up (Power-Down pin at ground) to record or playback. This pin also serves as a reset if the ISD1020A is recorded or played "into the stops." That is, all the way to the end of the device's 20-second memory. When that happens, the Power-Down pin must be cycled HIGH then back LOW again for the device to continue operation. This is by design. When two or more ISD1020As are cascaded together to make messages longer than 20 seconds, the device must stop operating when it reaches the end of its memory space so the next chip in the series can take over. This condition is called "memory overflow."

To get around the requirement to cycle the Power-Down pin after a memory overflow, the circuit design shown here automatically cycles the device through a power-down cycle each time the chip enable is activated. All four push buttons are connected to the $\overline{\text{CE}}$ pin and to C11 through diodes. The R16, C10 network "debounces" the chip enable input. When you press a push button, a sequence of events happens:

- 1. The $\overline{\text{CE}}$ input that is normally held HIGH through R6 is pulled LOW through a diode.
- 2. The combination of C11 and R5 on the base of Q1 causes a positive pulse to be generated into the PD pin of the ISD1020A.
- **3.** For the duration of this pulse, the ISD1020A is in a power-down state that resets a memory overflow condition if it exists.
- **4.** When the pulse ends and the PD pin returns to ground, the status of the $\overline{\text{CE}}$ pin is read.
- 5. Assuming the CE pin is still being pulled LOW (don't be too quick on the push button), the status of the address and P/R pins is read and the Record or Playback operation begins.

Components R2 and C2 control the AGC operation of the ISD1020A's internal microphone preamplifier. The AGC pin has an impedance of about 5K ohms. This resistance plus C2 determines the attack time of the AGC which should be very fast. R2 and C2 together determine the release time of the AGC which should be fairly slow.

C3 connects the output of the microphone preamplifier (ANA OUT, pin 21) to the analog input (ANA IN, pin 20) of the ISD1020A. These pins are brought out externally so the user can control the low frequency response of the recording or directly access the analog storage memory of the ISD1020A. A 1 μ F capacitor at this location sets the low frequency response to 80 Hz. Users who do not want to use the AGC should capacitively couple to the ANA IN pin with an 50 millivolt peak-to-peak signal.

The speaker output of the ISD1020A is designed to drive a 16-ohm speaker. To use an 8-ohm speaker, install R8 to bring the impedance into specification. If you use a 16 Ω speaker, R8 should be replaced with a wire jumper.

The ISD1000A series does not have a "RUN" output to show when a device is playing back speech. Such a signal is easy to create, however, using a pair of the two input NOR gates contained in a 4001. These gates (U2A and U2B) are connected in a "cross-coupled" configuration and are set by PD signal going LOW at the beginning of Playback and reset by EOM going LOW at the end of a message. The resulting signal drives the base of the Q2 2N2222 transistor through R21. U2D keeps the gate from being set during a record operation. U2C and the RC network C15 and R20 correct a possible race condition between the PD signal and EOM.

OPERATION

Operation of the circuit is simple. To record a message, change the Record/Playback switch to record, then press and hold the desired address button for the duration of the message. To play the message back, change the Record/Playback switch back to Playback and momentarily press the button. The ISD1020A will replay the message.

Keep in mind when recording a new message that if you record a message longer than the address space you have reserved for it, you will begin erasing the next message in the series (unless you go into memory overflow). If you then try to select the message you just erased part of, you will get the end of the new message starting at the message address of the message you just "corrupted." If you want to record a message longer than its allowed message space, just go ahead and do it. Just remember that the next message is not available in this instance.

U5 LM7805 R1 470 KΩ R2 47 KΩ 0 00 l KΩ S :: # R4 470 KΩ 0.1 F MESSAGE #3 R3 47 KΩ 25 K S R9 220 KΩ O.1 #F 8 E E C12 MESSAGE #2 48843248 02 0.1 #F U4 S3 S2 S3 S3 S3 8 C] [VCC R19 < 47 KΩ < MESSAGE #1 XCK NOW XCK 488488<u>48</u>8 D1 LED KRECORD ENABLE S3 MSG 2 S4 NSG 34 R16 470 KΩ

Figure 8: Radio Notepad Schematic

- 1. D7 is a polarity protection diode.
- 2. D8, D9, and D10 are IN914
- 3. R10, R11, R12, and R13 are 47 $K\Omega$.

RADIO NOTEPAD

The circuit in Figure 8 presents a method of storing three different 16-second messages using a speaker input. The suggested application is for recording messages from a radio receiver.

There are many applications that require the recording of audio directly from a speaker. A shortwave listener-hobbyist may want to record an event heard on a shortwave or two-way radio channel. There may be a call sign, a radio frequency or some other information announced over the air that needs recording for later review. In a public safety environment, a police dispatcher may want to record an incoming call for assistance to ensure no details are missed.

With the circuit in Figure 8, a simple two button sequence is all it takes to record the next 16 seconds. A single push of a button plays each message back. Three ISD1016As are used to hold independent messages. An ISD1020A could be used instead if desired. This circuit example also demonstrates an ISD1000A device run entirely from push buttons.

HOW IT WORKS

The heart of this application is a 4044 CMOS Quad NAND R-S Latch and a VN10 FET timer. The 4044 (U4) "remembers" which message button has been pressed when a Record or Playback operation is desired. The FET timer enables a record operation for its time period. The rest of the circuit is principally diode steered logic.

A Playback operation is initiated by pressing \$2, \$3 or \$4 (MSG 1, MSG 2 and MSG 3 respectively) which resets the appropriate section of U4. The output of the cleared Flip Flop goes LOW, enabling the correct \overline{CE} for the ISD1016A holding the message selected. This output also pulls C13 LOW causing Q1 to initiate a PD cycle clearing any possible overflow condition. The base of Q1 is pulled LOW, allowing R3 to pull its collector HIGH, resetting the PD pins of U1-U3. As R9 charges C13 back up the PD line returns LOW. When the PD cycle ends, the selected device plays back its stored message. When a set EOM bit is found or an over-

flow occurs in the operating ISD1016A, Playback stops and the \overline{EOM} signal goes LOW, setting the U4 flip flops through D8, D9 or D10. Or, a momentary press of the STOP button resets the set R/S flip-flops and initiates a PD cycle. This also ends Playback.

A record operation is started by first pressing the S1 "Record" button. This clears the Record Enable section of U4 (R0/S0/Q0) whose Q output goes to the P/\overline{R} input of all the ISD1016A's. This holds these pins LOW or in the record state. This flip-flop stays cleared until the Q3, R14, C14 network times out. When this happens, the signal from the collector of the Q2 NPN inverter transistor sets the first section of U4, returning all the P/\overline{R} inputs HIGH, back to Playback. If S2 through S4 is pressed while the Q3 timer is running, the appropriate ISD1016A will start recording. A press of the STOP button will end recording by forcing the chip enable lines HIGH out of U4 and setting an EOM bit in the recording device, U1-U3. The values of R14 and C14 are chosen so that the P/\overline{R} pins are held LOW throughout the complete record cycle, or in this example, greater than 16 seconds. If an ISD1020A is used, the value of R14 should be made greater so this time period is greater than 20 seconds.

OPERATION

To operate the radio notepad, connect the input across the speaker terminals and apply power. To record, press the record Enable S1 button then immediately press S2, S3 or S4. Recording will start with the press of the second button. The record Enable LED, D1, along with the RUN LED, D2, will indicate that a record operation is in progress. To stop recording, or to clear a record Enable condition before it times out, press the S5 Stop button. To Playback, press S2, S3 or S4. The message recorded in the appropriate ISD1016A will Playback until the 16 seconds is complete or a set EOM bit is found in the device's EOM memory. The RUN LED, D2, will indicate when a message is being played back. To stop Playback, press Stop.

Some experimentation with the setting of the R8 Record Level pot may be necessary to get good results.

USING THE ISD2500 SERIES WITH A MICROCONTROLLER

The record and playback duration of the ISD2500 series make it possible to perform several functions with a single device. A chip with 32 or more seconds of storage may be used in a number of ways. A library of permanent words, phrases or sounds may be individually played back under external control. Alternatively, this device might be used to record and randomly retrieve arbitrary length messages. A combination of these two approaches is also possible.

Combinational logic may be used to achieve these ends. This approach is complex, however. An inexpensive microcontroller is a simpler and much more flexible solution. The following notes demonstrate several methods of using a single chip microcontroller to control an ISD2500 device.

NOTE The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible. If a device is to be used on a bus oriented system, the address lines must be buffered and latched.

CONVENTIONAL MODE OPERATION

An obvious method of driving the device is to operate it in the conventional mode. The sequence for such an operation is as follows:

- Change the PD pin to LOW and delay T_{PUD} (see the ISD2500 series data sheets). This will power up the device.
- **2.** Apply the desired address to the address inputs.
- **3.** Apply the correct level to the P/\overline{R} pin as desired (0 = record, 1 = play).
- **4.** Pulse \overline{CE} LOW to begin Playback, hold \overline{CE} low to begin record, bring \overline{CE} back HIGH to end record.
- **5.** If low power is required, change PD back to HIGH when the operation is complete.

The timing of the above sequence is not critical at microcontroller speeds. For instance, required address setup timing (T_{SET}) is 300 nanoseconds before the falling edge of \overline{CE} . Few microcontrollers can execute fast enough to violate this timing.

A microcontroller may be used to detect the end of a normal speed Playback operation in at least two ways.

- Since the EOM pulse width in the fastest ISD2500 series parts (ISD2532/60) is over 12.5 milliseconds long, it is possible to poll this input and watch for it to go LOW.
- An alternative method would be to connect the EOM pin to the microcontroller's interrupt input. If an edge-triggered interrupt sense is available, it may be more efficient to sense the rising edge of EOM. This is because a new CE initiated operation cannot begin until EOM pin returns to the HIGH state.

The ISD2500 series includes the $\overline{\text{OVF}}$ pin to indicate the overflow or message full condition. During Playback the $\overline{\text{OVF}}$ pin pulses LOW for approximately 6 microseconds when overflow is reached. The $\overline{\text{EOM}}$ pin does not go LOW at overflow unless an EOM bit is set in last row of the analog memory. After the initial $\overline{\text{OVF}}$ pulse goes LOW, the $\overline{\text{OVF}}$ pin will track the $\overline{\text{CE}}$ input as long as the device remains in overflow. This pin is normally used to cascade multiple ISD2500 devices together.

The original short $\overline{\text{OVF}}$ pulse may be detected using the microcontroller's external interrupt input. An alternative technique would be to hold $\overline{\text{CE}}$ LOW, even during Playback. The $\overline{\text{OVF}}$ pin will now go LOW and stay LOW at overflow and may be detected by polling. In this example, a falling $\overline{\text{EOM}}$ must be detected and used to force $\overline{\text{CE}}$ back HIGH. $\overline{\text{CE}}$ must go back HIGH before $\overline{\text{EOM}}$ goes HIGH with $\overline{\text{CE}}$ still LOW, the set EOM bit will be skipped and the device will continue on playing back the next message.

MESSAGE CUEING "FAST FORWARD" OPERATION

Some applications may require the use of the Message Cueing M0 Operational Mode. This mode allows the user to "fast forward" through the message space of the device (see the section on Operational Mode). When operating in this mode, the ISD2500's internal timing is sped up by a factor of 800. The EOM pulse width now may be as small as 11 ms. (A general discussion of Message Cueing timing may be found in the section on Operational Modes.) This timing is too short to allow for polled operation in most microcontrollers. The external interrupt should be used to detect EOM in this instance.

Pin count is often a factor when using a microcontroller. The designer may not want to tie up 8 pins for address plus PD, \overline{CE} , P/\overline{R} . \overline{OVF} and \overline{EOM} . This is a total of 13 pins. An alternative approach is to use the Message Cueing M0 Operational Mode with the M4 consecutive addressing mode. This application requires the connection of only 6 pins to the microcontroller: PD, \overline{CE} , P/\overline{R} , \overline{OVF} , \overline{EOM} and M0. M4, A8 and A9 are permanently tied HIGH and all the rest of the address pins are tied LOW. Sequential recordings of multiple messages of random length and the playback of those messages in any order are possible in the following sequences.

Sequential Recording

- 1. M0 is left LOW throughout record.
- **2.** Change the PD pin to LOW and delay T_{PUD} .
- **3.** Change P/\overline{R} to LOW.
- **4.** Hold \overline{CE} low to begin the first record. Bring \overline{CE} back HIGH to end record.
- **5.** Additional record operations may be done using sequence 4. Each recording will be appended to the end of the previous with an EOM flag bit set at the end of each messages.
- **6.** OVF will go LOW if the device overflows during record.
- **7.** At the end of the record sequence, PD is taken HIGH to power down the device and to reset the internal address counter.

Playback of Messages in Any Order

To playback message "N," perform the following sequence:

- 1. Change the PD pin to LOW and delay T_{PUD} .
- **2.** Change P/\overline{R} to HIGH.
- **3.** If N = 1 (the first message), then A0 = 0, and pulse \overline{CE} LOW. The first message will play then stop.
- **4.** If N is greater than 1, you must first execute N-1 A0 Message Cueing Operational Mode cycles by doing the following:
 - **a.** Change A0 to HIGH.
 - **b.** Pulse \overline{CE} LOW for less than 10 μ s.
 - **c.** Either watch for a LOW $\overline{\text{EOM}}$ (may be as short as 11 μ s) or pause for approximately 100 ms.
 - d. Each time you find an EOM, you have reached the end of a message. You will have moved silently through a message at 800 times normal speed.
 - e. Subtract 1 from N. If N does not equal 1, proceed to sequence (a) and do it again.
- **5.** If N has been subtracted down to 1, then change A0 to 0 and pulse \overline{CE} LOW. The Nth message will play at normal speed.

NOTE The timings above are approximate. See the Operational Modes for a general discussion of Message Cueing Timing.

PUSH-BUTTON MODE OPERATION

The ISD2500 series device includes a new Operational Mode called "Push-Button Mode." This M6 Operational Mode changes the functionality of the \overline{CE} , PD and \overline{EOM} pins. The operations of these pins are fully explained in the Operational Mode section. A microcontroller may be used with this mode to gain several important extra features. Push-Button Mode allows the user to sequentially

playback several messages then change to record and add additional messages at the end of those already played. This also allows the designer to power-down the device between sequential record operations, an important feature in battery powered applications.

Sequential Record with Power-Down in Between

In the following sequences, M4, M6, A8 and A9 of an ISD2560 are tied together and to a pin of the microcontroller. The A0 Message Cueing Operational Mode is used as indicated. All the other address pins are tied LOW. It is only necessary to use 6 pins from the microcontroller, PD (Stop/Reset), $\overline{\text{CE}}$ (Start/Pause), $\overline{\text{EOM}}$ (run), P/ $\overline{\text{R}}$, A0 and the combined M4, M6, A8 and A9. These combined pins will be called Op Mode Control. $\overline{\text{EOM}}$ is tied to the microcontroller's external interrupt pin. The microcontroller should be set up for a negative edge triggered interrupt. $\overline{\text{OVF}}$ is not needed as explained below.

To achieve flexible message control, the micro-controller must keep track of the number of messages recorded and played back. This count will be used with the A0 Message Cueing "fast forward" function to record messages sequentially and play them back in any order.

NOTE A false interrupt is generated each time a control operation causes the EOM to fall. These interrupts should be ignored by the microcontroller. The EOM pin will go LOW and generate a wanted interrupt under two circumstances: during Playback or Message Cueing when a set EOM bit is encountered and during record when the device goes into overflow. This also allows the designer to determine when overflow is reached without looking at the overflow pin.

- 1. The sequence begins with PD HIGH, P/\overline{R} HIGH, \overline{CE} HIGH and Op Mode control LOW.
- 2. Set up to record of the first message by taking PD LOW, P/\overline{R} LOW, and Op Mode control HIGH.

- 3. When the OP Mode control pin goes HIGH, the EOM pin (which becomes the active HIGH run pin in Push-Button Mode) pin will go LOW to indicate the operation has not yet started. This will cause an interrupt in the microcontroller that should be "discarded."
- 4. To begin record, pulse \overline{CE} LOW (a pulse begins and ends record in Push-Button Mode). The \overline{EOM} pin will go HIGH to indicate an operation in progress. When recording is finished, pulse \overline{CE} LOW to end the record cycle. The \overline{EOM} pin will go LOW and generate another false interrupt.
- **5.** After the completion of the record, change the Op Mode control pin to HIGH, and take PD HIGH. This powers down the ISD2560 device to typically 1 microamp.
- 6. To record the second message, take PD HIGH (T_{PUD} delay), P/R HIGH, and Op Mode control HIGH (false interrupt). We are now positioned at the beginning of the first message. Take A0 HIGH and pulse CE LOW. This puts the device into Message Cueing "fast forward" and jumps to the end of the first message. The EOM pin will go HIGH and then LOW to indicate the end of the first message has been found. The EOM interrupt may be used by the microcontroller to process this.
- 7. A0 may now be taken LOW, P/R changed to LOW, and a new record cycle begun. A unique feature of Push-Button Mode keeps the internal address pointer of the ISD2560 from being reset during the change of P/R from HIGH to LOW. Recording of the second message will begin at the end of the first message will remain. The device may again be powered down.
- **8.** Subsequent recordings may be made using additional A0 Message Cueing operations.

Playback Operations

Playback of any message may be achieved using the Push-Button and AO Operational Modes.

- 1. The sequence begins with PD HIGH, P/R HIGH, CE HIGH and Op Mode control LOW.
- Change PD to LOW (T_{PUD}), and Op Mode control HIGH (false interrupt).
- **3.** Take A0 HIGH and execute N-1 Fast Forward operations.
- **4.** Take A0 LOW and pulse \overline{CE} LOW to begin playback of the desired message.
- **5.** A falling EOM indicates an end of message has been found.
- **6.** Take Op Mode control LOW and PD HIGH to power-down the device.

OTHER NOTES

A continuous LOW on the interrupt input of some microcontrollers may interfere with other types of interrupts. The reason that the device is taken out of Push-Button Mode after each operation is to make the EOM pin go HIGH in the static state. This frees up the microcontroller's interrupt structure.

All Push-Button Mode operations will be slowed by the debounce timer built into this function. A delay of T_{DB} will occur with each Push-Button Mode operation.

CONCLUSION

The above explanations show one of many possible ways to control the ISD2500 series device with a microcontroller. The designers should review this information and apply their unique perspective to the application they are designing.

RECORDING INDICATOR LIGHT

The circuit shown in Figure 9 is a simple method of using an LED to indicate when a record operation is in progress with an ISD1000A series device.

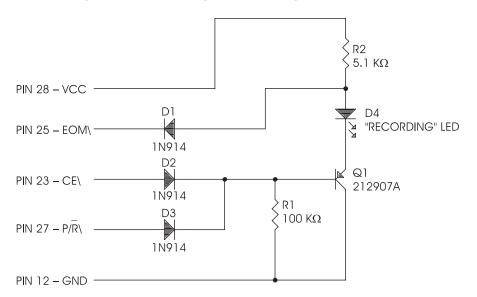


Figure 9: Recording Indicator Light for ISD1000A

NOTE: This circuit will turn on the LED only when actually recording. It requires a valid record selection (P/R LOW), and CE LOW to turn on. At the end of the time in the chip, EOM goes LOW and turns off the LED.

CIRCUIT EXPLANATION

This circuit uses a PNP transistor to cause an LED to light only during a record operation and only when the ISD1000A device is not in overflow. The logic is very simple: when $\overline{\text{CE}}$ is LOW and P/ $\overline{\text{R}}$ is LOW the PNP transistor conducts unless $\overline{\text{EOM}}$ is LOW.

C6 VCC **ISD1000A FAMILY DEVICE** $4.7 \mu F$ C8 LS1 **U2** 5 $220~\mu F$ **SPEAKER** R10 SPEAKER OUTPUT PINS $10~\text{K}\Omega$ POT LM386 $0.05 \mu F$ Expander ON Expander OFF R11 10Ω VCC R2 20 KΩ ≷R1 \$20 KΩ R4 $0.1~\mu F$ $10~{\rm K}\Omega$ +VIN1 -VIN1 VCC +VIN2 R7 19 200Ω VOUT1 -VIN2 18 RECIN1 CREC1 SUMOUT COMIN1 VREF C4 RECIN2 R6 R5. CREC2 SUMOUT2 COMIN2 SUMNO2 < 100 KΩ $10 \, \mu$ F 21 KΩ< 14 POT 4 C1 C2 GCIN1 GRND 10 μF 10 2.2 GCIN2 (R3 ±μF **NE575** <10 KΩ С3 $220 \mu F$

Figure 10: Expander Circuit for Low Noise Playback

NOTE: $V_{CC} = 5$ volts plus or minus 10 percent.

EXPANDER CIRCUIT FOR IMPROVED NOISE PERFORMANCE

The circuit in Figure 10 was developed to provide an enhanced signal to noise ratio in applications where the output of the ISD device would be amplified considerably. A public address system or warning device in a high noise environment could benefit from the lower "effective noise" provided by this circuit.

The Expander circuit was assembled to illustrate the difference between the direct SNR and the SNR through the NE575 device. Although the ISD device will drive the 16 Ω speaker directly, the NE575 cannot. It is designed for 600 Ω applications so the LM386 audio amplifier had to be added to drive the speaker.

The circuit is adjusted so that the peak audio level from the ISD device is the same direct to the LM386 or through the NE575 to the LM386. Then, when the NE575 is switched in, the noise floor is "pushed down" to an inaudible level.

The result is that a public address system will not have an audible "hiss" when playing a message.

The result can be dramatically demonstrated during playback by moving the switch between the two positions and listening carefully in the pauses between syllables.

The Phillips/Signetics NE575 is one of a group of compander circuits used in telecommunications. Normally one half of the chip compresses incoming audio by 2:1 to transmit over the communications channel. The other half takes the received audio and expands it back to its original dynamic range. It is this half that is used in Figure 10. The compressor is not used. The audio in the ISD1000A has already been "compressed" to a degree by the AGC of the microphone preamplifier. If the ANA IN pin were used for recording, then perhaps the compressor half of the NE575 would be used.

The NE575 is a 20-pin version but there are smaller, less expensive versions such as the NE576 or NE577. These are all fully described in the Phillips RF Data Book. The applications include cordless and cellular phones, wireless microphones, and consumer audio devices such as automotive CD players.