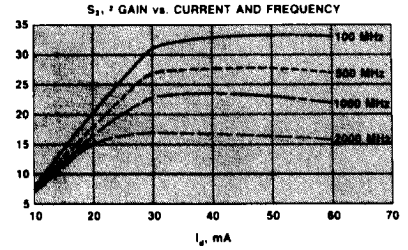
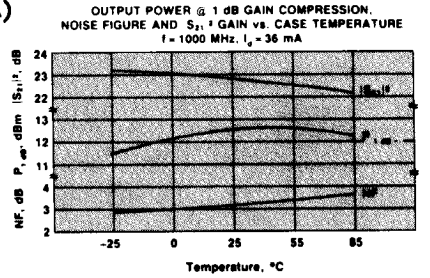
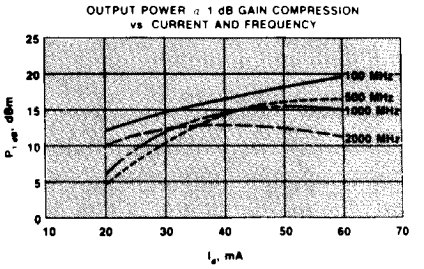
S-parameter data and performance curves

MAR-8 (T_A = 25°C, I_d = 36 mA)







Freq. MHz	S_{11} (Input Return Loss)			S_{21} (Power Gain)		S_{12} (Isolation Out-In)			S_{22} (Output Return Loss)			K
	dB	Mag	Ang	dB	Ang	dB	Mag	Ang	dB	Mag	Ang	
100	−15.92	0.61	−21	33.0	162	−40.00	0.01	38	−4.73	0.58	−24	0.79
500	−8.18	0.39	−77	27.8	109	−27.96	0.04	52	−9.37	0.34	−96	0.75
1000	−11.37	0.27	−113	23.0	80	−24.44	0.06	51	−13.56	0.21	−147	0.89
1500	−11.70	0.26	−139	19.4	62	−21.94	0.08	46	−14.89	0.18	174	0.96
2000	−10.46	0.30	−155	16.9	47	−20.00	0.10	41	−15.39	0.17	153	0.97
2500	−9.63	0.33	−180	14.8	32	−18.42	0.12	32	−14.42	0.19	127	1.01
3000	−8.87	0.36	167	12.9	20	−17.72	0.13	27	−17.08	0.14	111	1.07
3500	−7.54	0.42	153	11.4	6	−17.08	0.14	21	−17.72	0.13	107	1.06
4000	−6.94	0.45	141	9.8	−5	−16.48	0.15	14	−19.17	0.11	106	1.10

single and three-stage layouts

A typical MAR-layout is shown in Fig. 7 using 1/32″ PTFE woven-glass board—a reasonable compromise between cost durability, and electrical performance. Note that the transmission lines have no bends and are tapered near the package to minimize step discontinuities. Twelve plated through holes, including two under the emitter leads, provide solid ground planes and minimal emitter parasitics for best high frequency performance. The gaps in the transmission line are appropriate for 50 mil ceramic chip capacitors, which have relatively low associated parasitic inductances—typically about 0.5 nH. Mini-Circuits offers a wide variety of values, see Table 1A. The DC pad arrangement requires that a bias stabilization resistor be used, but makes the use of an RF choke optional. If the choke is not used, the stabilization resistor would be connected between the output 50-ohm line and the V_{CC} supply line, and the bypass capacitor would be attached between the V_{CC} line and ground. Spacing is appropriate for 1/4 watt carbon resistors, molded inductors, and 1 uF electrolytic capacitors. The layout has been designed so that Fig. 8 can be repeated for multiple cascaded stages. Overall circuit dimensions are 1″ × 1.5″ for a single stage, with each additional stage adding one inch to the overall length. A three-stage cascaded design using chip resistors and inductors (R and L in diagram) is shown in Fig. 8.

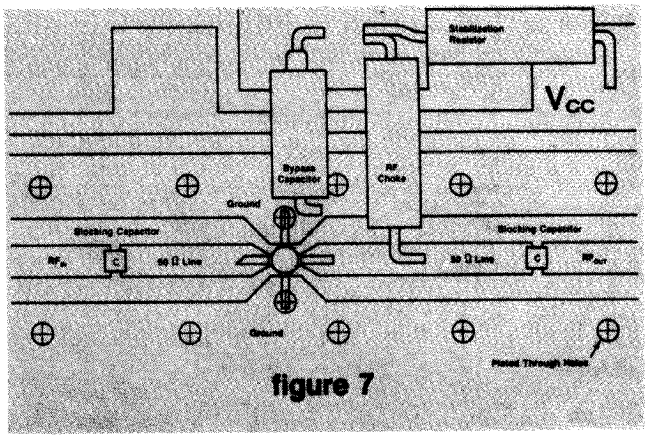


figure 7

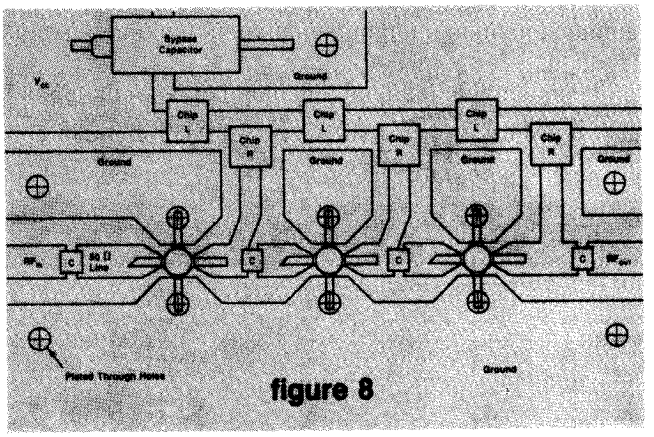


figure 8