APPLICATION OF MICROWAVE GaAs FETS

by

INTRODUCTION

The history of converting microwave communications, as well as other communications technologies, to solid state electronics is a long one. Early advances were first made in receivers, and then in transmitters. Progress in bipolar transistor technology and the production of new semiconductor crystals during the 1960's made possible the development of such new microwave diodes as the GUNN and the IMPATT (impact avalanche and transit time). For this reason, the decade might well be called the renaissance of microwave semiconductor devices. A series of microwave communications amplifiers appeared in the first half of the 1970's which used GUNN and IMPATT diodes. They played a leading role in the trend toward solid state technology. In the middle of the same decade, a commercially feasible gallium arsenide field effect transistor (GaAs FET) appeared, and the uses of this device are still increasing. In the latter half of the 1970's, demands grew for systems more reliable than those using IMPATT and GUNN diodes. Users were demanding greater reliability, and those engaged in research and development began working toward this goal. The work is still going on today.

The demands of the industry turned the emphasis away from creating new devices to developing competition among manufacturers of semiconductors to produce devices of higher performance and greater reliability. Commercialization of GaAs field effect transistors led to lower energy consumption and smaller microwave components and systems. These are still major concerns today. With new developments in information, communications and applied microwave systems, the GaAs FET has become an indispensable item.

I. THE FIELD EFFECT TRANSISTOR (FET)

In 1952, Shockley conceived the structure of the field effect type transistor and pointed out that it could be used for amplifier devices. Due to manufacturing difficulties, particularly in production technology, the field effect transistor was little known until the early 1960's. The level of technology at the time made it very difficult for people to understand the importance of the FET. But with the development of planar technology, the microwave semiconductor industry grew with explosive rapidity.

There are three major types of FETs. The simplest of the three is the junction FET (JFET). Because of its simplicity and ease of manufacture, the JFET was the earliest to be produced commercially. It was put on the market about the same time as the first microwave bipolar transistor.

With the development of semiconductor manufacturing technology and the need for lower energy consumption, the metal oxide semiconductor FET (MOSFET) appeared. The MOSFET, like the JFET, was first developed for applications in circuits that demanded high impedance, such as input circuits in analytical instruments. Field effect transistors, particularly the MOSFET, became widely known for their use as discrete devices in UHF band communications. However, having focused solely on performance for many years, nothing in the microwave band appeared on the market which was superior to the bipolar transistor.

Around the time silicon reached its peak as a transistor material, Schottky barrier type FETs made of gallium arsenide appeared and quickly gained popularity by demonstrating their high theoretical performance. This new device, known as the Gallium Arsenide Metal Semiconductor FET (GaAs MESFET) showed performance far superior to the bipolar transistor.

This new device provided lower noise and higher gain in established solid state applications. It also provided high frequency characteristics previously unavailable from bipolar transistors. It is made by using gallium arsenide (group III-V); one of the semiconductor compounds which has been researched continually since the latter half of the 1960's. The electron mobility of gallium arsenide is five to seven times that of silicon.

Gallium arsenide crystal technology was used to produce the GUNN, varactor and Schottky diodes, and proved to be far better than silicon in high frequency performance. A GUNN diode made of silicon would be inconceivable, so the appearance of the contemporary GaAs FET contributed greatly to developing and commercializing the GUNN diode. The reason for this is that even though the GaAs MESFET is a three terminal device, it is simple in structure and its performance depends only on the crystal quality. Advances in crystal technology have made the commercialization of FETs possible.

The GaAs FET is what is generally referred to as a "normally ON" type device. Its basic difference from the MOSFET is the use of a Schottky barrier at the gate instead of an oxide layer. This is an extremely important point. In other words, almost no GaAs FET gates are insulated from the channels in terms of direct current. Thus, even though GaAs FETs are called "normally ON" type devices, the maximum gate voltage must be zero. It does not use a dielectric like the MOSFET,

so if a positive voltage is applied at the gate, direct current flows through it. Since the gate is a very small piece of metal (0.5μ—1.0μ—2.0μ), the gate electrodes will fuse completely in almost all cases.

Figure 1 shows the properties of a GaAs MESFET. In almost all cases, a linear amplifier circuit biases the GaAs MESFET. This applies to other circuits as well, but considering gate bias alone, the range must be from I_{DSS}, i.e., $V_G = 0$ V, to $I_{DS} = 0$ (at pinch off, $V_G = V_P$). In this range, the voltage V_{DS} between the drain and the source has little effect on the current I_{DS} flowing through the channels. By changing the gate voltage, V_G, the drain to source (channel) current can be controlled. Figure 2 shows the transfer characteristics of a GaAs FET with n channels. This FET transfer characteristic is an important basic parameter in circuit design because it sets the bias conditions and operating point. The operating point line in Figure 2 is directly related to the mutual conductance, g_m.

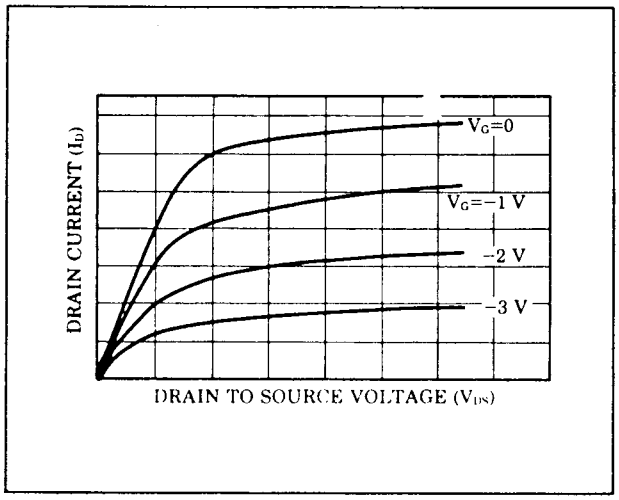


Figure 1. Typical GaAs FET DC Characteristics

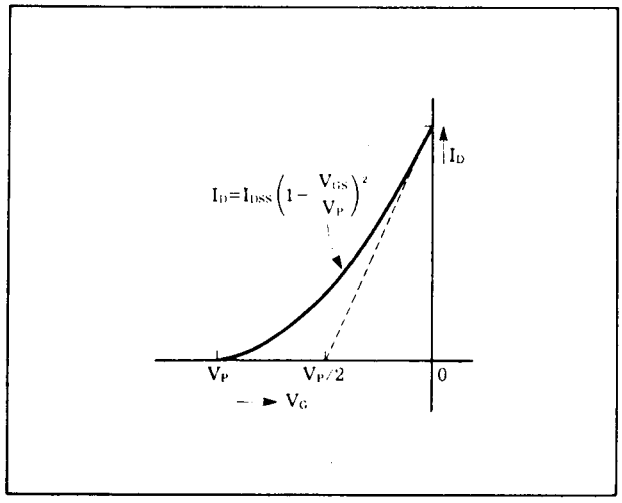


Figure 2. Square-Law Characteristic

Mutual conductance is defined as the ratio of the change in direct current to the minor change in voltage between gate sources. This is generally described as the square-law characteristic and is shown in the equation for I_D in Figure 2.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

When I_D in expression (1) is differentiated with respect to V_{GS}, the result is

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = g_m \qquad (2)$$

and the mutual conductance for each value of V_{GS} can be obtained.

II. GaAs FET BIAS AND OPERATING POINT

The most important characteristic to consider when designing a bias circuit for small signal GaAs FETs is the previously mentioned transfer characteristic. Generally, two methods can be used to bias a GaAs FET.

1. Dual Power Source Method

Figure 3 shows a bias circuit which uses the dual power source method. Since the condition

$$V_P < V_{GS} < 0$$

must always apply to a GaAs FET, V_{GS} can be derived from expression (1)

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad (3)$$

2. Self Bias Method (Auto-Bias)

Figure 4 shows the most universal method for reducing electrical potential between a gate and the source when there is only one power source. If the source resistance is R_S, and the operating current is I_D, then the drop in electric potential caused by R_S will be

$$I_D \times R_S$$

The actual electrical potential between the gate and the source will be

$$V_{GS} = -I_D \cdot R_S \qquad (4)$$

which is negative, so the FET can be turned on. The value R_S is obtained by combining expressions (3) and (4).

$$R_S = -\frac{V_{GS}}{I_D} = -\frac{V_P}{I_D}\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \quad (5)$$

Therefore, these are the basic bias principles.

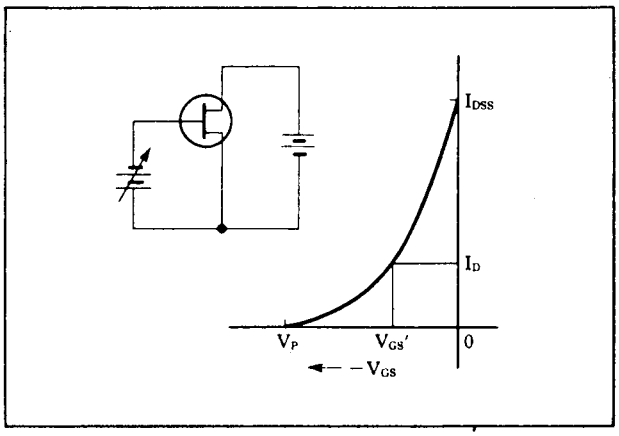


Figure 3. Dual Source Bias Method

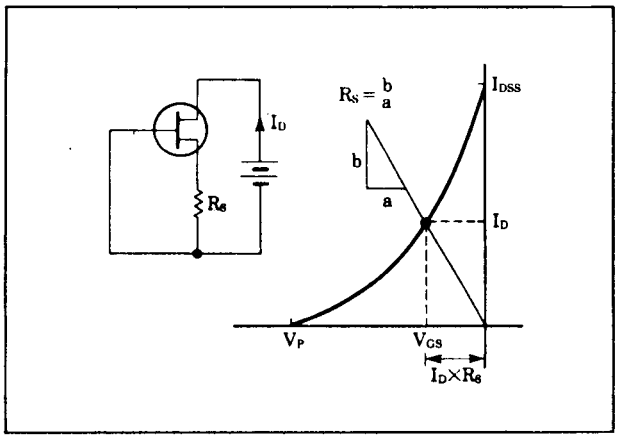


Figure 4. Self (Auto) Bias Method

Figure 5 shows the five general bias types: A, B, C, D, and E. Type A is the previously described dual power source bias method appropriate for use in the higher frequencies. When directly connecting the source to the ground terminal, source inductance can be made relatively small. By using this method, higher gain can be obtained and a lower noise factor anticipated in the higher frequencies.

All other bias methods insert a bypass capacitor into the source. Even if the high frequency performance of the bypass capacitors can be guaranteed, there will always be a loss (tan δ) resulting from the material's dielectric properties. Even with chip capacitors, there is always some inductance and care must be exercised when using them at higher frequencies. Types D and E in Figure 5 require only one power source. They are compatible with the previously described method. An advantage of this method is that if the source voltage should increase for any reason, that increase will be proportionate to the drop in potential caused by R_S, which is connected in series with the source,

$$R_S \times \Delta I_D$$

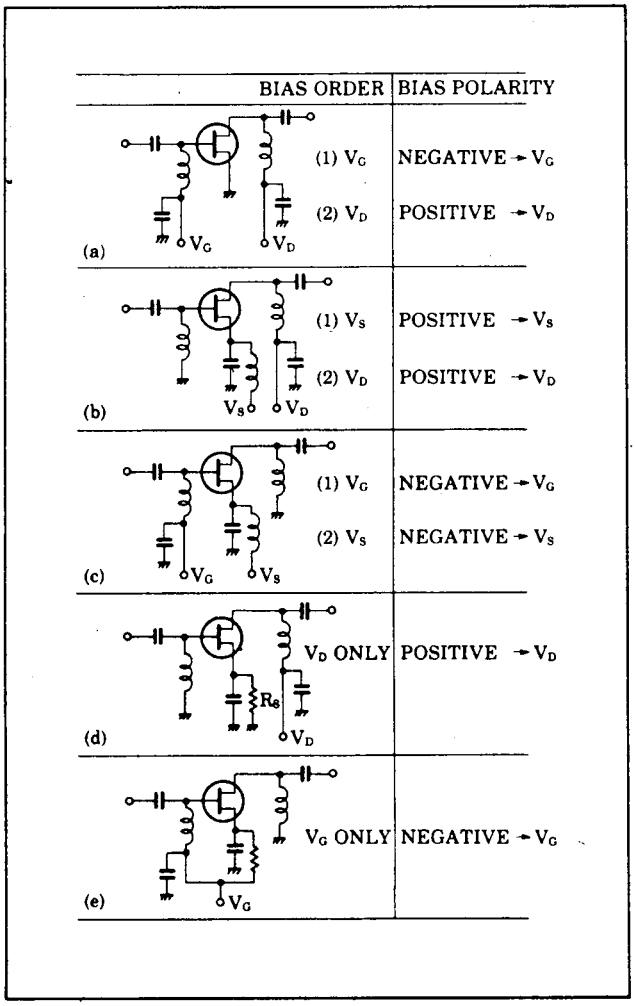


Figure 5. GaAs FET Bias Circuits

Here, ΔI_D is the increment in drain current caused by the increment in source voltage.

Drain current increase will be automatically suppressed, due to the proportionate negative bias on the gate. Generally, if a single source type (self-biasing type) is selected, D is used; if the only available source is a negative one, then E should be selected.

Figure 5 shows the order for adding bias when a dual power source is used. This is to prevent, as

much as possible, a large current from flowing through the FET. The GaAs FET being discussed here generally has a high mutual conductance, giving it excellent frequency characteristics. If the gate voltage is near zero, g_m is at a maximum and oscillation may occur. For this reason, a bias scheme should be adopted that first applies a negative bias to the gate and then turns on the drain with a positive bias. There are slight differences between a bias circuit for a small signal GaAs FET and one for a power GaAs FET, but the above methods can be considered for both.

Moving one step further, let's examine a practical bias circuit. It is important to:

1. Obtain the necessary operating voltage and operating current, and
2. Ensure a high level of stability.

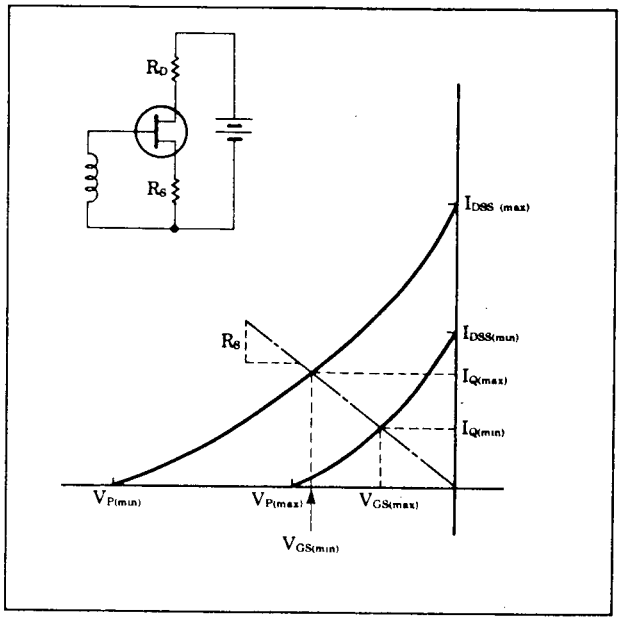


Figure 6. Possible Bias Points

Figure 6 shows the bias graph, indicating all possible bias points. Bias will be in the range determined by

$$V_{GSQ} = I_Q R_S$$

Given the bias range, the operating point for the maximum amplitude value, P, and the operating point where there is no signal, Q can be obtained. The change in I_Q from point P to point Q, or ΔI_Q, becomes

$$\Delta I_Q = I_{Q(max)} - I_{Q(min)}$$

This shows that with a variation in I_Q, the drain voltage will change only as $R_D \cdot \Delta I_Q$. If the signal midpoint is not fixed at the center of the bias line and wanders off in some direction, the wave form will be distorted. Also, the amplification operation will be degraded, and DC will flow through the gate. In a similar manner, the maximum variation in voltage between the gate and the source when there is no signal is

$$\Delta V_{GSQ} = V_{GSQ(max)} - V_{GSQ(min)}$$

I_Q is a function of both the temperature, T, and V_{GSQ}

$$I_Q = f(T, V_{GSQ})$$

If, with a variation in temperature of δT, I_Q changes by only δT_Q.

$$\delta I_Q = \frac{\partial I_Q}{\partial T} \cdot \delta T + \frac{\partial I_Q}{\partial V_{GSQ}} \cdot \delta V_{GSQ}$$

$$= \frac{\partial I_Q}{\partial T} \cdot \delta T - g_m \delta I_Q \cdot R_S$$

and from this

$$\delta I_Q (1 + g_m R_S) = \frac{\partial I_Q}{\partial T} \cdot \delta T$$

is obtained.

If $R_S = 0$, that is, if there is no series resistance, then

$$\frac{\partial I_Q}{\partial T} \cdot \delta T = \delta I_Q(0)$$

represents the drift. The bias stability coefficient is defined as

$$S = \frac{\text{Fluctuation in } I_Q \text{ with respect to } R_S}{\text{Fluctuation in } I_Q \text{ independent of } R_S}$$

$$= \frac{\delta I_Q}{\delta I_Q(0)} = \frac{1}{1 + g_m R_S} \qquad (6)$$

This means that fluctuation in the entire circuit is reduced by means of negative feedback due to R_S. This effect is particularly important when using small signal FETs.

Figure 7 gives an example of a bias circuit. Since I_{DSS} and V_P often vary between devices, it is important that the bias circuit can absorb such variation, the optimum operating point can always be established, and operation is stable regardless of ambient temperatures. The circuit in Figure 7 is basically a fixed bias circuit and not a

self-bias circuit. Feedback is applied to the circuit by the insertion of R_S into the source.

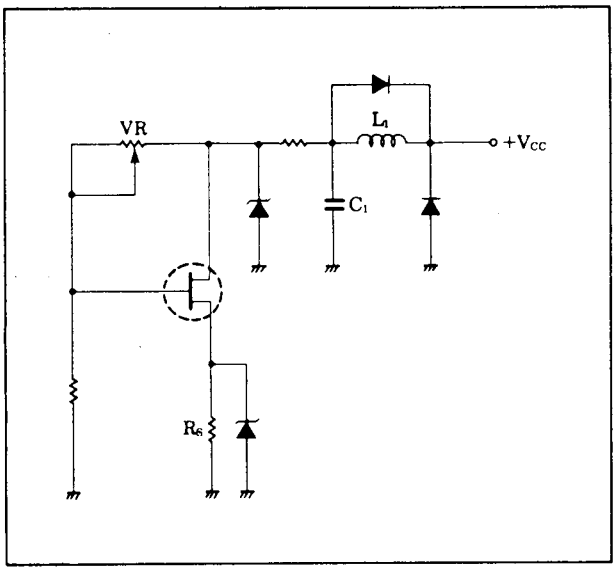


Figure 7. A Low Cost, Stable Bias Circuit

As stated previously, since the voltage between the gate and the source is $V_{GS} = -I_D R_S$ in a self-bias circuit, and if I_D is known, R_S can be readily determined. In such a fixed bias circuit as the previously mentioned dual source type, the gate voltage is selected independently of R_S and I_D. Thus, it is understood that the value R_S can be higher than that when using a self-bias circuit, and the stability coefficient S can therefore be improved.

III. GaAs FET CHARACTERISTICS AND APPLICATIONS

In this section, examples and explanations of GaAs FET applications will be given. The first issue is the argument as to whether or not the FET is better than the bipolar transistor because of the FET's cross modulation characteristic. Discussion will then turn to applications of the small signal FET and the large signal or power FET.

1. Distortion Factor

The transfer characteristic of a GaAs FET can be approximated using a quadratic equation, as was shown in expression (1). If the transfer characteristic could be perfectly represented by such an equation, then the second harmonic will increase to its maximum and will actually include the higher order harmonic components. To determine the value of the second harmonic for a basic frequency, substitute the total input voltage and total output current into the equation.

If there is no signal, the drain current I_D is

$$i_D = I_{DSS}\left(1 - \frac{v_{gs}}{V_P}\right)^2 \qquad (7)$$

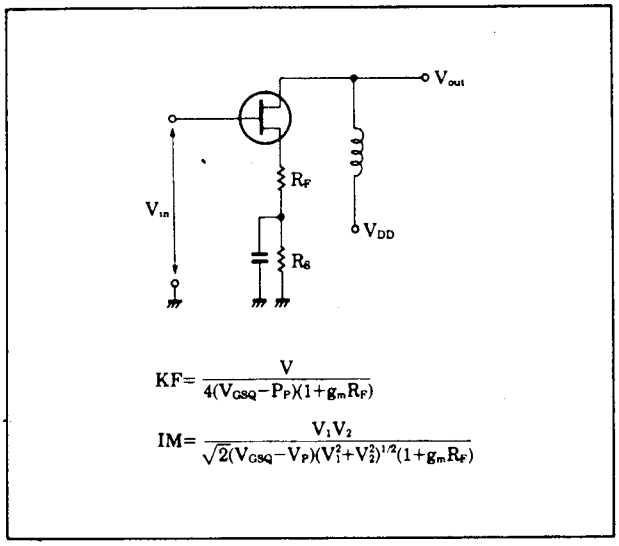


Figure 8. Improving the Distortion Factor Using a Series Feedback Resistance R_F

Adding a simple sine wave voltage $(V \sin \omega t)$ to the non-signal voltage results in

$$v_{gs} = V_{GSQ} + V \sin \omega t$$

If the expression is rearranged and substituted into the following, then the harmonic distortion KF is

$$KF = \frac{\textit{Relative value of second harmonic}}{\textit{Relative value of fundamental harmonic}}$$

$$= \frac{V}{4(V_{GS} - V_P)} \qquad (8)$$

V is the maximum amplitude of the signal.

As expression (8) shows, the distortion factor approaches its minimum as V_{GSQ} approaches zero. However, as the input signal increases and enters the realm of forward gate bias, quite naturally the distortion factor increases.

Next, we will consider what happens to the cross modulation (intermodulation) produced when two sine wave signals are amplified at the same time. That is

$$V_{GS} = V_{GSQ} + V_1 \sin \omega t + V_2 \sin \omega t$$

Since the output current includes the sum and difference components of two sine waves, cross

modulation (intermodulation) distortion, *IM*, is defined as follows:

$$IM = \frac{\text{Relative value of}}{\text{Relative value of}}$$

$$\frac{\text{cross modulation component}}{\text{fundamental harmonic}}$$

$$= \frac{V_1 V_2}{\sqrt{2}(V_{GSQ} - V_P)(V_1^2 + V_2^2)^{1/2}} \quad (9)$$

Even here, we see that the distortion factor decreases as bias is brought closer to $V_{GSQ} = 0$. The main cause of the distortion is the curve (non-linearity) in the transfer characteristic line, but there are other causes as well.

Distortion can also be caused by the change in output conductance, g_d, related to the operating point and the drain voltage, V_{DS}. To improve distortion, carefully select g_m and g_d, which to a certain degree work to reverse this effect.

Another point to consider is that since distortion can be produced internally, *KF* and *IM* can both be improved by applying feedback to the circuit.

As shown in Figure 8, by adding a resistance, R_F, in series with the source resistance, the distortion factor for the non-bypass feedback is calculated, using expressions (10) and (11).

$$KF = \frac{V}{4(V_{GSQ} - V_P)(1 + g_m R_F)} \quad (10)$$

$$IM = \frac{V_1 V_2}{\sqrt{2}(V_{GSQ} - V_P)(V_1^2 + V_2^2)^{1/2}(1 + g_m R_F)} \quad (11)$$

By applying feedback to the circuit, both the distortion factor and the bandwidth can be improved. The value of R_F will reduce the total gain only by its relative portion. It is possible to have a wide-band amplifier with a low distortion factor by initially designing the amplifier for high gain and tuning the gain to its optimum level by using feedback.

2. Small Signal FET Applications

The first practical and commercially available GaAs FET was introduced around 1973. Since then, many small signal amplifying devices with 1 μm gate lengths and smaller have been marketed.

The greatest advantages for these devices are found in the higher frequency bands. Compared to the silicon bipolar transistors and tunnel diodes, GaAs FETs are far better in terms of noise, gain and output-power saturation characteristics. Other than their primary use in ultra-high frequency amplifiers, such as those for electronic countermeasures (ECM), most small signal FET applications are in low-noise amplifiers. They are used in both line-of-sight and over-the-horizon microwave communications, and in earth stations communicating with satellites.

A low noise amplifier is designed by minimizing the noise measure, *M*, shown in expression (12).

$$M + 1 = 1 + \frac{NF - 1}{1 - (1/G)} \quad (12)$$

NF is the amplifier noise factor.

G is the amplifier gain.

In single-stage amplifiers, the general procedure for matching input circuits is to mimimize the noise factor, NF; for matching output circuits, the gain is maximized.

From observations of the input-output impedances of a GaAs FET, it is noted that there is generally a difference in impedance between maximum gain and minimum NF. This difference is particularly apparent at lower frequencies. As the frequencies go higher, the difference seems to decrease. The noise factor, which is a function of device gain, will be low when the gain is maximized at high frequencies. However, of the commercially available GaAs FETs having characteristics which allow a gain of 8 to 10 dB or more, there is still a difference between the impedance at maximum gain and the impedance at miminum NF. This difference will be seen until the frequency range approaches the X band.

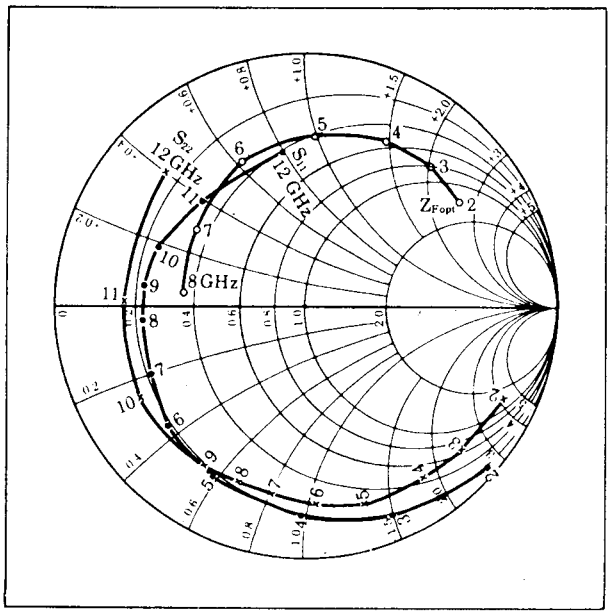


Figure 9. Frequency Characteristics of S_{11}, S_{22}, and Z_{Fopt} in the NE24406

Figure 9 shows S_{11} and S_{22}, indicating input-output impedance for the NE24406 and the signal source impedance when the noise factor, NF, is minimized. Circuits can be matched using these impedances. As mentioned previously, input circuit matching is accomplished by matching to Z_{Fopt}; and output circuit matching is accomplished by matching to S_{22}.

In the design of a multi-stage amplifier, the first and second stages are designed so that $(M + 1)$ will be minimized, and the third and subsequent stages are made in such a way that their gain is maximized. Or, alternately, the amplifier can be designed according to the characteristics determined by the frequency and the device.

One impedance matching circuit, shown in Figure 10(a), is the well known Tchebycheff filter type multi-stage impedance matching circuit. The distinctive feature of this circuit lies in its applicability to the input/output circuits of wide-band amplifiers. In many cases, the circuit is used in amplifiers covering the band range 8 GHz to 12 GHz and above. Although this type of matching network was originally applied to comparatively narrow bands (such as a 500 MHz bandwidth at 4 GHz), the matching circuits shown in Figure 10(b) and (c) are now believed to be best suited for bands having approximately a 10 to 15 percent ratio to the amplifier's center frequency.

For these bandwidths, the NF can be reduced to its lowest absolute value. If the widest possible bandwidth is the objective, then reduction of the NF to its absolute minimum is not possible throughout the band. In the former amplifier, the most important consideration is reducing, as much as possible, the loss in the impedance matching circuit. The Tchebycheff filter type impedance matching circuit in Figure 10(a) uses a large number of components and is not well suited for obtaining a low loss matching network.

As Figure 9 shows, both S_{11} and S_{22} go from capacitive to inductive with increasing frequencies. Consequently, S_{11} and S_{22} can use the circuit in Figure 10(b) for frequencies which exhibit a capacitive response, or the circuit of Figure 10(c) for the frequencies which exhibit an inductive response. In Figure 10(b), for frequencies slightly higher than the amplifier's center frequency, the GaAs FET input or output has a resonance of either L_1 or L_2 (with a reactance of 0), which is then matched to the desired impedance by the $\lambda/4$ impedance conversion circuit. This is only one of the countless possible impedance matching circuits. However, this is a very effective design method for low noise amplifiers requiring a band ratio of 10 to 15 percent when the amplifier's center frequency is 4 GHz or greater.

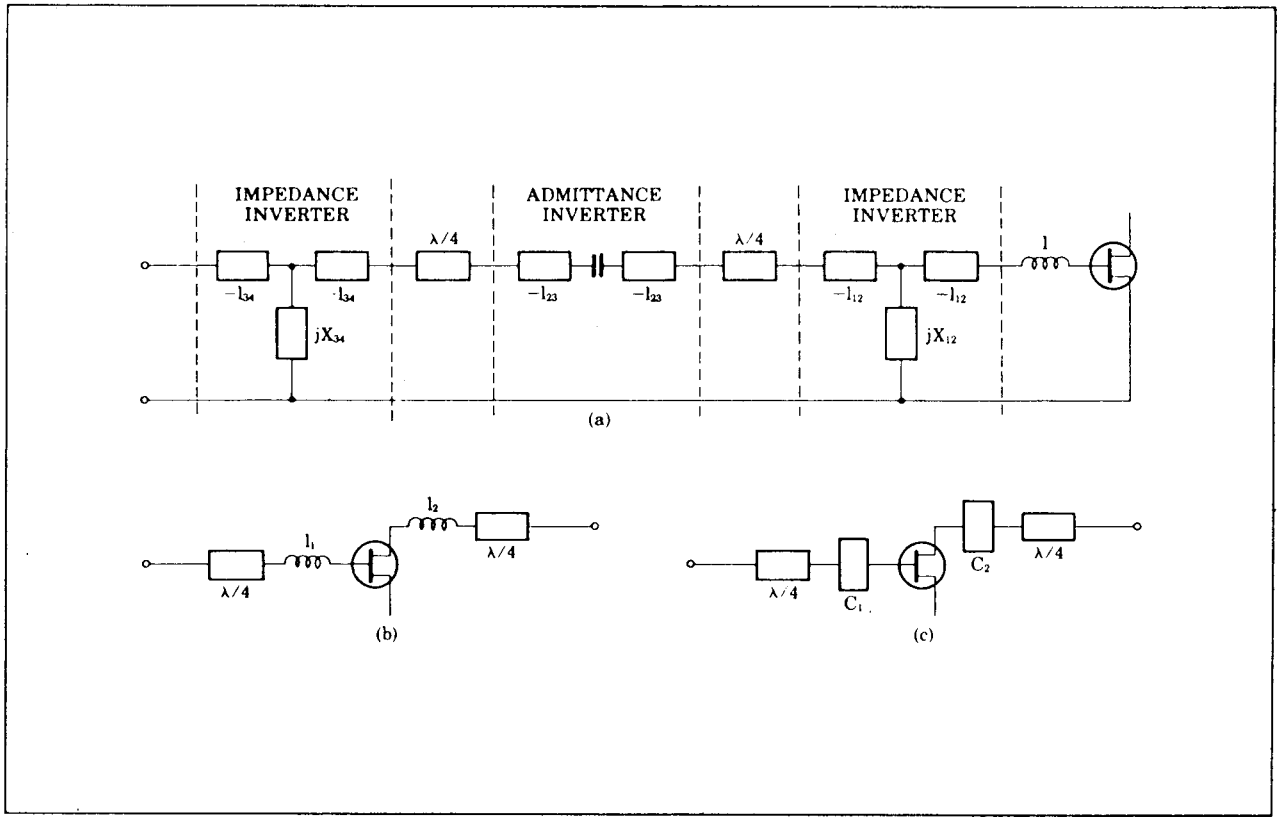
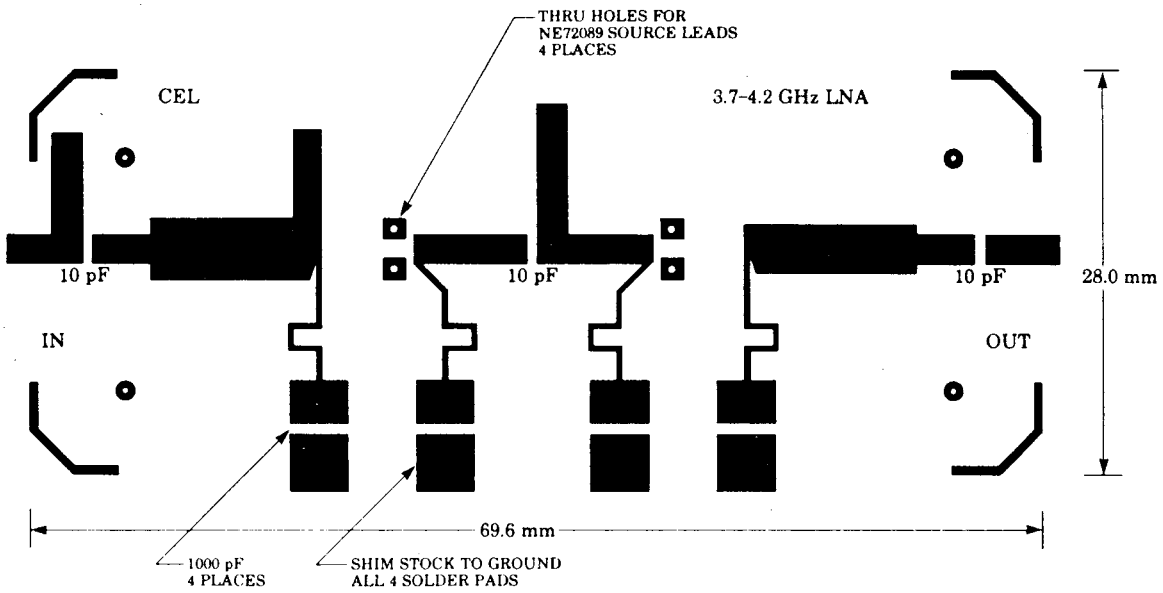


Figure 10. GaAs FET Matching Networks

3. Low Noise Amplifiers in the 4 GHz Band

Figure 11 is an example of a two-stage low-noise amplifier for the 3.7 to 4.2 GHz band using either the NE21889 or the NE72089. The matching circuit in Figure 11 is based on the same idea as Figure 10(b). It uses a microstrip with an 0.8 mm thickness teflon glass fiber substrate and transistor leads with lumped constant inductance. Figure 12 shows the schematics. Figure 13 shows the gain and noise factor normally obtained using this circuit.



Parts List: NE72089 FET (2 ea.) California Eastern Laboratories
10 pF Chip Capacitors (3 ea.) ATC #100A-100-J-P-X-50 or equivalent
1000 pF Chip Capacitors (4 ea.) Johanson #50R11W102KP or equivalent
1500 pF Feed-through Capacitors (4 ea.) Erie #2425-003-W5U0152AA or equivalent
Ferrite Beads (4 ea.) Fairrite #2643001301 or equivalent

Figure 11. PCB Layout of a 2-Stage Amplifier in the 3.7 GHz–4.2 GHz Band (actual size)

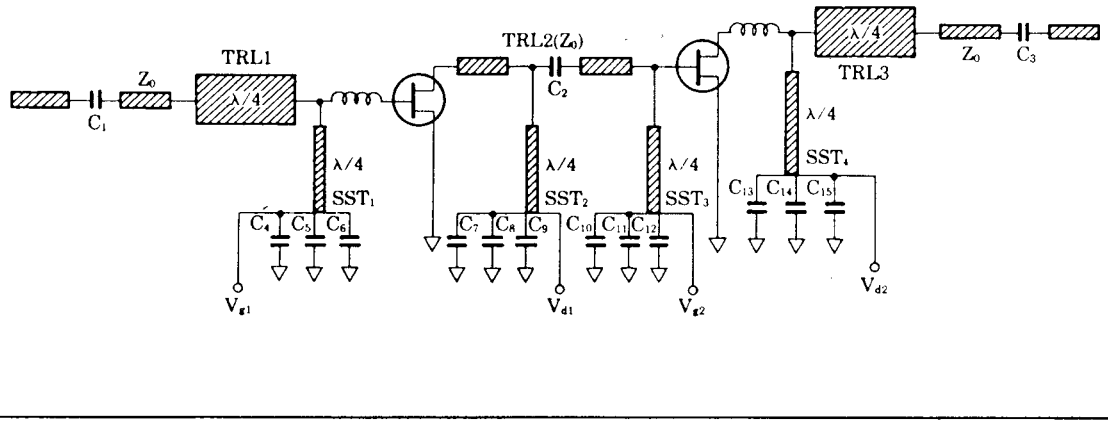


Figure 12. Schematics for a 3.7 GHz–4.2 GHz Band 2-Stage Amplifier

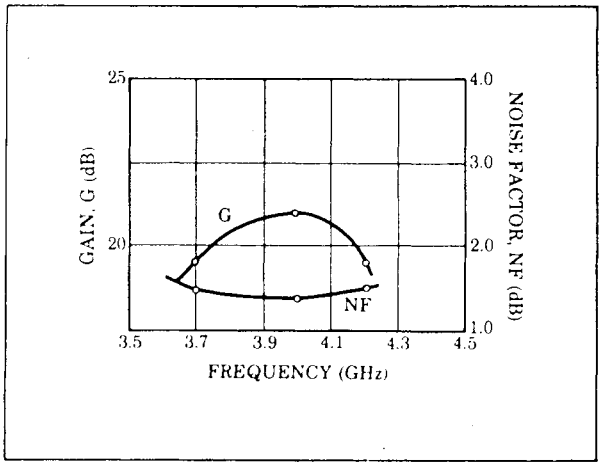


Figure 13. Frequency Characteristic of NF and G for the NE72089 2-Stage Amplifier

This two-stage amplifier uses the inductance in the first stage input section to produce resonance. Then, using the $\lambda/4$ impedance transformer, it forms a matching circuit for the 50Ω characteristic impedance. Since there is a relatively small difference in values between S_{11} and S_{22}, the intermediate stage matches impedance by the simple means of a transmission line.

Output matching is done in the same way as in the first step, i.e., the matching circuit shown in Figure 10(b) is used. Figure 11 is a full-scale pattern showing lines and open stubs inserted in parallel. Although these are not necessary for the ideal design, they are included to correct impedance matching problems caused by the printed circuit board connectors (microstrip to coaxial connection) and the DC blocking chip capacitors. They are inserted after the design is completed.

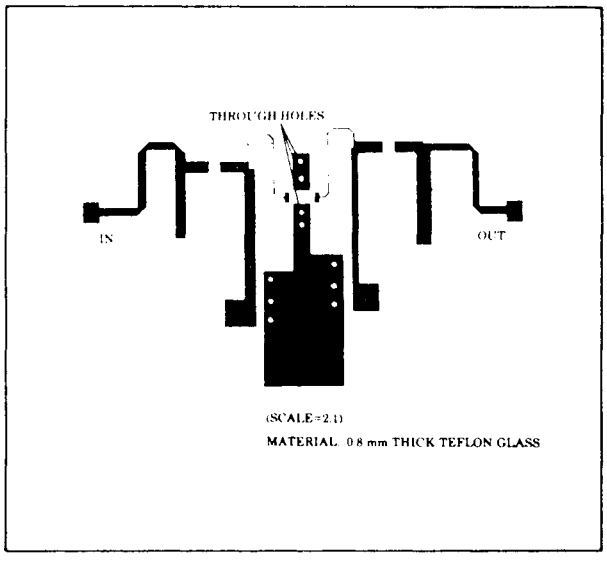


Figure 14. PCB Layout for 1.0–1.4 GHz Amplifier

4. Low Noise Amplifiers in the 1 GHz Band

Figure 14 shows a PCB layout for an amplifier designed for low noise operation in the 1 to 1.4 GHz band. Since the microstrip lines used are very thin, the diagram shown here is twice the actual size. During the design, it should be drawn four times the actual size and then reduced.

Figure 15 shows the equivalent circuit. In the design of this circuit, a band ratio of 10 to 15 percent was not obtained as with the previous amplifier. Instead, emphasis has shifted to making the band as wide as possible and the noise factor as low as possible. Since it is in the relatively low-frequency 1 GHz band, the loss due to the reactance elements (including the microstrip) was not given much concern. The Tchebycheff filter type multi-stage impedance matching circuit would have been used. However, considering the frequencies involved and the large physical size of such a circuit, a method was chosen that gives the transmission line as high an impedance as possible for input and output, and which would gradually match to the characteristics impedance of 50Ω. Figure 16 shows the typical performance characteristics of this amplifer.

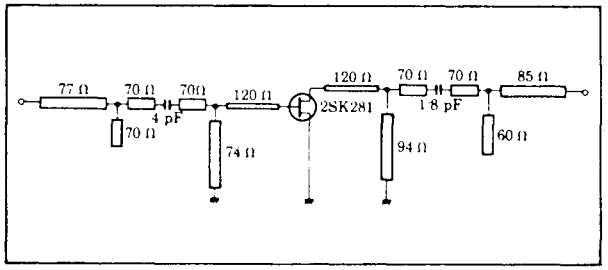


Figure 15. Equivalent Circuit for a NE72089 Low-Noise Amplifier

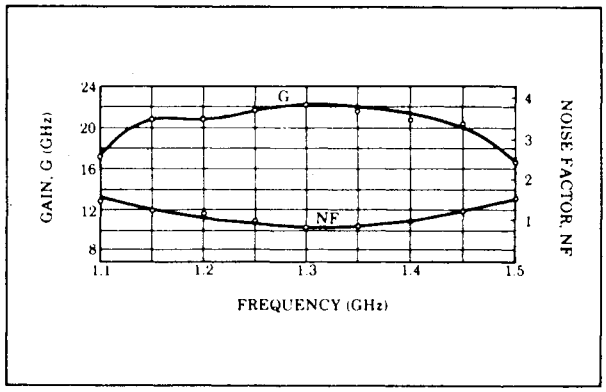


Figure 16. NE72089 Low-Noise Amplifier

When this amplifier was designed, a 4 pF blocking chip capacitor was used as part of the matching circuit, as shown in Figure 15. The input

matching circuit was designed chiefly to obtain matching for the noise factor. The data used for the NE72089 is shown below:

f	Γ_{Fopt}*	F_{min}	G	NF @ 50 Ω
1 GHz	0.59<32.5	0.6 dB	17.5 dB	1.73 dB
1.3 GHz	0.65<47.0	0.6 dB	15.0 dB	1.74 dB

V_{DS} = 3 V, I_{DS} = 10 mA

*(Γ_{Fopt} signifies the reflection coefficient obtained when comparing the signal course impedance with 50Ω when NF is minimized.)

The bias circuit used to actuate this amplifier is shown in Figure 17. The figure shows a bias circuit for a two-stage amplifier. For a single stage amplifier, only one half of the redundant portion of the circuit would be used. This circuit is a constant voltage, constant current type bias circuit, one of the most applicable examples of circuits for use in small-signal amplifiers.

5. Applications to Other Amplifiers

(A) A technique of attaining wide band performance by inserting a source inductance.

L. Neven, et al., have proposed a type of feedback circuit for relatively low frequency GaAs FET amplifiers. For amplifiers operating in the 1 GHz to 2 GHz range, these circuits guarantee a low noise factor as well as good input-output impedance.

Figure 18 shows what is considered the universal GaAs FET equivalent circuit. In this circuit, drain noise current, I_{dn}, is referred to the input by the Vander-Ziel theory, then the gate source resistances, R_i, becomes noiseless and, R_S remains noisy. The noise currents at the gate and drain have been removed from the two-port. The circuit in Figure 18 is better handled by computers, where the noise and signal are compared as a function of the externally added source inductance. In this instance, it is easier to consider the equivalent circuit shown in Figure 19.

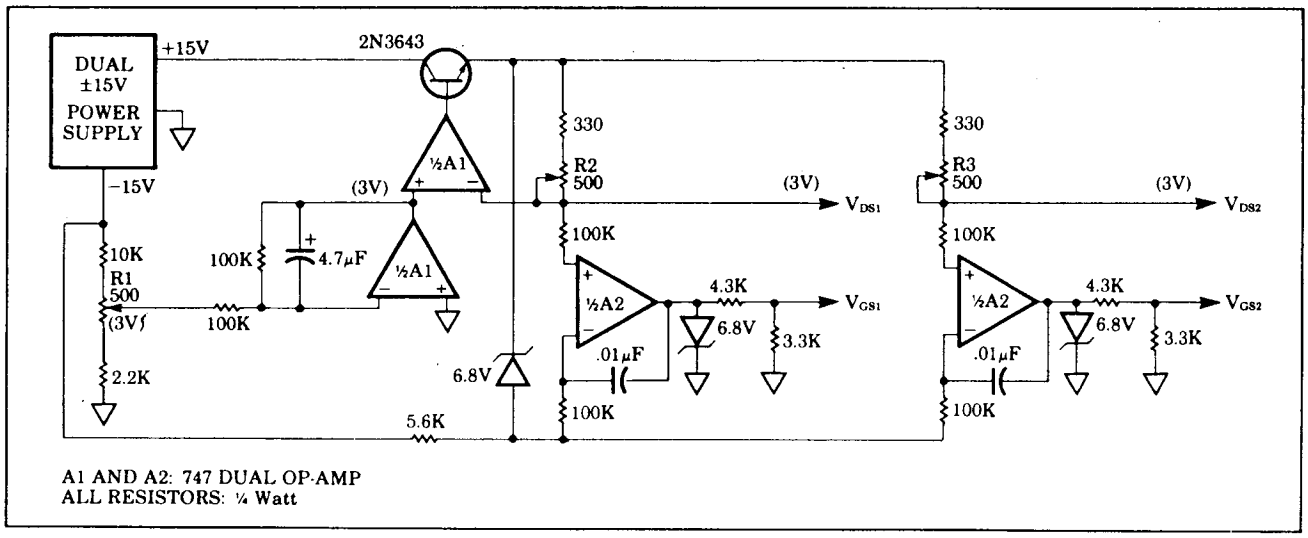


Figure 17. Two Stage GaAs FET LNA Bias Supply

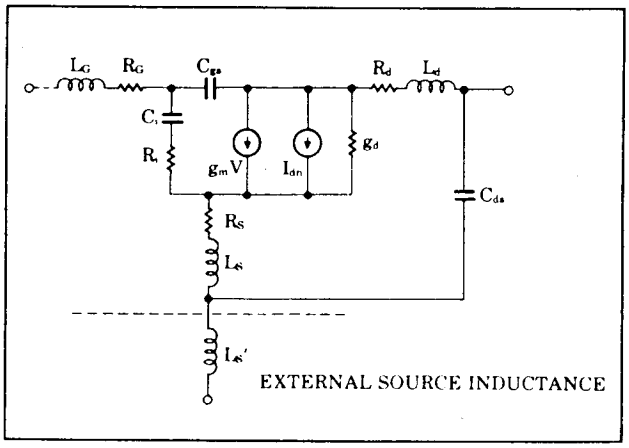


Figure 18. Universal GaAs FET Equivalent Circuit

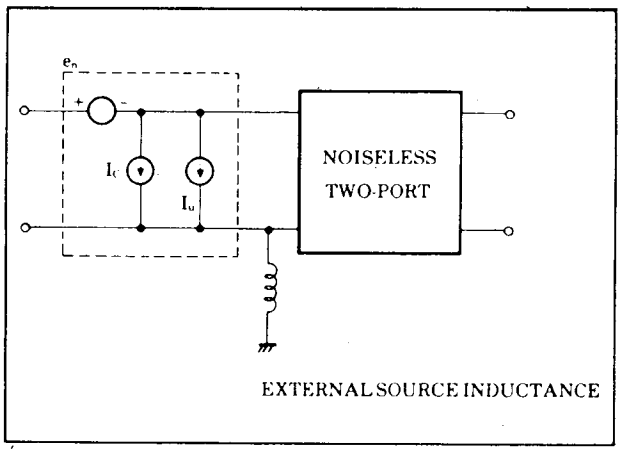


Figure 19. Cascade Connection of Device's Noise and S-Parameter Equivalent Circuits

To be continued in DUBUS Info 3/83