ChipCorder Application Information

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Application Information Section	ISD1000A Series	ISD1100 Series	ISD1200 Series	ISD1400 Series	ISD1500 Series	ISD2500 Series	ISD33000 Series	ISD4002 Series	ISD4003 Series
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Example Circuit: Microphone Circuit							■	■	■
Example Circuit: Single Transistor 3-Volt Speaker Driver							■	■	■
Using the ISD33000 Series with 5-Volt Powered Processors							■	■	■
Operations, Tricks, and Techniques in the ISD33000 Series							■	■	■
Using the ISD33000 Device with a Microcontroller							■	■	■
Using the ISD33000 Device with a Low-Cost Motorola Microcontroller							■	■	■
Message Management in the ISD33000 Series							■	■	■
A "C" Language Source Code Example to Use with the ISD33000 Series							■	■	■
AGC Circuit for the ISD33000 Series							■	■	■

APPLICATION INFORMATION FOR ALL ChipCorder PRODUCTS

Introduction

THE TECHNOLOGY AND THE PRODUCTS

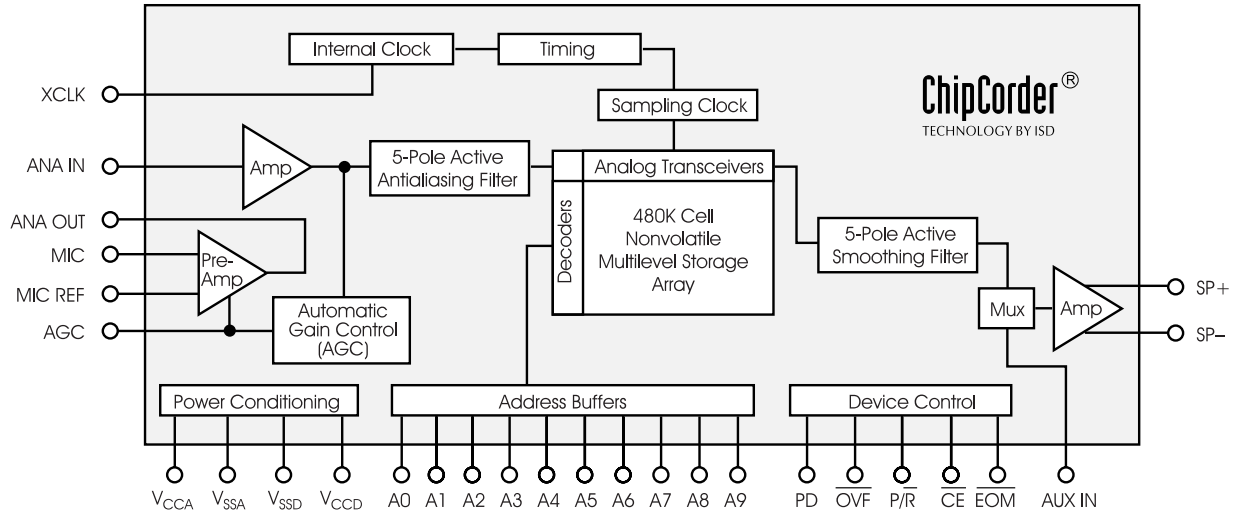
The ISD patented ChipCorder technology brings analog data into the semiconductor memory world. This "break through" EEPROM storage method allows analog data to be written directly into a single cell without A/D or D/A conversion. This results in:

- Increased density over equivalent digital methods
- Nonvolatile storage of analog data

Numerous schematics in the following sections show single-chip voice message systems. A block diagram of one family of ISD devices is shown in Figure 1. In this device, the external components (a microphone, loudspeaker, switches, a few resistors and capacitors, and a power source) are all that is required to build a complete voice record and playback system. All other functions (preamplifier, filters, AGC, power amplifier, control logic, and analog storage) are performed on-chip. This device, the ISD2500 and other products such as the ISD1100, ISD1200 and ISD1400 families emphasize simple push-button or parallel addressed microcontroller operation from a single 5-volt supply.

A new series of devices, starting with the ISD33000 family, emphasizes 3 volt operation and serial port control and may be tailored for specific markets. The ISD33000, for instance, does not have the on-chip microphone amplifier and speaker driver, allowing for a more cost-effective solution for those applications that already have those functions included elsewhere in the circuit.

Figure 1: ISD2560/75/90/120 Basic Block Diagram



OPERATIONAL OVERVIEW

During recording, the ISD device performs several stages of signal conditioning before the actual storage operation takes place.

For example, in those products with an included on-chip AGC, the first stages are composed of a preamplifier, amplifier and AGC blocks.

The preamplifier is connected to the microphone by a DC blocking capacitor that removes the DC component from the low level (2 to 20 mV) AC signal. Amplification is performed in two stages; initially by the input preamplifier and then by the fixed gain amplifier. The signal path is completed by connecting a capacitor between the ANA OUT and ANA IN pins.

Such an architecture allows system design flexibility, particularly for non-voice applications and also provides an additional pole for low frequency cutoff. The AGC circuit dynamically monitors the signal level at the amplifier output and sends a gain control voltage to the preamplifier. The preamplifier gain is automatically adjusted to maintain an optimum signal level into the filter. This gives the highest level of recorded signal while reducing clipping to a minimum.

The characteristic of the AGC circuit is described by two time constants; the attack time and the release time.

- Attack time is the time required by the AGC to reduce gain in response to an increasing input signal.
- Release time is the time constant of the gain increase in the presence of a decreasing signal.

The user can adjust both the attack and the release time by selecting values of the resistor and capacitor connected to the AGC pin. Certain default values will give optimum performance for normal speech; however, the accessibility of the resistance and the capacitance allows the user to tailor the AGC to his own particular needs. The 20 dB or so gain compression range on the preamplifier compensates for various microphone characteristics and also various levels of speech volume. The signal integrity is maintained. There is minimum clipping or other forms of distortion yet the dynamic signal range is increased by 20 dB.

All ISD devices next include a stage of signal conditioning performed by an input filter. As we will see later, the storage, although analog in nature, still employs sampling techniques. As a result the device requires an antialiasing filter to remove (or at least reduce to an insignificant level) input frequency components above half the sampling frequency. This is to satisfy the well-known Nyquist Criterion that applies to all sampled data systems.

Voice quality better than "telephone quality" (telephones cut off below 300 Hz) is achieved with a sampling frequency of 8 KHz. The high frequency cutoff of the low pass filter is then chosen to be 3.4 KHz, satisfying the Nyquist criterion, but still with a wide enough frequency band to allow for good quality voice reproduction. The filter is a continuous time, 5-pole low-pass filter with a roll-off of 40 dB per octave at 3.4 KHz.

Signal conditioning is now completed. The input waveform is then passed into the analog transceivers to be written into the Analog Storage Array. Samples are taken by the 8-KHz sample clock. These samples undergo a level shifting process to produce the high voltages required for the nonvolatile writing procedure, at the same time compensating for some of the practicalities related to Fowler-Nordheim tunneling. The sample clock is also used to increment the array decode so that the input samples are mapped sequentially into the array.

During playback, the recorded analog voltages are sequentially read from the storage array under control of the same sample clock, reconstructing the sampled waveform. The smoothing filter on the output path removes the sampling frequency component and the original waveform is restored.

The frequency of the sample clock affects record duration and quality. As the frequency increases the sound quality is improved, but, of course, the record duration is reduced. Conversely, a lower oscillator frequency gives increased duration at the cost of lower quality. The oscillator frequency

is trimmed to an accuracy better than 1% before the product leaves the factory. This is achieved by taking further advantage of the features of this technology. Trimming of oscillator components is done by programming nonvolatile trim bits that have been included on-chip.

The same process variables that affect the oscillator frequency also effect the filter cutoff frequency. When we trim the oscillator frequency, we also automatically trim the filter cutoff frequency.

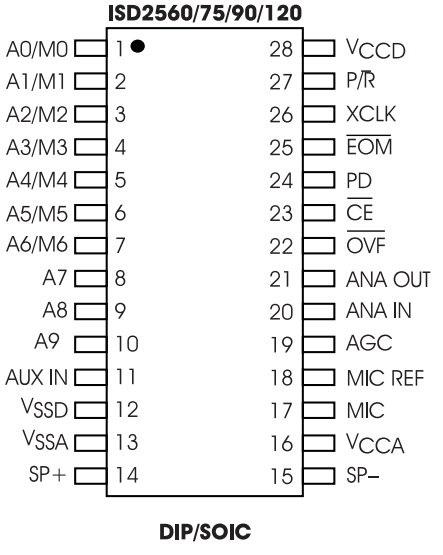
All ISD devices also include a smoothing filter connected to the output of the analog storage array. In devices without an on-chip speaker driver, this filter output is buffered and presented to an output pin.

Some ISD products include an on-chip speaker driver. In these devices, the output of the smoothing filter is connected through an analog multiplexer into the output power amplifier. Two output pins provide direct speaker drive capability of about 12.5 mW RMS (25 mW peak) into a 16 ohm speaker. This is enough to be clearly heard from the other side of a normal sized room. In some products the speaker driver is also available for system use via the AUX IN pin. From this input it can provide 50 mW RMS output.

The circuit design used in the ISD Series of devices results in the equivalent of 8 bits of storage in each EEPROM cell. Information is written into the cell in a closed loop fashion. A sample-and-hold circuit holds the data during the programming cycle and supplies the analog voltage to be stored to one input of a comparator. The other input to the comparator is the output of the storage cell itself. Electrons are pumped into the cell during multiple writes and the resulting stored level is fed back to the comparator.

When the comparator signals that the cell output voltage equals the level from the sample-and-hold, programming of that cell ceases. The minimum amount of charge injected into the cell during each write sets up system resolution. This is approximately 256 levels, which is equivalent to 8 bits of accuracy. Writing to the cell in this manner also eliminates cell to cell variations.

Figure 2: ISD2500 Pinout



The process used is based on the EEPROM floating gate technology. ISD guarantees 10 years of data retention but laboratory tests suggest that the typical data retention will be 100 years.

APPLICATION INFORMATION FOR ALL ISD ChipCorder PRODUCTS

Microphone and Speaker Selection

The ISD1000A series data sheet recommends a minimum speaker impedance of 16 Ω. An 8 Ω impedance speaker may be used that will result in a higher volume level and increased distortion. In addition, I_{CC} current will be higher. An 8 to 20 Ω resistor, in series with the speaker, controls volume and reduces I_{CC} playback current. Additionally, the speaker enclosure is important for best audio performance. Experiment with the sound cavity, grille, and foam baffle behind the speaker to optimize the system's performance.

Volume and audio improvements of 50 to 100 percent can be realized with improvements to the speaker enclosure that can include a sound baffle of foam or glass wool.

It is recommended that the ISD devices be evaluated initially using high quality speakers and low background noise to confirm the high voice quality possible. Then if trade-offs need to be made later on speaker size or quality, an informed quality versus cost decision can be made.

The selection of a good quality microphone and speaker enhances the audio performance of your application.

Two sources for 16-Ω speakers are:

MCM Electronics
Dayton, OH
(800) 543-4330

QUAM
Chicago, IL
(312) 488-5800

With the proper connections, some telephone handsets can also be used. Good quality audio techniques should be used so input signal noise and background noise will be minimized during recording.

Table 1: Speaker Sources

Mfg.	Device #	Shape	Weight	Freq. Resp.	Max. Watts
Quam	4A1Z16	3" sq.	0.25 lbs.	200–11K	3
Quam	35A05Z16	3 x 5 oval	0.50 lbs.	150–7K	2
Pioneer	ALLEC80-092F	4.5" round	1.50 lbs.	68–15K	30

MICROPHONE OPTIONS FOR THE ISD1000A, ISD1100, ISD1200, ISD1400, ISD1500, AND ISD2500 SERIES

Most schematics for the ISD single-chip voice record and playback devices show the use of a conventional electret or "capacitor" microphone. These microphones have several advantages over other common types. They have excellent frequency response and high output. They are available in many different sizes, from "grain-of-rice" to a standard 1/4-inch diameter. They are also rugged and inexpensive.

The ISD "standard" microphone application requires seven components to operate; see Figure 1. These components perform several functions.

- Microphone bias is supplied by a network composed of R2, R3, and R4, with C3 acting as a filter capacitor.
- C4 is a DC blocking capacitor between the microphone and the MIC pin on the ISD device.
- C5 acts as a coupling capacitor bringing microphone ground noise into the MIC REF pin.
- The MIC REF input provides a noise canceling (common mode rejection) input to reduce recorded noise.
- Since R3 and R4 are equal, the power supply noise will be equal and canceled by the common mode rejection of the microphone preamplifier.

These parts must be used with any microphone that requires DC bias. Another example would be a carbon microphone. These were used until recently in telephones or two way radios. However, there are other microphones that do not require a bias supply.

There are several types of microphones that are "self-generating." These microphones cause a current to flow (or a potential to be developed) directly from sound wave pressure. Two of these are dynamic and crystal microphones.

- A dynamic microphone uses a coil of wire and a magnet. One end of the magnet is tied to a diaphragm to generate a current proportional to sound pressure.
- A crystal microphone has a diaphragm connected to a crystalline structure. Sound pressure causes stress in the crystal. Through the piezoelectric effect the crystal generates a voltage.

Such self-generating microphones may be connected directly to an ISD device's microphone inputs.

The two microphone inputs to the ISD device are MIC and MIC REF. These two pins are differential inputs to the on-chip microphone preamplifier. A non-biased microphone, as discussed, may be connected directly across these two pins. No coupling capacitors are needed. This benefits the designer in several ways. Most obvious is the elimination of the components associated with the microphone bias. The secondary considerations may be as important.

Figure 2 shows how a non-biased microphone is connected to an ISD single-chip voice record/playback device. Only the components directly associated with the microphone are shown.

When an electret microphone is used, its signal must be referenced to the external circuit ground. This is because of the bias requirement. This creates two potential external sources of noise. Noise can come from the V_{CC} supply and from currents flowing in the circuit board ground.

The MIC REF pin is a common mode noise canceling input in the electret application. This method of noise reduction usually works well. It depends on good PC board layout rules and adequate bypassing of the V_{CCD} and V_{CCA} pins. When a non-biased microphone is used, however, these two noise sources are eliminated. A designer may find the circuit will perform adequately with no bypass capacitors at all.

Several readily available microphones will drive ISD1000A, ISD1100, ISD1200, ISD1400 ISD1500, and ISD2500 series devices. The following notes have been determined experimentally from a sample of microphone elements.

- Crystal, ceramic, and dynamic microphone elements (as well as crystal earphones) will work when connected directly to the MIC and MIC REF inputs of ISD devices.
- In general, the crystal and dynamic microphones have more output level and the ceramic elements less.
- The best quality was achieved using the dynamic microphone.
- A piezo speaker element (sometimes called a sounder) will work adequately for some applications. It must be mechanically mounted to some sort of sounding board (such as a piece of cardboard). The cardboard becomes a sounding board and couples the sound pressure into the element. Note that piezo sounders come in active and passive styles. The active piezo elements are actually noise makers and cannot be used as microphones.

Catalog suppliers such as Mouser (1-800-346-6873) carry microphone elements of several types that will work adequately. The Mouser catalog shows electret, crystal, ceramic, and dynamic microphones plus crystal earphones.

One source for piezo speaker elements is Radio Shack (part number is 273-091).

ELECTRET MICROPHONE SPECIFICATIONS

Specifications for the electret microphone are:

- 1 KΩ impedence
- Omni-directional
- 64 dB sensitivity
- 50 Hz to 8 KHz frequency
- Less than 1 mA current drain
- Greater than 40 dB S/N ratio
- Operates 2 to 10 VDC

These microphone specifications are not critical; however, microphones with these characteristics have been found to operate satisfactory.

Three sources for electret microphones are:

Mouser Electronics
(800) 346-6873
#25LM049 (PC mount)
#25LM045 (Coax leads)

Radio Shack
(800) 433-2024
#270-090 (PC mount)
#270-092 (Coax leads)
#273-091 (Piezo)

DIGI-KEY
(800) 344-4539
#P9931-ND (PC mount)

PREFERRED ELECTRET MICROPHONE CIRCUIT

Figure 1 shows a differential circuit for the standard ISD device microphone input. In this circuit, an electret microphone is used to differentially drive the microphone preamplifier. The microphone is connected directly between MIC and MIC REF. Since R3 and R4 are equal resistors, power supply noise will be a common mode signal. Common mode rejection inherent in the microphone preamplifier will attenuate any noise.

Figure 1: Differential Electret Microphone Circuit

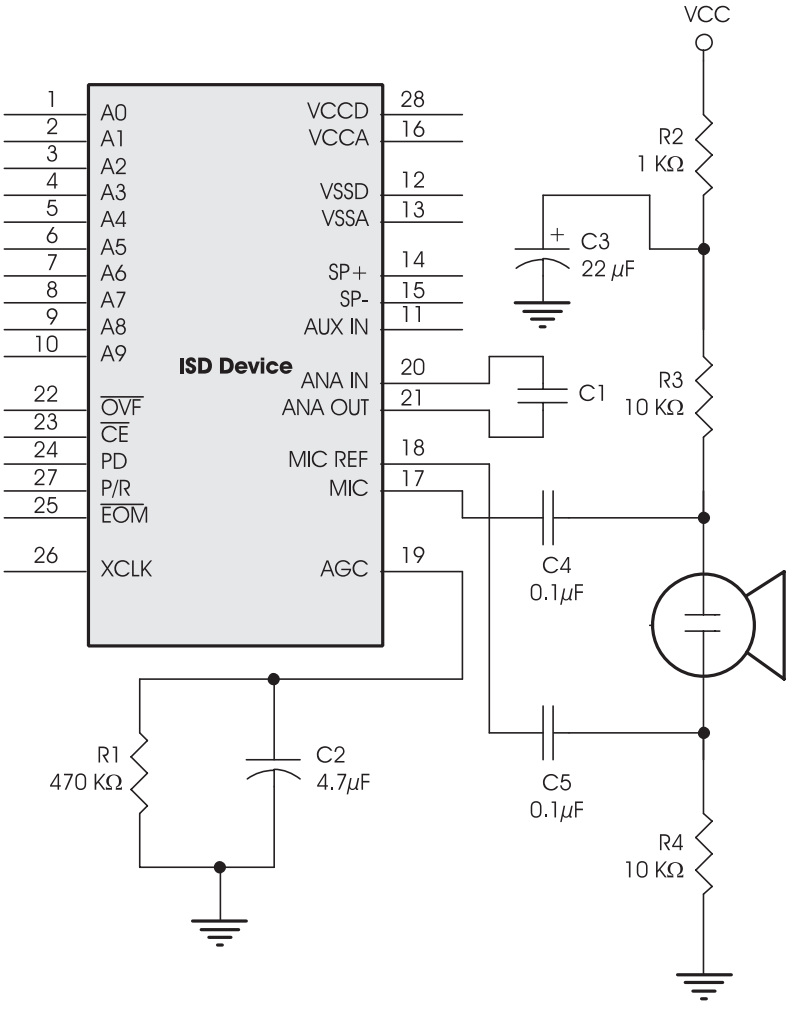
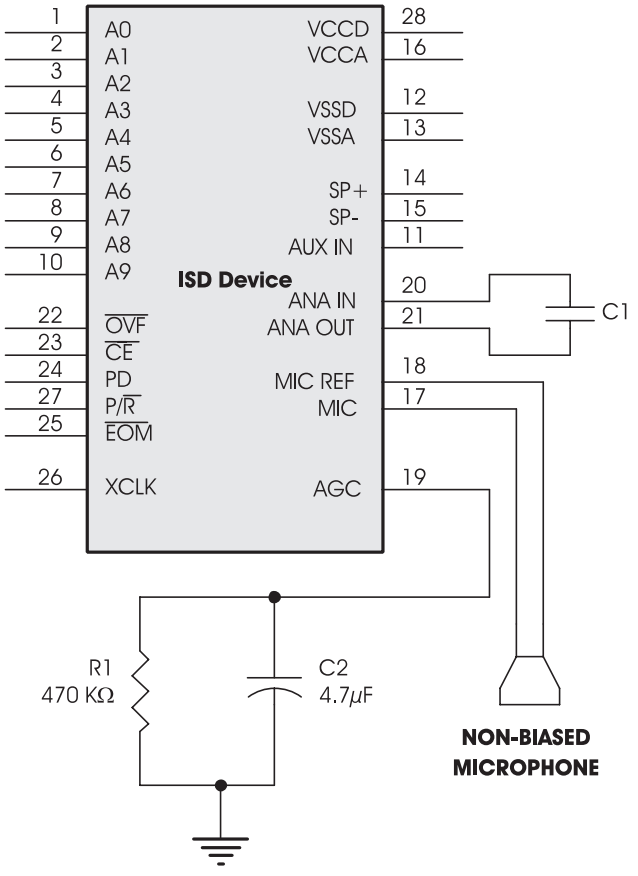


Figure 2: Self-Biasing Microphone



APPLICATION INFORMATION FOR ALL ISD ChipCorder PRODUCTS

Address Segment Resolution

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A 1416 2532 2560	1110 1210 1020A 1420 2540 2575	1212 2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
	Address Inputs																		
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0									
0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0 1	0.1	0.125	0.15	0.2	0.15	0.1875	0.225	0.3
2	0	0	0	0	0	0	0	0	1	0	0 2	0.2	0.25	0.3	0.4	0.3	0.375	0.45	0.6
3	0	0	0	0	0	0	0	0	1	1	0 3	0.3	0.375	0.45	0.6	0.45	0.5625	0.675	0.9
4	0	0	0	0	0	0	0	1	0	0	0 4	0.4	0.5	0.6	0.8	0.6	0.75	0.9	1.2
5	0	0	0	0	0	0	0	1	0	1	0 5	0.5	0.625	0.75	1	0.75	0.9375	1.125	1.5
6	0	0	0	0	0	0	0	1	1	0	0 6	0.6	0.75	0.9	1.2	0.9	1.125	1.35	1.8
7	0	0	0	0	0	0	0	1	1	1	0 7	0.7	0.875	1.05	1.4	1.05	1.3125	1.575	2.1
8	0	0	0	0	0	0	1	0	0	0	0 8	0.8	1	1.2	1.6	1.2	1.5	1.8	2.4
9	0	0	0	0	0	0	1	0	0	1	0 9	0.9	1.125	1.35	1.8	1.35	1.6875	2.025	2.7
10	0	0	0	0	0	0	1	0	1	0	0 A	1	1.25	1.5	2	1.5	1.875	2.25	3
11	0	0	0	0	0	0	1	0	1	1	0 B	1.1	1.375	1.65	2.2	1.65	2.0625	2.475	3.3
12	0	0	0	0	0	0	1	1	0	0	0 C	1.2	1.5	1.8	2.4	1.8	2.25	2.7	3.6
13	0	0	0	0	0	0	1	1	0	1	0 D	1.3	1.625	1.95	2.6	1.95	2.4375	2.925	3.9
14	0	0	0	0	0	0	1	1	1	0	0 E	1.4	1.75	2.1	2.8	2.1	2.625	3.15	4.2
15	0	0	0	0	0	0	1	1	1	1	0 F	1.5	1.875	2.25	3	2.25	2.8125	3.375	4.5
16	0	0	0	0	0	1	0	0	0	0	1 0	1.6	2	2.4	3.2	2.4	3	3.6	4.8
17	0	0	0	0	0	1	0	0	0	1	1 1	1.7	2.125	2.55	3.4	2.55	3.1875	3.825	5.1
18	0	0	0	0	0	1	0	0	1	0	1 2	1.8	2.25	2.7	3.6	2.7	3.375	4.05	5.4
19	0	0	0	0	0	1	0	0	1	1	1 3	1.9	2.375	2.85	3.8	2.85	3.5625	4.275	5.7
20	0	0	0	0	0	1	0	1	0	0	1 4	2	2.5	3	4	3	3.75	4.5	6
21	0	0	0	0	0	1	0	1	0	1	1 5	2.1	2.625	3.15	4.2	3.15	3.9375	4.725	6.3
22	0	0	0	0	0	1	0	1	1	0	1 6	2.2	2.75	3.3	4.4	3.3	4.125	4.95	6.6
23	0	0	0	0	0	1	0	1	1	1	1 7	2.3	2.875	3.45	4.6	3.45	4.3125	5.175	6.9

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
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DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0									
24	0	0	0	0	0	1	1	0	0	0	1 8	2.4	3	3.6	4.8	3.6	4.5	5.4	7.2
25	0	0	0	0	0	1	1	0	0	1	1 9	2.5	3.125	3.75	5	3.75	4.6875	5.625	7.5
26	0	0	0	0	0	1	1	0	1	0	1 A	2.6	3.25	3.9	5.2	3.9	4.875	5.85	7.8
27	0	0	0	0	0	1	1	0	1	1	1 B	2.7	3.375	4.05	5.4	4.05	5.0625	6.075	8.1
28	0	0	0	0	0	1	1	1	0	0	1 C	2.8	3.5	4.2	5.6	4.2	5.25	6.3	8.4
29	0	0	0	0	0	1	1	1	0	1	1 D	2.9	3.625	4.35	5.8	4.35	5.4375	6.525	8.7
30	0	0	0	0	0	1	1	1	1	0	1 E	3	3.75	4.5	6	4.5	5.625	6.75	9
31	0	0	0	0	0	1	1	1	1	1	1 F	3.1	3.875	4.65	6.2	4.65	5.8125	6.975	9.3
32	0	0	0	0	1	0	0	0	0	0	2 0	3.2	4	4.8	6.4	4.8	6	7.2	9.6
33	0	0	0	0	1	0	0	0	0	1	2 1	3.3	4.125	4.95	6.6	4.95	6.1875	7.425	9.9
34	0	0	0	0	1	0	0	0	1	0	2 2	3.4	4.25	5.1	6.8	5.1	6.375	7.65	10.2
35	0	0	0	0	1	0	0	0	1	1	2 3	3.5	4.375	5.25	7	5.25	6.5625	7.875	10.5
36	0	0	0	0	1	0	0	1	0	0	2 4	3.6	4.5	5.4	7.2	5.4	6.75	8.1	10.8
37	0	0	0	0	1	0	0	1	0	1	2 5	3.7	4.625	5.55	7.4	5.55	6.9375	8.325	11.1
38	0	0	0	0	1	0	0	1	1	0	2 6	3.8	4.75	5.7	7.6	5.7	7.125	8.55	11.4
39	0	0	0	0	1	0	0	1	1	1	2 7	3.9	4.875	5.85	7.8	5.85	7.3125	8.775	11.7
40	0	0	0	0	1	0	1	0	0	0	2 8	4	5	6	8	6	7.5	9	12
41	0	0	0	0	1	0	1	0	0	1	2 9	4.1	5.125	6.15	8.2	6.15	7.6875	9.225	12.3
42	0	0	0	0	1	0	1	0	1	0	2 A	4.2	5.25	6.3	8.4	6.3	7.875	9.45	12.6
43	0	0	0	0	1	0	1	0	1	1	2 B	4.3	5.375	6.45	8.6	6.45	8.0625	9.675	12.9
44	0	0	0	0	1	0	1	1	0	0	2 C	4.4	5.5	6.6	8.8	6.6	8.25	9.9	13.2
45	0	0	0	0	1	0	1	1	0	1	2 D	4.5	5.625	6.75	9	6.75	8.4375	10.125	13.5
46	0	0	0	0	1	0	1	1	1	0	2 E	4.6	5.75	6.9	9.2	6.9	8.625	10.35	13.8
47	0	0	0	0	1	0	1	1	1	1	2 F	4.7	5.875	7.05	9.4	7.05	8.8125	10.575	14.1
48	0	0	0	0	1	1	0	0	0	0	3 0	4.8	6	7.2	9.6	7.2	9	10.8	14.4
49	0	0	0	0	1	1	0	0	0	1	3 1	4.9	6.125	7.35	9.8	7.35	9.1875	11.025	14.7
50	0	0	0	0	1	1	0	0	1	0	3 2	5	6.25	7.5	10	7.5	9.375	11.25	15
51	0	0	0	0	1	1	0	0	1	1	3 3	5.1	6.375	7.65	10.2	7.65	9.5625	11.475	15.3
52	0	0	0	0	1	1	0	1	0	0	3 4	5.2	6.5	7.8	10.4	7.8	9.75	11.7	15.6
53	0	0	0	0	1	1	0	1	0	1	3 5	5.3	6.625	7.95	10.6	7.95	9.9375	11.925	15.9
54	0	0	0	0	1	1	0	1	1	0	3 6	5.4	6.75	8.1	10.8	8.1	10.125	12.15	16.2
55	0	0	0	0	1	1	0	1	1	1	3 7	5.5	6.875	8.25	11	8.25	10.3125	12.375	16.5
56	0	0	0	0	1	1	1	0	0	0	3 8	5.6	7	8.4	11.2	8.4	10.5	12.6	16.8
57	0	0	0	0	1	1	1	0	0	1	3 9	5.7	7.125	8.55	11.4	8.55	10.6875	12.825	17.1
58	0	0	0	0	1	1	1	0	1	0	3 A	5.8	7.25	8.7	11.6	8.7	10.875	13.05	17.4
59	0	0	0	0	1	1	1	0	1	1	3 B	5.9	7.375	8.85	11.8	8.85	11.0625	13.275	17.7
60	0	0	0	0	1	1	1	1	0	0	3 C	6	7.5	9	12	9	11.25	13.5	18

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A 1416	1110 1210 1020A 1420	1212					
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
61	0	0	0	0	1	1	1	1	0	1	3 D	6.1	7.625	9.15	12.2	9.15	11.4375	13.725	18.3
62	0	0	0	0	1	1	1	1	1	0	3 E	6.2	7.75	9.3	12.4	9.3	11.625	13.95	18.6
63	0	0	0	0	1	1	1	1	1	1	3 F	6.3	7.875	9.45	12.6	9.45	11.8125	14.175	18.9
64	0	0	0	1	0	0	0	0	0	0	4 0	6.4	8	9.6	12.8	9.6	12	14.4	19.2
65	0	0	0	1	0	0	0	0	0	1	4 1	6.5	8.125	9.75	13	9.75	12.1875	14.625	19.5
66	0	0	0	1	0	0	0	0	1	0	4 2	6.6	8.25	9.9	13.2	9.9	12.375	14.85	19.8
67	0	0	0	1	0	0	0	0	1	1	4 3	6.7	8.375	10.05	13.4	10.05	12.5625	15.075	20.1
68	0	0	0	1	0	0	0	1	0	0	4 4	6.8	8.5	10.2	13.6	10.2	12.75	15.3	20.4
69	0	0	0	1	0	0	0	1	0	1	4 5	6.9	8.625	10.35	13.8	10.35	12.9375	15.525	20.7
70	0	0	0	1	0	0	0	1	1	0	4 6	7	8.75	10.5	14	10.5	13.125	15.75	21
71	0	0	0	1	0	0	0	1	1	1	4 7	7.1	8.875	10.65	14.2	10.65	13.3125	15.975	21.3
72	0	0	0	1	0	0	1	0	0	0	4 8	7.2	9	10.8	14.4	10.8	13.5	16.2	21.6
73	0	0	0	1	0	0	1	0	0	1	4 9	7.3	9.125	10.95	14.6	10.95	13.6875	16.425	21.9
74	0	0	0	1	0	0	1	0	1	0	4 A	7.4	9.25	11.1	14.8	11.1	13.875	16.65	22.2
75	0	0	0	1	0	0	1	0	1	1	4 B	7.5	9.375	11.25	15	11.25	14.0625	16.875	22.5
76	0	0	0	1	0	0	1	1	0	0	4 C	7.6	9.5	11.4	15.2	11.4	14.25	17.1	22.8
77	0	0	0	1	0	0	1	1	0	1	4 D	7.7	9.625	11.55	15.4	11.55	14.4375	17.325	23.1
78	0	0	0	1	0	0	1	1	1	0	4 E	7.8	9.75	11.7	15.6	11.7	14.625	17.55	23.4
79	0	0	0	1	0	0	1	1	1	1	4 F	7.9	9.875	11.85	15.8	11.85	14.8125	17.775	23.7

"End of Message Storage Space for ISD1110, ISD1210, and ISD1212 Devices"

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A	1020A						
												1416	1420						
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
80	0	0	0	1	0	1	0	0	0	0	5 0	8	10	12	16	12	15	18	24
81	0	0	0	1	0	1	0	0	0	1	5 1	8.1	10.125	12.15	16.2	12.15	15.1875	18.225	24.3
82	0	0	0	1	0	1	0	0	1	0	5 2	8.2	10.25	12.3	16.4	12.3	15.375	18.45	24.6
83	0	0	0	1	0	1	0	0	1	1	5 3	8.3	10.375	12.45	16.6	12.45	15.5625	18.675	24.9
84	0	0	0	1	0	1	0	1	0	0	5 4	8.4	10.5	12.6	16.8	12.6	15.75	18.9	25.2
85	0	0	0	1	0	1	0	1	0	1	5 5	8.5	10.625	12.75	17	12.75	15.9375	19.125	25.5
86	0	0	0	1	0	1	0	1	1	0	5 6	8.6	10.75	12.9	17.2	12.9	16.125	19.35	25.8
87	0	0	0	1	0	1	0	1	1	1	5 7	8.7	10.875	13.05	17.4	13.05	16.3125	19.575	26.1
88	0	0	0	1	0	1	1	0	0	0	5 8	8.8	11	13.2	17.6	13.2	16.5	19.8	26.4
89	0	0	0	1	0	1	1	0	0	1	5 9	8.9	11.125	13.35	17.8	13.35	16.6875	20.025	26.7
90	0	0	0	1	0	1	1	0	1	0	5 A	9	11.25	13.5	18	13.5	16.875	20.25	27
91	0	0	0	1	0	1	1	0	1	1	5 B	9.1	11.375	13.65	18.2	13.65	17.0625	20.475	27.3
92	0	0	0	1	0	1	1	1	0	0	5 C	9.2	11.5	13.8	18.4	13.8	17.25	20.7	27.6
93	0	0	0	1	0	1	1	1	0	1	5 D	9.3	11.625	13.95	18.6	13.95	17.4375	20.925	27.9
94	0	0	0	1	0	1	1	1	1	0	5 E	9.4	11.75	14.1	18.8	14.1	17.625	21.15	28.2
95	0	0	0	1	0	1	1	1	1	1	5 F	9.5	11.875	14.25	19	14.25	17.8125	21.375	28.5
96	0	0	0	1	1	0	0	0	0	0	6 0	9.6	12	14.4	19.2	14.4	18	21.6	28.8
97	0	0	0	1	1	0	0	0	0	1	6 1	9.7	12.125	14.55	19.4	14.55	18.1875	21.825	29.1
98	0	0	0	1	1	0	0	0	1	0	6 2	9.8	12.25	14.7	19.6	14.7	18.375	22.05	29.4
99	0	0	0	1	1	0	0	0	1	1	6 3	9.9	12.375	14.85	19.8	14.85	18.5625	22.275	29.7
100	0	0	0	1	1	0	0	1	0	0	6 4	10	12.5	15	20	15	18.75	22.5	30
101	0	0	0	1	1	0	0	1	0	1	6 5	10.1	12.625	15.15	20.2	15.15	18.9375	22.725	30.3
102	0	0	0	1	1	0	0	1	1	0	6 6	10.2	12.75	15.3	20.4	15.3	19.125	22.95	30.6
103	0	0	0	1	1	0	0	1	1	1	6 7	10.3	12.875	15.45	20.6	15.45	19.3125	23.175	30.9
104	0	0	0	1	1	0	1	0	0	0	6 8	10.4	13	15.6	20.8	15.6	19.5	23.4	31.2
105	0	0	0	1	1	0	1	0	0	1	6 9	10.5	13.125	15.75	21	15.75	19.6875	23.625	31.5
106	0	0	0	1	1	0	1	0	1	0	6 A	10.6	13.25	15.9	21.2	15.9	19.875	23.85	31.8
107	0	0	0	1	1	0	1	0	1	1	6 B	10.7	13.375	16.05	21.4	16.05	20.0625	24.075	32.1
108	0	0	0	1	1	0	1	1	0	0	6 C	10.8	13.5	16.2	21.6	16.2	20.25	24.3	32.4
109	0	0	0	1	1	0	1	1	0	1	6 D	10.9	13.625	16.35	21.8	16.35	20.4375	24.525	32.7
110	0	0	0	1	1	0	1	1	1	0	6 E	11	13.75	16.5	22	16.5	20.625	24.75	33
111	0	0	0	1	1	0	1	1	1	1	6 F	11.1	13.875	16.65	22.2	16.65	20.8125	24.975	33.3
112	0	0	0	1	1	1	0	0	0	0	7 0	11.2	14	16.8	22.4	16.8	21	25.2	33.6
113	0	0	0	1	1	1	0	0	0	1	7 1	11.3	14.125	16.95	22.6	16.95	21.1875	25.425	33.9
114	0	0	0	1	1	1	0	0	1	0	7 2	11.4	14.25	17.1	22.8	17.1	21.375	25.65	34.2
115	0	0	0	1	1	1	0	0	1	1	7 3	11.5	14.375	17.25	23	17.25	21.5625	25.875	34.5
116	0	0	0	1	1	1	0	1	0	0	7 4	11.6	14.5	17.4	23.2	17.4	21.75	26.1	34.8

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A	1020A						
												1416	1420						
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
117	0	0	0	1	1	1	0	1	0	1	7 5	11.7	14.625	17.55	23.4	17.55	21.9375	26.325	35.1
118	0	0	0	1	1	1	0	1	1	0	7 6	11.8	14.75	17.7	23.6	17.7	22.125	26.55	35.4
119	0	0	0	1	1	1	0	1	1	1	7 7	11.9	14.875	17.85	23.8	17.85	22.3125	26.775	35.7
120	0	0	0	1	1	1	1	0	0	0	7 8	12	15	18	24	18	22.5	27	36
121	0	0	0	1	1	1	1	0	0	1	7 9	12.1	15.125	18.15	24.2	18.15	22.6875	27.225	36.3
122	0	0	0	1	1	1	1	0	1	0	7 A	12.2	15.25	18.3	24.4	18.3	22.875	27.45	36.6
123	0	0	0	1	1	1	1	0	1	1	7 B	12.3	15.375	18.45	24.6	18.45	23.0625	27.675	36.9
124	0	0	0	1	1	1	1	1	0	0	7 C	12.4	15.5	18.6	24.8	18.6	23.25	27.9	37.2
125	0	0	0	1	1	1	1	1	0	1	7 D	12.5	15.625	18.75	25	18.75	23.4375	28.125	37.5
126	0	0	0	1	1	1	1	1	1	0	7 E	12.6	15.75	18.9	25.2	18.9	23.625	28.35	37.8
127	0	0	0	1	1	1	1	1	1	1	7 F	12.7	15.875	19.05	25.4	19.05	23.8125	28.575	38.1
128	0	0	1	0	0	0	0	0	0	0	8 0	12.8	16	19.2	25.6	19.2	24	28.8	38.4
129	0	0	1	0	0	0	0	0	0	1	8 1	12.9	16.125	19.35	25.8	19.35	24.1875	29.025	38.7
130	0	0	1	0	0	0	0	0	1	0	8 2	13	16.25	19.5	26	19.5	24.375	29.25	39
131	0	0	1	0	0	0	0	0	1	1	8 3	13.1	16.375	19.65	26.2	19.65	24.5625	29.475	39.3
132	0	0	1	0	0	0	0	1	0	0	8 4	13.2	16.5	19.8	26.4	19.8	24.75	29.7	39.6
133	0	0	1	0	0	0	0	1	0	1	8 5	13.3	16.625	19.95	26.6	19.95	24.9375	29.925	39.9
134	0	0	1	0	0	0	0	1	1	0	8 6	13.4	16.75	20.1	26.8	20.1	25.125	30.15	40.2
135	0	0	1	0	0	0	0	1	1	1	8 7	13.5	16.875	20.25	27	20.25	25.3125	30.375	40.5
136	0	0	1	0	0	0	1	0	0	0	8 8	13.6	17	20.4	27.2	20.4	25.5	30.6	40.8
137	0	0	1	0	0	0	1	0	0	1	8 9	13.7	17.125	20.55	27.4	20.55	25.6875	30.825	41.1
138	0	0	1	0	0	0	1	0	1	0	8 A	13.8	17.25	20.7	27.6	20.7	25.875	31.05	41.4
139	0	0	1	0	0	0	1	0	1	1	8 B	13.9	17.375	20.85	27.8	20.85	26.0625	31.275	41.7
140	0	0	1	0	0	0	1	1	0	0	8 C	14	17.5	21	28	21	26.25	31.5	42
141	0	0	1	0	0	0	1	1	0	1	8 D	14.1	17.625	21.15	28.2	21.15	26.4375	31.725	42.3
142	0	0	1	0	0	0	1	1	1	0	8 E	14.2	17.75	21.3	28.4	21.3	26.625	31.95	42.6
143	0	0	1	0	0	0	1	1	1	1	8 F	14.3	17.875	21.45	28.6	21.45	26.8125	32.175	42.9
144	0	0	1	0	0	1	0	0	0	0	9 0	14.4	18	21.6	28.8	21.6	27	32.4	43.2
145	0	0	1	0	0	1	0	0	0	1	9 1	14.5	18.125	21.75	29	21.75	27.1875	32.625	43.5
146	0	0	1	0	0	1	0	0	1	0	9 2	14.6	18.25	21.9	29.2	21.9	27.375	32.85	43.8
147	0	0	1	0	0	1	0	0	1	1	9 3	14.7	18.375	22.05	29.4	22.05	27.5625	33.075	44.1
148	0	0	1	0	0	1	0	1	0	0	9 4	14.8	18.5	22.2	29.6	22.2	27.75	33.3	44.4
149	0	0	1	0	0	1	0	1	0	1	9 5	14.9	18.625	22.35	29.8	22.35	27.9375	33.525	44.7
150	0	0	1	0	0	1	0	1	1	0	9 6	15	18.75	22.5	30	22.5	28.125	33.75	45
151	0	0	1	0	0	1	0	1	1	1	9 7	15.1	18.875	22.65	30.2	22.65	28.3125	33.975	45.3
152	0	0	1	0	0	1	1	0	0	0	9 8	15.2	19	22.8	30.4	22.8	28.5	34.2	45.6
153	0	0	1	0	0	1	1	0	0	1	9 9	15.3	19.125	22.95	30.6	22.95	28.6875	34.425	45.9

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A 1416	1020A 1420						
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
154	0	0	1	0	0	1	1	0	1	0	9 A	15.4	19.25	23.1	30.8	23.1	28.875	34.65	46.2
155	0	0	1	0	0	1	1	0	1	1	9 B	15.5	19.375	23.25	31	23.25	29.0625	34.875	46.5
156	0	0	1	0	0	1	1	1	0	0	9 C	15.6	19.5	23.4	31.2	23.4	29.25	35.1	46.8
157	0	0	1	0	0	1	1	1	0	1	9 D	15.7	19.625	23.55	31.4	23.55	29.4375	35.325	47.1
158	0	0	1	0	0	1	1	1	1	0	9 E	15.8	19.75	23.7	31.6	23.7	29.625	35.55	47.4
159	0	0	1	0	0	1	1	1	1	1	9 F	15.9	19.875	23.85	31.8	23.85	29.8125	35.775	47.7
"End of Message Storage Space for ISD1416, ISD1420, ISD1016A, and ISD1020A Devices"																			

											Sample Rates							
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
											ISD Part Numbers							
	Address Inputs										2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	2560	2575	2590	25120	33120	33150	33180	33240
160	0	0	1	0	1	0	0	0	0	0	A 0	16	20	24	32	24	30	36	48
161	0	0	1	0	1	0	0	0	0	1	A 1	16.1	20.125	24.15	32.2	24.15	30.1875	36.225	48.3
162	0	0	1	0	1	0	0	0	1	0	A 2	16.2	20.25	24.3	32.4	24.3	30.375	36.45	48.6
163	0	0	1	0	1	0	0	0	1	1	A 3	16.3	20.375	24.45	32.6	24.45	30.5625	36.675	48.9
164	0	0	1	0	1	0	0	1	0	0	A 4	16.4	20.5	24.6	32.8	24.6	30.75	36.9	49.2
165	0	0	1	0	1	0	0	1	0	1	A 5	16.5	20.625	24.75	33	24.75	30.9375	37.125	49.5
166	0	0	1	0	1	0	0	1	1	0	A 6	16.6	20.75	24.9	33.2	24.9	31.125	37.35	49.8
167	0	0	1	0	1	0	0	1	1	1	A 7	16.7	20.875	25.05	33.4	25.05	31.3125	37.575	50.1
168	0	0	1	0	1	0	1	0	0	0	A 8	16.8	21	25.2	33.6	25.2	31.5	37.8	50.4
169	0	0	1	0	1	0	1	0	0	1	A 9	16.9	21.125	25.35	33.8	25.35	31.6875	38.025	50.7
170	0	0	1	0	1	0	1	0	1	0	A A	17	21.25	25.5	34	25.5	31.875	38.25	51
171	0	0	1	0	1	0	1	0	1	1	A B	17.1	21.375	25.65	34.2	25.65	32.0625	38.475	51.3
172	0	0	1	0	1	0	1	1	0	0	A C	17.2	21.5	25.8	34.4	25.8	32.25	38.7	51.6
173	0	0	1	0	1	0	1	1	0	1	A D	17.3	21.625	25.95	34.6	25.95	32.4375	38.925	51.9
174	0	0	1	0	1	0	1	1	1	0	A E	17.4	21.75	26.1	34.8	26.1	32.625	39.15	52.2
175	0	0	1	0	1	0	1	1	1	1	A F	17.5	21.875	26.25	35	26.25	32.8125	39.375	52.5
176	0	0	1	0	1	1	0	0	0	0	B 0	17.6	22	26.4	35.2	26.4	33	39.6	52.8
177	0	0	1	0	1	1	0	0	0	1	B 1	17.7	22.125	26.55	35.4	26.55	33.1875	39.825	53.1
178	0	0	1	0	1	1	0	0	1	0	B 2	17.8	22.25	26.7	35.6	26.7	33.375	40.05	53.4
179	0	0	1	0	1	1	0	0	1	1	B 3	17.9	22.375	26.85	35.8	26.85	33.5625	40.275	53.7
180	0	0	1	0	1	1	0	1	0	0	B 4	18	22.5	27	36	27	33.75	40.5	54
181	0	0	1	0	1	1	0	1	0	1	B 5	18.1	22.625	27.15	36.2	27.15	33.9375	40.725	54.3

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
182	0	0	1	0	1	1	0	1	1	0	B 6	18.2	22.75	27.3	36.4	27.3	34.125	40.95	54.6
183	0	0	1	0	1	1	0	1	1	1	B 7	18.3	22.875	27.45	36.6	27.45	34.3125	41.175	54.9
184	0	0	1	0	1	1	1	0	0	0	B 8	18.4	23	27.6	36.8	27.6	34.5	41.4	55.2
185	0	0	1	0	1	1	1	0	0	1	B 9	18.5	23.125	27.75	37	27.75	34.6875	41.625	55.5
186	0	0	1	0	1	1	1	0	1	0	B A	18.6	23.25	27.9	37.2	27.9	34.875	41.85	55.8
187	0	0	1	0	1	1	1	0	1	1	B B	18.7	23.375	28.05	37.4	28.05	35.0625	42.075	56.1
188	0	0	1	0	1	1	1	1	0	0	B C	18.8	23.5	28.2	37.6	28.2	35.25	42.3	56.4
189	0	0	1	0	1	1	1	1	0	1	B D	18.9	23.625	28.35	37.8	28.35	35.4375	42.525	56.7
190	0	0	1	0	1	1	1	1	1	0	B E	19	23.75	28.5	38	28.5	35.625	42.75	57
191	0	0	1	0	1	1	1	1	1	1	B F	19.1	23.875	28.65	38.2	28.65	35.8125	42.975	57.3
192	0	0	1	1	0	0	0	0	0	0	C 0	19.2	24	28.8	38.4	28.8	36	43.2	57.6
193	0	0	1	1	0	0	0	0	0	1	C 1	19.3	24.125	28.95	38.6	28.95	36.1875	43.425	57.9
194	0	0	1	1	0	0	0	0	1	0	C 2	19.4	24.25	29.1	38.8	29.1	36.375	43.65	58.2
195	0	0	1	1	0	0	0	0	1	1	C 3	19.5	24.375	29.25	39	29.25	36.5625	43.875	58.5
196	0	0	1	1	0	0	0	1	0	0	C 4	19.6	24.5	29.4	39.2	29.4	36.75	44.1	58.8
197	0	0	1	1	0	0	0	1	0	1	C 5	19.7	24.625	29.55	39.4	29.55	36.9375	44.325	59.1
198	0	0	1	1	0	0	0	1	1	0	C 6	19.8	24.75	29.7	39.6	29.7	37.125	44.55	59.4
199	0	0	1	1	0	0	0	1	1	1	C 7	19.9	24.875	29.85	39.8	29.85	37.3125	44.775	59.7
200	0	0	1	1	0	0	1	0	0	0	C 8	20	25	30	40	30	37.5	45	60
201	0	0	1	1	0	0	1	0	0	1	C 9	20.1	25.125	30.15	40.2	30.15	37.6875	45.225	60.3
202	0	0	1	1	0	0	1	0	1	0	C A	20.2	25.25	30.3	40.4	30.3	37.875	45.45	60.6
203	0	0	1	1	0	0	1	0	1	1	C B	20.3	25.375	30.45	40.6	30.45	38.0625	45.675	60.9
204	0	0	1	1	0	0	1	1	0	0	C C	20.4	25.5	30.6	40.8	30.6	38.25	45.9	61.2
205	0	0	1	1	0	0	1	1	0	1	C D	20.5	25.625	30.75	41	30.75	38.4375	46.125	61.5
206	0	0	1	1	0	0	1	1	1	0	C E	20.6	25.75	30.9	41.2	30.9	38.625	46.35	61.8
207	0	0	1	1	0	0	1	1	1	1	C F	20.7	25.875	31.05	41.4	31.05	38.8125	46.575	62.1
208	0	0	1	1	0	1	0	0	0	0	D 0	20.8	26	31.2	41.6	31.2	39	46.8	62.4
209	0	0	1	1	0	1	0	0	0	1	D 1	20.9	26.125	31.35	41.8	31.35	39.1875	47.025	62.7
210	0	0	1	1	0	1	0	0	1	0	D 2	21	26.25	31.5	42	31.5	39.375	47.25	63
211	0	0	1	1	0	1	0	0	1	1	D 3	21.1	26.375	31.65	42.2	31.65	39.5625	47.475	63.3
212	0	0	1	1	0	1	0	1	0	0	D 4	21.2	26.5	31.8	42.4	31.8	39.75	47.7	63.6
213	0	0	1	1	0	1	0	1	0	1	D 5	21.3	26.625	31.95	42.6	31.95	39.9375	47.925	63.9
214	0	0	1	1	0	1	0	1	1	0	D 6	21.4	26.75	32.1	42.8	32.1	40.125	48.15	64.2
215	0	0	1	1	0	1	0	1	1	1	D 7	21.5	26.875	32.25	43	32.25	40.3125	48.375	64.5
216	0	0	1	1	0	1	1	0	0	0	D 8	21.6	27	32.4	43.2	32.4	40.5	48.6	64.8
217	0	0	1	1	0	1	1	0	0	1	D 9	21.7	27.125	32.55	43.4	32.55	40.6875	48.825	65.1
218	0	0	1	1	0	1	1	0	1	0	D A	21.8	27.25	32.7	43.6	32.7	40.875	49.05	65.4
219	0	0	1	1	0	1	1	0	1	1	D B	21.9	27.375	32.85	43.8	32.85	41.0625	49.275	65.7
220	0	0	1	1	0	1	1	1	0	0	D C	22	27.5	33	44	33	41.25	49.5	66

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
221	0	0	1	1	0	1	1	1	0	1	D D	22.1	27.625	33.15	44.2	33.15	41.4375	49.725	66.3
222	0	0	1	1	0	1	1	1	1	0	D E	22.2	27.75	33.3	44.4	33.3	41.625	49.95	66.6
223	0	0	1	1	0	1	1	1	1	1	D F	22.3	27.875	33.45	44.6	33.45	41.8125	50.175	66.9
224	0	0	1	1	1	0	0	0	0	0	E 0	22.4	28	33.6	44.8	33.6	42	50.4	67.2
225	0	0	1	1	1	0	0	0	0	1	E 1	22.5	28.125	33.75	45	33.75	42.1875	50.625	67.5
226	0	0	1	1	1	0	0	0	1	0	E 2	22.6	28.25	33.9	45.2	33.9	42.375	50.85	67.8
227	0	0	1	1	1	0	0	0	1	1	E 3	22.7	28.375	34.05	45.4	34.05	42.5625	51.075	68.1
228	0	0	1	1	1	0	0	1	0	0	E 4	22.8	28.5	34.2	45.6	34.2	42.75	51.3	68.4
229	0	0	1	1	1	0	0	1	0	1	E 5	22.9	28.625	34.35	45.8	34.35	42.9375	51.525	68.7
230	0	0	1	1	1	0	0	1	1	0	E 6	23	28.75	34.5	46	34.5	43.125	51.75	69
231	0	0	1	1	1	0	0	1	1	1	E 7	23.1	28.875	34.65	46.2	34.65	43.3125	51.975	69.3
232	0	0	1	1	1	0	1	0	0	0	E 8	23.2	29	34.8	46.4	34.8	43.5	52.2	69.6
233	0	0	1	1	1	0	1	0	0	1	E 9	23.3	29.125	34.95	46.6	34.95	43.6875	52.425	69.9
234	0	0	1	1	1	0	1	0	1	0	E A	23.4	29.25	35.1	46.8	35.1	43.875	52.65	70.2
235	0	0	1	1	1	0	1	0	1	1	E B	23.5	29.375	35.25	47	35.25	44.0625	52.875	70.5
236	0	0	1	1	1	0	1	1	0	0	E C	23.6	29.5	35.4	47.2	35.4	44.25	53.1	70.8
237	0	0	1	1	1	0	1	1	0	1	E D	23.7	29.625	35.55	47.4	35.55	44.4375	53.325	71.1
238	0	0	1	1	1	0	1	1	1	0	E E	23.8	29.75	35.7	47.6	35.7	44.625	53.55	71.4
239	0	0	1	1	1	0	1	1	1	1	E F	23.9	29.875	35.85	47.8	35.85	44.8125	53.775	71.7
240	0	0	1	1	1	1	0	0	0	0	F 0	24	30	36	48	36	45	54	72
241	0	0	1	1	1	1	0	0	0	1	F 1	24.1	30.125	36.15	48.2	36.15	45.1875	54.225	72.3
242	0	0	1	1	1	1	0	0	1	0	F 2	24.2	30.25	36.3	48.4	36.3	45.375	54.45	72.6
243	0	0	1	1	1	1	0	0	1	1	F 3	24.3	30.375	36.45	48.6	36.45	45.5625	54.675	72.9
244	0	0	1	1	1	1	0	1	0	0	F 4	24.4	30.5	36.6	48.8	36.6	45.75	54.9	73.2
245	0	0	1	1	1	1	0	1	0	1	F 5	24.5	30.625	36.75	49	36.75	45.9375	55.125	73.5
246	0	0	1	1	1	1	0	1	1	0	F 6	24.6	30.75	36.9	49.2	36.9	46.125	55.35	73.8
247	0	0	1	1	1	1	0	1	1	1	F 7	24.7	30.875	37.05	49.4	37.05	46.3125	55.575	74.1
248	0	0	1	1	1	1	1	0	0	0	F 8	24.8	31	37.2	49.6	37.2	46.5	55.8	74.4
249	0	0	1	1	1	1	1	0	0	1	F 9	24.9	31.125	37.35	49.8	37.35	46.6875	56.025	74.7
250	0	0	1	1	1	1	1	0	1	0	F A	25	31.25	37.5	50	37.5	46.875	56.25	75
251	0	0	1	1	1	1	1	0	1	1	F B	25.1	31.375	37.65	50.2	37.65	47.0625	56.475	75.3
252	0	0	1	1	1	1	1	1	0	0	F C	25.2	31.5	37.8	50.4	37.8	47.25	56.7	75.6
253	0	0	1	1	1	1	1	1	0	1	F D	25.3	31.625	37.95	50.6	37.95	47.4375	56.925	75.9
254	0	0	1	1	1	1	1	1	1	0	F E	25.4	31.75	38.1	50.8	38.1	47.625	57.15	76.2
255	0	0	1	1	1	1	1	1	1	1	F F	25.5	31.875	38.25	51	38.25	47.8125	57.375	76.5
256	0	1	0	0	0	0	0	0	0	0	10 0	25.6	32	38.4	51.2	38.4	48	57.6	76.8
257	0	1	0	0	0	0	0	0	0	1	10 1	25.7	32.125	38.55	51.4	38.55	48.1875	57.825	77.1
258	0	1	0	0	0	0	0	0	1	0	10 2	25.8	32.25	38.7	51.6	38.7	48.375	58.05	77.4
259	0	1	0	0	0	0	0	0	1	1	10 3	25.9	32.375	38.85	51.8	38.85	48.5625	58.275	77.7

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
260	0	1	0	0	0	0	0	1	0	0	10 4	26	32.5	39	52	39	48.75	58.5	78
261	0	1	0	0	0	0	0	1	0	1	10 5	26.1	32.625	39.15	52.2	39.15	48.9375	58.725	78.3
262	0	1	0	0	0	0	0	1	1	0	10 6	26.2	32.75	39.3	52.4	39.3	49.125	58.95	78.6
263	0	1	0	0	0	0	0	1	1	1	10 7	26.3	32.875	39.45	52.6	39.45	49.3125	59.175	78.9
264	0	1	0	0	0	0	1	0	0	0	10 8	26.4	33	39.6	52.8	39.6	49.5	59.4	79.2
265	0	1	0	0	0	0	1	0	0	1	10 9	26.5	33.125	39.75	53	39.75	49.6875	59.625	79.5
266	0	1	0	0	0	0	1	0	1	0	10 A	26.6	33.25	39.9	53.2	39.9	49.875	59.85	79.8
267	0	1	0	0	0	0	1	0	1	1	10 B	26.7	33.375	40.05	53.4	40.05	50.0625	60.075	80.1
268	0	1	0	0	0	0	1	1	0	0	10 C	26.8	33.5	40.2	53.6	40.2	50.25	60.3	80.4
269	0	1	0	0	0	0	1	1	0	1	10 D	26.9	33.625	40.35	53.8	40.35	50.4375	60.525	80.7
270	0	1	0	0	0	0	1	1	1	0	10 E	27	33.75	40.5	54	40.5	50.625	60.75	81
271	0	1	0	0	0	0	1	1	1	1	10 F	27.1	33.875	40.65	54.2	40.65	50.8125	60.975	81.3
272	0	1	0	0	0	1	0	0	0	0	11 0	27.2	34	40.8	54.4	40.8	51	61.2	81.6
273	0	1	0	0	0	1	0	0	0	1	11 1	27.3	34.125	40.95	54.6	40.95	51.1875	61.425	81.9
274	0	1	0	0	0	1	0	0	1	0	11 2	27.4	34.25	41.1	54.8	41.1	51.375	61.65	82.2
275	0	1	0	0	0	1	0	0	1	1	11 3	27.5	34.375	41.25	55	41.25	51.5625	61.875	82.5
276	0	1	0	0	0	1	0	1	0	0	11 4	27.6	34.5	41.4	55.2	41.4	51.75	62.1	82.8
277	0	1	0	0	0	1	0	1	0	1	11 5	27.7	34.625	41.55	55.4	41.55	51.9375	62.325	83.1
278	0	1	0	0	0	1	0	1	1	0	11 6	27.8	34.75	41.7	55.6	41.7	52.125	62.55	83.4
279	0	1	0	0	0	1	0	1	1	1	11 7	27.9	34.875	41.85	55.8	41.85	52.3125	62.775	83.7
280	0	1	0	0	0	1	1	0	0	0	11 8	28	35	42	56	42	52.5	63	84
281	0	1	0	0	0	1	1	0	0	1	11 9	28.1	35.125	42.15	56.2	42.15	52.6875	63.225	84.3
282	0	1	0	0	0	1	1	0	1	0	11 A	28.2	35.25	42.3	56.4	42.3	52.875	63.45	84.6
283	0	1	0	0	0	1	1	0	1	1	11 B	28.3	35.375	42.45	56.6	42.45	53.0625	63.675	84.9
284	0	1	0	0	0	1	1	1	0	0	11 C	28.4	35.5	42.6	56.8	42.6	53.25	63.9	85.2
285	0	1	0	0	0	1	1	1	0	1	11 D	28.5	35.625	42.75	57	42.75	53.4375	64.125	85.5
286	0	1	0	0	0	1	1	1	1	0	11 E	28.6	35.75	42.9	57.2	42.9	53.625	64.35	85.8
287	0	1	0	0	0	1	1	1	1	1	11 F	28.7	35.875	43.05	57.4	43.05	53.8125	64.575	86.1
288	0	1	0	0	1	0	0	0	0	0	12 0	28.8	36	43.2	57.6	43.2	54	64.8	86.4
289	0	1	0	0	1	0	0	0	0	1	12 1	28.9	36.125	43.35	57.8	43.35	54.1875	65.025	86.7
290	0	1	0	0	1	0	0	0	1	0	12 2	29	36.25	43.5	58	43.5	54.375	65.25	87
291	0	1	0	0	1	0	0	0	1	1	12 3	29.1	36.375	43.65	58.2	43.65	54.5625	65.475	87.3
292	0	1	0	0	1	0	0	1	0	0	12 4	29.2	36.5	43.8	58.4	43.8	54.75	65.7	87.6
293	0	1	0	0	1	0	0	1	0	1	12 5	29.3	36.625	43.95	58.6	43.95	54.9375	65.925	87.9
294	0	1	0	0	1	0	0	1	1	0	12 6	29.4	36.75	44.1	58.8	44.1	55.125	66.15	88.2
295	0	1	0	0	1	0	0	1	1	1	12 7	29.5	36.875	44.25	59	44.25	55.3125	66.375	88.5
296	0	1	0	0	1	0	1	0	0	0	12 8	29.6	37	44.4	59.2	44.4	55.5	66.6	88.8
297	0	1	0	0	1	0	1	0	0	1	12 9	29.7	37.125	44.55	59.4	44.55	55.6875	66.825	89.1
298	0	1	0	0	1	0	1	0	1	0	12 A	29.8	37.25	44.7	59.6	44.7	55.875	67.05	89.4

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
299	0	1	0	0	1	0	1	0	1	1	12 B	29.9	37.375	44.85	59.8	44.85	56.0625	67.275	89.7
300	0	1	0	0	1	0	1	1	0	0	12 C	30	37.5	45	60	45	56.25	67.5	90
301	0	1	0	0	1	0	1	1	0	1	12 D	30.1	37.625	45.15	60.2	45.15	56.4375	67.725	90.3
302	0	1	0	0	1	0	1	1	1	0	12 E	30.2	37.75	45.3	60.4	45.3	56.625	67.95	90.6
303	0	1	0	0	1	0	1	1	1	1	12 F	30.3	37.875	45.45	60.6	45.45	56.8125	68.175	90.9
304	0	1	0	0	1	1	0	0	0	0	13 0	30.4	38	45.6	60.8	45.6	57	68.4	91.2
305	0	1	0	0	1	1	0	0	0	1	13 1	30.5	38.125	45.75	61	45.75	57.1875	68.625	91.5
306	0	1	0	0	1	1	0	0	1	0	13 2	30.6	38.25	45.9	61.2	45.9	57.375	68.85	91.8
307	0	1	0	0	1	1	0	0	1	1	13 3	30.7	38.375	46.05	61.4	46.05	57.5625	69.075	92.1
308	0	1	0	0	1	1	0	1	0	0	13 4	30.8	38.5	46.2	61.6	46.2	57.75	69.3	92.4
309	0	1	0	0	1	1	0	1	0	1	13 5	30.9	38.625	46.35	61.8	46.35	57.9375	69.525	92.7
310	0	1	0	0	1	1	0	1	1	0	13 6	31	38.75	46.5	62	46.5	58.125	69.75	93
311	0	1	0	0	1	1	0	1	1	1	13 7	31.1	38.875	46.65	62.2	46.65	58.3125	69.975	93.3
312	0	1	0	0	1	1	1	0	0	0	13 8	31.2	39	46.8	62.4	46.8	58.5	70.2	93.6
313	0	1	0	0	1	1	1	0	0	1	13 9	31.3	39.125	46.95	62.6	46.95	58.6875	70.425	93.9
314	0	1	0	0	1	1	1	0	1	0	13 A	31.4	39.25	47.1	62.8	47.1	58.875	70.65	94.2
315	0	1	0	0	1	1	1	0	1	1	13 B	31.5	39.375	47.25	63	47.25	59.0625	70.875	94.5
316	0	1	0	0	1	1	1	1	0	0	13 C	31.6	39.5	47.4	63.2	47.4	59.25	71.1	94.8
317	0	1	0	0	1	1	1	1	0	1	13 D	31.7	39.625	47.55	63.4	47.55	59.4375	71.325	95.1
318	0	1	0	0	1	1	1	1	1	0	13 E	31.8	39.75	47.7	63.6	47.7	59.625	71.55	95.4
319	0	1	0	0	1	1	1	1	1	1	13 F	31.9	39.875	47.85	63.8	47.85	59.8125	71.775	95.7
"End of Message Storage Space for ISD2532, ISD2540, ISD2548, and ISD2564 Devices"																			

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
320	0	1	0	1	0	0	0	0	0	0	14 0	32	40	48	64	48	60	72	96
321	0	1	0	1	0	0	0	0	0	1	14 1	32.1	40.125	48.15	64.2	48.15	60.1875	72.225	96.3
322	0	1	0	1	0	0	0	0	1	0	14 2	32.2	40.25	48.3	64.4	48.3	60.375	72.45	96.6
323	0	1	0	1	0	0	0	0	1	1	14 3	32.3	40.375	48.45	64.6	48.45	60.5625	72.675	96.9
324	0	1	0	1	0	0	0	1	0	0	14 4	32.4	40.5	48.6	64.8	48.6	60.75	72.9	97.2
325	0	1	0	1	0	0	0	1	0	1	14 5	32.5	40.625	48.75	65	48.75	60.9375	73.125	97.5
326	0	1	0	1	0	0	0	1	1	0	14 6	32.6	40.75	48.9	65.2	48.9	61.125	73.35	97.8
327	0	1	0	1	0	0	0	1	1	1	14 7	32.7	40.875	49.05	65.4	49.05	61.3125	73.575	98.1

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
328	0	1	0	1	0	0	1	0	0	0	14 8	32.8	41	49.2	65.6	49.2	61.5	73.8	98.4
329	0	1	0	1	0	0	1	0	0	1	14 9	32.9	41.125	49.35	65.8	49.35	61.6875	74.025	98.7
330	0	1	0	1	0	0	1	0	1	0	14 A	33	41.25	49.5	66	49.5	61.875	74.25	99
331	0	1	0	1	0	0	1	0	1	1	14 B	33.1	41.375	49.65	66.2	49.65	62.0625	74.475	99.3
332	0	1	0	1	0	0	1	1	0	0	14 C	33.2	41.5	49.8	66.4	49.8	62.25	74.7	99.6
333	0	1	0	1	0	0	1	1	0	1	14 D	33.3	41.625	49.95	66.6	49.95	62.4375	74.925	99.9
334	0	1	0	1	0	0	1	1	1	0	14 E	33.4	41.75	50.1	66.8	50.1	62.625	75.15	100.2
335	0	1	0	1	0	0	1	1	1	1	14 F	33.5	41.875	50.25	67	50.25	62.8125	75.375	100.5
336	0	1	0	1	0	1	0	0	0	0	15 0	33.6	42	50.4	67.2	50.4	63	75.6	100.8
337	0	1	0	1	0	1	0	0	0	1	15 1	33.7	42.125	50.55	67.4	50.55	63.1875	75.825	101.1
338	0	1	0	1	0	1	0	0	1	0	15 2	33.8	42.25	50.7	67.6	50.7	63.375	76.05	101.4
339	0	1	0	1	0	1	0	0	1	1	15 3	33.9	42.375	50.85	67.8	50.85	63.5625	76.275	101.7
340	0	1	0	1	0	1	0	1	0	0	15 4	34	42.5	51	68	51	63.75	76.5	102
341	0	1	0	1	0	1	0	1	0	1	15 5	34.1	42.625	51.15	68.2	51.15	63.9375	76.725	102.3
342	0	1	0	1	0	1	0	1	1	0	15 6	34.2	42.75	51.3	68.4	51.3	64.125	76.95	102.6
343	0	1	0	1	0	1	0	1	1	1	15 7	34.3	42.875	51.45	68.6	51.45	64.3125	77.175	102.9
344	0	1	0	1	0	1	1	0	0	0	15 8	34.4	43	51.6	68.8	51.6	64.5	77.4	103.2
345	0	1	0	1	0	1	1	0	0	1	15 9	34.5	43.125	51.75	69	51.75	64.6875	77.625	103.5
346	0	1	0	1	0	1	1	0	1	0	15 A	34.6	43.25	51.9	69.2	51.9	64.875	77.85	103.8
347	0	1	0	1	0	1	1	0	1	1	15 B	34.7	43.375	52.05	69.4	52.05	65.0625	78.075	104.1
348	0	1	0	1	0	1	1	1	0	0	15 C	34.8	43.5	52.2	69.6	52.2	65.25	78.3	104.4
349	0	1	0	1	0	1	1	1	0	1	15 D	34.9	43.625	52.35	69.8	52.35	65.4375	78.525	104.7
350	0	1	0	1	0	1	1	1	1	0	15 E	35	43.75	52.5	70	52.5	65.625	78.75	105
351	0	1	0	1	0	1	1	1	1	1	15 F	35.1	43.875	52.65	70.2	52.65	65.8125	78.975	105.3
352	0	1	0	1	1	0	0	0	0	0	16 0	35.2	44	52.8	70.4	52.8	66	79.2	105.6
353	0	1	0	1	1	0	0	0	0	1	16 1	35.3	44.125	52.95	70.6	52.95	66.1875	79.425	105.9
354	0	1	0	1	1	0	0	0	1	0	16 2	35.4	44.25	53.1	70.8	53.1	66.375	79.65	106.2
355	0	1	0	1	1	0	0	0	1	1	16 3	35.5	44.375	53.25	71	53.25	66.5625	79.875	106.5
356	0	1	0	1	1	0	0	1	0	0	16 4	35.6	44.5	53.4	71.2	53.4	66.75	80.1	106.8
357	0	1	0	1	1	0	0	1	0	1	16 5	35.7	44.625	53.55	71.4	53.55	66.9375	80.325	107.1
358	0	1	0	1	1	0	0	1	1	0	16 6	35.8	44.75	53.7	71.6	53.7	67.125	80.55	107.4
359	0	1	0	1	1	0	0	1	1	1	16 7	35.9	44.875	53.85	71.8	53.85	67.3125	80.775	107.7
360	0	1	0	1	1	0	1	0	0	0	16 8	36	45	54	72	54	67.5	81	108
361	0	1	0	1	1	0	1	0	0	1	16 9	36.1	45.125	54.15	72.2	54.15	67.6875	81.225	108.3
362	0	1	0	1	1	0	1	0	1	0	16 A	36.2	45.25	54.3	72.4	54.3	67.875	81.45	108.6
363	0	1	0	1	1	0	1	0	1	1	16 B	36.3	45.375	54.45	72.6	54.45	68.0625	81.675	108.9
364	0	1	0	1	1	0	1	1	0	0	16 C	36.4	45.5	54.6	72.8	54.6	68.25	81.9	109.2
365	0	1	0	1	1	0	1	1	0	1	16 D	36.5	45.625	54.75	73	54.75	68.4375	82.125	109.5

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
366	0	1	0	1	1	0	1	1	1	0	16 E	36.6	45.75	54.9	73.2	54.9	68.625	82.35	109.8
367	0	1	0	1	1	0	1	1	1	1	16 F	36.7	45.875	55.05	73.4	55.05	68.8125	82.575	110.1
368	0	1	0	1	1	1	0	0	0	0	17 0	36.8	46	55.2	73.6	55.2	69	82.8	110.4
369	0	1	0	1	1	1	0	0	0	1	17 1	36.9	46.125	55.35	73.8	55.35	69.1875	83.025	110.7
370	0	1	0	1	1	1	0	0	1	0	17 2	37	46.25	55.5	74	55.5	69.375	83.25	111
371	0	1	0	1	1	1	0	0	1	1	17 3	37.1	46.375	55.65	74.2	55.65	69.5625	83.475	111.3
372	0	1	0	1	1	1	0	1	0	0	17 4	37.2	46.5	55.8	74.4	55.8	69.75	83.7	111.6
373	0	1	0	1	1	1	0	1	0	1	17 5	37.3	46.625	55.95	74.6	55.95	69.9375	83.925	111.9
374	0	1	0	1	1	1	0	1	1	0	17 6	37.4	46.75	56.1	74.8	56.1	70.125	84.15	112.2
375	0	1	0	1	1	1	0	1	1	1	17 7	37.5	46.875	56.25	75	56.25	70.3125	84.375	112.5
376	0	1	0	1	1	1	1	0	0	0	17 8	37.6	47	56.4	75.2	56.4	70.5	84.6	112.8
377	0	1	0	1	1	1	1	0	0	1	17 9	37.7	47.125	56.55	75.4	56.55	70.6875	84.825	113.1
378	0	1	0	1	1	1	1	0	1	0	17 A	37.8	47.25	56.7	75.6	56.7	70.875	85.05	113.4
379	0	1	0	1	1	1	1	0	1	1	17 B	37.9	47.375	56.85	75.8	56.85	71.0625	85.275	113.7
380	0	1	0	1	1	1	1	1	0	0	17 C	38	47.5	57	76	57	71.25	85.5	114
381	0	1	0	1	1	1	1	1	0	1	17 D	38.1	47.625	57.15	76.2	57.15	71.4375	85.725	114.3
382	0	1	0	1	1	1	1	1	1	0	17 E	38.2	47.75	57.3	76.4	57.3	71.625	85.95	114.6
383	0	1	0	1	1	1	1	1	1	1	17 F	38.3	47.875	57.45	76.6	57.45	71.8125	86.175	114.9
384	0	1	1	0	0	0	0	0	0	0	18 0	38.4	48	57.6	76.8	57.6	72	86.4	115.2
385	0	1	1	0	0	0	0	0	0	1	18 1	38.5	48.125	57.75	77	57.75	72.1875	86.625	115.5
386	0	1	1	0	0	0	0	0	1	0	18 2	38.6	48.25	57.9	77.2	57.9	72.375	86.85	115.8
387	0	1	1	0	0	0	0	0	1	1	18 3	38.7	48.375	58.05	77.4	58.05	72.5625	87.075	116.1
388	0	1	1	0	0	0	0	1	0	0	18 4	38.8	48.5	58.2	77.6	58.2	72.75	87.3	116.4
389	0	1	1	0	0	0	0	1	0	1	18 5	38.9	48.625	58.35	77.8	58.35	72.9375	87.525	116.7
390	0	1	1	0	0	0	0	1	1	0	18 6	39	48.75	58.5	78	58.5	73.125	87.75	117
391	0	1	1	0	0	0	0	1	1	1	18 7	39.1	48.875	58.65	78.2	58.65	73.3125	87.975	117.3
392	0	1	1	0	0	0	1	0	0	0	18 8	39.2	49	58.8	78.4	58.8	73.5	88.2	117.6
393	0	1	1	0	0	0	1	0	0	1	18 9	39.3	49.125	58.95	78.6	58.95	73.6875	88.425	117.9
394	0	1	1	0	0	0	1	0	1	0	18 A	39.4	49.25	59.1	78.8	59.1	73.875	88.65	118.2
395	0	1	1	0	0	0	1	0	1	1	18 B	39.5	49.375	59.25	79	59.25	74.0625	88.875	118.5
396	0	1	1	0	0	0	1	1	0	0	18 C	39.6	49.5	59.4	79.2	59.4	74.25	89.1	118.8
397	0	1	1	0	0	0	1	1	0	1	18 D	39.7	49.625	59.55	79.4	59.55	74.4375	89.325	119.1
398	0	1	1	0	0	0	1	1	1	0	18 E	39.8	49.75	59.7	79.6	59.7	74.625	89.55	119.4
399	0	1	1	0	0	0	1	1	1	1	18 F	39.9	49.875	59.85	79.8	59.85	74.8125	89.775	119.7
"End of Message Storage Space for ISD33060, ISD33075, ISD33090, and ISD33120-4 Devices"																			

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
400	0	1	1	0	0	1	0	0	0	0	19 0	40	50	60	80	60	75	90	120
401	0	1	1	0	0	1	0	0	0	1	19 1	40.1	50.125	60.15	80.2	60.15	75.1875	90.225	120.3
402	0	1	1	0	0	1	0	0	1	0	19 2	40.2	50.25	60.3	80.4	60.3	75.375	90.45	120.6
403	0	1	1	0	0	1	0	0	1	1	19 3	40.3	50.375	60.45	80.6	60.45	75.5625	90.675	120.9
404	0	1	1	0	0	1	0	1	0	0	19 4	40.4	50.5	60.6	80.8	60.6	75.75	90.9	121.2
405	0	1	1	0	0	1	0	1	0	1	19 5	40.5	50.625	60.75	81	60.75	75.9375	91.125	121.5
406	0	1	1	0	0	1	0	1	1	0	19 6	40.6	50.75	60.9	81.2	60.9	76.125	91.35	121.8
407	0	1	1	0	0	1	0	1	1	1	19 7	40.7	50.875	61.05	81.4	61.05	76.3125	91.575	122.1
408	0	1	1	0	0	1	1	0	0	0	19 8	40.8	51	61.2	81.6	61.2	76.5	91.8	122.4
409	0	1	1	0	0	1	1	0	0	1	19 9	40.9	51.125	61.35	81.8	61.35	76.6875	92.025	122.7
410	0	1	1	0	0	1	1	0	1	0	19 A	41	51.25	61.5	82	61.5	76.875	92.25	123
411	0	1	1	0	0	1	1	0	1	1	19 B	41.1	51.375	61.65	82.2	61.65	77.0625	92.475	123.3
412	0	1	1	0	0	1	1	1	0	0	19 C	41.2	51.5	61.8	82.4	61.8	77.25	92.7	123.6
413	0	1	1	0	0	1	1	1	0	1	19 D	41.3	51.625	61.95	82.6	61.95	77.4375	92.925	123.9
414	0	1	1	0	0	1	1	1	1	0	19 E	41.4	51.75	62.1	82.8	62.1	77.625	93.15	124.2
415	0	1	1	0	0	1	1	1	1	1	19 F	41.5	51.875	62.25	83	62.25	77.8125	93.375	124.5
416	0	1	1	0	1	0	0	0	0	0	1A 0	41.6	52	62.4	83.2	62.4	78	93.6	124.8
417	0	1	1	0	1	0	0	0	0	1	1A 1	41.7	52.125	62.55	83.4	62.55	78.1875	93.825	125.1
418	0	1	1	0	1	0	0	0	1	0	1A 2	41.8	52.25	62.7	83.6	62.7	78.375	94.05	125.4
419	0	1	1	0	1	0	0	0	1	1	1A 3	41.9	52.375	62.85	83.8	62.85	78.5625	94.275	125.7
420	0	1	1	0	1	0	0	1	0	0	1A 4	42	52.5	63	84	63	78.75	94.5	126
421	0	1	1	0	1	0	0	1	0	1	1A 5	42.1	52.625	63.15	84.2	63.15	78.9375	94.725	126.3
422	0	1	1	0	1	0	0	1	1	0	1A 6	42.2	52.75	63.3	84.4	63.3	79.125	94.95	126.6
423	0	1	1	0	1	0	0	1	1	1	1A 7	42.3	52.875	63.45	84.6	63.45	79.3125	95.175	126.9
424	0	1	1	0	1	0	1	0	0	0	1A 8	42.4	53	63.6	84.8	63.6	79.5	95.4	127.2
425	0	1	1	0	1	0	1	0	0	1	1A 9	42.5	53.125	63.75	85	63.75	79.6875	95.625	127.5
426	0	1	1	0	1	0	1	0	1	0	1A A	42.6	53.25	63.9	85.2	63.9	79.875	95.85	127.8
427	0	1	1	0	1	0	1	0	1	1	1A B	42.7	53.375	64.05	85.4	64.05	80.0625	96.075	128.1
428	0	1	1	0	1	0	1	1	0	0	1A C	42.8	53.5	64.2	85.6	64.2	80.25	96.3	128.4
429	0	1	1	0	1	0	1	1	0	1	1A D	42.9	53.625	64.35	85.8	64.35	80.4375	96.525	128.7
430	0	1	1	0	1	0	1	1	1	0	1A E	43	53.75	64.5	86	64.5	80.625	96.75	129
431	0	1	1	0	1	0	1	1	1	1	1A F	43.1	53.875	64.65	86.2	64.65	80.8125	96.975	129.3
432	0	1	1	0	1	1	0	0	0	0	1B 0	43.2	54	64.8	86.4	64.8	81	97.2	129.6
433	0	1	1	0	1	1	0	0	0	1	1B 1	43.3	54.125	64.95	86.6	64.95	81.1875	97.425	129.9
434	0	1	1	0	1	1	0	0	1	0	1B 2	43.4	54.25	65.1	86.8	65.1	81.375	97.65	130.2
435	0	1	1	0	1	1	0	0	1	1	1B 3	43.5	54.375	65.25	87	65.25	81.5625	97.875	130.5
436	0	1	1	0	1	1	0	1	0	0	1B 4	43.6	54.5	65.4	87.2	65.4	81.75	98.1	130.8
437	0	1	1	0	1	1	0	1	0	1	1B 5	43.7	54.625	65.55	87.4	65.55	81.9375	98.325	131.1

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
438	0	1	1	0	1	1	0	1	1	0	1B 6	43.8	54.75	65.7	87.6	65.7	82.125	98.55	131.4
439	0	1	1	0	1	1	0	1	1	1	1B 7	43.9	54.875	65.85	87.8	65.85	82.3125	98.775	131.7
440	0	1	1	0	1	1	1	0	0	0	1B 8	44	55	66	88	66	82.5	99	132
441	0	1	1	0	1	1	1	0	0	1	1B 9	44.1	55.125	66.15	88.2	66.15	82.6875	99.225	132.3
442	0	1	1	0	1	1	1	0	1	0	1B A	44.2	55.25	66.3	88.4	66.3	82.875	99.45	132.6
443	0	1	1	0	1	1	1	0	1	1	1B B	44.3	55.375	66.45	88.6	66.45	83.0625	99.675	132.9
444	0	1	1	0	1	1	1	1	0	0	1B C	44.4	55.5	66.6	88.8	66.6	83.25	99.9	133.2
445	0	1	1	0	1	1	1	1	0	1	1B D	44.5	55.625	66.75	89	66.75	83.4375	100.125	133.5
446	0	1	1	0	1	1	1	1	1	0	1B E	44.6	55.75	66.9	89.2	66.9	83.625	100.35	133.8
447	0	1	1	0	1	1	1	1	1	1	1B F	44.7	55.875	67.05	89.4	67.05	83.8125	100.575	134.1
448	0	1	1	1	0	0	0	0	0	0	1C 0	44.8	56	67.2	89.6	67.2	84	100.8	134.4
449	0	1	1	1	0	0	0	0	0	1	1C 1	44.9	56.125	67.35	89.8	67.35	84.1875	101.025	134.7
450	0	1	1	1	0	0	0	0	1	0	1C 2	45	56.25	67.5	90	67.5	84.375	101.25	135
451	0	1	1	1	0	0	0	0	1	1	1C 3	45.1	56.375	67.65	90.2	67.65	84.5625	101.475	135.3
452	0	1	1	1	0	0	0	1	0	0	1C 4	45.2	56.5	67.8	90.4	67.8	84.75	101.7	135.6
453	0	1	1	1	0	0	0	1	0	1	1C 5	45.3	56.625	67.95	90.6	67.95	84.9375	101.925	135.9
454	0	1	1	1	0	0	0	1	1	0	1C 6	45.4	56.75	68.1	90.8	68.1	85.125	102.15	136.2
455	0	1	1	1	0	0	0	1	1	1	1C 7	45.5	56.875	68.25	91	68.25	85.3125	102.375	136.5
456	0	1	1	1	0	0	1	0	0	0	1C 8	45.6	57	68.4	91.2	68.4	85.5	102.6	136.8
457	0	1	1	1	0	0	1	0	0	1	1C 9	45.7	57.125	68.55	91.4	68.55	85.6875	102.825	137.1
458	0	1	1	1	0	0	1	0	1	0	1C A	45.8	57.25	68.7	91.6	68.7	85.875	103.05	137.4
459	0	1	1	1	0	0	1	0	1	1	1C B	45.9	57.375	68.85	91.8	68.85	86.0625	103.275	137.7
460	0	1	1	1	0	0	1	1	0	0	1C C	46	57.5	69	92	69	86.25	103.5	138
461	0	1	1	1	0	0	1	1	0	1	1C D	46.1	57.625	69.15	92.2	69.15	86.4375	103.725	138.3
462	0	1	1	1	0	0	1	1	1	0	1C E	46.2	57.75	69.3	92.4	69.3	86.625	103.95	138.6
463	0	1	1	1	0	0	1	1	1	1	1C F	46.3	57.875	69.45	92.6	69.45	86.8125	104.175	138.9
464	0	1	1	1	0	1	0	0	0	0	1D 0	46.4	58	69.6	92.8	69.6	87	104.4	139.2
465	0	1	1	1	0	1	0	0	0	1	1D 1	46.5	58.125	69.75	93	69.75	87.1875	104.625	139.5
466	0	1	1	1	0	1	0	0	1	0	1D 2	46.6	58.25	69.9	93.2	69.9	87.375	104.85	139.8
467	0	1	1	1	0	1	0	0	1	1	1D 3	46.7	58.375	70.05	93.4	70.05	87.5625	105.075	140.1
468	0	1	1	1	0	1	0	1	0	0	1D 4	46.8	58.5	70.2	93.6	70.2	87.75	105.3	140.4
469	0	1	1	1	0	1	0	1	0	1	1D 5	46.9	58.625	70.35	93.8	70.35	87.9375	105.525	140.7
470	0	1	1	1	0	1	0	1	1	0	1D 6	47	58.75	70.5	94	70.5	88.125	105.75	141
471	0	1	1	1	0	1	0	1	1	1	1D 7	47.1	58.875	70.65	94.2	70.65	88.3125	105.975	141.3
472	0	1	1	1	0	1	1	0	0	0	1D 8	47.2	59	70.8	94.4	70.8	88.5	106.2	141.6
473	0	1	1	1	0	1	1	0	0	1	1D 9	47.3	59.125	70.95	94.6	70.95	88.6875	106.425	141.9
474	0	1	1	1	0	1	1	0	1	0	1D A	47.4	59.25	71.1	94.8	71.1	88.875	106.65	142.2
475	0	1	1	1	0	1	1	0	1	1	1D B	47.5	59.375	71.25	95	71.25	89.0625	106.875	142.5
476	0	1	1	1	0	1	1	1	0	0	1D C	47.6	59.5	71.4	95.2	71.4	89.25	107.1	142.8

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
477	0	1	1	1	0	1	1	1	0	1	1D D	47.7	59.625	71.55	95.4	71.55	89.4375	107.325	143.1
478	0	1	1	1	0	1	1	1	1	0	1D E	47.8	59.75	71.7	95.6	71.7	89.625	107.55	143.4
479	0	1	1	1	0	1	1	1	1	1	1D F	47.9	59.875	71.85	95.8	71.85	89.8125	107.775	143.7
480	0	1	1	1	1	0	0	0	0	0	1E 0	48	60	72	96	72	90	108	144
481	0	1	1	1	1	0	0	0	0	1	1E 1	48.1	60.125	72.15	96.2	72.15	90.1875	108.225	144.3
482	0	1	1	1	1	0	0	0	1	0	1E 2	48.2	60.25	72.3	96.4	72.3	90.375	108.45	144.6
483	0	1	1	1	1	0	0	0	1	1	1E 3	48.3	60.375	72.45	96.6	72.45	90.5625	108.675	144.9
484	0	1	1	1	1	0	0	1	0	0	1E 4	48.4	60.5	72.6	96.8	72.6	90.75	108.9	145.2
485	0	1	1	1	1	0	0	1	0	1	1E 5	48.5	60.625	72.75	97	72.75	90.9375	109.125	145.5
486	0	1	1	1	1	0	0	1	1	0	1E 6	48.6	60.75	72.9	97.2	72.9	91.125	109.35	145.8
487	0	1	1	1	1	0	0	1	1	1	1E 7	48.7	60.875	73.05	97.4	73.05	91.3125	109.575	146.1
488	0	1	1	1	1	0	1	0	0	0	1E 8	48.8	61	73.2	97.6	73.2	91.5	109.8	146.4
489	0	1	1	1	1	0	1	0	0	1	1E 9	48.9	61.125	73.35	97.8	73.35	91.6875	110.025	146.7
490	0	1	1	1	1	0	1	0	1	0	1E A	49	61.25	73.5	98	73.5	91.875	110.25	147
491	0	1	1	1	1	0	1	0	1	1	1E B	49.1	61.375	73.65	98.2	73.65	92.0625	110.475	147.3
492	0	1	1	1	1	0	1	1	0	0	1E C	49.2	61.5	73.8	98.4	73.8	92.25	110.7	147.6
493	0	1	1	1	1	0	1	1	0	1	1E D	49.3	61.625	73.95	98.6	73.95	92.4375	110.925	147.9
494	0	1	1	1	1	0	1	1	1	0	1E E	49.4	61.75	74.1	98.8	74.1	92.625	111.15	148.2
495	0	1	1	1	1	0	1	1	1	1	1E F	49.5	61.875	74.25	99	74.25	92.8125	111.375	148.5
496	0	1	1	1	1	1	0	0	0	0	1F 0	49.6	62	74.4	99.2	74.4	93	111.6	148.8
497	0	1	1	1	1	1	0	0	0	1	1F 1	49.7	62.125	74.55	99.4	74.55	93.1875	111.825	149.1
498	0	1	1	1	1	1	0	0	1	0	1F 2	49.8	62.25	74.7	99.6	74.7	93.375	112.05	149.4
499	0	1	1	1	1	1	0	0	1	1	1F 3	49.9	62.375	74.85	99.8	74.85	93.5625	112.275	149.7
500	0	1	1	1	1	1	0	1	0	0	1F 4	50	62.5	75	100	75	93.75	112.5	150
501	0	1	1	1	1	1	0	1	0	1	1F 5	50.1	62.625	75.15	100.2	75.15	93.9375	112.725	150.3
502	0	1	1	1	1	1	0	1	1	0	1F 6	50.2	62.75	75.3	100.4	75.3	94.125	112.95	150.6
503	0	1	1	1	1	1	0	1	1	1	1F 7	50.3	62.875	75.45	100.6	75.45	94.3125	113.175	150.9
504	0	1	1	1	1	1	1	0	0	0	1F 8	50.4	63	75.6	100.8	75.6	94.5	113.4	151.2
505	0	1	1	1	1	1	1	0	0	1	1F 9	50.5	63.125	75.75	101	75.75	94.6875	113.625	151.5
506	0	1	1	1	1	1	1	0	1	0	1F A	50.6	63.25	75.9	101.2	75.9	94.875	113.85	151.8
507	0	1	1	1	1	1	1	0	1	1	1F B	50.7	63.375	76.05	101.4	76.05	95.0625	114.075	152.1
508	0	1	1	1	1	1	1	1	0	0	1F C	50.8	63.5	76.2	101.6	76.2	95.25	114.3	152.4
509	0	1	1	1	1	1	1	1	0	1	1F D	50.9	63.625	76.35	101.8	76.35	95.4375	114.525	152.7
510	0	1	1	1	1	1	1	1	1	0	1F E	51	63.75	76.5	102	76.5	95.625	114.75	153
511	0	1	1	1	1	1	1	1	1	1	1F F	51.1	63.875	76.65	102.2	76.65	95.8125	114.975	153.3
512	1	0	0	0	0	0	0	0	0	0	20 0	51.2	64	76.8	102.4	76.8	96	115.2	153.6
513	1	0	0	0	0	0	0	0	0	1	20 1	51.3	64.125	76.95	102.6	76.95	96.1875	115.425	153.9
514	1	0	0	0	0	0	0	0	1	0	20 2	51.4	64.25	77.1	102.8	77.1	96.375	115.65	154.2

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
515	1	0	0	0	0	0	0	0	1	1	20 3	51.5	64.375	77.25	103	77.25	96.5625	115.875	154.5
516	1	0	0	0	0	0	0	1	0	0	20 4	51.6	64.5	77.4	103.2	77.4	96.75	116.1	154.8
517	1	0	0	0	0	0	0	1	0	1	20 5	51.7	64.625	77.55	103.4	77.55	96.9375	116.325	155.1
518	1	0	0	0	0	0	0	1	1	0	20 6	51.8	64.75	77.7	103.6	77.7	97.125	116.55	155.4
519	1	0	0	0	0	0	0	1	1	1	20 7	51.9	64.875	77.85	103.8	77.85	97.3125	116.775	155.7
520	1	0	0	0	0	0	1	0	0	0	20 8	52	65	78	104	78	97.5	117	156
521	1	0	0	0	0	0	1	0	0	1	20 9	52.1	65.125	78.15	104.2	78.15	97.6875	117.225	156.3
522	1	0	0	0	0	0	1	0	1	0	20 A	52.2	65.25	78.3	104.4	78.3	97.875	117.45	156.6
523	1	0	0	0	0	0	1	0	1	1	20 B	52.3	65.375	78.45	104.6	78.45	98.0625	117.675	156.9
524	1	0	0	0	0	0	1	1	0	0	20 C	52.4	65.5	78.6	104.8	78.6	98.25	117.9	157.2
525	1	0	0	0	0	0	1	1	0	1	20 D	52.5	65.625	78.75	105	78.75	98.4375	118.125	157.5
526	1	0	0	0	0	0	1	1	1	0	20 E	52.6	65.75	78.9	105.2	78.9	98.625	118.35	157.8
527	1	0	0	0	0	0	1	1	1	1	20 F	52.7	65.875	79.05	105.4	79.05	98.8125	118.575	158.1
528	1	0	0	0	0	1	0	0	0	0	21 0	52.8	66	79.2	105.6	79.2	99	118.8	158.4
529	1	0	0	0	0	1	0	0	0	1	21 1	52.9	66.125	79.35	105.8	79.35	99.1875	119.025	158.7
530	1	0	0	0	0	1	0	0	1	0	21 2	53	66.25	79.5	106	79.5	99.375	119.25	159
531	1	0	0	0	0	1	0	0	1	1	21 3	53.1	66.375	79.65	106.2	79.65	99.5625	119.475	159.3
532	1	0	0	0	0	1	0	1	0	0	21 4	53.2	66.5	79.8	106.4	79.8	99.75	119.7	159.6
533	1	0	0	0	0	1	0	1	0	1	21 5	53.3	66.625	79.95	106.6	79.95	99.9375	119.925	159.9
534	1	0	0	0	0	1	0	1	1	0	21 6	53.4	66.75	80.1	106.8	80.1	100.125	120.15	160.2
535	1	0	0	0	0	1	0	1	1	1	21 7	53.5	66.875	80.25	107	80.25	100.3125	120.375	160.5
536	1	0	0	0	0	1	1	0	0	0	21 8	53.6	67	80.4	107.2	80.4	100.5	120.6	160.8
537	1	0	0	0	0	1	1	0	0	1	21 9	53.7	67.125	80.55	107.4	80.55	100.6875	120.825	161.1
538	1	0	0	0	0	1	1	0	1	0	21 A	53.8	67.25	80.7	107.6	80.7	100.875	121.05	161.4
539	1	0	0	0	0	1	1	0	1	1	21 B	53.9	67.375	80.85	107.8	80.85	101.0625	121.275	161.7
540	1	0	0	0	0	1	1	1	0	0	21 C	54	67.5	81	108	81	101.25	121.5	162
541	1	0	0	0	0	1	1	1	0	1	21 D	54.1	67.625	81.15	108.2	81.15	101.4375	121.725	162.3
542	1	0	0	0	0	1	1	1	1	0	21 E	54.2	67.75	81.3	108.4	81.3	101.625	121.95	162.6
543	1	0	0	0	0	1	1	1	1	1	21 F	54.3	67.875	81.45	108.6	81.45	101.8125	122.175	162.9
544	1	0	0	0	1	0	0	0	0	0	22 0	54.4	68	81.6	108.8	81.6	102	122.4	163.2
545	1	0	0	0	1	0	0	0	0	1	22 1	54.5	68.125	81.75	109	81.75	102.1875	122.625	163.5
546	1	0	0	0	1	0	0	0	1	0	22 2	54.6	68.25	81.9	109.2	81.9	102.375	122.85	163.8
547	1	0	0	0	1	0	0	0	1	1	22 3	54.7	68.375	82.05	109.4	82.05	102.5625	123.075	164.1
548	1	0	0	0	1	0	0	1	0	0	22 4	54.8	68.5	82.2	109.6	82.2	102.75	123.3	164.4
549	1	0	0	0	1	0	0	1	0	1	22 5	54.9	68.625	82.35	109.8	82.35	102.9375	123.525	164.7
550	1	0	0	0	1	0	0	1	1	0	22 6	55	68.75	82.5	110	82.5	103.125	123.75	165
551	1	0	0	0	1	0	0	1	1	1	22 7	55.1	68.875	82.65	110.2	82.65	103.3125	123.975	165.3
552	1	0	0	0	1	0	1	0	0	0	22 8	55.2	69	82.8	110.4	82.8	103.5	124.2	165.6
553	1	0	0	0	1	0	1	0	0	1	22 9	55.3	69.125	82.95	110.6	82.95	103.6875	124.425	165.9

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
554	1	0	0	0	1	0	1	0	1	0	22 A	55.4	69.25	83.1	110.8	83.1	103.875	124.65	166.2
555	1	0	0	0	1	0	1	0	1	1	22 B	55.5	69.375	83.25	111	83.25	104.0625	124.875	166.5
556	1	0	0	0	1	0	1	1	0	0	22 C	55.6	69.5	83.4	111.2	83.4	104.25	125.1	166.8
557	1	0	0	0	1	0	1	1	0	1	22 D	55.7	69.625	83.55	111.4	83.55	104.4375	125.325	167.1
558	1	0	0	0	1	0	1	1	1	0	22 E	55.8	69.75	83.7	111.6	83.7	104.625	125.55	167.4
559	1	0	0	0	1	0	1	1	1	1	22 F	55.9	69.875	83.85	111.8	83.85	104.8125	125.775	167.7
560	1	0	0	0	1	1	0	0	0	0	23 0	56	70	84	112	84	105	126	168
561	1	0	0	0	1	1	0	0	0	1	23 1	56.1	70.125	84.15	112.2	84.15	105.1875	126.225	168.3
562	1	0	0	0	1	1	0	0	1	0	23 2	56.2	70.25	84.3	112.4	84.3	105.375	126.45	168.6
563	1	0	0	0	1	1	0	0	1	1	23 3	56.3	70.375	84.45	112.6	84.45	105.5625	126.675	168.9
564	1	0	0	0	1	1	0	1	0	0	23 4	56.4	70.5	84.6	112.8	84.6	105.75	126.9	169.2
565	1	0	0	0	1	1	0	1	0	1	23 5	56.5	70.625	84.75	113	84.75	105.9375	127.125	169.5
566	1	0	0	0	1	1	0	1	1	0	23 6	56.6	70.75	84.9	113.2	84.9	106.125	127.35	169.8
567	1	0	0	0	1	1	0	1	1	1	23 7	56.7	70.875	85.05	113.4	85.05	106.3125	127.575	170.1
568	1	0	0	0	1	1	1	0	0	0	23 8	56.8	71	85.2	113.6	85.2	106.5	127.8	170.4
569	1	0	0	0	1	1	1	0	0	1	23 9	56.9	71.125	85.35	113.8	85.35	106.6875	128.025	170.7
570	1	0	0	0	1	1	1	0	1	0	23 A	57	71.25	85.5	114	85.5	106.875	128.25	171
571	1	0	0	0	1	1	1	0	1	1	23 B	57.1	71.375	85.65	114.2	85.65	107.0625	128.475	171.3
572	1	0	0	0	1	1	1	1	0	0	23 C	57.2	71.5	85.8	114.4	85.8	107.25	128.7	171.6
573	1	0	0	0	1	1	1	1	0	1	23 D	57.3	71.625	85.95	114.6	85.95	107.4375	128.925	171.9
574	1	0	0	0	1	1	1	1	1	0	23 E	57.4	71.75	86.1	114.8	86.1	107.625	129.15	172.2
575	1	0	0	0	1	1	1	1	1	1	23 F	57.5	71.875	86.25	115	86.25	107.8125	129.375	172.5
576	1	0	0	1	0	0	0	0	0	0	24 0	57.6	72	86.4	115.2	86.4	108	129.6	172.8
577	1	0	0	1	0	0	0	0	0	1	24 1	57.7	72.125	86.55	115.4	86.55	108.1875	129.825	173.1
578	1	0	0	1	0	0	0	0	1	0	24 2	57.8	72.25	86.7	115.6	86.7	108.375	130.05	173.4
579	1	0	0	1	0	0	0	0	1	1	24 3	57.9	72.375	86.85	115.8	86.85	108.5625	130.275	173.7
580	1	0	0	1	0	0	0	1	0	0	24 4	58	72.5	87	116	87	108.75	130.5	174
581	1	0	0	1	0	0	0	1	0	1	24 5	58.1	72.625	87.15	116.2	87.15	108.9375	130.725	174.3
582	1	0	0	1	0	0	0	1	1	0	24 6	58.2	72.75	87.3	116.4	87.3	109.125	130.95	174.6
583	1	0	0	1	0	0	0	1	1	1	24 7	58.3	72.875	87.45	116.6	87.45	109.3125	131.175	174.9
584	1	0	0	1	0	0	1	0	0	0	24 8	58.4	73	87.6	116.8	87.6	109.5	131.4	175.2
585	1	0	0	1	0	0	1	0	0	1	24 9	58.5	73.125	87.75	117	87.75	109.6875	131.625	175.5
586	1	0	0	1	0	0	1	0	1	0	24 A	58.6	73.25	87.9	117.2	87.9	109.875	131.85	175.8
587	1	0	0	1	0	0	1	0	1	1	24 B	58.7	73.375	88.05	117.4	88.05	110.0625	132.075	176.1
588	1	0	0	1	0	0	1	1	0	0	24 C	58.8	73.5	88.2	117.6	88.2	110.25	132.3	176.4
589	1	0	0	1	0	0	1	1	0	1	24 D	58.9	73.625	88.35	117.8	88.35	110.4375	132.525	176.7
590	1	0	0	1	0	0	1	1	1	0	24 E	59	73.75	88.5	118	88.5	110.625	132.75	177
591	1	0	0	1	0	0	1	1	1	1	24 F	59.1	73.875	88.65	118.2	88.65	110.8125	132.975	177.3

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
592	1	0	0	1	0	1	0	0	0	0	25 0	59.2	74	88.8	118.4	88.8	111	133.2	177.6
593	1	0	0	1	0	1	0	0	0	1	25 1	59.3	74.125	88.95	118.6	88.95	111.1875	133.425	177.9
594	1	0	0	1	0	1	0	0	1	0	25 2	59.4	74.25	89.1	118.8	89.1	111.375	133.65	178.2
595	1	0	0	1	0	1	0	0	1	1	25 3	59.5	74.375	89.25	119	89.25	111.5625	133.875	178.5
596	1	0	0	1	0	1	0	1	0	0	25 4	59.6	74.5	89.4	119.2	89.4	111.75	134.1	178.8
597	1	0	0	1	0	1	0	1	0	1	25 5	59.7	74.625	89.55	119.4	89.55	111.9375	134.325	179.1
598	1	0	0	1	0	1	0	1	1	0	25 6	59.8	74.75	89.7	119.6	89.7	112.125	134.55	179.4
599	1	0	0	1	0	1	0	1	1	1	25 7	59.9	74.875	89.85	119.8	89.85	112.3125	134.775	179.7
"End of Message Storage Space for ISD2560, ISD2575, ISD2590, and ISD25120 Devices"																			

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
600	1	0	0	1	0	1	1	0	0	0	25 8					90	112.5	135	180
601	1	0	0	1	0	1	1	0	0	1	25 9					90.15	112.6875	135.225	180.3
602	1	0	0	1	0	1	1	0	1	0	25 A					90.3	112.875	135.45	180.6
603	1	0	0	1	0	1	1	0	1	1	25 B					90.45	113.0625	135.675	180.9
604	1	0	0	1	0	1	1	1	0	0	25 C					90.6	113.25	135.9	181.2
605	1	0	0	1	0	1	1	1	0	1	25 D					90.75	113.4375	136.125	181.5
606	1	0	0	1	0	1	1	1	1	0	25 E					90.9	113.625	136.35	181.8
607	1	0	0	1	0	1	1	1	1	1	25 F					91.05	113.8125	136.575	182.1
608	1	0	0	1	1	0	0	0	0	0	26 0					91.2	114	136.8	182.4
609	1	0	0	1	1	0	0	0	0	1	26 1					91.35	114.1875	137.025	182.7
610	1	0	0	1	1	0	0	0	1	0	26 2					91.5	114.375	137.25	183
611	1	0	0	1	1	0	0	0	1	1	26 3					91.65	114.5625	137.475	183.3
612	1	0	0	1	1	0	0	1	0	0	26 4					91.8	114.75	137.7	183.6
613	1	0	0	1	1	0	0	1	0	1	26 5					91.95	114.9375	137.925	183.9
614	1	0	0	1	1	0	0	1	1	0	26 6					92.1	115.125	138.15	184.2
615	1	0	0	1	1	0	0	1	1	1	26 7					92.25	115.3125	138.375	184.5
616	1	0	0	1	1	0	1	0	0	0	26 8					92.4	115.5	138.6	184.8
617	1	0	0	1	1	0	1	0	0	1	26 9					92.55	115.6875	138.825	185.1
618	1	0	0	1	1	0	1	0	1	0	26 A					92.7	115.875	139.05	185.4
619	1	0	0	1	1	0	1	0	1	1	26 B					92.85	116.0625	139.275	185.7
620	1	0	0	1	1	0	1	1	0	0	26 C					93	116.25	139.5	186
621	1	0	0	1	1	0	1	1	0	1	26 D					93.15	116.4375	139.725	186.3

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
622	1	0	0	1	1	0	1	1	1	0	26 E					93.3	116.625	139.95	186.6
623	1	0	0	1	1	0	1	1	1	1	26 F					93.45	116.8125	140.175	186.9
624	1	0	0	1	1	1	0	0	0	0	27 0					93.6	117	140.4	187.2
625	1	0	0	1	1	1	0	0	0	1	27 1					93.75	117.1875	140.625	187.5
626	1	0	0	1	1	1	0	0	1	0	27 2					93.9	117.375	140.85	187.8
627	1	0	0	1	1	1	0	0	1	1	27 3					94.05	117.5625	141.075	188.1
628	1	0	0	1	1	1	0	1	0	0	27 4					94.2	117.75	141.3	188.4
629	1	0	0	1	1	1	0	1	0	1	27 5					94.35	117.9375	141.525	188.7
630	1	0	0	1	1	1	0	1	1	0	27 6					94.5	118.125	141.75	189
631	1	0	0	1	1	1	0	1	1	1	27 7					94.65	118.3125	141.975	189.3
632	1	0	0	1	1	1	1	0	0	0	27 8					94.8	118.5	142.2	189.6
633	1	0	0	1	1	1	1	0	0	1	27 9					94.95	118.6875	142.425	189.9
634	1	0	0	1	1	1	1	0	1	0	27 A					95.1	118.875	142.65	190.2
635	1	0	0	1	1	1	1	0	1	1	27 B					95.25	119.0625	142.875	190.5
636	1	0	0	1	1	1	1	1	0	0	27 C					95.4	119.25	143.1	190.8
637	1	0	0	1	1	1	1	1	0	1	27 D					95.55	119.4375	143.325	191.1
638	1	0	0	1	1	1	1	1	1	0	27 E					95.7	119.625	143.55	191.4
639	1	0	0	1	1	1	1	1	1	1	27 F					95.85	119.8125	143.775	191.7
640	1	0	1	0	0	0	0	0	0	0	28 0					96	120	144	192
641	1	0	1	0	0	0	0	0	0	1	28 1					96.15	120.1875	144.225	192.3
642	1	0	1	0	0	0	0	0	1	0	28 2					96.3	120.375	144.45	192.6
643	1	0	1	0	0	0	0	0	1	1	28 3					96.45	120.5625	144.675	192.9
644	1	0	1	0	0	0	0	1	0	0	28 4					96.6	120.75	144.9	193.2
645	1	0	1	0	0	0	0	1	0	1	28 5					96.75	120.9375	145.125	193.5
646	1	0	1	0	0	0	0	1	1	0	28 6					96.9	121.125	145.35	193.8
647	1	0	1	0	0	0	0	1	1	1	28 7					97.05	121.3125	145.575	194.1
648	1	0	1	0	0	0	1	0	0	0	28 8					97.2	121.5	145.8	194.4
649	1	0	1	0	0	0	1	0	0	1	28 9					97.35	121.6875	146.025	194.7
650	1	0	1	0	0	0	1	0	1	0	28 A					97.5	121.875	146.25	195
651	1	0	1	0	0	0	1	0	1	1	28 B					97.65	122.0625	146.475	195.3
652	1	0	1	0	0	0	1	1	0	0	28 C					97.8	122.25	146.7	195.6
653	1	0	1	0	0	0	1	1	0	1	28 D					97.95	122.4375	146.925	195.9
654	1	0	1	0	0	0	1	1	1	0	28 E					98.1	122.625	147.15	196.2
655	1	0	1	0	0	0	1	1	1	1	28 F					98.25	122.8125	147.375	196.5
656	1	0	1	0	0	1	0	0	0	0	29 0					98.4	123	147.6	196.8
657	1	0	1	0	0	1	0	0	0	1	29 1					98.55	123.1875	147.825	197.1
658	1	0	1	0	0	1	0	0	1	0	29 2					98.7	123.375	148.05	197.4
659	1	0	1	0	0	1	0	0	1	1	29 3					98.85	123.5625	148.275	197.7
660	1	0	1	0	0	1	0	1	0	0	29 4					99	123.75	148.5	198
661	1	0	1	0	0	1	0	1	0	1	29 5					99.15	123.9375	148.725	198.3

											Sample Rates								
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs										ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
662	1	0	1	0	0	1	0	1	1	0	29 6					99.3	124.125	148.95	198.6
663	1	0	1	0	0	1	0	1	1	1	29 7					99.45	124.3125	149.175	198.9
664	1	0	1	0	0	1	1	0	0	0	29 8					99.6	124.5	149.4	199.2
665	1	0	1	0	0	1	1	0	0	1	29 9					99.75	124.6875	149.625	199.5
666	1	0	1	0	0	1	1	0	1	0	29 A					99.9	124.875	149.85	199.8
667	1	0	1	0	0	1	1	0	1	1	29 B					100.05	125.0625	150.075	200.1
668	1	0	1	0	0	1	1	1	0	0	29 C					100.2	125.25	150.3	200.4
669	1	0	1	0	0	1	1	1	0	1	29 D					100.35	125.4375	150.525	200.7
670	1	0	1	0	0	1	1	1	1	0	29 E					100.5	125.625	150.75	201
671	1	0	1	0	0	1	1	1	1	1	29 F					100.65	125.8125	150.975	201.3
672	1	0	1	0	1	0	0	0	0	0	2A 0					100.8	126	151.2	201.6
673	1	0	1	0	1	0	0	0	0	1	2A 1					100.95	126.1875	151.425	201.9
674	1	0	1	0	1	0	0	0	1	0	2A 2					101.1	126.375	151.65	202.2
675	1	0	1	0	1	0	0	0	1	1	2A 3					101.25	126.5625	151.875	202.5
676	1	0	1	0	1	0	0	1	0	0	2A 4					101.4	126.75	152.1	202.8
677	1	0	1	0	1	0	0	1	0	1	2A 5					101.55	126.9375	152.325	203.1
678	1	0	1	0	1	0	0	1	1	0	2A 6					101.7	127.125	152.55	203.4
679	1	0	1	0	1	0	0	1	1	1	2A 7					101.85	127.3125	152.775	203.7
680	1	0	1	0	1	0	1	0	0	0	2A 8					102	127.5	153	204
681	1	0	1	0	1	0	1	0	0	1	2A 9					102.15	127.6875	153.225	204.3
682	1	0	1	0	1	0	1	0	1	0	2A A					102.3	127.875	153.45	204.6
683	1	0	1	0	1	0	1	0	1	1	2A B					102.45	128.0625	153.675	204.9
684	1	0	1	0	1	0	1	1	0	0	2A C					102.6	128.25	153.9	205.2
685	1	0	1	0	1	0	1	1	0	1	2A D					102.75	128.4375	154.125	205.5
686	1	0	1	0	1	0	1	1	1	0	2A E					102.9	128.625	154.35	205.8
687	1	0	1	0	1	0	1	1	1	1	2A F					103.05	128.8125	154.575	206.1
688	1	0	1	0	1	1	0	0	0	0	2B 0					103.2	129	154.8	206.4
689	1	0	1	0	1	1	0	0	0	1	2B 1					103.35	129.1875	155.025	206.7
690	1	0	1	0	1	1	0	0	1	0	2B 2					103.5	129.375	155.25	207
691	1	0	1	0	1	1	0	0	1	1	2B 3					103.65	129.5625	155.475	207.3
692	1	0	1	0	1	1	0	1	0	0	2B 4					103.8	129.75	155.7	207.6
693	1	0	1	0	1	1	0	1	0	1	2B 5					103.95	129.9375	155.925	207.9
694	1	0	1	0	1	1	0	1	1	0	2B 6					104.1	130.125	156.15	208.2
695	1	0	1	0	1	1	0	1	1	1	2B 7					104.25	130.3125	156.375	208.5
696	1	0	1	0	1	1	1	0	0	0	2B 8					104.4	130.5	156.6	208.8
697	1	0	1	0	1	1	1	0	0	1	2B 9					104.55	130.6875	156.825	209.1
698	1	0	1	0	1	1	1	0	1	0	2B A					104.7	130.875	157.05	209.4
699	1	0	1	0	1	1	1	0	1	1	2B B					104.85	131.0625	157.275	209.7
700	1	0	1	0	1	1	1	1	0	0	2B C					105	131.25	157.5	210
701	1	0	1	0	1	1	1	1	0	1	2B D					105.15	131.4375	157.725	210.3

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
702	1	0	1	0	1	1	1	1	1	0	2B E					105.3	131.625	157.95	210.6
703	1	0	1	0	1	1	1	1	1	1	2B F					105.45	131.8125	158.175	210.9
704	1	0	1	1	0	0	0	0	0	0	2C 0					105.6	132	158.4	211.2
705	1	0	1	1	0	0	0	0	0	1	2C 1					105.75	132.1875	158.625	211.5
706	1	0	1	1	0	0	0	0	1	0	2C 2					105.9	132.375	158.85	211.8
707	1	0	1	1	0	0	0	0	1	1	2C 3					106.05	132.5625	159.075	212.1
708	1	0	1	1	0	0	0	1	0	0	2C 4					106.2	132.75	159.3	212.4
709	1	0	1	1	0	0	0	1	0	1	2C 5					106.35	132.9375	159.525	212.7
710	1	0	1	1	0	0	0	1	1	0	2C 6					106.5	133.125	159.75	213
711	1	0	1	1	0	0	0	1	1	1	2C 7					106.65	133.3125	159.975	213.3
712	1	0	1	1	0	0	1	0	0	0	2C 8					106.8	133.5	160.2	213.6
713	1	0	1	1	0	0	1	0	0	1	2C 9					106.95	133.6875	160.425	213.9
714	1	0	1	1	0	0	1	0	1	0	2C A					107.1	133.875	160.65	214.2
715	1	0	1	1	0	0	1	0	1	1	2C B					107.25	134.0625	160.875	214.5
716	1	0	1	1	0	0	1	1	0	0	2C C					107.4	134.25	161.1	214.8
717	1	0	1	1	0	0	1	1	0	1	2C D					107.55	134.4375	161.325	215.1
718	1	0	1	1	0	0	1	1	1	0	2C E					107.7	134.625	161.55	215.4
719	1	0	1	1	0	0	1	1	1	1	2C F					107.85	134.8125	161.775	215.7
720	1	0	1	1	0	1	0	0	0	0	2D 0					108	135	162	216
721	1	0	1	1	0	1	0	0	0	1	2D 1					108.15	135.1875	162.225	216.3
722	1	0	1	1	0	1	0	0	1	0	2D 2					108.3	135.375	162.45	216.6
723	1	0	1	1	0	1	0	0	1	1	2D 3					108.45	135.5625	162.675	216.9
724	1	0	1	1	0	1	0	1	0	0	2D 4					108.6	135.75	162.9	217.2
725	1	0	1	1	0	1	0	1	0	1	2D 5					108.75	135.9375	163.125	217.5
726	1	0	1	1	0	1	0	1	1	0	2D 6					108.9	136.125	163.35	217.8
727	1	0	1	1	0	1	0	1	1	1	2D 7					109.05	136.3125	163.575	218.1
728	1	0	1	1	0	1	1	0	0	0	2D 8					109.2	136.5	163.8	218.4
729	1	0	1	1	0	1	1	0	0	1	2D 9					109.35	136.6875	164.025	218.7
730	1	0	1	1	0	1	1	0	1	0	2D A					109.5	136.875	164.25	219
731	1	0	1	1	0	1	1	0	1	1	2D B					109.65	137.0625	164.475	219.3
732	1	0	1	1	0	1	1	1	0	0	2D C					109.8	137.25	164.7	219.6
733	1	0	1	1	0	1	1	1	0	1	2D D					109.95	137.4375	164.925	219.9
734	1	0	1	1	0	1	1	1	1	0	2D E					110.1	137.625	165.15	220.2
735	1	0	1	1	0	1	1	1	1	1	2D F					110.25	137.8125	165.375	220.5
736	1	0	1	1	1	0	0	0	0	0	2E 0					110.4	138	165.6	220.8
737	1	0	1	1	1	0	0	0	0	1	2E 1					110.55	138.1875	165.825	221.1
738	1	0	1	1	1	0	0	0	1	0	2E 2					110.7	138.375	166.05	221.4
739	1	0	1	1	1	0	0	0	1	1	2E 3					110.85	138.5625	166.275	221.7
740	1	0	1	1	1	0	0	1	0	0	2E 4					111	138.75	166.5	222
741	1	0	1	1	1	0	0	1	0	1	2E 5					111.15	138.9375	166.725	222.3

											Sample Rates								
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs										ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
742	1	0	1	1	1	0	0	1	1	0	2E 6					111.3	139.125	166.95	222.6
743	1	0	1	1	1	0	0	1	1	1	2E 7					111.45	139.3125	167.175	222.9
744	1	0	1	1	1	0	1	0	0	0	2E 8					111.6	139.5	167.4	223.2
745	1	0	1	1	1	0	1	0	0	1	2E 9					111.75	139.6875	167.625	223.5
746	1	0	1	1	1	0	1	0	1	0	2E A					111.9	139.875	167.85	223.8
747	1	0	1	1	1	0	1	0	1	1	2E B					112.05	140.0625	168.075	224.1
748	1	0	1	1	1	0	1	1	0	0	2E C					112.2	140.25	168.3	224.4
749	1	0	1	1	1	0	1	1	0	1	2E D					112.35	140.4375	168.525	224.7
750	1	0	1	1	1	0	1	1	1	0	2E E					112.5	140.625	168.75	225
751	1	0	1	1	1	0	1	1	1	1	2E F					112.65	140.8125	168.975	225.3
752	1	0	1	1	1	1	0	0	0	0	2F 0					112.8	141	169.2	225.6
753	1	0	1	1	1	1	0	0	0	1	2F 1					112.95	141.1875	169.425	225.9
754	1	0	1	1	1	1	0	0	1	0	2F 2					113.1	141.375	169.65	226.2
755	1	0	1	1	1	1	0	0	1	1	2F 3					113.25	141.5625	169.875	226.5
756	1	0	1	1	1	1	0	1	0	0	2F 4					113.4	141.75	170.1	226.8
757	1	0	1	1	1	1	0	1	0	1	2F 5					113.55	141.9375	170.325	227.1
758	1	0	1	1	1	1	0	1	1	0	2F 6					113.7	142.125	170.55	227.4
759	1	0	1	1	1	1	0	1	1	1	2F 7					113.85	142.3125	170.775	227.7
760	1	0	1	1	1	1	1	0	0	0	2F 8					114	142.5	171	228
761	1	0	1	1	1	1	1	0	0	1	2F 9					114.15	142.6875	171.225	228.3
762	1	0	1	1	1	1	1	0	1	0	2F A					114.3	142.875	171.45	228.6
763	1	0	1	1	1	1	1	0	1	1	2F B					114.45	143.0625	171.675	228.9
764	1	0	1	1	1	1	1	1	0	0	2F C					114.6	143.25	171.9	229.2
765	1	0	1	1	1	1	1	1	0	1	2F D					114.75	143.4375	172.125	229.5
766	1	0	1	1	1	1	1	1	1	0	2F E					114.9	143.625	172.35	229.8
767	1	0	1	1	1	1	1	1	1	1	2F F					115.05	143.8125	172.575	230.1
768	1	1	0	0	0	0	0	0	0	0	30 0					115.2	144	172.8	230.4
769	1	1	0	0	0	0	0	0	0	1	30 1					115.35	144.1875	173.025	230.7
770	1	1	0	0	0	0	0	0	1	0	30 2					115.5	144.375	173.25	231
771	1	1	0	0	0	0	0	0	1	1	30 3					115.65	144.5625	173.475	231.3
772	1	1	0	0	0	0	0	1	0	0	30 4					115.8	144.75	173.7	231.6
773	1	1	0	0	0	0	0	1	0	1	30 5					115.95	144.9375	173.925	231.9
774	1	1	0	0	0	0	0	1	1	0	30 6					116.1	145.125	174.15	232.2
775	1	1	0	0	0	0	0	1	1	1	30 7					116.25	145.3125	174.375	232.5
776	1	1	0	0	0	0	1	0	0	0	30 8					116.4	145.5	174.6	232.8
777	1	1	0	0	0	0	1	0	0	1	30 9					116.55	145.6875	174.825	233.1
778	1	1	0	0	0	0	1	0	1	0	30 A					116.7	145.875	175.05	233.4
779	1	1	0	0	0	0	1	0	1	1	30 B					116.85	146.0625	175.275	233.7
780	1	1	0	0	0	0	1	1	0	0	30 C					117	146.25	175.5	234
781	1	1	0	0	0	0	1	1	0	1	30 D					117.15	146.4375	175.725	234.3

											Sample Rates								
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs										ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
782	1	1	0	0	0	0	1	1	1	0	30 E					117.3	146.625	175.95	234.6
783	1	1	0	0	0	0	1	1	1	1	30 F					117.45	146.8125	176.175	234.9
784	1	1	0	0	0	1	0	0	0	0	31 0					117.6	147	176.4	235.2
785	1	1	0	0	0	1	0	0	0	1	31 1					117.75	147.1875	176.625	235.5
786	1	1	0	0	0	1	0	0	1	0	31 2					117.9	147.375	176.85	235.8
787	1	1	0	0	0	1	0	0	1	1	31 3					118.05	147.5625	177.075	236.1
788	1	1	0	0	0	1	0	1	0	0	31 4					118.2	147.75	177.3	236.4
789	1	1	0	0	0	1	0	1	0	1	31 5					118.35	147.9375	177.525	236.7
790	1	1	0	0	0	1	0	1	1	0	31 6					118.5	148.125	177.75	237
791	1	1	0	0	0	1	0	1	1	1	31 7					118.65	148.3125	177.975	237.3
792	1	1	0	0	0	1	1	0	0	0	31 8					118.8	148.5	178.2	237.6
793	1	1	0	0	0	1	1	0	0	1	31 9					118.95	148.6875	178.425	237.9
794	1	1	0	0	0	1	1	0	1	0	31 A					119.1	148.875	178.65	238.2
795	1	1	0	0	0	1	1	0	1	1	31 B					119.25	149.0625	178.875	238.5
796	1	1	0	0	0	1	1	1	0	0	31 C					119.4	149.25	179.1	238.8
797	1	1	0	0	0	1	1	1	0	1	31 D					119.55	149.4375	179.325	239.1
798	1	1	0	0	0	1	1	1	1	0	31 E					119.7	149.625	179.55	239.4
799	1	1	0	0	0	1	1	1	1	1	31 F					119.85	149.8125	179.775	239.7

APPLICATION INFORMATION FOR ALL ISD ChipCorder PRODUCTS

Frequently Asked Questions

1. I can't get enough audio output from the chip. It isn't loud enough.

Are you using the speaker directly across the speaker leads? Is it in a box? Volume varies greatly depending on the enclosure. The ISD-ES001 Evaluation System with an efficient 4-inch speaker drives us out of the room. We use a 20-Ω resistor in series to keep peace in the lab. If you experiment and still need more volume you can use an audio amplifier chip, as shown in "Using the Device."

2. How do I copy recordings from my tape recorder into your chip?

Take audio from Line Out of the tape deck and attenuate it with a resistor voltage divider. Apply to ANA IN through a DC-blocking capacitor such as a 1.0 µF. The Line Out of a tape deck is ≈100–150 mV RMS and must be attenuated to 50 mV P-P (Peak-to-Peak) for our chips. See Figure 4: Prototype 3 Volt AGC Circuit under the section "AGC Circuit for the ISD33000 Series" for a circuit example.

3. I record several messages into the chip but it always plays beyond the end of the message, into the next, playing everything until it reaches the end of the chip!

You are probably holding $\overline{CE}$ (Chip Enable), pin 23, LOW as you did when recording. If you hold $\overline{CE}$ LOW it will play beyond the End-of-Message (EOM) marker into the next message. For playback you need only pulse $\overline{CE}$ LOW momentarily. Then it will play the message, stopping at the end.

4. I hear a lot of noise when I play back my recording. How much should there be?

Is it "hiss" or a "buzz or hum" sort of noise? The normal low-level background noise comes across as a very weak "hiss." It is about the same as a long distance phone call. If it is a "hum," there may several ways to reduce it. First, are you using the differential microphone circuit illustrated in the "Microphone and Speaker Selection." How is V_{CCD}, pin 28, bypassed? See Good "Audio Design Practices" and "Single-Chip Board Layout Diagrams" for layout details. It is sometimes difficult to get good noise performance on wire wrap or "proto board."

5. How many messages can I put in my chip? There are eight address lines. Does this mean there are eight messages?

No. It means that the messages are accessed with binary coding. The starting point of each message is defined by its binary code. (See the address table in "Address Segment Resolution.") In the shorter devices (ISD1110, ISD1210), there are 80 addresses available for starting messages. In the mid-sized devices (ISD1016A, ISD1420), there are 160 potential starting addresses. In the larger devices (ISD2560/75/90/120), there are 600 starting addresses. These are explained in "Basic Addressing."

6. My chip won't do anything. It just sits there when I try to make it record or play.

Is pin 24, PD (Power-Down), HIGH or LOW? It must be LOW for the chip to come out of standby, draw current and operate.

7. My chip will record a message but will only play the message back once until I remove the power. Then it will play one more time only.

The chip probably played to the end of memory and is in "overflow." Pulse pin 24, PD, HIGH briefly to reset the address counter back to the beginning to play the message again. Any time the chip plays all the way to the end, the address counter must be reset (ISD1000A and ISD2500 only).

8. My prototype circuit works intermittently (or not at all). It records, but can only playback once or twice before I have to power it off to work again.

Do you have pin 26, TEST/XCLK, grounded? There must be no floating digital inputs. All address pins, control pins, and TEST/XCLK must be defined as HIGH or LOW.

9. My chip gets hot when I plug it in and doesn't sound very good.

Do you have one of the speaker leads, SP+ or SP–, grounded? These leads must NOT be grounded. They can be connected directly to the speaker or left floating.

10. Is a development system available?

Yes. See the section "ISD Development Systems." Contact an ISD representative for price and availability.

11. Will the ISD chip run from a 9 VDC battery?

Not directly! Use a voltage regulator to get down to 5 VDC for the chip. It is possible to run it from four AA cells at 6 VDC, however.

12. Can the ISD chips play a sound backwards?

No, the addressing technique doesn't allow it.

13. Can the ISD33000 run at 5 volts?

No, the operating voltage of the ISD33000 family is 3 volts ±10 percent. You need to regulate the supply voltage down to 3 volts.

14. I am confused about the SPI command format for the ISD33000. Do you have an application note that describes the SPI command format.

Yes, See the section "Operations, Tricks and Techniques."

15. I need a low-cost AGC circuit to use with the ISD33000. What do you recommend?

Please see "AGC Circuit for ISD33000" (also see Figure 4: AGC Schematic under the section "A 'C' Language Source code Example for Use with the ISD33000 Series" for a low cost AGC.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Device Operation

GENERAL DESCRIPTION

All ISD single-chip voice record/playback devices are analog sampled data systems. Current product offerings include the ISD1000A series, the ISD1100 series, the ISD1200 series, the ISD1400 series, and the ISD2500 series. Each series member has an on-chip microphone preamplifier, AGC, antialiasing and smoothing filters, high-density multilevel storage array, speaker driver, control interface and internal precision reference clock. The difference between the ISD technology and other competing voice storage technologies is that no A-D or D-A converters are required. As each sample is taken, it is temporarily stored in a sample and hold circuit and eventually "recorded" into a single EEPROM cell. Since we are recording with the equivalent of 8 bits of accuracy, it would require 3.8 million bits of digital memory (as well as the A-D and D-A converters) to equal the 480,000 cells contained in the ISD2500 series device's storage array.

The sample rates versus storage time and filter upper pass band for each device in the above series are shown in Table 1. Filter specification applies to the antialiasing filter and the smoothing filter.

How the frequency response is determined will be covered later in this document.

NOTE *All pin numbers quoted assume a DIP package and an ISD1000A, ISD1100, ISD1200, ISD1400 or ISD2500 device.*

Table 1: Sample Rate, Storage Time, and Frequency Response

Device Part Number	Sample Rate (KHz)	Storage Time (seconds)	Filter Pass Band (Hz)
ISD1016A	8.0	16	3400
ISD1020A	6.4	20	2700
ISD1110	6.4	10	2600
ISD1112	5.3	12	2200
ISD1210	6.4	10	2600
ISD1212	5.3	12	2200
ISD1416	8.0	16	3300
ISD1420	6.4	20	2600
ISD2532/60	8.0	32/60	3400
ISD2540/75	6.4	40/75	2700
ISD2548/90	5.3	48/90	2300
ISD2564/120	4.0	64/120	1700

All analog circuits in the ISD device series are referenced to an internally generated analog ground bias of approximately 1.5 volts. A designer can measure this bias level externally at the MIC INPUT (pin 17), MIC REF (pin 18), and ANA IN input (pin 20). This measurement will be within ±20 mV of the internal value. All connections to these pins should be capacitively coupled so that this bias is not disturbed.

MIC (PIN 17)

The on-chip microphone amplifier is designed to amplify signals in the 1 to 20 millivolt range. This gain controlled transconductance amplifier has an input impedance of ≈10 KΩ and a maximum gain of 24 dB. A typical electret microphone supplies a level adequate to drive this amplifier. Since the input impedance is known, the low end frequency response is determined by the audio source and the input coupling capacitor. In the ISD1000A data sheet example, an electret microphone is used with a 0.1 μF coupling capacitor. This becomes a high pass filter with an approximate low end cutoff frequency response of 160 Hz. This is determined by first assuming that the input signal will be attenuated 3 dB at frequencies below where the reactance of the input capacitor equals the internal impedance of the microphone input. The equation for this is:

$$F_{3dB} = \frac{1}{2\pi RC}$$

Since R nominally equals 10 KΩ, this equation may be further simplified to:

$$F_{3dB} = \frac{1}{62832 \times C}$$

where C is in Farads

An on-chip AGC circuit controls the gain of the microphone preamplifier. Its gain will vary from 0 to 20 dB as required to maintain an appropriate input level.

MIC REF (PIN 18)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise canceling or common mode rejection input to the device. The preferred circuit for connecting the microphone is the differential circuit illustrated in the "Microphone and Speaker Selection" section of Application Information. This configuration gives even better noise rejection than the next method. Alternatively, a capacitor is connected from this pin to analog ground. This capacitor should have exactly the same value as the Microphone preamplifier input coupling capacitor. The ground for the microphone should be physically close to the ground connection for the MIC REF capacitor. The addition of this "noise-canceling" input gives approximately 10 dB of improvement in the background noise level over not using it. If this input is not used, it must be left unconnected.

AGC (PIN 19)

The applications schematic in the data sheet shows R2 and C2 connected from pin 19 to ground. These two components set up the attack and release time constants for the internal Automatic Gain Control circuit in the microphone preamplifier. The attack time is determined by a network consisting of an internal R and external C while the release time is determined by the two external components in parallel. Nominal values of 470 KΩ (R2) and 4.7 μF (C2) give satisfactory results in most cases.

ANA OUT (PIN 21)

ANA OUT is the direct output of the microphone preamplifier. In a typical application, this output is capacitively coupled to the ANA IN pin.

ANA IN (PIN 20)

The ANA IN pin feeds an input amplifier with an input impedance of ≈2.7 KΩ. As with the microphone input, the coupling capacitor that connects ANA IN to ANA OUT sets the low end frequency response of this section of the circuit. With the ISD1000A data sheet circuit example value of 0.1 μF for C1 and C3, the system low end frequency response is the series combination of these two single pole high pass filters. Since the MIC circuit has a pole at approximately 160 Hz, the result will be a system high pass with a 3 dB point at a slightly higher frequency than either pole or approximately 600 Hz. With the 4.5 to 6.5 VDC operating voltage range of a 5.1 KΩ resistor is normally used in series with the coupling capacitor to slightly drop the voltage fed to the array to prevent distortion; this changes the frequencies slightly.

ANTIALIASING AND SMOOTHING FILTERS

The antialiasing and smoothing filters are actually a single filter that is multiplexed into each circuit function as needed for Record and Playback. This filter is constructed using conventional (non-switched capacitor) circuit techniques with no external components. It is a 5-pole Chebychev filter with <2 dB of ripple. The 3 dB point of this filter is set for each of the devices in the ISD series. The response is in Table 1 at the beginning of this section.

SAMPLE AND HOLD REGISTERS

Some of the complexity of the internal design of the ISD devices can be grasped once the user understands the internal workings of the device. Looking only at the ISD1016A device during Record, samples are taken of the incoming waveform every 125 μs (8 KHz sample rate). It takes about 10 ms to "record" an incoming sample into the storage array. Therefore two banks of at least 80 sample and hold registers are required to buffer the incoming samples. It is the hold time of these capacitors that determine the minimum sample frequency. One bank will be receiving incoming samples serially in real-time while the other bank is connected in parallel to program multiple cells simultaneously.

STORAGE ARRAY

The EEPROM storage array of the ISD1000A series is organized as 160 rows. Other ISD device series may have a different organization. In a later chapter you will find out how to control where a message can be started for record or playback. In the ISD1000A series there are 160 possible starting addresses; you start record or playback from the beginning of one of the 160 rows. Whenever a message is recorded or played back, you proceed through a row until the end, at which time the internal row address counter advances by one and you continue at the beginning of the next row. The address counter is internal to the ISD devices. The address pins of the device are inputs only. The "current" address is not directly available.

$\overline{\text{EOM}}$ (PIN 25) AND EOM BITS (ISD1000A AND ISD2500 SERIES)

An inherent requirement for addressing multiple words or "messages" in the ISD1000A and ISD2500 devices is knowing where the message ends. Anytime a Record cycle is stopped by a rising $\overline{\text{CE}}$ signal, an EOM bit is set in a separate digital EEPROM memory inside the ISD device. When a message playback is begun with a pulsed $\overline{\text{CE}}$ signal, that playback will continue until an EOM bit is found.

Each of the rows of the storage array in an ISD1000A or ISD2500 device is addressed individually. There are four evenly spaced EOM locations that point into each row. In the ISD1000A device, this equates to 4 x 160 or 640 EOM locations. The ISD2500 series devices have 4 X 600 or 2400 possible EOM locations. The 8 KHz sample rate products available from ISD are addressable on 100 millisecond boundaries and the EOM resolution is 25 ms. Thus the maximum delay from the end of a message to the output of an $\overline{\text{EOM}}$ signal is 25 ms. The $\overline{\text{EOM}}$ signal is low going and lasts for 12.5 ms. The rising edge of $\overline{\text{EOM}}$ actually marks the end of the message. So, audio will continue to be output from a ISD device during the time $\overline{\text{EOM}}$ is low and will stop at its rising edge. These times will vary with other sample rate devices available from ISD. See the appropriate ISD data sheet for these timings.

In the ISD1000A series, the $\overline{EOM}$ pin also carries the Overflow indication. At Overflow in playback, the $\overline{EOM}$ pin will go LOW and stay LOW until Overflow is cleared. At Overflow in record, the $\overline{CE}$ input signal will transfer to the $\overline{EOM}$ output.

$\overline{RECLED}$ (PIN 25) AND EOM BITS (ISD1100, ISD1200 AND ISD1400 SERIES)

This pin on the ISD1100, ISD1200, and ISD1400 series carries two signals. The identified signal, $\overline{RECLED}$, pulls LOW at the start of a Record operation initiated by taking the $\overline{REC}$ pin LOW. It has adequate drive capability to control an LED through a 1 KΩ resistor to V_{CC}. This signal will go back HIGH at the end of a Record operation when the $\overline{REC}$ pin is taken back HIGH or the end of the device memory is reached.

The ISD1100, ISD1200, and ISD1400 series also contain an EOM structure similar to that in the ISD1000A series. There are half as many possible EOM bits per row, however, giving a 50 ms. End of Message resolution, for instance, in the ISD1416 device. To maintain the ability to determine when a Playback cycle is finished, the $\overline{RECLED}$ pin also carries an $\overline{EOM}$ signal. It pulses LOW at the end of a message during a Playback cycle. If this pin is connected to an LED as indicated in the previous paragraph, it may be seen to "blink" on momentarily at the end of each message during playback.

There is no Overflow signal in the ISD1100, ISD1200, and ISD1400 series. If a message ends at the end of the device memory, an EOM bit is set at memory end. When this message is played back, a normal LOW going EOM pulse is generated to the $\overline{RECLED}$ pin.

$\overline{OVF}$ (PIN 22, ISD2500 SERIES ONLY)

One of the major features added in the ISD2500 was the separation of the Overflow ($\overline{OVF}$) and end-of-message ($\overline{EOM}$) output signals into two separate pins, $\overline{OVF}$ and $\overline{EOM}$. This more efficiently enables multi-device cascade. In the ISD2500 series, the $\overline{EOM}$ pin only pulses LOW during playback when a set EOM bit is encountered. It **does not** pulse LOW at Overflow. Instead, the $\overline{OVF}$ pin pulses LOW for approximately 6 ms when an Overflow condition is reached.

After Overflow is reached, the $\overline{CE}$ signal is coupled through the device to the $\overline{OVF}$ output. This means that the input $\overline{CE}$ signal "appears" at the $\overline{OVF}$ output of any device in overflow.

To understand why this operates this way, consider several ISD2500 devices connected in cascade. To cascade properly, each $\overline{OVF}$ is connected to the $\overline{CE}$ of the following device. The $\overline{OVF}$ of the final device will be discussed later. The $\overline{CE}$ now "daisy chains" through devices that are in overflow. Changing the state or pulsing $\overline{CE}$ LOW at the input of the first device in cascade will directly control the first device down the line that is not in overflow.

Operation of $\overline{OVF}$ in Record

Since the $\overline{CE}$ signal is held LOW during recording, $\overline{OVF}$ goes LOW and stays LOW at Overflow. It does not pulse LOW. When the $\overline{CE}$ input goes LOW, $\overline{OVF}$ follows it LOW.

Operation of $\overline{OVF}$ in Playback

Normal Playback operations begin by pulsing $\overline{CE}$ LOW and then back HIGH. In this case, the $\overline{OVF}$ pin will pulse LOW at Overflow to cause playback to begin in the next device in the cascade. If the system uses a continuous LOW $\overline{CE}$ during Playback, the $\overline{OVF}$ pin will go LOW and stay LOW at Overflow. The LOW pulse will not be output.

NOTE *The $\overline{EOM}$ output of the ISD2500 series device does not pulse LOW when the Overflow condition is reached. A message being played back can end with a set EOM bit, or, because it runs into overflow. If the designer needs a single logic output to indicate that a message has ended, it is necessary to or the $\overline{EOM}$ and $\overline{OVF}$ outputs together. Since these are active LOW signals, a two-input and gate may be used to generate an active LOW combined signal. Alternatively, two diodes and a pull up resistor may be used. (Note that the $\overline{OVF}$ signal is a 6 µs long pulse.)*

SPEAKER OUTPUT, SP+ (PIN 14) & SP– (PIN 15)

The ISD devices include a differential speaker driver. It has the capability to drive 50 milliwatts into 16 Ω from the AUX IN pin. From the memory array, with a properly recorded signal, it will provide 12.6 mW output power. The signals are exactly 180 degrees out of phase. A lower impedance speaker may be used but distortion and peak I_{CC} current will increase as the speaker impedance decreases. Do not use an impedance less than 8 Ω. These outputs may be used single ended with the signal taken from either pin but should never be shorted together or tied to ground. When driving a single ended connection, capacitive coupling is recommended because of the possible large DC bias current that could result (100 mA). If the outputs are used single ended, the unused pin must be left unconnected. **Do not ground the unused output.**

When the power-down pin is low (device powered up) and the Playback/Record pin is high (Playback Mode) both speaker pins will be at an average value of about 1.5 volts. When the device is in Record or is Powered Down, the two speaker outputs will be pulled hard to ground. **Do not parallel the speaker outputs with other signals without taking this into consideration. The speaker outputs can sink and source large amounts of current!**

The speaker outputs are internally pulled to ground to protect the output transistors on the ISD devices. Remember, these outputs are normally connected to a speaker. A speaker is an electromechanical device with the ability to inductively generate a large voltage spike if abruptly struck or dropped.

AUX INPUT (PIN 11, ISD1000A AND ISD2500 SERIES)

When an ISD device is in the Playback Mode (Playback/Record Pin 27 HIGH), not powered down (power-down Pin 24 LOW) and not actively playing back a message, the AUX IN is an input to the speaker output. This analog path to the differential speaker driver has a voltage gain of a little less than 0 dB. The input impedance is ≈10 KΩ to analog ground. Other signal sources can therefore use the speaker output drivers. This input is also used in Cascading applications. This pin is not connected on the ISD1100, ISD1200, and ISD1400 devices.

$\overline{\text{PLAYL}}$ (PIN 23, ISD1100, ISD1200, AND ISD1400)

The $\overline{\text{PLAYL}}$ pin starts a Playback cycle when taken LOW. The Playback cycle will continue until an EOM is reached as long as $\overline{\text{PLAYL}}$ is held LOW. If the $\overline{\text{PLAYL}}$ pin is taken back HIGH during playback, playback will immediately stop. When playback stops (because of $\overline{\text{PLAYL}}$ going LOW or an EOM being reached) the device will automatically go into a power-down state.

The $\overline{\text{PLAYL}}$ pin may also be used to interrupt a Playback cycle initiated by the $\overline{\text{PLAYE}}$ pin by cycling $\overline{\text{PLAYL}}$ LOW then back HIGH. A Playback cycle may also be interrupted by the $\overline{\text{REC}}$ pin. See the heading entitled "$\overline{\text{REC}}$ (Pin 27, ISD1100, ISD1200, and ISD1400)" below.

The ISD1100 device has a pull-up resistor to V_{CC} on the $\overline{\text{PLAYL}}$ pin. This pull-up resistor is approximately 100 KΩ.

$\overline{\text{PLAYE}}$ (PIN 24, ISD1100, ISD1200, AND ISD1400)

The $\overline{\text{PLAYE}}$ pin starts a Playback cycle when taken LOW. This is an edge triggered event and playback will continue, even if $\overline{\text{PLAYE}}$ is taken back HIGH. Playback will stop when a set EOM bit is reached or interrupted by the $\overline{\text{PLAYL}}$ pin as explained above. When playback stops, the device will automatically power-down. A Playback cycle may also be interrupted by the $\overline{\text{REC}}$ pin. See the heading entitled "$\overline{\text{REC}}$ (Pin 27, ISD1100, ISD1200, and ISD1400)" below.

The ISD1100 device has a pull-up resistor to V_{CC} on the $\overline{PLAYE}$ pin. This pull-up resistor is approximately 100 KΩ.

$\overline{REC}$ (PIN 27, ISD1100, ISD1200, AND ISD1400)

The $\overline{REC}$ pin initiates a Record cycle when taken LOW. This is a level activated signal and Record will end when $\overline{REC}$ is taken back HIGH. The device will automatically power down when $\overline{REC}$ goes HIGH.

NOTE *If $\overline{REC}$ is held LOW after the end of device memory is reached, the device will not power down until this pin is allowed to go back HIGH.*

The $\overline{REC}$ control pin takes priority over both $\overline{PLAYL}$ and $\overline{PLAYE}$ pins. Taking $\overline{REC}$ LOW during a Playback cycle will immediately interrupt playback and begin a Record cycle.

The ISD1100 device includes a pull-up resistor to V_{CC} on the $\overline{REC}$ pin. This pull-up resistor is approximately 100 KΩ.

MICROCONTROLLER INTERFACE (PINS 23, 24, 27, ISD1000A AND ISD2500 SERIES)

The $\overline{CE}$, PD and P/$\overline{R}$ pins on the ISD devices are internally debounced. They can be driven by toggle switches. There will be a number of circuit examples given later to demonstrate their ease of use in various applications. These same inputs are flexible enough, however, to be driven from a microcontroller. The above named pins along with $\overline{EOM}$ are all TTL compatible and can be driven from a microcontroller system.

NOTE *The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible. If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

OVERFLOW (ISD1000A, ISD2500)

The internal logic of ISD devices is designed to allow easy cascading of chips. This will extend the total storage time available to the user. To accomplish this, the device changes Operation Modes when completely full. This change in mode is called Overflow. Once a device is in Overflow, it will not respond to a new $\overline{CE}$ cycle until cleared from this state. In both the ISD1000A and ISD2500 device series, a PD cycle is required to clear the Overflow state. The length of power-down cycle required to reset an Overflow condition is T_{SET}. The device will now respond to a $\overline{CE}$ pulse.

The ISD1100, ISD1200, and ISD1400 series do not have a comparable Overflow state.

PRECISION CLOCK WITH EXTERNAL DRIVE (PIN 26)

The ISD devices include an on-chip temperature compensated reference oscillator that controls the sample rate of the device. This oscillator requires no external parts. The sample rate is derived from a set of dividers following the internal oscillator circuitry.

An external clock may be used to drive the ISD devices through the XCLK pin (Pin 26). Driving from an external clock can be useful for system synchronization. Otherwise, this pin is normally tied LOW to ensure that the internal oscillator drives the device. If a TTL level clock is fed into this pin, the internal oscillator switches off and the external clock runs the device. The XCLK pin feeds a ÷2 flip-flop. Thus, the external clock must be twice the desired internal clock. It also means that the duty cycle of the external clock drive is not important.

NOTE *Care should be taken to ensure that the 1 and 0 logic level requirements are met when driving any ISD device input. Over or under shoot outside the data sheet limits may cause an increase in device noise. This is especially important when externally driving the XCLK pin.*

It is important to remember that the antialiasing and smoothing filters are fixed and do not change with the external clock rate. As a result, it is possible to have problems with aliasing into the passband if the clock is driven slower than the designed speed. When the clock is driven faster than the designed speed, the filters will still control the passband upper limit to the original value and there may be no advantage in doing this. Table 2 shows the external clock speed requirement for each of the standard ISD devices.

NOTE *The frequency range is limited by factors that may change from device to device and are not tested. The ISD devices are only guaranteed to operate at their design frequency. Customers may vary this clock frequency only at their own risk. You should know that the primary factors involved in the upper and lower clock frequency limits are sample-and-hold "droop" on the low end of the range and EEPROM programming speed on the high end.*

The information under the previous heading Sample and Hold Registers, described how internal sample-and-hold registers temporarily store the analog sample until the EEPROM programming step. At some low end speed (which varies from device to device) the analog voltage stored in the sample-and-hold registers will droop unacceptably.

As you speed up the device, at some frequency there will no longer be enough time to successfully program the EEPROM storage locations. Significant reduction in signal quality will occur.

EXTERNAL CLOCK DRIVE USING THE ISD1100, ISD1200 OR ISD1400

In the ISD1000A or ISD2500 device series, some customers experienced difficulties in switching from internal to external clock and back again. Particularly, any noise or spikes at the wrong time could convince the part it was in the external mode when there was no clock present. Then the device would cease to function, ignoring all inputs until the power was removed and reapplied.

Table 2: External Clock Drive Frequencies

Device Part Number	Int. Osc. Freq. (KHz)	Ext. Drive Freq. (KHz)	Sample Rate (KHz)	Filter Pass Band (Hz)
ISD1016A	512.0	1,024.0	8.0	3400
ISD1020A	409.6	819.2	6.4	2700
ISD1110	409.6	819.2	6.4	2600
ISD1112	341.3	682.7	5.3	2200
ISD1210	409.6	819.2	6.4	2600
ISD1212	341.3	682.7	5.3	2200
ISD1416	512.0	1,024.0	8.0	3300
ISD1420	409.6	819.2	6.4	2600
ISD2532/60	512.0	1,024.0	8.0	3400
ISD2540/75	409.6	819.2	6.4	2700
ISD2548/90	341.3	682.7	5.3	2300
ISD2564/120	256.0	512.0	4.0	1700

The ISD1100, ISD1200, and ISD1400 series is designed so the device will not end up in a locked up state. This is accomplished by logic that automatically switches the device back to internal clock whenever the three pins, $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$, are all HIGH. In this way, the device is always looking for command inputs with the internal clock if the external clock is off.

Expressing this a different way, to use the external clock, one of the three inputs must be LOW. A recording is made by having an external clock present at the XCLK pin when $\overline{REC}$ goes LOW. The $\overline{PLAYL}$ input should be brought LOW simultaneously (or shortly after) with $\overline{REC}$. At the end of the recording $\overline{REC}$ is brought HIGH. This begins the "finish recording" process. Because the device continues to sample and record for the remaining portion of the row until it reaches an EOM location, $\overline{PLAYL}$ must be kept LOW for another 50 to 75 msec (see Figure 1). This keeps the device in the external clock mode until everything is written to memory. If only $\overline{REC}$ is used there will be a short "chirp" or change in pitch at the very end of the recording.

Playback with the external clock requires that the $\overline{PLAYL}$ pin be used, not the $\overline{PLAYE}$. This is because the device will switch to external clock when $\overline{PLAYE}$ goes LOW but will immediately revert to the internal clock when $\overline{PLAYE}$ goes HIGH again.

For applications where one wants to vary the pitch of playback the $\overline{PLAYL}$ pin must be used for playback. Another alternative is to record with the external clock and then use the internal clock and $\overline{PLAYE}$ for playing back the messages. This eliminates the need for external timing of the $\overline{PLAYL}$ signal in playback.

NOTE *The ISD1100, ISD1200 and ISD1400 devices include a pull-down resistor to V_{SS} on the XCLK pin. This pull-down resistor is approximately 100 KΩ.*

MESSAGE ADDRESSING

The ISD devices allow the designer to select individual messages using eight or ten address input lines. From 80 to 600 individual message start locations can be addressed. Each message has an internal End Of Message (EOM) bit that is saved with a recording to indicate when the message is complete. This capability is discussed in detail in the Basic Addressing section page 8.

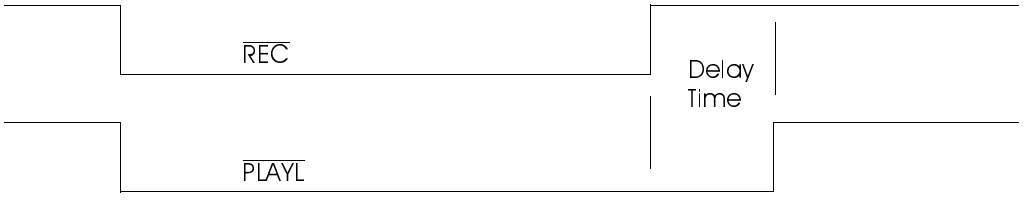
The ISD1100 device includes pull-up resistors to V_{CC} on address lines A6 and A7 and pull-down resistors to A0 through A5. These pull-up or pull-down resistors are approximately 100 KΩ.

NOTE *The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible. If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

Table 3: Delay Time from $\overline{\text{REC}}$ to $\overline{\text{PLAYL}}$ Rising Edges

Device Type	Duration (seconds)	Internal Sample Rate (KHz)	Delay Time to Finish Recording (msec)
ISD1110/ISD1210	10	6.4	62.50
ISD1112/ISD1212	12	5.3	75.00
ISD1416	16	8.0	50.00
ISD1420	20	6.4	62.50

Figure 1: Delay Time from $\overline{\text{REC}}$ to $\overline{\text{PLAYL}}$ Rising Edges



OPERATIONAL MODES

The address maps of the ISD devices have unique address locations set aside for special operating modes. This part of the address map is unique in that all Operational Modes use addresses with the two most significant address bits HIGH simultaneously. These do not latch. An Operational Mode function is only in effect for the operational cycle initiated by the falling edge $\overline{\text{CE}}$ (ISD1000A or ISD2500) or on the falling edge of $\overline{\text{PLAYL}}$, $\overline{\text{PLAYE}}$, or $\overline{\text{REC}}$ (ISD1100, ISD1200, and ISD1400). If an Operational Mode is not selected in the next operational cycle, a plain address cycle will be performed.

Because the Operational Modes do not latch, the user cannot simultaneously address individual messages and execute an Operational Mode. All Operational Modes start at address <00000000> unless they themselves modify or control chip addressing. The Operational Modes are discussed in detail under the Application "Operational Modes."

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Using the Device

CHIP ENABLE INITIATED RECORD AND PLAYBACK CYCLES (ISD1000A, ISD2500)

The ISD data sheets describe a $\overline{CE}$ initiated Record and playback cycle. The designer sets the PD pin LOW to power up the device, sets up the address and P/$\overline{R}$ pins, waits T_{PUD}, and then drops $\overline{CE}$. The device then operates as desired. Once $\overline{CE}$ has fallen, the device ignores further transitions on the address and P/$\overline{R}$ pins. When PD has been LOW more than T_{PUD} before address and P/$\overline{R}$ pins are changed, these pins must be stable T_{SET} time before $\overline{CE}$ falls (T_{SET} is always very much shorter than T_{PUD}).

RECORD

$\overline{CE}$ controls start and stop of a Record cycle. The falling edge of $\overline{CE}$ starts Record and the rising edge stops Record within 12.5 to 37.5 msec. This time is utilized by the chip to complete programming cycles that may be under way.

PLAYBACK

A momentary LOW $\overline{CE}$ (at least T_{CE} long) initiates a playback cycle. After a playback cycle initiated by a momentary $\overline{CE}$ has been started, it will end one of three possible ways:

- The device reads an internal end of message (EOM) bit set HIGH. At this time, a T_{EOM} long $\overline{EOM}$ signal will be output while audio continues to be played out of the device. At the end of the $\overline{EOM}$ pulse, the audio output will cease.
- The device goes into the overflow condition (this assumes that an Operational Mode action is not under way; Operational Mode use of $\overline{EOM}$ will be covered later). $\overline{EOM}$ will go LOW and remain in that state. Audio output will continue for an additional T_{EOM} after $\overline{EOM}$ goes LOW. This means that the $\overline{EOM}$ signal actually goes LOW T_{EOM} before the device finishes playing its memory.
- A long Power-Down cycle is performed. If PD is held HIGH for at least T_{PUD} the playback cycle will be interrupted.

PD INITIATED RECORD AND PLAYBACK CYCLES (ISD1000A, ISD2500)

A Record or Playback cycle may be initiated by a falling PD. Address and P/$\overline{R}$ pins should be set up as desired and $\overline{CE}$ held LOW. When PD is changed to a LOW, the appropriate cycle will begin T_{PUD} after PD falls.

In this case, initially, the device will be powered down. When the PD pin is taken LOW, the device will "wake up" (i.e., come out of the Power-Down condition), read the current address and control pins, then execute the desired operation.

RECORD AND PLAYBACK CYCLES IN THE ISD1100/1200/1400 SERIES

The ISD1100/1200/1400 have a different interface than the ISD1000A and ISD2500. These devices do not have a PD pin. Power-down is always automatic. They also do not have $\overline{CE}$ or P/$\overline{R}$ pins. All operations start by changing state on a single input pin.

The ISD1100/1200/1400 interface consists of the following input pins: $\overline{REC}$, $\overline{PLAYE}$, $\overline{PLAYL}$. The only digital output is called $\overline{RECLED}$. Record is accomplished by holding the $\overline{REC}$ pin LOW for the duration of the Record. $\overline{RECLED}$ stays LOW during Record. Playback is started with a pulse on the $\overline{PLAYE}$ or "play edge" pin and will end with Automatic Power-Down when a set $\overline{EOM}$ or overflow is reached. $\overline{RECLED}$ pulses LOW momentarily at the end of the message. This pulse is an $\overline{EOM}$ pulse. The $\overline{PLAYL}$ or "play level" pin must be held LOW for the duration of the Playback. If it is taken back HIGH, Playback ceases. A $\overline{PLAYL}$ initiated Playback cycle will stop and Power-Down when a set EOM or overflow is reached even when the input is held LOW. Power-down is always automatic, regardless of how the Record or Playback cycle is ended.

The ISD1100 series has built in pull-up resistors on all three control inputs ($\overline{PLAYL}$, $\overline{PLAYE}$, and $\overline{REC}$). The presence of these on-chip resistors enables simple push buttons to control each input without other external components.

The ISD1100 series also has pull-up resistors on address lines A6 and A7 and pull-down resistors on A0 through A5. A Record or Playback Operation that begins with the address pins set in this manner will proceed exactly as if the device was addressed at address 0 with no Operational Mode set.

Additionally, the XCLK pin of the ISD1100 also has a pull-down resistor.

Care should be taken when using an ISD1100 series device in extremely LOW power applications. The input pins should not be continuously held "opposite" the associated on-chip resistor. Each pin with a pull-up or pull-down resistor has the potential for drawing approximately 50 μAmps of current when held at other than the correct supply voltage. For instance, if A6 and A7 were connected to V_{SS} in a circuit using an ISD1110, approximately 100 μAmps would be continuously dissipated. This current would be dissipated even when the device is powered down. The ISD1200 and ISD1400 devices do not have these pull-up or pull-down resistors.

CASCADING MULTIPLE DEVICES (ISD1000A, ISD2500)

Devices from several of the ISD device families may be cascaded together to enable the designer to achieve longer record and playback times. Both the ISD1000A series and the ISD2500 series have internal logic to enable the designer to easily cascade multiple devices. There is less than two microseconds of dropout when changing from device to device.

CASCADING THE ISD2500 SERIES

A complete cascading application for the ISD2500 series with a detailed explanation of its operation is included in the circuit example section that follows. There is also an explanation in the "Operational Modes" section under Application Information.

NOTE *The ISD2500 series includes additional logic to enable additional cascading features not provided in the ISD1000A series. This is covered in detail in the "Device Operation" under Application Information.*

CASCADING THE ISD1000A SERIES

In brief, the operation of $\overline{CE}$ and $\overline{EOM}$ during cascade operation proceeds as follows:

1. Set up the Operational Mode for cascade (A2, A5, A6 and A7 all HIGH).
2. A Record or Playback cycle is started with $\overline{CE}$.
3. When the first device in the cascade goes into overflow to indicate it is at memory end, the $\overline{EOM}$ pin goes LOW to provide a $\overline{CE}$ signal to the next device in the cascade.
4. Following devices are enabled in the same manner down the line.

Audio processing in the cascade mode may be handled several different ways. The easiest application uses the first device's microphone preamplifier and it's ANA OUT output during record to drive the ANA IN pins of each device in the cascade circuit. During playback, the SP+ output is fed back to the preceding device's AUX input. The first device in the series is connected to a speaker and provides the audio output for the system. Other methods will be discussed in the applications section.

ADDRESSING ACROSS A MULTI-DEVICE BOUNDARY (ISD1000A, ISD2500)

Some users of the ISD analog storage devices may need more address space than provided in a single device. The following description discusses methods by which the ISD1000A series may be used to achieve additional storage space. A method of accomplishing this with the ISD2500 series is included in the "Circuit Examples" under Application Information.

ADDRESS ACROSS A MULTIDEVICE BOUNDARY USING THE ISD1000A SERIES

There are two ways to approach this application. The simpler solution occurs when any single message is short and it is possible to contain any given selection of messages within a single ISD1000A. In this case, each device is addressed individually and the short message to be played is selected as needed.

The more complicated application requires a message field that is totally independent of chip boundaries. The ISD1000A device combines two functions in the $\overline{EOM}$ output pin. These two functions are end-of-message indication and overflow. If the system using the ISD1000A can retain a time map of each word or phrase stored, it can arbitrate this signal and determine which condition is occurring. It is necessary to have a system time resolution of less than 25 ms to accomplish this. It may also be necessary to externally drive the ISD1000A device's clock to achieve proper time synchronization.

When the controlling logic or microprocessor determines that an overflow has occurred, it will immediately drop $\overline{CE}$ to the next ISD1000A so that the audio output can continue.

The Operational Mode used in the cascading application described in "Device Operation" cannot be used when addressing across a chip boundary. This is because Operational Mode and the addressing of individual messages do not coexist.

LOOPING CONSIDERATIONS

There are several applications that require continuous, or intermittent, looping of record or playback of audio sound effects, voice, etc. All ISD single-chip voice record/playback devices have the ability to perform this task either self-contained on-chip or with external logic. The circuit example section of this document includes several different applications that fit different requirements.

Two basic methods are used to loop record or playback ISD devices. The first method uses an Operational Mode to carry out the loop. Only a message that begins at address 000 (the beginning of the memory) and does not completely fill the memory may be looped this way with the ISD1000A devices. The memory may be completely full in the ISD1100/1200/1400 or ISD2500 series.

The second method uses external logic to create a looping condition. A signal from $\overline{EOM}$ or $\overline{RECLED}$ is used to pulse $\overline{CE}$ or $\overline{PLAYE}$ to start a new repetitive playback cycle.

LOOPING WITH A CONTINUOUS TONE

Some customers want looping to generate a continuous tone for an extended period of time. The ISD Applications group achieved this using the $\overline{CE}$ initiated looping method in an ISD1016A with moderate results. A perfect waveform match at the transition between the end of memory (indicated by the $\overline{EOM}$) and beginning of the next cycle through the loop is difficult to achieve. The worst case 25 ms $\overline{EOM}$ granularity defines the problem.

Intermittent looping may be achieved using a timer (such as an NE555) reset by the $\overline{EOM}$ output. Upon time-out, the timer executes a new $\overline{CE}$ or Power-Down cycle starting the playback over.

CONTINUOUS RECORD LOOPING (ISD1000A)

Another frequently requested application schematic is a continuously looping record. Several considerations must be kept in mind including the write wear out mechanism inherent in EEPROM memory cells. A discussion of this phenomenon is found under Write Endurance Considerations in this chapter. A second consideration is how important it is for the user to know exactly where the looping record ends. If the looping record always ends on memory overflow, then the application is simple. If an accurate replay of the "last N seconds" is required, stopping at a random time, then the circuit requirements are more complex.

A looping record application in an ISD1000A device uses the $\overline{EOM}$ signal to start a new $\overline{CE}$ Record cycle. Since $\overline{EOM}$ is the overflow indication during Record, this signal indicates the end of the memory space. It is time to start Record over at the beginning of the memory. If you choose to stop the loop and playback the memory at the EOM boundary, then the memory contains the last N seconds of recorded data according to which of the ISD devices were used in the application.

The more complex (and more general) requirement is that the Record loop end at a random time. If $\overline{CE}$ is taken HIGH during a looping Record cycle the internal address location of this event is not available to external logic. An EOM bit is written into the memory to indicate this location. The ISD devices do not include a mechanism to read out the memory location of this EOM. Also, the transition from Record to Playback resets the internal address counter to 000.

It is easy to determine the point where recording ended in the Record Loop Application. It will be marked with a set EOM bit. The message cueing Operational Mode may be used to find this location in a few milliseconds and playback may then begin at exactly where Recording ceased.

CONTINUOUS RECORD LOOPING (ISD1100/1200/1400 AND ISD2500)

The M3 Looping Operational Mode is available in the ISD1100/1200/1400 and ISD2500 series devices during Record as well as Playback. Continuous record looping is possible in those products using only Operational Mode input address strapping.

AUDIO DRIVE LEVELS AND IMPEDANCES

The ISD devices may be driven by an external source other than a microphone. The characteristics of the two inputs are shown in Table 1.

EXTERNAL COMPONENTS

The ISD products require only a few external components in most applications. A list of these components and comments follow:

BYPASS CAPACITORS

A playback only application typically does not need bypass capacitors. In fact, a playback only application in an ISD1000A or ISD2500 can operate with switches and a speaker and no other components. An ISD1100 playback only circuit only requires the chip, a push-button and the speaker (since the $\overline{PLAYE}$ pull-up resistor is contained on-chip). Several of the circuits in the "Circuit Example" section under Application Information.

A record and playback application should have low impedance high frequency bypass capacitors from each V_{CC} power supply pin to ground. A value of 0.1 μF is recommended. In addition, a

large capacitor for low frequency bypassing should be used to further decouple the power supply. A value of 10 to 100 μF should work adequately.

Table 1: Drive Levels and Impedances

	MIC (Pin 17)	ANA IN (Pin 20)
Input Impedance	≈10 KΩ	≈2.7 KΩ
Max. Drive Level	20 mV p-p	50 mV p-p
AGC Control	up to 20 dB	none

COUPLING CAPACITORS

An application that directly drives one of the input pins of the ISD device requires a coupling capacitor to DC isolate the input. The design issues of concern are the required voltage specification for the capacitor, capacitor leakage and capacitor value. The value of the capacitor is determined by the required frequency response and this is covered elsewhere in this document.

NOTE ISD does not recommend using tantalum capacitors in coupling capacitor applications.

RESISTORS

In a typical application, resistors are not used in any gain or level critical areas. A 10 percent tolerance is adequate for most applications.

POWER SUPPLY CONSIDERATIONS

Standard ISD devices are designed to operate from a single 4.5 to 6.5 volt power supply, except for the ISD33000 series, which operates from a single 2.7 to 3.3 volt power supply. This supply should have a low internal impedance and be noise free. These factors are especially critical during the recording process; any high frequency noise appearing at the V_{CCA} supply pin (pin 16) may be recorded into the device's memory array. For this reason, it is also important that the connections to the power supply be short, and have little series resistance or inductance. Additionally, some types of power supplies tend to contain noise that falls within the passband of the ISD device. For instance, aircraft power supplies operating from 400 cycle AC or switching power supplies may require additional DC filtering to ensure they are "quiet."

Playback only applications are not as critical and can stand a higher internal power supply source impedance without appreciable sound quality degradation.

BATTERY OPERATION

Batteries are often used to power ISD applications. All ISD product families now support operation from 4.5 to 6.5 volts, except for the ISD33000 series, which supports operation from 2.7 to 3.3 volts. Higher voltage sources must be regulated down to this range. A simple shunt zener diode regulated supply is adequate for the average application that does not require low power. In multichip situations the zener is inadequate and a three terminal regulator must be used.

The designer of any passively regulated battery source supply should keep in mind that the internal resistance of a battery increases rapidly as it approaches a discharged condition. If this impedance is not lowered by effective decoupling, record quality will degrade.

If reliable high quality record and playback are required from a battery source supply, the designer should use a higher voltage battery and an active regulation device such as a 5-volt three terminal regulator.

LOW POWER OPERATION

Many applications of the ISD devices need long-life low-power battery operation. The ISD1100/1200/1400 and ISD2500 Families have automatic power down options to help achieve this goal. If the ISD1000A series is used, the PD pin must be taken HIGH using external circuitry to gain the very low power standby state. By using any of the

above procedures, standby currents near the "shelf life" of many batteries may be achieved. The actual battery life, of course, depends on how often the device is operated.

RECORD/PLAYBACK NOISE CONSIDERATIONS

A number of factors influence the practicable signal-to-noise record performance of the ISD devices. The power supply sensitivity has already been covered. Proper PC board layout can effect a large improvement in signal-to-noise by keeping the noise generating parts of the circuit separated from the low level input pins. The pins with a noise sensitivity are MIC (pin 17), ANA IN (pin 20), AGC (pin 19), and MIC REF (pin 18). Additional information on PC board layout may be found in the "Single-Chip Board Layout Diagrams" under Application Information.

The principal noise source from the ISD devices is V_{CCD}, pin 28, and during a Record cycle only. The frequency distribution of this noise may be found in several regions. One source is centered around 80 Hz which is the repetition rate of the internally generated EEPROM programming power supply. Another source may be found between 30 MHz and 200 MHz in a number of discrete bands. An FCC recognized testing lab has done an evaluation of the radiation from an unshielded ISD1016A recording application. The results from that investigation show the emissions to be below the FCC Class B Radiation Limit for a computational device. The results are available from ISD upon request.

There is no substantial noise source during a playback cycle. However one will hear the inherent noise from the array. This is a very low level "hiss." When viewed on an oscilloscope, the amplitude will be about 10 mV p-p from either speaker lead to ground. Measured with an AC meter this noise will be less than 4 mV RMS. This is from a recording made with ANA IN, pin 20, connected to ground through a 0.1 μF capacitor.

One potential noise source during record or playback of ISD single-chip voice record/playback devices is voltage over- or under-shoot on signals connected to the address and control pins. Continuous or very short duration signals (for instance address transition "ringing") greater than 0.3 volt over V_{CC} or under V_{DD} may cause a considerable increase in recorded noise. Care should be taken to ensure signals on all pins are always within data sheet specifications (currently 0.3 volts over- or under-shoot).

LOW NOISE AND/OR HIGH-POWER OUTPUT APPLICATIONS

Some applications need extremely low noise record and playback. A good example of such a requirement is where the output of an ISD device is going to be amplified and used to drive a high power public address speaker system. One method of achieving an improved signal-to-noise ratio is to use the speaker outputs to drive an expander circuit such as found in the Philips/Signetics NE575 Low Voltage Compandor. Since the ISD device records using automatic gain control, the expander half of the NE575 may be used by itself to re-establish the dynamic range of the original recording and attenuate background noise. The results are impressive with virtually no detectable noise in the "dead time" between words and phrases. Other circuits similar to the Phillips chip can achieve comparable results.

Additionally, a circuit such as the NE575 or high-power amplifier stage should be driven differentially from the ISD device. When the speaker + (or –) output is used to drive the next stage in a single ended configuration, a transient is generated when the speaker outputs are pulled to ground during the Power-Down or a Record Operation. This transient results in a loud pop. If output is taken differentially, this transient is minimized because both pins are taken to ground together.

An example application using the NE575 expander driven differentially is found in the "Circuit Examples" under Application Information. An example of an amplified speaker output circuit may also be found on the next page.

MAKING IT SOUND LOUDER

Many applications for ISD devices use very small speakers, often less than two inches in diameter. The basic sampling system used by all ISD single-chip voice record/playback devices in itself supports a wide frequency response, only limited in low frequency by the value of the coupling capacitors in the microphone and ANA IN to ANA OUT circuits. Small speakers usually do not reproduce low frequencies well. The result is that a "full bandwidth" recording often does not sound very loud when played through such a speaker. Another way to look at this is that the low frequency components consume much of the output power of the ISD speaker driver. This power is not usable by a small speaker.

One method of recording "louder" signals that reproduce well through a small speaker is to limit the ISD device's low-end frequency response. This may easily be done by decreasing the size of the coupling capacitors used in the microphone circuit. The ISD1400 data sheet shows 0.1 μF capacitors connected to MIC and MIC REF. This value results in signals above 160 Hz being recorded without attenuation. A better choice for a small speaker system is to change these capacitors to 0.01 μF. This results in a low end pole of approximately 1500 HZ, sharply rolling off frequency response below this value.

The resulting recording will be made without the low frequencies that distort a small speaker. The relative "loudness" of the playback will be increased.

The circuit designer should try several values of capacitance to determine what is best for a specific application.

REALLY MAKING IT LOUDER

The on-chip speaker drivers present in all current ISD single chip voice record/playback devices have adequate power output for most applications. Some applications, however, need more speaker power than these chips provide. Fortunately, a number of manufacturers make single chip or single module speaker amplifiers that range from a few hundred milliwatts to 50 watts or more into an 8 Ω load.

Most of these speaker amplifier devices are supported by manufacturer's applications information that shows a single ended connection to the audio source. In the case of the ISD products, however, there are advantages to a balanced feed to the amplifier circuit. The potential pop resulting from a Power-Down cycle, for instance, may be avoided by driving the speaker amplifier from both SP+ and SP–. Fortunately, many of the available speaker driver products have an operational amplifier front end that includes a differential input.

The following two circuits demonstrate the general method that may be used to increase the speaker drive from ISD products.

NOTE *ISD customers are strongly encouraged to obtain the appropriate data sheet from the listed manufacturer to determine exact device specifications and the suitability of these devices in their specific application.*

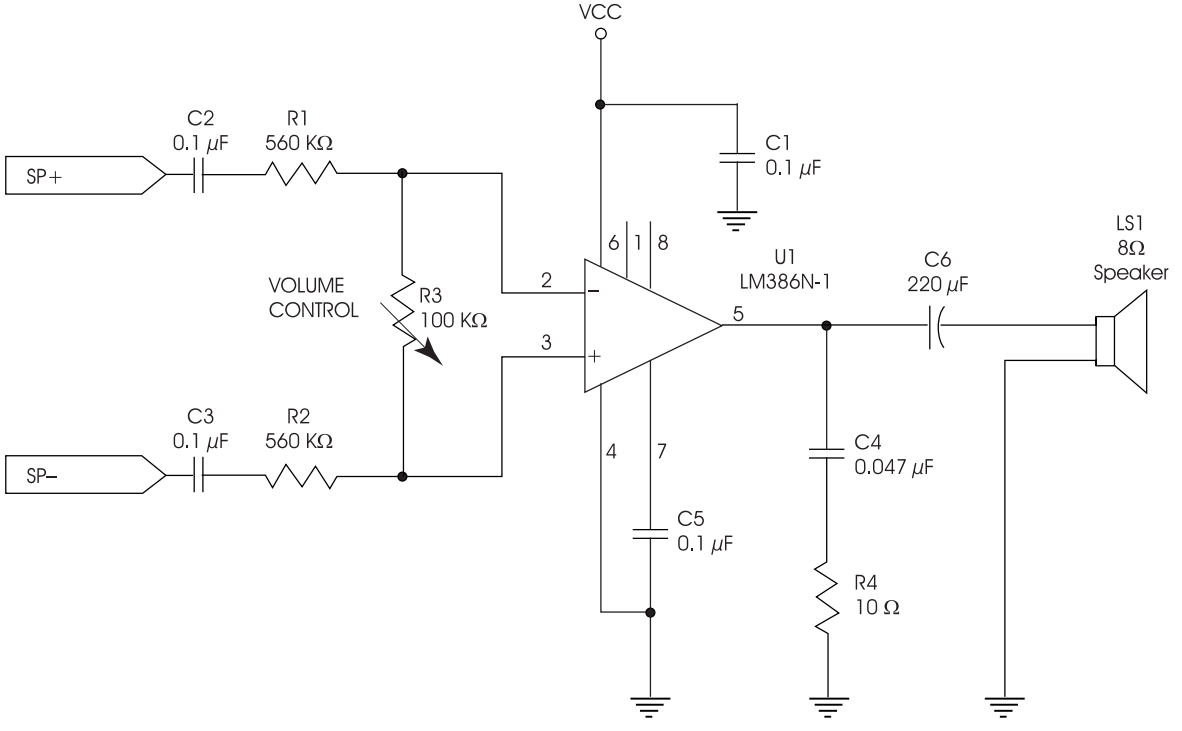
USING THE NATIONAL SEMICONDUCTOR CORPORATION LM386 LOW VOLTAGE AUDIO POWER AMPLIFIER

The NSC LM386 amplifier was designed for use in low voltage consumer applications. According to the NSC data sheet, it will operate over a voltage range of 4 to 12 volts or 5 to 18 volts. The voltage gain is adjustable from 20 to 200. At 6 volts the typical power output is 325 mW, at 9 volts it is 700 mW. (These numbers are at 10 percent THD.) In the circuit in Figure 1, the output level of the ISD device must be attenutated by resistors R1 and R2 before it can be applied to the inputs of the LM386. This is because the ISD device output leads are designed to drive a speaker directly to 12.5 mW. The voltage swing drives the LM386 into distortion if not reduced. At 5 volts, the value required is approximately 1 MΩ; at 9 volts the resistors can be at 560 KΩ. This is because the input pins of the LM386 have about a 50 KΩ to ground impedance, forming a voltage divider. Using 560 KΩ resistors and putting the 100 KΩ potentiometer R3 across the input pins creates a volume control.

The LM386 data sheet includes various applications circuits, all single ended. To eliminate the "pop" that can occur with the ISD speaker outputs being used single ended, the LM386 is used differentially. This lets the common mode rejection of the LM386 reduce the "pop" considerably. Because the differential connection is DC isolated, the LM386 can be run at any voltage in its allowable range while the ISD device remains at 5 volts. This give the designer some options as far as required power output for the particular application.

In the example circuit in Figure 1, pins 1 and 8 are left open for minimum gain of 20 in the LM386N-1. Then a volume control is provided in the potentiometer (R3) across pins 2 and 3.

Figure 1: LM386 Speaker Driver

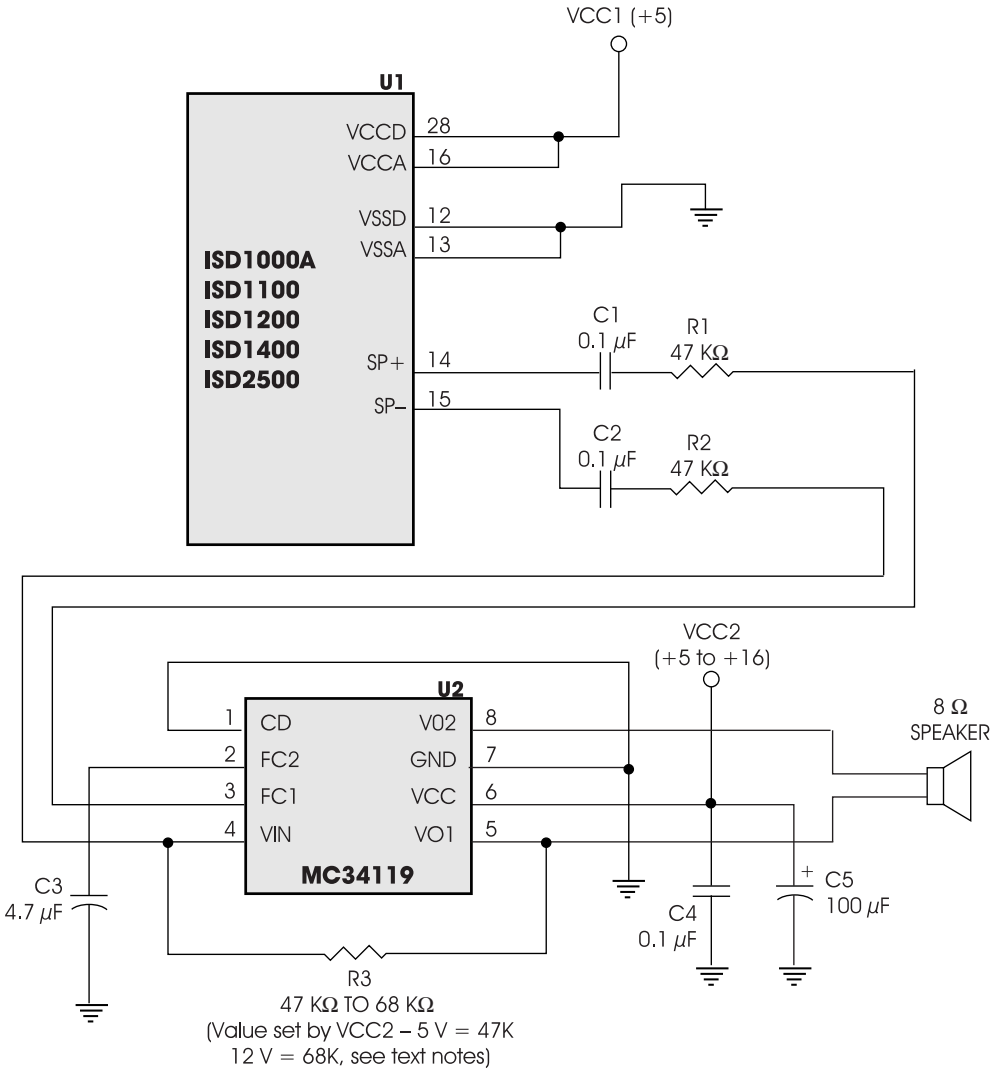


USING THE MOTOROLA MC34119 LOW-POWER AUDIO AMPLIFIER

The MC34119 low power audio amplifier integrated circuit, shown in Figure 2, was intended primarily for telephone applications. According to the Motorola data sheet, it operates over a voltage range from 2 to 16 volts and can supply up to 250 mW into a 32 Ω speaker. It can drive speaker loads down to 8 Ω. The MC34119 does not automatically power down. If the CD pin (pin 1) is taken to V_{CC}, however, the device will power down to typically less than 1/2 mA.

The circuit used with the MC34119 is similar to that used with the NSC device. The FC1 and VIN inputs are driven differentially from the ISD Speaker outputs. Speaker volume is set by adjusting the value of R3 which is a feedback resistor used to set gain in the MC34119. Care should be taken so that the Motorola amplifier's package power dissipation specification is not exceeded. The designer may wish to derive a control signal to drive the CD pin to lower circuit power consumption when not in use.

Figure 2: MC34119 Speaker Driver



WRITE ENDURANCE CONSIDERATIONS

Conventional EEPROM technology exhibits a long term failure mechanism defined by the term "Write Endurance." This means that each bit in the memory may be reliably erased and written only a certain number of times. Numbers commonly specified by EEPROM digital memory manufacturers for this phenomenon are 10^5 write cycles.

The ISD devices realistically exhibit a Write Endurance number of one to two orders of magnitude better than conventional EEPROM products for two reasons:

- The writing process used by ISD results in less stress on the memory cell. Digital EEPROMs program the cell with a large in-rush of current. This in effect "blasts" a "1" or "0" into the cell. The ISD devices meter small amounts of charge onto the cell during the closed loop writing sequence.
- A single cell failure during the programming of a digital EEPROM is devastating and renders the memory unusable. A single cell failure in a ISD device results in an imperceptible change in distortion. In fact, many random failures

would have to occur before recording quality would noticeably degrade.

ISD believes that typically 10^5 write cycles may be executed in an ISD device without noticeable effect on record and playback quality.

RECORDING TECHNIQUES

Some applications require the recording of sound from some other media into an ISD device. This is easily accomplished if care is observed in several areas:

Input levels

Care should be exercised during recording to ensure that the input level specifications are observed. If levels are too low, background noise may be objectionable. Too high a level during Record may cause clipping of the output waveform during playback.

ANA IN input

Driving the ANA IN input will result in the highest quality and lowest distortion recording. The effective dynamic range, however, will be less than when driving the MIC input because of the AGC in the microphone preamplifier. (50 mV P-P maximum to ANA IN.)

MIC input

Driving the MIC pin gives the largest dynamic range during record. However, this AGC controlled amplifier stage will contribute some distortion due to the gain control process. (20 mV p-p maximum to MIC.)

Program material

The user should experiment with the programming to be recorded. Certain types of music, speech, sounds, etc., may record better through one input than another. Also, program material with a large dynamic range may give unacceptable results because quiet passages may sound noisy while loud passages are distorted.

UNEXPECTED RECORD

Sometimes an unexpected recording takes place when a circuit is powered up. This "undesired recording" puts an EOM at the very beginning of the memory. Then, when one goes to playback the previously recorded message, it is gone! Actually, it is still there but the EOM is detected in the first row and the device quits playing. The original message is no longer accessible for normal playback from address 000.

The reason for this undesired effect is in the type of network used to control the $\overline{CE}$ pin. (The same effect can be observed on the ISD1100/1200/1400 $\overline{REC}$ pin.) Although the ISD device has a power down circuit so one does not need to disconnect the battery, some customers chose to disconnect the battery anyway. Depending upon their circuit design they may be able to eliminate all standby current this way. However, even when the power is normally connected all the time, the problem can appear when changing the battery.

This is because the V_{CC} voltage to the device may rise faster than the voltage at the control pins. The normal state of the control pins is HIGH. They are taken LOW to signal a request. They are normally held HIGH by external pull-up resistors. As long as power is applied, this is just fine. But, depending on the capacitance at the pin, and the value of the pull-up resistor, when the power is applied, the pin may go HIGH more slowly than the internal V_{CC}. So, after the device has sufficient V_{CC} to operate, 100 nanoseconds after the internal POR delay, it will detect a LOW at $\overline{CE}$. If P/$\overline{R}$ is also LOW, it will begin a Record Operation that will end very quickly as the time constant of the resistance and capacitance attached to the $\overline{CE}$ pin lets the voltage rise above the detection threshold.

A simple method to eliminate this situation is to have a capacitor (a starting value could be 0.001 μF) connected from the control pin to V_{CC}. Then, with power up, that capacitor will bring the pin voltage up with V_{CC} as it rises. This is because one cannot change the voltage across a capacitor instantaneously. Once the voltage is HIGH, the pull-up resistor will keep the pin HIGH until it is activated. Thus, the spurious Record command is eliminated.

It is important to note that this situation will not be noticed in all circuit designs, being dependent upon the capacitance of the printed circuit board and the device input itself. However, it should be accounted for to ensure the reliability of any design.

MESSAGE CONCATENATION

Prompting applications often need the concatenation of words or phrases to build sentences. This requires the ability to directly address a word or phrase, start the operation, then detect when the word has completed. This capability is included in all families of ISD Analog Storage Devices. The following example message demonstrates one method of achieving this goal.

Play the sentence "I like computers." An ISD2560 had been previously recorded with the following words, "I" located at address 95 (decimal), "like" located at address 140, and "computers" located at address 490.

The address of 95 (HEX 5F or 0101 1111) is placed on the ISD2560's address pins. A normal playback cycle is started by pulsing $\overline{CE}$ LOW. After the playback begins, $\overline{CE}$ remains HIGH. When playback ends, $\overline{EOM}$ will go LOW for 12.5 ms, then come back HIGH. Playback of the word "I" will not actually end until $\overline{EOM}$ goes back HIGH.

The address of 140 is now placed on the ISD2560's address inputs and another playback cycle is begun. The word "like" will now play and will not complete until the $\overline{EOM}$ signal pulses LOW, then goes back HIGH.

The address of 490 is now placed on the ISD2560's address inputs and a final playback cycle is begun. As with the other two steps, the word "computer" will not finish being played until $\overline{EOM}$ goes back HIGH.

CONCATENATION CONSIDERATIONS

There is an art to successfully creating good sounding concatenation. Timing, inflection, pitch and rhythm all work to help or hinder the finished "product" of words and phrases. The first step in successful concatenation is the preparation of a script of phrases and sentences to be recorded. From this script comes a list of needed words. It may be necessary to record and store some words more than once due to the required inflection in different phrases.

A master recording is made from this script. This recording is processed, if necessary, to eliminate unneeded pauses and noise. The master recording is then used to create a master chip with all the words and phrases at known addresses. Now we can say "I like computers" without anyone moving their lips.

CREATING A MASTER SOUND FILE

The following steps show one method of generating a master chip. A Creative Labs Sound Blaster 16™ is used with the ISD-SD101 Sound Development and Programming System.

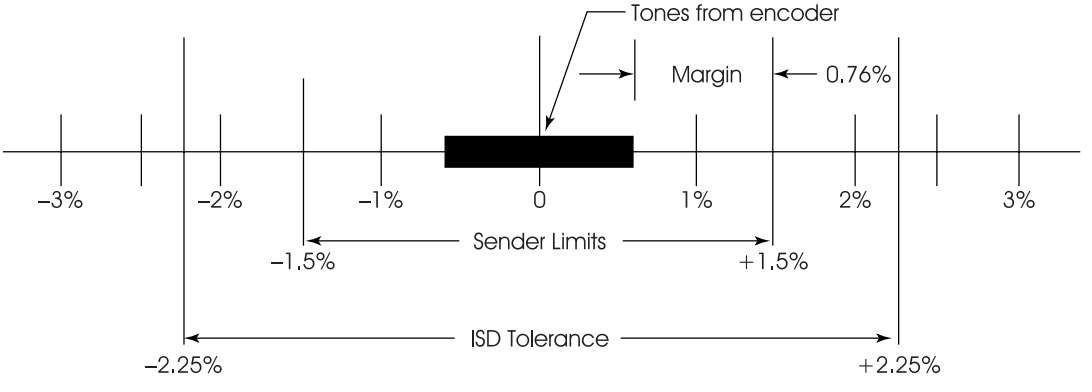
1. The list of words (with correct inflection indicated in some manner) is given to the announcer who makes an analog or digital recording of each one. This recording is loaded into the memory of an IBM® compatible PC using a Creative Labs Sound Blaster 16 operating under Windows™ versions 3.1 and 3.11. **The speech is stored in an 8-bit .wav file sampled at 22,050 Hz in the monophonic mode.**
2. The Creative WaveStudio™ program (or a similar sound editor) is used to edit each word from the list. Quiet periods, delays and noise may be edited out using this software. Record level may be changed and special effects added.
3. The editing software is used to generate one file per word or phrase in .wav format. These files are then converted to the .voc format.

4. The ISD-SD101 Sound Development and Programming System software is now loaded. The word and phrase .voc files are selected and brought into the program.
5. The graphical interface of the ISD-SD101 Software is used to position each sound file into the selected ISD device memory. Address boundaries, EOM locations and unused space are visually identifiable.
6. When required positioning and mapping of the sound files is achieved, the ISD-SD101 Software allows the generation of an address map of the sound files and creates a .chp file to be used to program one or more ISD devices.
7. The ISD-SD101 may be used to program up to eight devices at one time in a production environment.

SENDING & STORING DTMF WITH ISD DEVICES

Many people have asked about using the ISD devices to store and send DTMF dialing digits. This seems practicable since they are using the devices to store the message that will be sent when the telephone connection is made. By doing this they may eliminate an additional DTMF dialer chip in the product. The DTMF digits are "In-Band Signaling" as they are in the same frequency range as the voice passed through the telephone or radio network.

Figure 3: DTMF versus ISD Frequency Tolerance



Much of the time this idea will work well, especially if the voltage or temperature is not varied on the ISD device between record and playback. To be confident that this idea will always work, the ISD devices must be clocked from external clock sources with a tolerance of less than ±0.25 percent (refer to Figure 3).

This is because of the following facts:

- The Bell Telephone DTMF sending tolerance is ±1.5 percent of the nominal values.
- DTMF encoder chips are crystal controlled but, because of their divider chains, are actually creating tones that are +0.74/–0.54 percent, for example, when the crystal is exactly 3.579545 MHz.
- The internal oscillator specification for most ISD devices is ±2.25 percent over voltage and temperature.

Dividing the margin in half to allow for the worst case variation between Record and Play Modes gives 0.38 percent. This suggests a tolerance of better than ±0.25 percent is needed on the external clock signal provided to pin 26 of the ISD devices. It can be either TTL or CMOS levels. Using the ISD2560 as an example, the internal clock frequency is 1.024 MHz for the 8 KHz sampling rate.

In a typical application that utilizes a microprocessor or microcontroller there is a crystal oscillator to provide the system clock. This is often 2, 4, or 8 MHz. By using the necessary divider stages a 1 MHz signal could be made available to the ISD2560. This is close enough to 1.024 MHz to use without any problem. The requirement is not so much exact frequency as it is constant or repeatable frequency. The main system crystal can provide that.

OPERATION ABOVE 5.5 VOLTS

The standard operational voltage specification for packaged ISD products (except the ISD2500 series) is 4.5 to 5.5 volts. Above 5.5 volts, distortion may increase unless care is taken to make sure the internal storage array is not overdriven. ISD recommends that a resistor of 5.1 KΩ be put in series with the capacitor between ANA IN and ANA OUT. An example of this network may be found between pins 20 and 21 in "Circuit Examples" under Application Information.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Basic Addressing

ISD single-chip voice record/playback devices include the capability of addressing multiple messages in a single chip. The address inputs provide the ability to partition the message space into a number of equal segments. They also provide access to the Operational Mode options of the device. The address inputs are positive logic and may be thought of as either binary or hex addressed. The binary convention is used in this manual.

Note that the address lines do not correspond to individual message numbers. One or more address lines must be HIGH and set to the correct *binary address* for a message to start anywhere in the memory.

The several series members have different sizes and addressing capability. Table 1 details these differences.

All the above devices are addressed in a similar manner. When addressing one of the 160 "message addresses" of the ISD1000A, for example, we are actually controlling a register in the device called the Message Start Pointer (MSP). The MSP points to where the next Record or Playback operation will begin. Usually, the address inputs pre-load the MSP when a chip enable or power-down initiated operation takes place. The Operational Mode Section will explain the exceptions.

Table 1: Array Size, Addresses, and Message Segments

Devices	Array Size	Binary Number of Add.	Actual Message Segments
ISD1100 Series	64K	256	80
ISD1200 Series	64K	256	80
ISD1400 Series	128K	256	160
ISD1000A Series	128K	256	160
ISD2532/40/48/64	256K	512	320
ISD2560/75/90/120	480K	1024	600

Table 2 shows the storage time, message resolution and the possible number of message addresses for the currently available ISD products.

To determine the value in the MSP, divide the message resolution of the device by the number of counts. For example, to start recording or playing back at the 4-second boundary of an ISD1016A, load the device with an address of 40 (when converted to binary, the actual physical address is 0010100).

Note that in addressing an ISD device, the address is how far "into" the message space MSP the is pointing. The address does not show how much time remains in the memory.

Table 2: Address Resolution

Device Part Number	Storage Time (seconds)	Msg. Resolution (msec)	Number of Message Addresses
ISD1016A	16	100	160
ISD1020A	20	125	160
ISD1110	10	125	80
ISD1112	12	150	80
ISD1210	10	125	80
ISD1212	12	150	80
ISD1416	16	100	160
ISD1420	20	125	160
ISD2532/60	32/60	100	320/600
ISD2540/75	40/75	125	320/600
ISD2548/90	48/90	150	320/600
ISD2564/120	64/120	200	320/600

NOTE: *Storage time and resolution subject to clock tolerances.*

Tables 2, 3, and 4 show example address boundaries for the ISD single-chip voice record/playback series products. They also show the address boundaries of unused space and the Operational Modes.

Message Addressing and Operational Mode Operations are mutually exclusive modes of the ISD devices. When Operational Mode is used, the MSP is always initialized to 0 (Unless an overriding Operational Mode is selected. See "Operational Modes" on under Application Information).

The ISD devices may be thought of as analog tape recorders with the capability of positioning the record/playback head anywhere on the tape at the address resolution given for each device. In the rest of this explanation on addressing, the ISD1016A will be used as the example. For a full list of all the ISD device address locations with time conversions for each device, see "Address Segment Resolution" under Application Information.

EXAMPLE OF RECORD AND PLAYBACK AT AN ADDRESS BOUNDARY

For this example, we are going to record a message starting at the 10 second boundary in an ISD1016A. Start by taking the PD pin to a LOW state and delaying T_{PUD} (see data sheet for the timing of the various ISD devices). An address of 100 (100 X .1 = 10 seconds) should be applied to the address pins. Converting 100 to binary we get the address of 01100100. Next take the P/$\overline{R}$ pin LOW. To begin record, take $\overline{CE}$ LOW and hold it in that state for the duration of the record time. When $\overline{CE}$ is taken back HIGH, the recording will end and an EOM bit is set in the EOM memory.

Table 3: ISD1100 and ISD1200 Address Space

Dec.	Binary								ISD1100/1200 (Seconds)
	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0.125
8	0	0	0	0	1	0	0	0	1.0
10	0	0	0	0	1	0	1	0	1.25
13	0	0	0	0	1	1	0	1	1.625
50	0	0	1	1	0	0	0	0	6.25
64	0	1	0	0	0	0	0	0	8.0
79	0	1	0	0	1	1	1	1	9.875
80	0	1	0	1	0	0	0	0	
through	Unused address space. An ISD1100/1200 device addressed in this region will default to an overflow condition.								
191	1	0	1	1	1	1	1	1	
192	1	1	0	0	0	0	0	0	
through	This address space used by the ISD1100/1200 Operational Modes.								
255	1	1	1	1	1	1	1	1	

To playback a message previously recorded at the 10-second boundary, the address pins are again loaded with an address of 100, and with PD LOW and P/$\overline{R}$ HIGH, $\overline{CE}$ is pulsed LOW. The ISD1016A will play back the message, stopping when it finds the set EOM bit. At the same time, the $\overline{EOM}$ pin will pulse LOW to indicate a message end. Whenever a Record operation is in progress and passes through the time of a previously set EOM bit, the bit is cleared. Thus, the EOM is recorded over and "erased."

SIMPLIFIED ADDRESSING SCHEMES

The ISD devices have eight, nine or ten address lines, depending upon which series is considered. For full control of the addressing this means that an 8- or 10-bit latch or microcontroller port must be used to completely address the ISD analog storage chip.

Table 4: ISD1000A and ISD1400 Address Space

Dec.	Binary								ISD1016A ISD1416 (Seconds)	ISD1020A ISD1420 (Seconds)
	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0.1	0.125
8	0	0	0	0	1	0	0	0	0.8	1.0
10	0	0	0	0	1	0	1	0	1.0	1.25
13	0	0	0	0	1	0	0	0	1.3	1.625
50	0	0	1	1	0	0	1	0	5.0	6.25
100	0	1	1	0	0	1	0	0	10.0	12.5
159	1	0	0	1	1	1	1	1	15.9	19.875
160	1	0	1	0	0	0	0	0		
through	Unused address space. An ISD1000A/1400 device addressed in this region will default to an overflow condition.									
191	1	0	1	1	1	1	1	1		
192	1	1	0	0	0	0	0	0		
through	This address space used by the ISD1000A/1400 Operational Modes.									
255	1	1	1	1	1	1	1	1		

Table 5: ISD2500 Address Space

Dec.	Binary										ISD2560 (Seconds)	ISD2575 (Seconds)	ISD2590 (Seconds)	ISD25120 (Seconds)
	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0	0	0	0	1	1	0	0	1	0	5.0	6.25	7.5	10.0
100	0	0	0	1	1	0	0	1	0	0	10.0	12.5	15.0	20.0
250	0	0	1	1	1	1	1	0	1	0	25.0	31.25	37.5	50.0
300	0	1	0	0	1	0	1	1	0	0	30.0	37.5	45.0	60.0
400	0	1	1	0	0	1	0	0	0	0	40.0	50.0	60.0	80.0
500	0	1	1	1	1	1	0	1	0	0	50.0	62.5	75.0	100.0
599	1	0	0	1	0	1	0	1	1	1	59.9	74.875	89.85	119.8
600	1	0	0	1	0	1	1	0	0	0				
through	Unused address space. An ISD2500 device addressed in this region will default to an overflow condition.													
767	1	0	1	1	1	1	1	1	1	1				
768	1	1	0	0	0	0	0	0	0	0				
through	This address space used by the ISD2500 Operational Modes.													
1023	1	1	1	1	1	1	1	1	1	1				

Many product designs use small, inexpensive microcontroller chips and do not have sufficient port pins to handle the ISD device for full addressing. This need not be a serious obstacle. Most of these same applications do not need 100 ms. resolution of the address space. They can operate with less resolution. For each degree of resolution that is not used, one less port pin is needed. The following table (a simple binary count) illustrates this principle using an ISD1016A or ISD1416 as the example.

Table 6 indicates that by grounding the four least significant address bits, A0–A3, one can still address messages with a 1.6 second resolution using only four port or latch outputs. This would provide ten different 1.6-second message segments in an ISD1016A (ten 2-second messages in an ISD1020A) and might make it possible to use a smaller, less expensive microcontroller.

Table 6: ISD1016A or ISD1416 Address Resolution

Address Line	No. of Address Lines	Address Resolution (sec)
A0	8	0.1
A1	7	0.2
A2	6	0.4
A3	5	0.8
A4	4	1.6
A5	3	3.2
A6	2	6.4
A7	1	12.8

By some study of the addressing scheme many different combinations of simplified addressing can be developed. Another example is to have four 2.5-second messages in an ISD1110 or ISD1210 device by using only two address lines from the controller.

Table 7: ISD1110 or ISD1210 Four Message Approach

Msg #	Addr	A7	A6	A5	A4	A3	A2	A1	A0
1	000	0	0	0	0	0	0	0	0
2	020	0	0	0	1	0	1	0	0
3	040	0	0	1	0	1	0	0	0
4	060	0	0	1	1	1	1	0	0
				L1	L0	L1	L0		

Address lines A0, A1, A6, and A7 are all tied to ground. Address line A2 is tied to A4 (this is now L0) and A3 is tied to A5 (this is now L1). Then, Table 8 becomes a simple 2-bit binary count that requires only the two port lines (L0, L1) for four 2.5-second messages.

Table 8: Two-line Select

Msg #	Addr.	L1	L0
1	000	0	0
2	020	0	1
3	040	1	0
4	060	1	1

For the ISD2560/75/90/120 series of devices there are ten address lines that can be used for the 100-msec resolution. As with the other devices, this can be greatly simplified to reduce addressing lines needed. The following table compares the tradeoffs between the number of address lines used, the number of messages possible and the size of those messages derived.

Table 9: ISD2560 Addressing

Lines Used	# of Msgs.	Msg Size (Sec.)	Notes
4	9	6.4	Last msg. = 8.8 sec.
6	7	8.0	Last msg. = 12 sec.
7	8	7.2	Last msg. = 9.6 sec.
7	6	10.0	Exact fit
8	8	7.6	Last msg. = 6.8 sec.

Similar techniques work for the ISD2575, the difference being the timing or message size.

Table 10: ISD2575 Addressing

Lines Used	# of Msgs.	Msg Size (Sec)	Notes
4	9	8.0	Last msg. = 11 sec.
5	18	4.0	Last msg. = 7 sec.
6	12	6.0	Last msg. = 9 sec.
8	10	7.5	Exact fit

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Operational Modes

The Operational Mode option of ISD single-chip voice record/playback devices adds flexibility and utility to the system designer. The Operational Mode control bits allow simple cascade operation, automated looping on first message, automated power-down for the ISD2500, and other functions that simplify many designs. The use of each bit of the Operational Mode is explained in this chapter with some suggested applications.

The ISD1000A, ISD1100, ISD1200, and ISD1400 devices have eight address bit inputs with 256 possible address combinations. The first 160 of these addresses are used for direct access to message locations in the ISD1000A and ISD1400 series. The first 80 addresses are used for direct access in the ISD1100 and ISD1200 series. The last 64 possible addresses are used for Operational Mode operations in all of the above devices. These are where the address map shows both addresses A6 (pin 9) and A7 (pin 10) tied HIGH. These pins are the MSB (Most Significant Bits) for this series. Complete address maps for all the ISD device series are discussed in the "Basic Addressing" section and illustrated in the "Address Segment Resolution" section under Application Information.

In the ISD2560/75/90/120 devices the first 600 (of 1024 possible) addresses are used for direct access to message locations. The last 256 are used for Operational Mode operations. These are where the address map shows both addresses A8 (pin 9) and A9 (pin 10) tied HIGH. These same pins are the MSB for this series also. The ISD2500 series address map is discussed in the "Basic Addressing" chapter and illustrated in the "Address Segment Resolution" under Application Information.

In the following discussion of Operational Modes, it is always assumed that the MSB pins are tied HIGH to enable an Operational Mode cycle.

There are two important considerations in use of the Operational Mode.

- First, all Operational Mode operations start initially at address 0, or the beginning of the ISD device's message space.

  Later operations may start at other address locations, if the proper Operational Mode bit is set. However, in most cases, when the device is changed from Playback to Record, from Record to Playback, or a Power-Down cycle is executed, the internal address pointer is always reset to 0.
- Second, the Operational Mode bits DO NOT LATCH. An Operational Mode operation is executed anytime $\overline{CE}$ goes LOW and the MSB addresses are HIGH. If the next $\overline{CE}$ operation finds one or both of these bits LOW, a message address operation is executed. This means Playback or Record (according to the state of the Playback/Record pin) begins at whatever message address is loaded into the address pins. The state of any previous Operational Mode is lost.

NOTE *The following listed Operational Modes apply to all ISD single-chip voice record/playback devices unless otherwise noted.*

NOTE *"AN" (where N is the mode number) refers to the ISD1000A, ISD1100, ISD1200, or ISD1400. "MN" refers to the ISD2500.*

ADDRESS BIT A0/M0 (PIN 1)—MESSAGE CUEING (ISD1000A/ISD2500)

The Message Cueing Operational Mode (formerly fast forward) allows an ISD device user to rapidly access messages without knowing their physical addresses. It is only necessary to know the relative location of a message to find it. This mode is normally used with bit A4 consecutive addressing option.

An example of how to use this mode is shown in the following paragraphs:

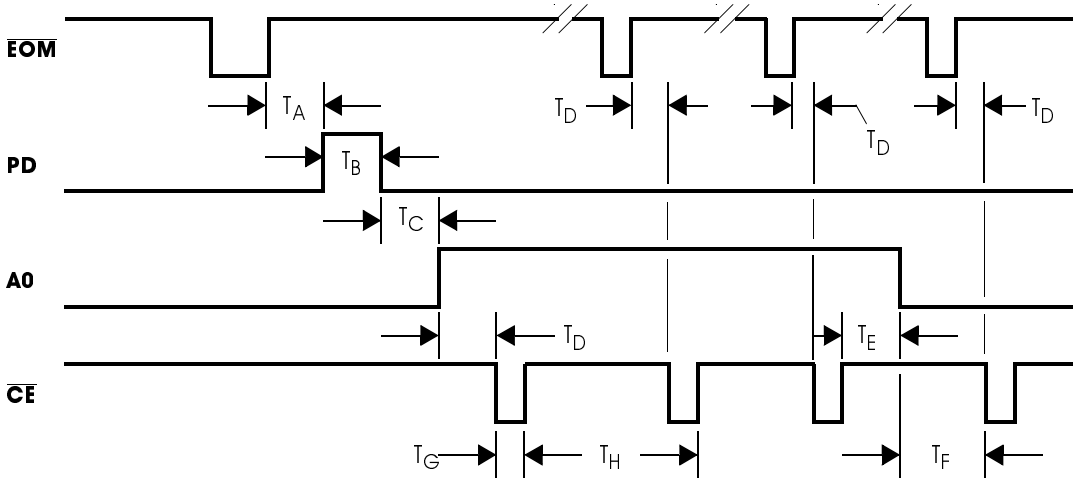
1. First set $\overline{CE}$ HIGH, P/$\overline{R}$ LOW and PD LOW. In addition the address inputs should be set up for Operational Mode and the A4 bit HIGH. All other address bits should be LOW.
2. Record the first message by holding $\overline{CE}$ LOW for several seconds. End the first message by bringing $\overline{CE}$ back HIGH.
3. Record a second message in the same manner. Since the A4 Consecutive Addressing Operational Mode is selected, the internal address will NOT be reset. This second message will be placed immediately after the first message. Its physical address falls at the beginning of the first row of the message array following the set EOM that marks the end of the first message.
4. Record a third message in the same manner. There are now three sequential messages recorded in the device.

Recover only the third message in the following manner:

1. Change the P/$\overline{R}$ input HIGH to place the device in Playback Mode. Leave Operational Mode set with A4 HIGH and additionally change A0 to HIGH. The ISD device is now ready to access messages using the Message Cueing Option.
2. Pulse $\overline{CE}$ LOW for 10 μs or less. Note that this time is critical. This operation will begin the Message Cueing function by rapidly scanning through the EOM bit memory. The device advances through the memory at 800 times normal speed with the audio output stages disabled. If the $\overline{CE}$ signal is still LOW when a set EOM bit is found, it will be ignored. A 10 μs $\overline{CE}$ pulse width means that an EOM located in the next row can be found and no EOM bits will be skipped.
3. After the first $\overline{CE}$ pulse and EOM bit, the internal address counter in the device will be pointing at the beginning of the second message. Again pulse $\overline{CE}$ LOW for 10 μs. The internal address counter is now pointing at the beginning of the third message.
4. Change the A0 address bit to a LOW. A momentary LOW pulse of $\overline{CE}$ will now cause the device to Playback the third message through the speaker at normal speed. It will cease Playback when a set EOM is found (assuming $\overline{CE}$ is back HIGH).

NOTE *Figure 1 and Table 1 show the timing for a representative example Message Cueing situation. In the example, a previous message has just ended. The user now wants to play the fourth message. To do this, the system must give three $\overline{CE}$ pulses with A0 HIGH and a fourth with A0 LOW, waiting for the $\overline{EOM}$ pulse between each $\overline{CE}$ pulse.*

Figure 1: Message Cueing Timing Diagram



NOTE: *A4/M4 HIGH.*

ADDRESS BIT A0 (PIN 1)—MESSAGE CUEING (ISD1100, ISD1200, ISD1400)

The basic operation of this Operational Mode is similar to that of the ISD1000A/ISD2500 series and allows the same capability.

Table 1: Message Cueing Values (8 Khz Sample Rate Device)

Time	Min.	Max
T_A	0	
T_B	12.5 msec	
T_C	0	
T_D (T_{SET})	300 nsec	
T_E	0	
T_F (T_{SET})	300 nsec	
T_G (T_{CE})	100 nsec	10 µsec
T_H	variable	
$T_C + T_D$	25 msec	

The following demonstration assumes three messages are pre-recorded into the device as in the previous example. We wish to play the third message:

1. With $\overline{PLAYL}$, $\overline{PLAYE}$, $\overline{REC}$ all HIGH, the address inputs are set up in Operational Mode (A6 and A7 HIGH) with A0 and A4 HIGH.
2. Pulse $\overline{PLAYE}$ LOW to begin the Operational Mode sequence

NOTE Minimum $\overline{PLAYE}$ pulse width is approximately 300 ns. The "fast forward" operation will stop at a set EOM even if $\overline{PLAYE}$ is held LOW).

The ISD1100, ISD1200, and ISD1400 devices will advance through memory at 800 times normal speed and stop at the first set EOM bit found in memory.

3. This operation is repeated a second time. When this operation is finished, the internal address counter is pointing at the beginning of the third message.
4. Change A0 to LOW and pulse $\overline{PLAYE}$ LOW to playback the third message at normal speed.

NOTE For the ISD1100 only. Since the A6 and A7 pins are pulled HIGH by on-chip resistors, it is only necessary to control A0 through A5 when an Operational Mode is desired. The A6 and A7 pins may be left floating.

ADDRESS BIT A1/M1 (PIN 2) (ISD1000A, ISD2500)—EOM MARKER DELETE CONTROL

The A1 Operational Mode allows sequentially recorded individual messages to be combined into a single message with only one EOM bit set at the end of the final message. Operationally, this option inhibits the increment of the internal address counter at the end of a Record operation. An example of how this might be used follows:

1. Set up for Record as explained previously in Operational Mode with the A4 and A1 mode bits HIGH. Change $\overline{CE}$ to LOW and record for a few seconds ending the record process by taking $\overline{CE}$ back HIGH.
2. At this time, the internal address counter of the device remains pointing at the beginning of the final row in the first message in the storage array. Part or most of this row has been recorded with analog data from the first message but it was not filled past the ending boundary of that row. An EOM bit has been set at the appropriate place in the EOM memory indicating where the first message ended.
3. With A4 and A1 remaining HIGH in Operational Mode, a new Record cycle is begun by changing $\overline{CE}$ to a LOW. Since the address counter is still pointing at the ending row of the storage array, this last row is erased and re-recorded by this second message. At the same time, the previously set EOM bit (written at the end of the first message) is also erased. End the Record of this second message by changing $\overline{CE}$ back HIGH.
4. The address and control lines of the device can now be changed to do a normal Playback at the beginning of the memory. The two previously recorded messages will Playback as one message with only one EOM bit set at the end of the second message.

NOTE The analog data written into the last row in the storage array of the first message will be lost.

ADDRESS BIT A1 (PIN 2) (ISD1100, ISD1200, ISD1400)—EOM MARKER DELETE CONTROL

This Operational Mode operates similar to that in the ISD1000A and ISD2500 devices. When A1 and A4 are held HIGH in Operational Mode, subsequent EOM bits will be over written by a new Record cycle. The final EOM bit will remain. The only difference between ISD1000A/ISD2500 functionality and the operation of this mode with the ISD1100, ISD1200, and ISD1400 devices are that the Record operation is controlled with the single $\overline{REC}$ pin.

ADDRESS BIT A2 (PIN 3) (ISD1000A ONLY)—EOM CONTROL

The $\overline{EOM}$ output of the ISD1000A series of devices performs a dual role. When playing back messages not ending with memory full, $\overline{EOM}$ pulses LOW for 12.5 ms to indicate an end-of-message mark has been found. $\overline{EOM}$ goes LOW and stays LOW when the device is in Record or Playback and fills the message memory (message overflow). If chip enable is HIGH, Playback will stop at that point. If address bit A2 is set in Operational Mode, the EOM indication is turned off. This mode does not work in the ISD2500 series devices because there are separate output pins for $\overline{EOM}$ and $\overline{OVF}$. Also, this mode does not work in the ISD1100, ISD1200, and ISD1400 devices because their Overflow condition looks identical to an EOM.

ADDRESS BIT A3/M3 (PIN 4) (ISD1000A, ISD2500)—CONTINUOUS PLAYBACK CONTROL OR LOOPING

Some applications require the continuous repeat of a message for an extended period. The A3 Operational Mode bit allows the automatic Playback repeat of the message located at the beginning of the ISD1000A or ISD2500 series message space. This continues as long as the $\overline{CE}$ pin is held LOW. **The only exception to this operation is that the message to be repeated cannot totally fill the ISD1000A.** The ISD2500 can loop with a message that completely fills its message space.

Example: It is desired to repeat a 10-second message. The 10-second message is first recorded into the ISD1000A or ISD2500 causing an EOM mark to be written at that ending point. Next, the A7, A6, and A3 address bits are strapped HIGH (A9[1], A8 and A3 are strapped HIGH in the ISD2500). With power-down LOW and P/$\overline{R}$ HIGH, taking $\overline{CE}$ LOW will cause the message to begin playing. When the end-of-message mark is reached, the status of the $\overline{CE}$ pin is read. If it is LOW, the message immediately begins playing again. While $\overline{CE}$ is LOW, the message will repeat; if $\overline{CE}$ is taken HIGH during the Playback of a message, the message will complete, then stop.

This Operational Mode may also be used to perform looping record in the ISD2500. To accomplish this, a normal Record cycle is begun with A9, A8 and A3 held HIGH. Recording will start at the beginning of memory and continue to the end of memory. At this point, the internal address counters of the ISD2500 will reset and recording will begin anew at the beginning of memory. This operation will continue as long as $\overline{CE}$ is held LOW.

ADDRESS BIT A3 (PIN 4) (ISD1100, ISD1200, ISD1400)—CONTINUOUS PLAYBACK CONTROL/LOOPING

This Operational Mode is initiated by a negative transition on $\overline{PLAYE}$ pin with A7, A6 and A3 held HIGH. Then $\overline{PLAYE}$ is brought back HIGH. Looping will continue indefinitely with all three control pins ($\overline{PLAYL}$, $\overline{PLAYE}$, $\overline{REC}$) held HIGH.

To stop the looping, $\overline{PLAYL}$ pin is momentarily taken LOW, then back HIGH. As long as A7, A6 and A3 remain HIGH, a new Playback loop will begin with the next negative transition on the $\overline{PLAYE}$ pin.

Another way to control looping is to use the $\overline{PLAYL}$ pin alone. Taking this pin LOW begins the looping and it continues until the pin is taken HIGH again. This is a continuous control rather than the pulsed control of the previous paragraph.

As in the ISD2500, this same operation will work with a Record cycle. As long as $\overline{REC}$ is held LOW in this Operational Mode, recording will loop and continue.

ADDRESS BIT A4/M4 (PIN 5) (ISD1000A, ISD2500)—MESSAGE START POINTER RESET—CONSECUTIVE ADDRESSING

When this bit is HIGH in Operational Mode, the internal address pointer that controls the location of the start of Record or Playback is only reset LOW when the Record/Playback Mode is changed or a power-down cycle is executed. For example, assume two or more messages are recorded in an ISD device. With bits A4, A6 and A7 set HIGH (A8 and A9 for ISD2500), a Playback cycle executed by a LOW going $\overline{CE}$ pulse (with $\overline{CE}$ immediately returning HIGH) will proceed with Playback of the first message. It will stop when the EOM mark is found at the end of that message. Since the device is in the A4 Operational Mode, the next chip enable will start Playback of the second message. If the user wants to hear the first message again, a power-down positive going pulse of at least 12.5 ms will reset the message address pointer.

NOTE A momentary change of state of the Record/Playback input will not reset the message address pointer. A falling $\overline{CE}$ must occur after the state change. If the user tries to reset the message pointer using a Record cycle the first message will be erased.

The A4 bit works the same during a Record cycle, except that the chip enable is level activated instead of edge activated (chip enable is always level activated during Record). At the end of each Record cycle, the message start pointer will be left at the beginning of the next message space to be recorded.

1. *The 2 MSBs for the ISD2560/75/90/120 are A9 and A8. For the ISD2532/40/48/64 they are A8 and A7.*

NOTE There is no way to record a message following another message (using Operational Mode) if the message start pointer has been reset. Sequential messages must be recorded without changing to Playback or executing a power-down cycle.

ADDRESS BIT A4 (PIN 5) (ISD1100, ISD1200, ISD1400) – MESSAGE START POINTER RESET (CONSECUTIVE ADDRESSING)

This mode operates in ISD1100, ISD1200, and ISD1400 device series identical to the operation in other ISD voice storage products. As long as A4 is held HIGH in Operational Mode, the internal address counter will not be reset with subsequent Record or Playback operations. If a Playback cycle is followed by a Record cycle, the address counter *will not* be reset. The new message will be recorded directly after the last message played.

The internal address counter can be reset in this mode by momentarily changing A4 from HIGH to LOW and back HIGH during the device's static powered down state.

ADDRESS BIT A5/M5 (PIN 6) (ISD1000A & ISD2500 ONLY)—CE LEVEL ACTIVATED

The default mode of the ISD devices is for $\overline{CE}$ to be edge activated on Playback and level activated on Record. Normal Playback is begun with $\overline{CE}$ pulsed LOW and will end when an EOM mark is encountered. With bit A5 HIGH in Operational Mode, $\overline{CE}$ becomes level activated during Playback. If address bits A7, A6, and A5 are all HIGH, a falling $\overline{CE}$ will start Playback at the beginning of the message space and will continue while $\overline{CE}$ is LOW. If $\overline{CE}$ is taken back HIGH, the Playback will stop and a second $\overline{CE}$ going LOW will restart Playback at the beginning of the message. Additionally, bit A4 can also be taken HIGH. $\overline{CE}$ activation starts Playback at the message beginning and if $\overline{CE}$ is later taken HIGH, message Playback will immediately cease. If $\overline{CE}$ is now taken back LOW, Playback will resume at the point at which it just stopped.

NOTE As long as $\overline{CE}$ is LOW, EOM marks will be ignored. If the Playback (or Record) proceeds into the overflow condition, a power-down cycle is required before any additional Record or Playback operation can begin.

This mode is not available in the ISD1100, ISD1200, and ISD1400 series devices.

ADDRESS BIT M6 (PIN 7) (ISD2500 ONLY) – ISD2500 PUSH-BUTTON MODE

In the ISD2500 series of devices there is an additional Operational Mode, not available in other ISD series devices. This is the Push-Button Mode that is provided for a very simple, minimum part count, application. When this mode is selected the functionality of three pins change to alternate uses. Pin 23, $\overline{CE}$, becomes Start/Pause and is activated by a LOW going pulse. Pin 24, PD, becomes Stop/Reset and is activated by a HIGH going pulse. Pin 25, $\overline{EOM}$, becomes RUN, with an active HIGH indication. (See the ISD2500 series data sheets for illustrations of how to use this mode with a microcontroller.)

Table 2: Push-Button Mode Control Pins for ISD2500

Pin Number	Pin Name	Changes for Push-Button Mode
Pin 23	$\overline{CE}$	Becomes $\overline{START}$ or $\overline{PAUSE}$ (–edge activated)
Pin 24	PD	Becomes STOP + RESET (+level activated)
Pin 25	$\overline{EOM}$	Becomes RUN to drive LED
Pin 22	$\overline{OVF}$	Remains the same

Start/Pause is used to start the device in either the Record or Playback Mode, depending upon the state of pin 27. Applying a LOW pulse here will begin the operation that will continue until it reaches the end of the chip, an EOM marker (in the Playback Mode), the Stop/Reset pin is pulsed HIGH, or the Start/Pause pin is pulsed again.

In the Record Mode, beginning at address 0, a series of messages can be recorded by pressing the Start/Pause button multiple times. Each *odd* numbered press of the button starts the next message. Each *even* press of the button stops the current message being recorded. The next message is then recorded at the beginning of the next address row when the button is pressed again. If no further messages are desired, or the end of the chip has been reached, pressing the Stop/Reset button will stop any recording in progress, record an EOM marker, and reset the address counter to 0.

In the Playback Mode, each time Start/Pause is pressed, the next message will be played. It will stop when it reaches the EOM marker and wait for the next command.

In the Push-Button Mode pin 25, $\overline{EOM}$, becomes RUN. This is an active HIGH signal that is true whenever a Record or Play operation is in progress. It is designed to drive a low-power LED as an indicator. It will indicate whether the last push of the Start/Pause button started an operation or paused one.

One important feature of the Push-Button Mode is that the ISD2500 device automatically enters the Power-Down Mode at the end of each operation *without* losing the message start pointer value. This means that the next operation will begin at the desired location. It is not reset by automatic power-down as it is on the ISD1000A devices when put into power-down with the PD pin.

Several descriptions of Push-Button Mode operations follow to help the user understand how to use these functions. These operations are illustrated in the State Diagram Flow Chart diagram found in Figure 3 that follows these descriptions, and shows each possible state of the ISD2500 device and what state it can transition to next.

POWER-UP CONDITION

The numbers in square brackets [] in Figure 3 indicate the current position of the operation in the State Diagram.

Number [1] indicates the power-up condition. Pushing the Stop button at this point does nothing.

RECORD

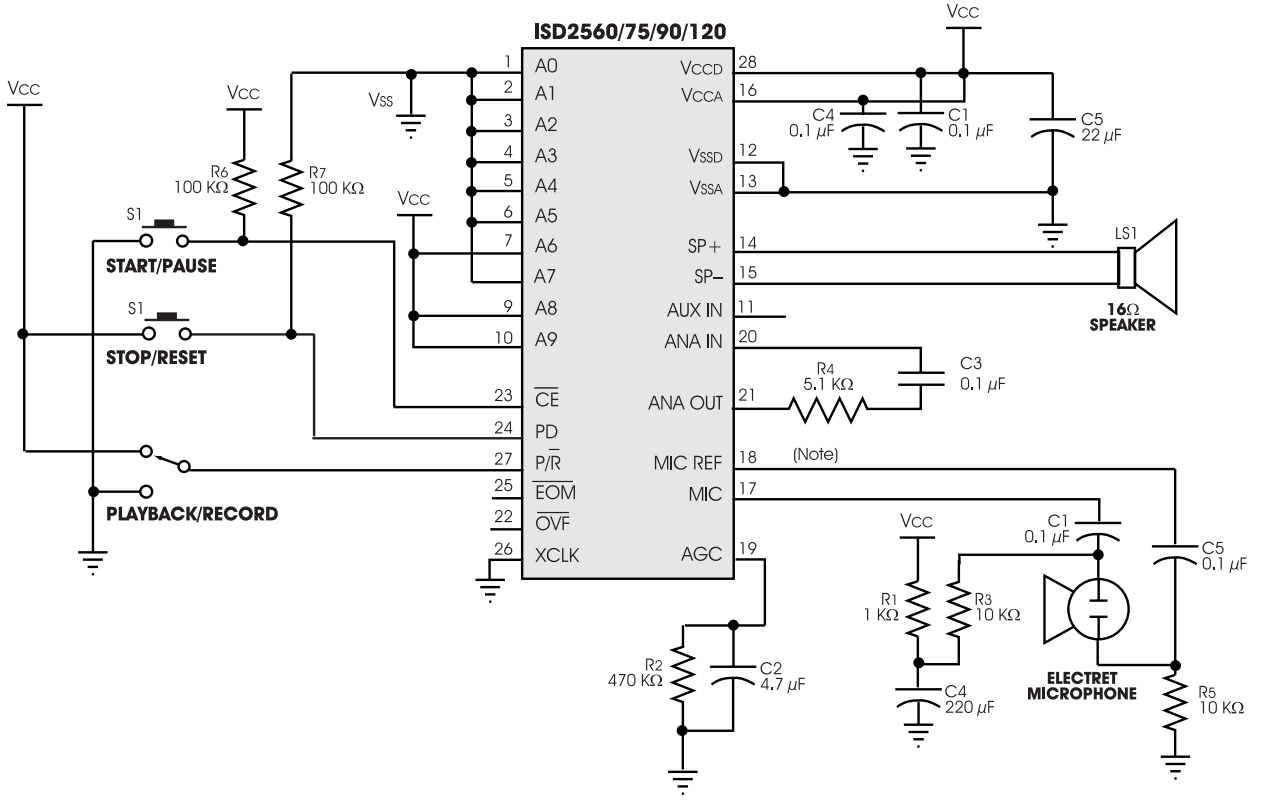
Setting the P/$\overline{R}$ to a 0 and then pressing the Start/Pause button starts the chip recording from address 000. [2] This recording will stop for three reasons: [5] The recording can reach the end of the chip and overflow. [3] It can be paused by hitting the Start/Pause button again. [4] One could hit the Stop button.

If the recording had stopped because of overflow [5], pressing the Start/Pause button again will not do anything. Hitting the Stop button will reset the address counter to 000. [1] The chip is ready for any new operation. Or, switching P/$\overline{R}$ to a 1 and hitting Start/Pause will start the chip playing from the beginning of the chip. [6]

If the recording stopped because the Stop button was pressed, an EOM is set and then the address counter is reset. The chip returns to step [1], ready for the next operation.

If the recording had stopped because of Start/Pause being pressed, it finishes recording and writes an EOM, [3], then three choices are available. Pressing the Start/Pause button again, the chip resumes recording from the beginning of the next row. [2] Pressing Stop resets the address counter and returns the chip to step [1] to await the next operation. Or, switching P/$\overline{R}$ to a 1 and pressing Start/Pause will start the chip playing from the beginning of the chip. [6]

Figure 2: Application Example—Push-Button Mode



RECORD-TO-PLAY

From either state [3] or [5], switching P/$\overline{R}$ to a 1 and hitting Start/Pause will reset the address counter and start the chip playing from the beginning. [6] If, during the recording, P/$\overline{R}$ had been switched to a 1 and Start/Pause had been pressed, the pause will be from the Record Mode, setting an EOM bit. The next Start/Pause will then play from address 0.

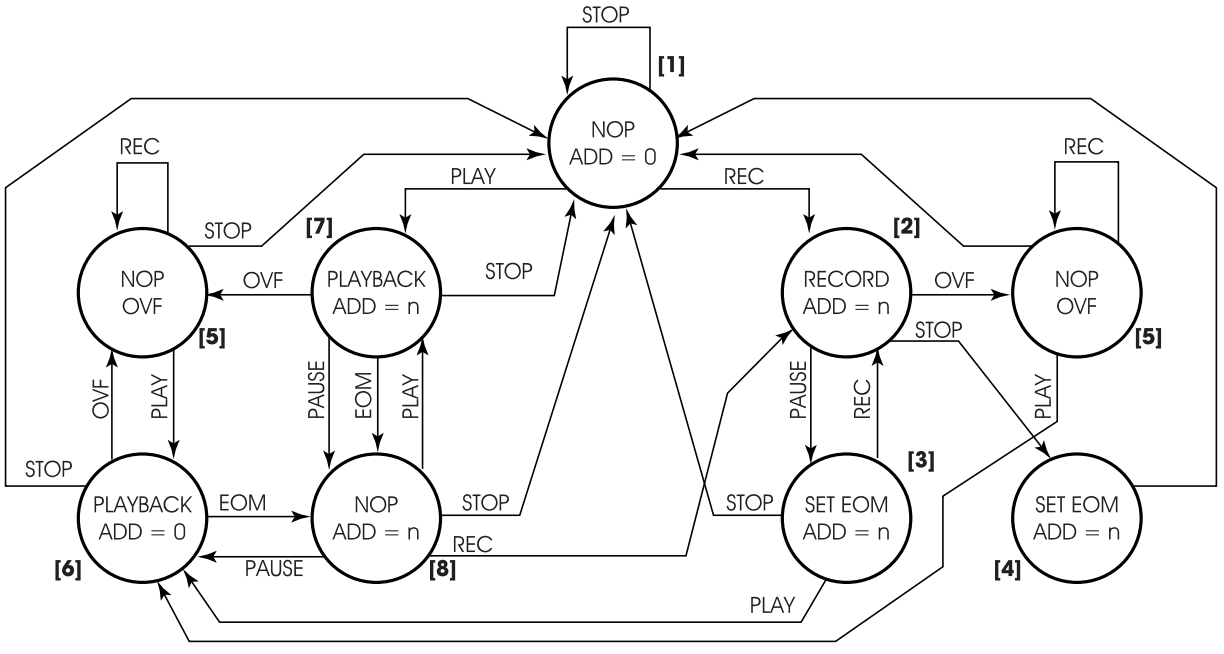
PLAYBACK

From position [1], if P/$\overline{R}$ had been a 1, and Start/Pause had been pushed, the chip would have begun playing from the beginning of the chip, address 000. [7] Playback would continue until one of four conditions was reached. (1) The message can reach the end of the chip and overflow. [5] (2) It can be paused by pressing the Start/Pause button again. [8] (3) One could press the Stop button. [1] (4) The message could reach an EOM bit. [8] If, while playing the message, P/$\overline{R}$ had been switched to a 0 and Start/Pause had been pressed, the chip will pause from the Play Mode. Then, if the Start/Pause is pressed with P/$\overline{R}$ = 0, a Record will start from the present position. If P/$\overline{R}$ = 1, a normal play will resume.

(1) If the chip reached overflow [5], pressing Start/Pause again will reset the address counter and the chip will begin to play from the beginning again. [6] (State [6] is very similar to state [7] except that the address counter has been reset. EOM and "Pause" send it to state [8] as they do from state [7]. Stop goes back to state [1] and $\overline{OVF}$ goes back to state [5].)

If, instead of pressing Start/Pause again from [5], one presses "Stop," the address counter would reset and the chip would return to state [1]. It would not play, and would await the next operation. Switching P/$\overline{R}$ to a 0 and pressing Start/Pause at the overflow will not do anything. The chip will remain in state [5].

Figure 3: ISD2500 Series Push-Button Mode State Diagram Flow Chart



(2) If the message had stopped because the Start/Pause button had been pressed [8], it does not reset the address counter. Three choices are available from state [8]: First, pressing Start/Pause again will make the chip resume [7] from the beginning of the row. Second, pressing Stop will reset the address counter and return the chip to state [1] awaiting the next operation. The third choice is to change from Play to Record [2] as explained in the following section.

(3) If the message had stopped because the Stop button had been pressed, the address counter was reset and the chip returned to state [1], ready for the next operation.

(4) Stopping for the EOM also places the chip in state [8], similar to pressing the Start/Pause while playing. The address counter is not reset. Instead, it is incremented to the beginning of the next row. This is slightly different from the pause that puts the counter at the beginning of the current row. Unless the pause occurred during the very last scan, in which case it will go to the beginning of the next row]

PLAY-TO-RECORD

Switching P/$\overline{R}$ to a 0 from state [8] and hitting Start/Pause will make the chip begin recording. This is without resetting the address counter from where it stopped playing. [2] This puts a new message on the chip, following the ones, or portions thereof, that were already played back. Note that it might be significant if state [8] was entered from the EOM or "Pause" as to where the recording will begin.

SOME SIMPLE ONE LINERS

- Pressing Stop from any state resets the entire chip, returning it to state [1].
- Pressing Start/Pause when playing or recording will pause the operation, pressing it again will resume that same operation.
- Pause in Record Mode will plant EOM bits *each* time. (Unless M1, delete EOM is set HIGH also.)
- Setting M1 true in the Push-Button Mode will mean that the pause EOM bits will be erased upon resuming Record. Only the last one at the end of the Record operation will remain.

(Going from [3] to [1] or [6] leaves the EOM in place.)

- EOM bits in playback will pause the chip [8]. Each time you press Start/Pause plays the next message.
- The EOM is not erased when going from [8] to [2] with M1 true.
- In the Push-Button Record Mode the $\overline{CE}$ (Start/Pause) button does not need to be held down for the duration of the recording.
- Switching P/$\overline{R}$ to the opposite state during an operation, then pressing Start/Pause does not change the normal pause operation.
- When the Start/Pause is pressed to resume an operation it initiates the current state of P/$\overline{R}$ independently of the state of P/$\overline{R}$ when the part was paused.

STATE DIAGRAM FLOW CHART DEFINITIONS

The lines represent a push-button action, an end of message or an overflow:

$\overline{REC}$ = P/$\overline{R}$ = 0 from NOP operation with Start/Pause = Negative Pulse

PAUSE (from $\overline{REC}$) = P/$\overline{R}$ = x from $\overline{REC}$ with Start/Pause = Negative Pulse

PLAY = P/$\overline{R}$ = 1 from NOP operation with Start/Pause = Negative Pulse

PAUSE (from PLAY) = P/$\overline{R}$ = x from PLAY with Start/Pause = Negative Pulse

STOP = P/$\overline{R}$ = x, $\overline{CE}$ = x, PD = Positive Pulse

The circles represent an operation:

NOP = No Operation

PLAYBACK = Playback starting at ADD = Previous operation or 0

RECORD = Record starting at ADD = Previous operation or 0

$\overline{OVF}$ = Overflow

(add = n) = current operation will start at the ending address location of the previous operation.

COMBINING OPERATIONAL MODE BITS

Some Operational Mode bit functions can be combined to give maximum flexibility to using the ISD devices. As mentioned in the discussions above, some modes are not applicable for Record operations and some combinations of bits are inherently unusable. For instance, the A0 fast forward bit cannot be used with the A5 $\overline{CE}$ level activation bit. Common sense will in most cases show what combinations will work. If in doubt, check the data sheet or try their operation.

OPERATIONAL MODE SUMMARY

ISD1000A:
Modes A0 through A5.

ISD1100, ISD1200, and ISD1400:
Mode A0, A1, A3 and A4.

ISD2500:
Modes M0, M1, M3 through M6.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Circuit Examples for ISD1000A and ISD2500 Products

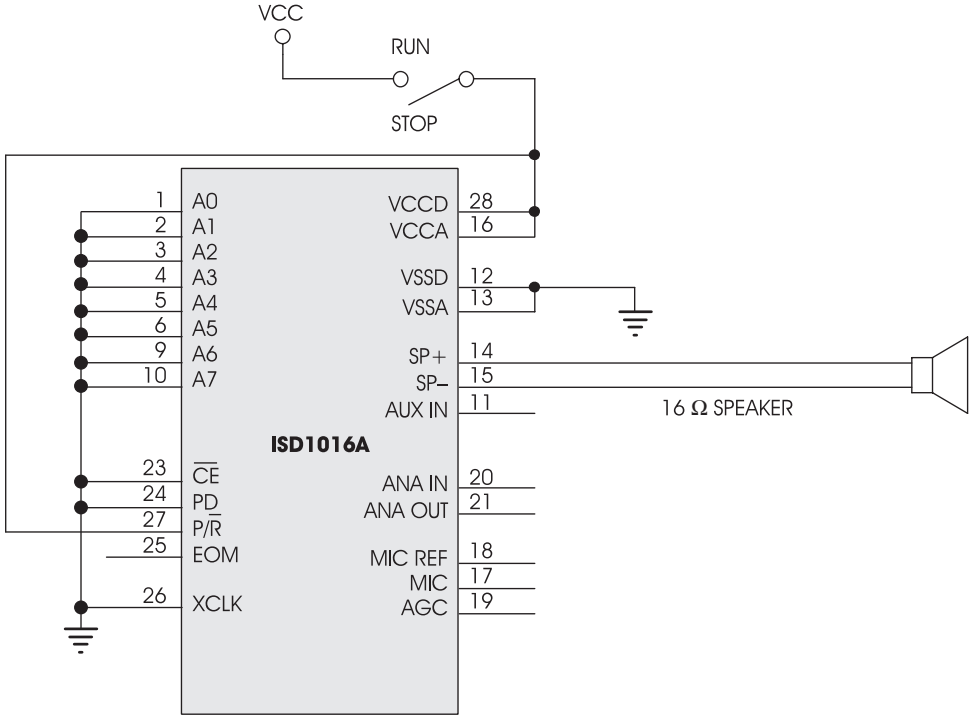
This chapter provides various applications of the ISD series of devices. Most can use the ISD1016A or ISD1020A, as required for the exact application. In many cases, the schematic shows an ISD1016A or the ISD2500 device in the socket.

SIMPLEST PLAYBACK ONLY

The circuit in the figure below represents the simplest playback-only implementation of an ISD1000A series device.

This schematic shows the minimum device count playback-only circuit. Change SW1 to the +5 volt "RUN" position and the contents of the ISD1000A will play one time, then stop. Because $\overline{CE}$ is strapped LOW, set EOM bits will be ignored (though an EOM pulse will be output through the $\overline{EOM}$ pin when a set EOM bit is encountered) and the device will play until it goes into overflow. A momentary change of SW1 to "STOP" then back to "RUN" will cause the contents of the ISD1000A to be played a second time.

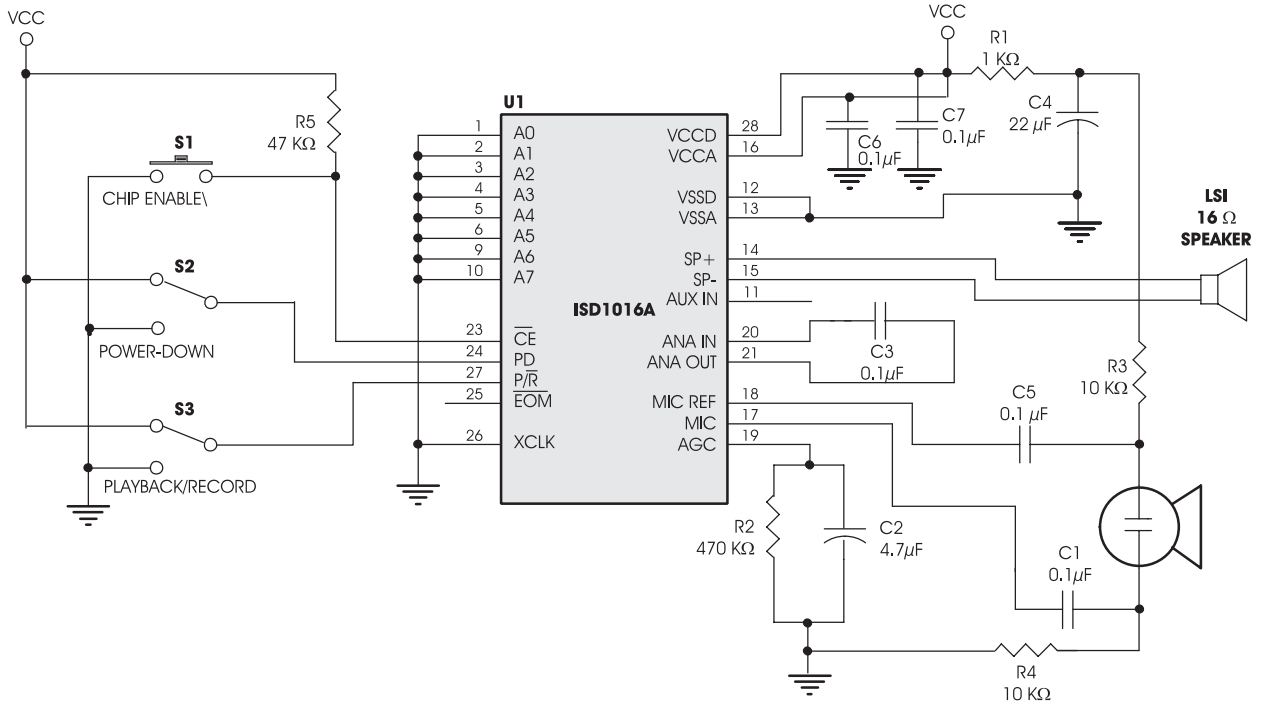
Figure 1: Simplest Playback Only



SIMPLEST PLAYBACK/RECORD

The next circuit represents the simplest implementation of a record and playback non-addressed application. This circuit can use either an ISD1000A or ISD2500 device and is the same schematic found in the data sheets. To operate, start with chip enable HIGH. To record, change the Playback/Record switch to LOW, make sure the power-down switch is LOW, then change the chip enable switch to LOW. Record for the time period of the ISD device used. To playback, momentarily set the power-down switch to HIGH, then back to LOW, change the Playback/Record switch to HIGH, then pulse the chip enable switch LOW, then back HIGH. The previously recorded message will Playback. If the message did not totally fill the device, the power-down cycle is not required. If the chip enable switch is held LOW while in Playback, the entire contents of the device will play regardless of any EOM bits being set.

Figure 2: Simplest Playback/Record Schematic



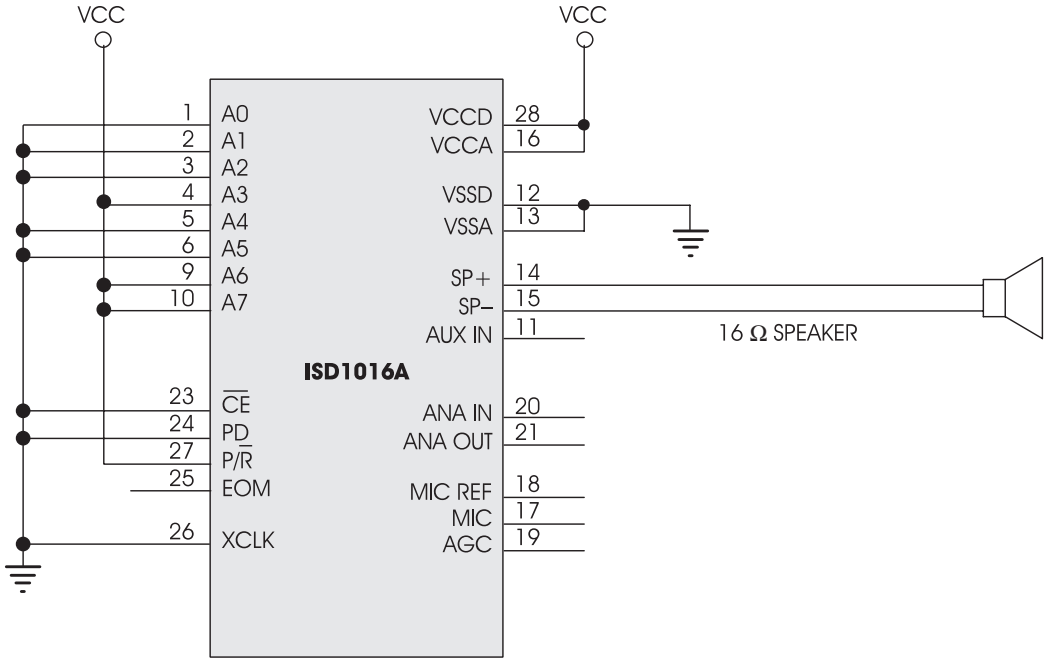
PLAYBACK LOOPING

Many audio applications require repetitive playback or looping on the same message for an extended time. The ISD1000A series of devices may be used to satisfy this requirement using either the built in Operational Mode or using a small amount of external logic. Both applications may be controlled by the Chip Enable pin so looping can be started and stopped or run continuously when power is applied.

PLAYBACK LOOPING USING OPERATIONAL MODE

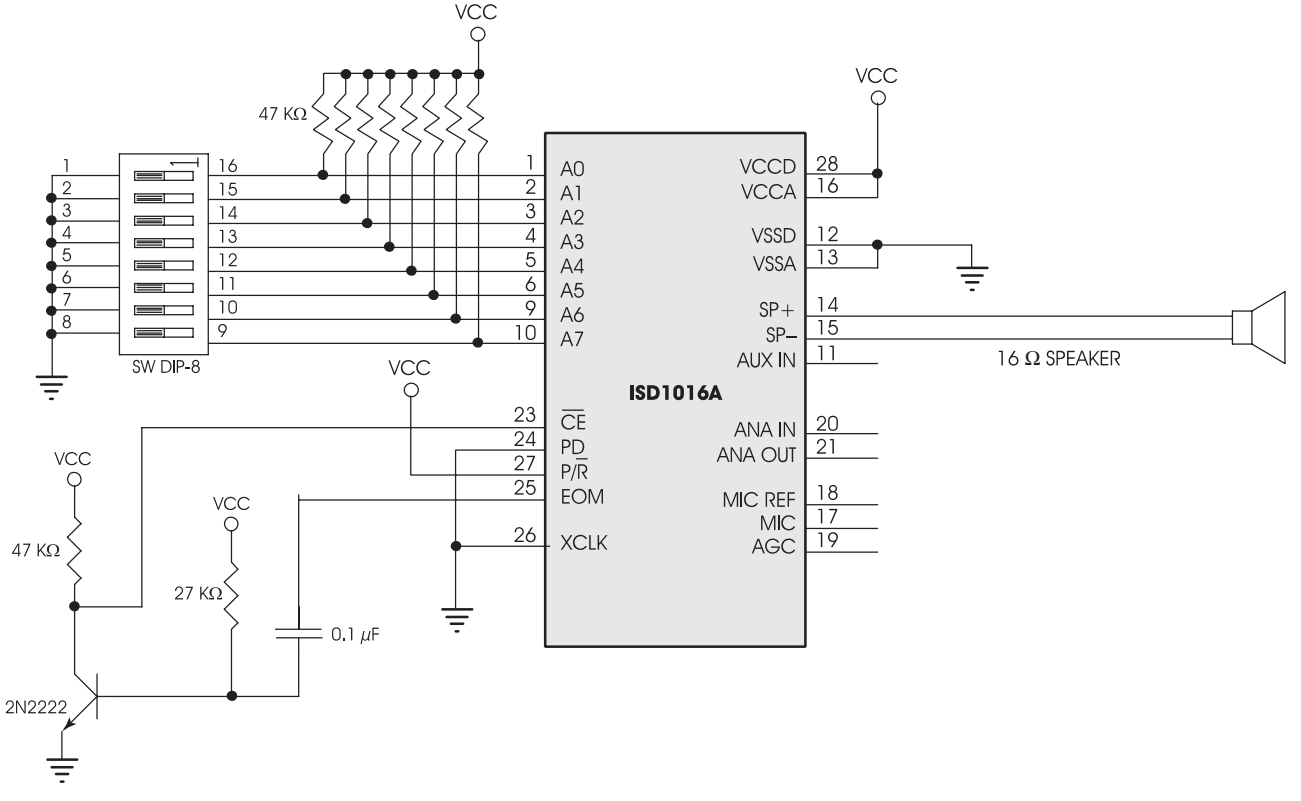
Figure 3 shows that Operational Mode may be used to accomplish playback looping if the message starts at Address 0 (the beginning of the memory) and does not require the full 16 seconds of analog storage. Operational Mode may not be used if the starting address is not zero or the message completely fills the ISD1016A.

Figure 3: Operation Mode Playback Looping



NOTE: *Circuit loops beginning at 000 and the message cannot reach 160 (end).*

Figure 4: Chip Enable Initiated Looping



A message is first recorded into an ISD1016A with all the address bits tied LOW. This positions this message at the beginning of the ISD1016A's address space. Next, the device is put into Operational Mode by connecting Address bits A7 and A6 HIGH (+5 VDC). Bit A3 is also connected HIGH to enable continuous repeat. With PD LOW, P/$\overline{R}$ HIGH, and $\overline{CE}$ held LOW, the beginning message in the ISD1016A will repeat. If $\overline{CE}$ is taken back HIGH after a message has begun, the ISD1016A will complete the message, then stop. If $\overline{CE}$ is strapped LOW, when power is applied, the message will repeat continuously.

CHIP ENABLE INITIATED LOOPING

Figure 4 shows a simple one transistor circuit that may be used to achieve playback looping using chip enable. This circuit may not be used if the ISD1000A series device is completely full.

The $\overline{EOM}$ pulse at the end of a message is differentiated to produce about a 15 ms positive going pulse into the $\overline{CE}$ pin. When this pulse falls, the address is loaded into the device by the DIP switch and a new Playback cycle starts at that address. Since the original message has continued to play during this pulse, the message is smoothly restarted without a break.

THREE MINUTE CASCADE USING THE ISD2560

The circuit illustrated in Figure 5 demonstrates a method of cascading three ISD2560 devices to obtain up to three minutes of storage.

The ISD2560 may be easily cascaded to increase the storage capacity of a system. Two methods are discussed in the following paragraphs. The first method shows three devices cascaded in a mode where a number of messages may be sequentially recorded starting at the beginning of memory. A message may be recorded across the boundary of two devices. The transition between the two devices will be transparent to the user. Message cueing, the A0 Operational Mode (fast forward) may then be used to rapidly access and playback any of the recorded messages. It is not necessary to know the exact address location of each message. Only the sequential message number need be known.

The second method shows how to directly address and record or playback a message at any point in the three devices' memory space. A message may be recorded or played back across the boundary of two devices. The transition between the two devices will again be transparent to the user.

In the two examples shown, three ISD2560s have been cascaded resulting in a total record/playback time of three minutes. Alternatively, ISD2575s or ISD2590s could be used to achieve 3 minutes 45 seconds, or 4 minutes 30 seconds, respectively.

In each example, U1, the first ISD2560 in the series, contains the microphone preamplifier and the speaker output for the entire system. This is in addition to having the first 60 seconds of analog memory. The remainder of the ICs being cascaded serve only as memory elements. The ANA OUT (microphone preamplifier output) pin of U1 is connected through blocking capacitors to the ANA IN of each of the three devices in the cascade. Additionally, the SP+ of U3 is fed back to U2's AUX IN pin and U2's SP+ is connected back to U1's AUX IN pin. Thus, the ANA IN pins are fed in parallel from U1's microphone preamplifier while the speaker outputs "daisy chain" back to U1's speaker amplifier.

SEQUENTIAL RECORD AND MESSAGE CUEING EXAMPLE

Operational Mode is used to set up the ISD2560 for proper cascade operation. The ISD2560 is placed into Operational Mode by connecting address bits A8 and A9 HIGH. The remainder of the Operational Mode bits are tied LOW except as follows:

Figure 5: 3-Minute Cascade Schematic

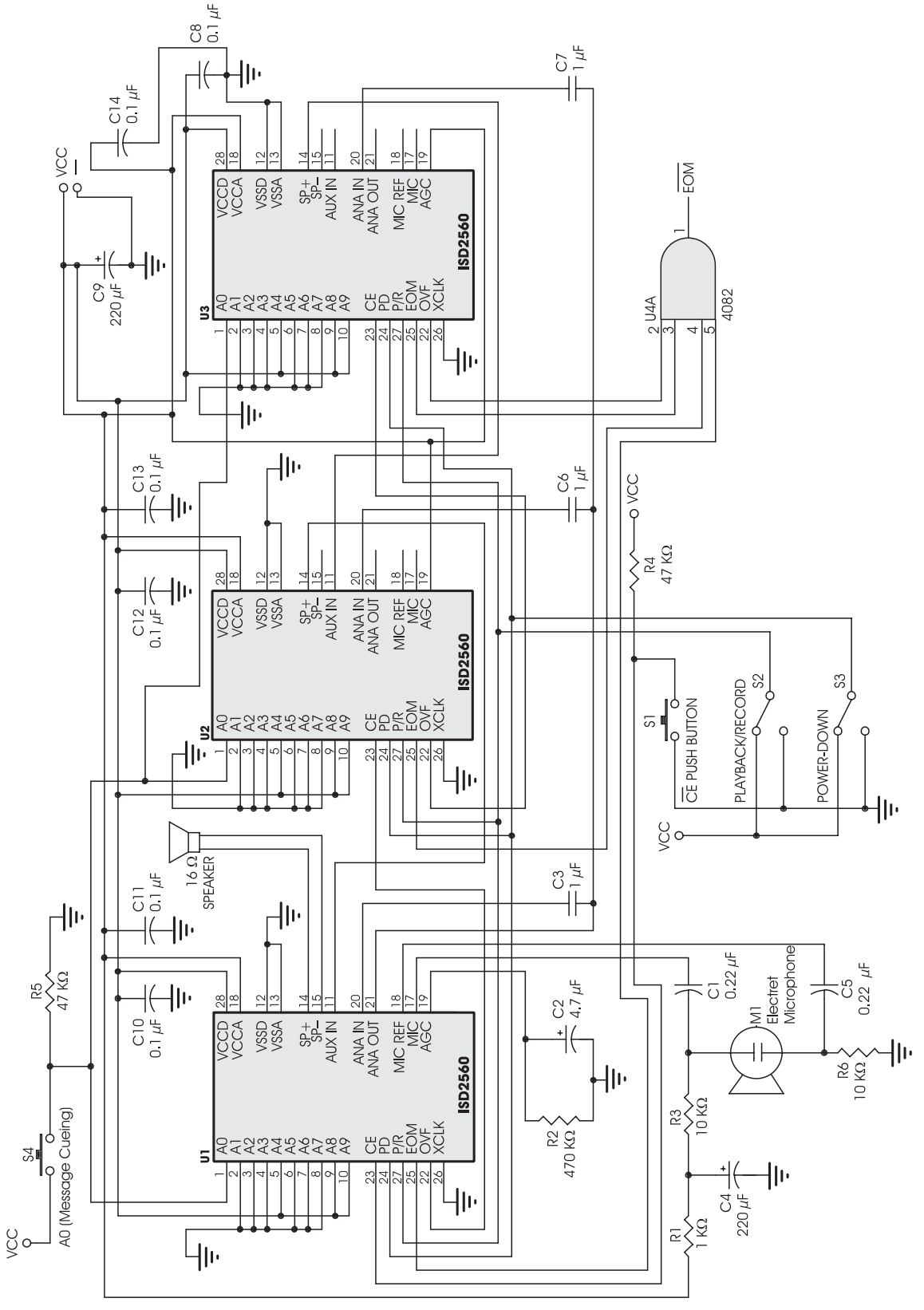
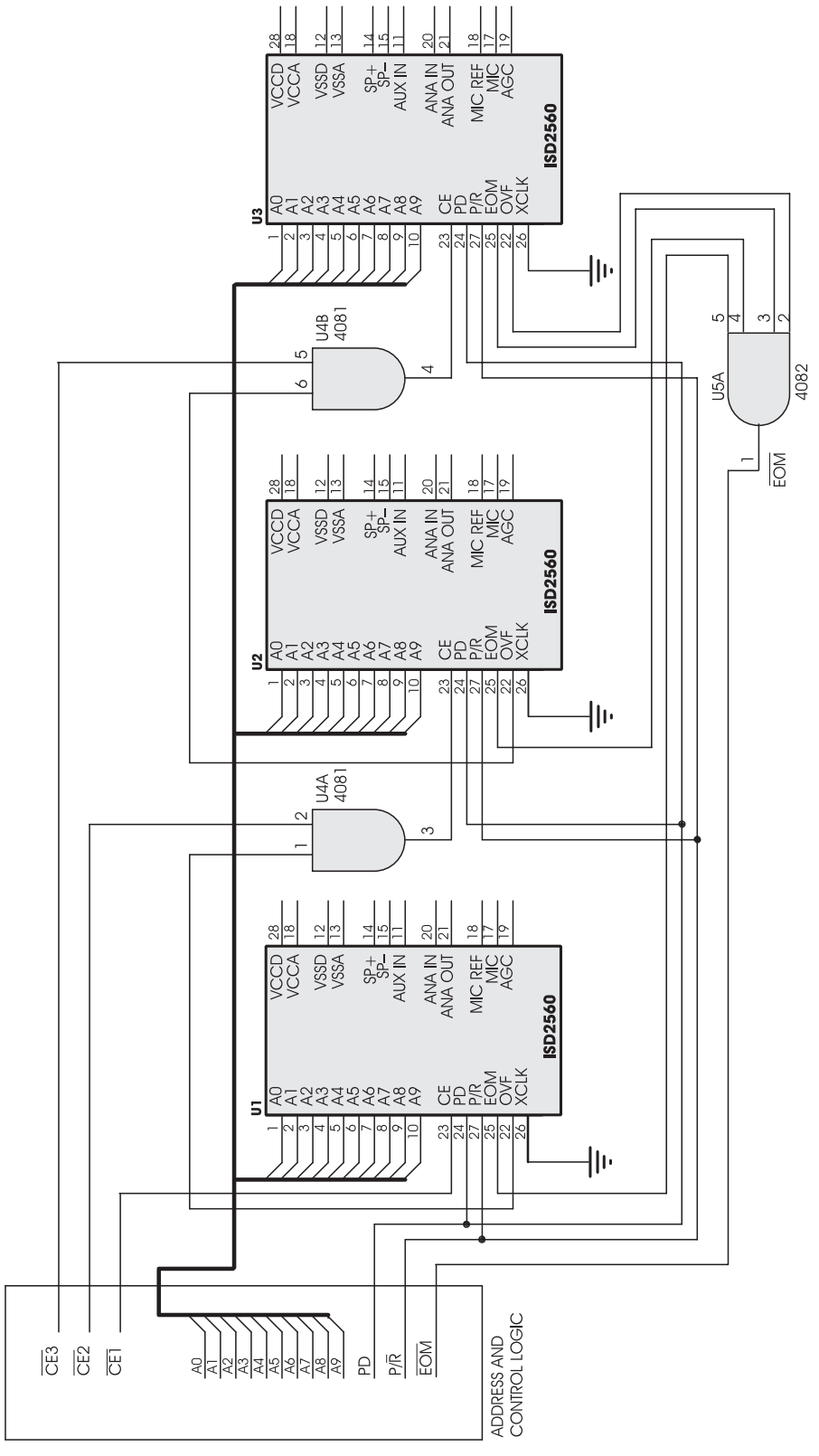


Figure 6: ISD2560 Cascade and Direct Addressing



1. *All Record or Playback cycles must start with a power-down cycle.*
2. *Address lines should be applied T_{SET} before the falling CE and return to 0 after T_{HOLD} time. Address lines must then remain at 0 throughout a Record or Playback cycle.*

Bit A4 is HIGH to cause the Message Start Pointer (MSP) to *only* be reset when the system's mode is changed between Record and Playback. (Normally the MSP is initialized anytime the Chip Enable pin goes LOW.)

NOTE *The MSP controls where the ISD2500 is going to begin to record or playback on the next operation. It is also initialized when the Power-Down Cycle is initiated.*

The result of this configuration is that messages will be stacked sequentially during record across chip boundaries in a manner transparent to the user. Changing from Record to Playback resets the MSP back to the beginning of the first message in the series. The next Playback proceeds under control of chip enable.

Record Operation

To begin recording, place the Record/Playback switch in the record position and hold chip enable LOW for the duration of the recording. To record the second message, repeat the operation; recording will now begin at the end of the first message. Additional recordings may be placed sequentially into the cascaded devices until the memory is full. The $\overline{OVF}$ pulse out of the last memory may be used as a "memory full" indicator.

Playback Operation

To playback the first recorded messages, change the P/$\overline{R}$ pin to a HIGH and pulse the $\overline{CE}$ pin LOW. The first message will playback and stop at the set EOM bit. A second LOW $\overline{CE}$ pulse will start playback of the second message. Each message may start or stop anywhere in the cascade memory. The A0 Message Cueing Operational Mode may also be used to access messages anywhere in the cascade memory. This "fast forward" operation will transparently cross the boundary between two devices. A0 Message Cueing is discussed in detail in the section on Operational Modes.

DIRECT ADDRESSING EXAMPLE

The second cascade circuit shows the added logic necessary for direct address of messages anywhere in the three devices' memories. Only a single 2 input AND gate is required for each chip cascade. For simplicity, the analog circuitry is left off this schematic.

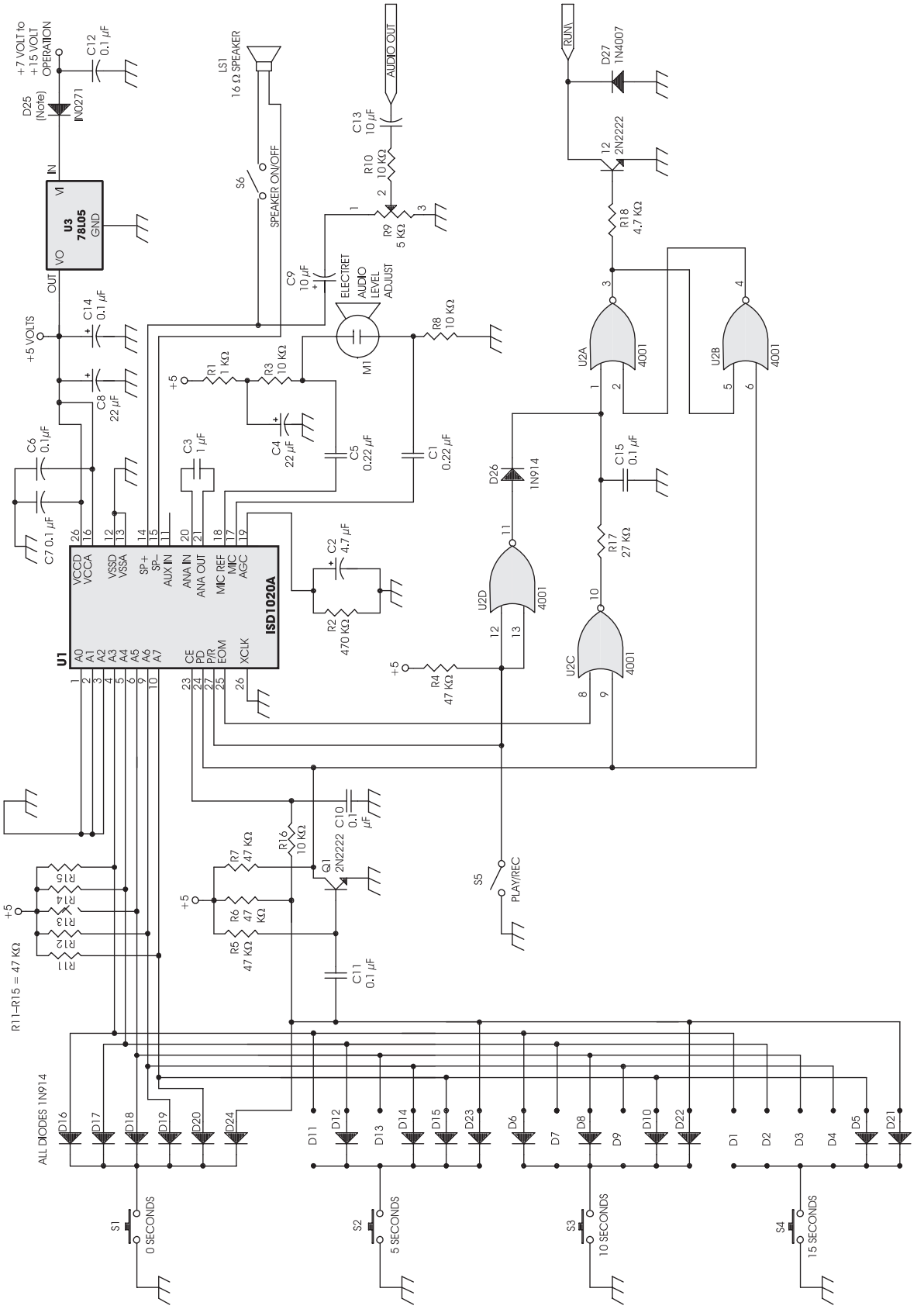
To address any message, the user must know the starting address of the message and in which device it begins. For instance, a message might begin in device U2 at address 400, or 40 seconds into the memory. This message may run over into U3 with no problems. To start playback of this message, PD must be taken LOW and P/$\overline{R}$ taken HIGH. The address 400 (decimal) must be placed on the address bus. This equates to 190 Hex.

Next the $\overline{CE}$2 line is taken LOW and playback begins. Playback will continue until a set EOM bit is found. The pulse will appear at the $\overline{EOM}$ output from U5A. Note that this will be a 12.5 ms pulse unless the message ends at overflow at U3. In this case, the $\overline{EOM}$ pulse will be approximately 6 μs long.

PUSH BUTTON FOUR MEMORY RECORD/PLAYBACK

A version of the circuit shown in Figure 7 first appeared in December 1991 *QST Magazine*. It demonstrates how a single ISD1020A may be used to store up to four 5-second messages that may be individually retrieved using a single push button for each.

Figure 7: Push-Button Four Memory Schematic



NOTE: *D25 is polarity protection.*

HOW THE CIRCUIT WORKS

The ISD1020A can be operated in several different modes. In this project, it operates in an "addressed" mode. The eight address pins of the device determine where the Record and Playback operations begin. The ISD1020A can be looked at as a miniature tape recorder. It has the ability to pre-position the Playback/Record head anywhere on this 20-second tape before we begin an operation. The device has 160 valid addresses, giving an address resolution of 0.125 seconds. This means eight address counts equal 1 second of record time.

To determine what address to give the device, we must first convert seconds into binary counts. A 1-second resolution is adequate for our purposes. Since eight counts equal 1 second and eight is an "even" binary multiple, we can ignore all the counts less than eight. We do this by strapping A0, A1 and A2 to ground and just programming the five remaining bits. Using push buttons and diodes, we can select any interval between 1 and 19 seconds for the start of record or playback.

As shown in Table 1, the four start message locations are 0 seconds (beginning of memory), 5 seconds, 10 seconds and 15 seconds. This defines four 5-second messages.

Table 1: Address Boundaries Example

Chart 1		Chart 2	
Message Start Location	Addr Pins AAAAAAAA 76543210	Message Start Location	Addr Pins AAAAAAAA 76543210
Seconds		Seconds	
0	00000000	0	00000000
5	00101000	4	00100000
10	01010000	8	01000000
15	01111000	14	01110000

Table 1 shows the binary addressing for these intervals. The message start locations could have as easily been defined as 0 seconds, 4 seconds, 8 seconds, and 14 seconds giving two 4-second messages and two 6-second messages. Chart 2 shows this second set of intervals. You can experiment with the diode positions for various addresses but keep in mind that the highest message start address the ISD1020A will recognize is binary 10011111 or 159 decimal. Since A0, A1 and A2 are always at ground, the highest recognizable address is at the 19-second boundary or 10011000.

The Playback/Record function of the ISD1020A is determined by the P/$\overline{R}$ pin (pin 27) of the device. Simply tie it LOW for Record and to +5 V for Playback.

The ISD1020A requires the Chip Enable pin (pin 23) to start HIGH, pulse LOW for Playback and stay at a LOW level during record. All the address and the Playback/Record inputs must be set up before the Chip Enable pin goes LOW. At the end of recording, returning the Chip Enable pin to a HIGH ends the recording and inserts an end of message bit into the ISD1020A's memory. When the Chip Enable pin is pulsed LOW when the Playback/Record pin is HIGH, the device will playback what is recorded until it encounters an end of message bit. It then stops Playback and waits for the next control input.

The one remaining input to the ISD1020A is the power-down or PD pin (pin 24). This pin controls the power requirements of the ISD1020A. When taken to +5 volts, the chip uses less than 10 microamps of current. The device must be powered up (Power-Down pin at ground) to record or playback. This pin also serves as a reset if the ISD1020A is recorded or played "into the stops." That is, all the way to the end of the device's 20-second memory. When that happens, the Power-Down pin must be cycled HIGH then back LOW again for the device to continue operation. This is by design. When two or more ISD1020As are cascaded together to make messages longer than 20 seconds, the device must stop operating when it reaches the end of its memory space so the next chip in the series can take over. This condition is called "memory overflow."

To get around the requirement to cycle the Power-Down pin after a memory overflow, the circuit design shown here automatically cycles the device through a power-down cycle each time the chip enable is activated. All four push buttons are connected to the $\overline{CE}$ pin and to C11 through diodes. The R16, C10 network "debounces" the chip enable input. When you press a push button, a sequence of events happens:

1. The $\overline{CE}$ input that is normally held HIGH through R6 is pulled LOW through a diode.
2. The combination of C11 and R5 on the base of Q1 causes a positive pulse to be generated into the PD pin of the ISD1020A.
3. For the duration of this pulse, the ISD1020A is in a power-down state that resets a memory overflow condition if it exists.
4. When the pulse ends and the PD pin returns to ground, the status of the $\overline{CE}$ pin is read.
5. Assuming the $\overline{CE}$ pin is still being pulled LOW (don't be too quick on the push button), the status of the address and P/$\overline{R}$ pins is read and the Record or Playback operation begins.

Components R2 and C2 control the AGC operation of the ISD1020A's internal microphone preamplifier. The AGC pin has an impedance of about 5K ohms. This resistance plus C2 determines the attack time of the AGC which should be very fast. R2 and C2 together determine the release time of the AGC which should be fairly slow.

C3 connects the output of the microphone preamplifier (ANA OUT, pin 21) to the analog input (ANA IN, pin 20) of the ISD1020A. These pins are brought out externally so the user can control the low frequency response of the recording or directly access the analog storage memory of the ISD1020A. A 1 μF capacitor at this location sets the low frequency response to 80 Hz. Users who do not want to use the AGC should capacitively couple to the ANA IN pin with an 50 millivolt peak-to-peak signal.

The speaker output of the ISD1020A is designed to drive a 16-ohm speaker. To use an 8-ohm speaker, install R8 to bring the impedance into specification. If you use a 16 Ω speaker, R8 should be replaced with a wire jumper.

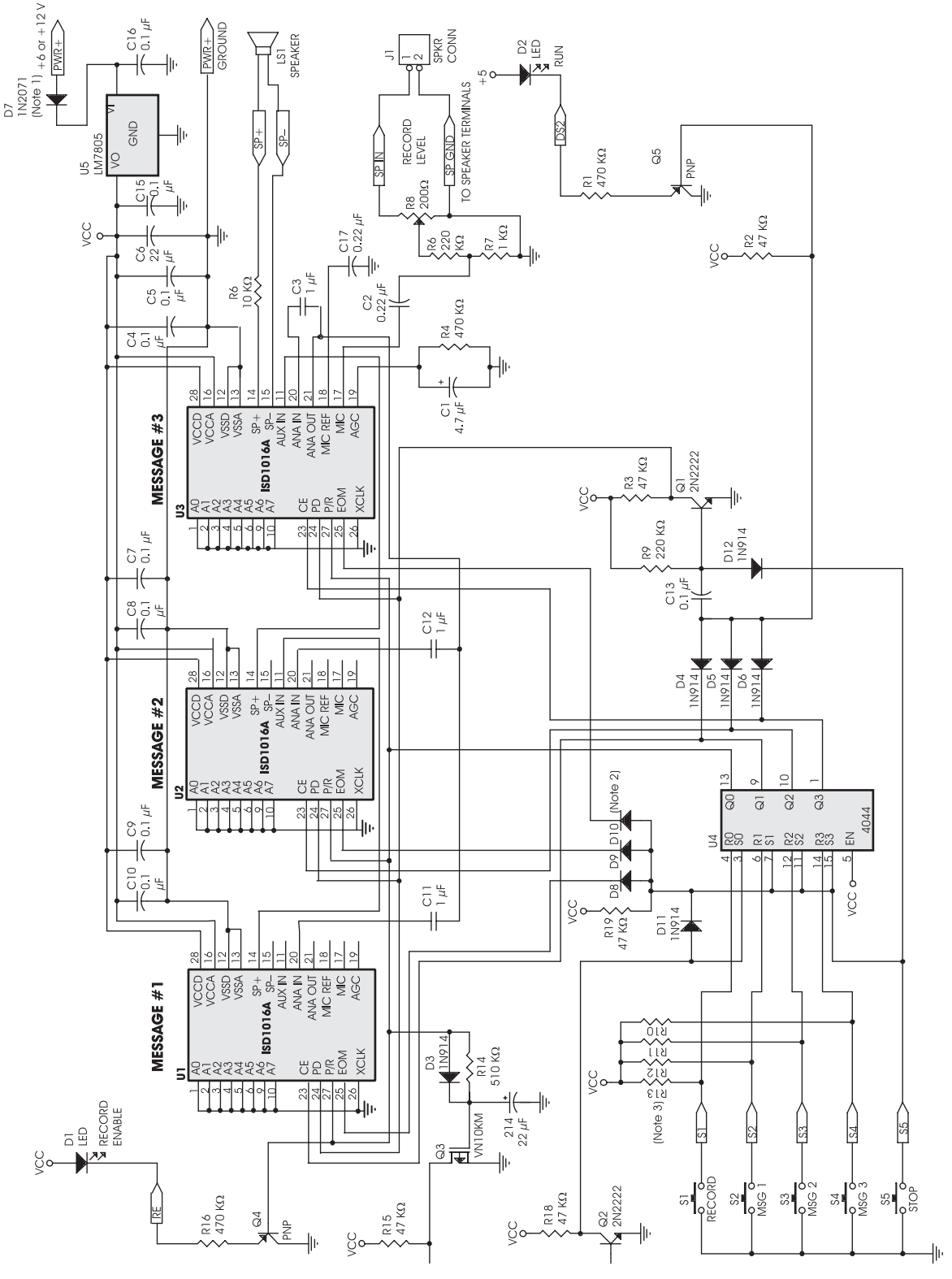
The ISD1000A series does not have a "RUN" output to show when a device is playing back speech. Such a signal is easy to create, however, using a pair of the two input NOR gates contained in a 4001. These gates (U2A and U2B) are connected in a "cross-coupled" configuration and are set by PD signal going LOW at the beginning of Playback and reset by $\overline{EOM}$ going LOW at the end of a message. The resulting signal drives the base of the Q2 2N2222 transistor through R21. U2D keeps the gate from being set during a record operation. U2C and the RC network C15 and R20 correct a possible race condition between the PD signal and $\overline{EOM}$.

OPERATION

Operation of the circuit is simple. To record a message, change the Record/Playback switch to record, then press and hold the desired address button for the duration of the message. To play the message back, change the Record/Playback switch back to Playback and momentarily press the button. The ISD1020A will replay the message.

Keep in mind when recording a new message that if you record a message longer than the address space you have reserved for it, you will begin erasing the next message in the series (unless you go into memory overflow). If you then try to select the message you just erased part of, you will get the end of the new message starting at the message address of the message you just "corrupted." If you *want* to record a message longer than its allowed message space, just go ahead and do it. Just remember that the next message is not available in this instance.

Figure 8: Radio Notepad Schematic



1. *D7 is a polarity protection diode.*
2. *D8, D9, and D10 are IN914*
3. *R10, R11, R12, and R13 are 47 KΩ.*

RADIO NOTEPAD

The circuit in Figure 8 presents a method of storing three different 16-second messages using a speaker input. The suggested application is for recording messages from a radio receiver.

There are many applications that require the recording of audio directly from a speaker. A shortwave listener-hobbyist may want to record an event heard on a shortwave or two-way radio channel. There may be a call sign, a radio frequency or some other information announced over the air that needs recording for later review. In a public safety environment, a police dispatcher may want to record an incoming call for assistance to ensure no details are missed.

With the circuit in Figure 8, a simple two button sequence is all it takes to record the next 16 seconds. A single push of a button plays each message back. Three ISD1016As are used to hold independent messages. An ISD1020A could be used instead if desired. This circuit example also demonstrates an ISD1000A device run entirely from push buttons.

HOW IT WORKS

The heart of this application is a 4044 CMOS Quad NAND R-S Latch and a VN10 FET timer. The 4044 (U4) "remembers" which message button has been pressed when a Record or Playback operation is desired. The FET timer enables a record operation for its time period. The rest of the circuit is principally diode steered logic.

A Playback operation is initiated by pressing S2, S3 or S4 (MSG 1, MSG 2 and MSG 3 respectively) which resets the appropriate section of U4. The output of the cleared Flip Flop goes LOW, enabling the correct $\overline{CE}$ for the ISD1016A holding the message selected. This output also pulls C13 LOW causing Q1 to initiate a PD cycle clearing any possible overflow condition. The base of Q1 is pulled LOW, allowing R3 to pull its collector HIGH, resetting the PD pins of U1-U3. As R9 charges C13 back up the PD line returns LOW. When the PD cycle ends, the selected device plays back its stored message. When a set EOM bit is found or an overflow occurs in the operating ISD1016A, Playback stops and the $\overline{EOM}$ signal goes LOW, setting the U4 flip flops through D8, D9 or D10. Or, a momentary press of the STOP button resets the set R/S flip-flops and initiates a PD cycle. This also ends Playback.

A record operation is started by first pressing the S1 "Record" button. This clears the Record Enable section of U4 (R0/S0/Q0) whose Q output goes to the P/$\overline{R}$ input of all the ISD1016A's. This holds these pins LOW or in the record state. This flip-flop stays cleared until the Q3, R14, C14 network times out. When this happens, the signal from the collector of the Q2 NPN inverter transistor sets the first section of U4, returning all the P/$\overline{R}$ inputs HIGH, back to Playback. If S2 through S4 is pressed while the Q3 timer is running, the appropriate ISD1016A will start recording. A press of the STOP button will end recording by forcing the chip enable lines HIGH out of U4 and setting an EOM bit in the recording device, U1–U3. The values of R14 and C14 are chosen so that the P/$\overline{R}$ pins are held LOW throughout the complete record cycle, or in this example, greater than 16 seconds. If an ISD1020A is used, the value of R14 should be made greater so this time period is greater than 20 seconds.

OPERATION

To operate the radio notepad, connect the input across the speaker terminals and apply power. To record, press the record Enable S1 button then immediately press S2, S3 or S4. Recording will start with the press of the second button. The record Enable LED, D1, along with the RUN LED, D2, will indicate that a record operation is in progress. To stop recording, or to clear a record Enable condition before it times out, press the S5 Stop button. To Playback, press S2, S3 or S4. The message recorded in the appropriate ISD1016A will Playback until the 16 seconds is complete or a set EOM bit is found in the device's EOM memory. The RUN LED, D2, will indicate when a message is being played back. To stop Playback, press Stop.

Some experimentation with the setting of the R8 Record Level pot may be necessary to get good results.

USING THE ISD2500 SERIES WITH A MICROCONTROLLER

The record and playback duration of the ISD2500 series make it possible to perform several functions with a single device. A chip with 32 or more seconds of storage may be used in a number of ways. A library of permanent words, phrases or sounds may be individually played back under external control. Alternatively, this device might be used to record and randomly retrieve arbitrary length messages. A combination of these two approaches is also possible.

Combinational logic may be used to achieve these ends. This approach is complex, however. An inexpensive microcontroller is a simpler and much more flexible solution. The following notes demonstrate several methods of using a single chip microcontroller to control an ISD2500 device.

NOTE ***The address lines of all ISD single-chip record/playback devices are not microprocessor bus compatible.*** *If a device is to be used on a bus oriented system, the address lines must be buffered and latched.*

CONVENTIONAL MODE OPERATION

An obvious method of driving the device is to operate it in the conventional mode. The sequence for such an operation is as follows:

1. Change the PD pin to LOW and delay T_{PUD} (see the ISD2500 series data sheets). This will power up the device.
2. Apply the desired address to the address inputs.
3. Apply the correct level to the P/$\overline{R}$ pin as desired (0 = record, 1 = play).
4. Pulse $\overline{CE}$ LOW to begin Playback, hold $\overline{CE}$ low to begin record, bring $\overline{CE}$ back HIGH to end record.
5. If low power is required, change PD back to HIGH when the operation is complete.

The timing of the above sequence is not critical at microcontroller speeds. For instance, required address setup timing (T_{SET}) is 300 nanoseconds before the falling edge of $\overline{CE}$. Few microcontrollers can execute fast enough to violate this timing.

A microcontroller may be used to detect the end of a normal speed Playback operation in at least two ways.

- Since the $\overline{EOM}$ pulse width in the fastest ISD2500 series parts (ISD2532/60) is over 12.5 milliseconds long, it is possible to poll this input and watch for it to go LOW.
- An alternative method would be to connect the $\overline{EOM}$ pin to the microcontroller's interrupt input. If an edge-triggered interrupt sense is available, it may be more efficient to sense the rising edge of $\overline{EOM}$. This is because a new $\overline{CE}$ initiated operation cannot begin until $\overline{EOM}$ pin returns to the HIGH state.

The ISD2500 series includes the $\overline{OVF}$ pin to indicate the overflow or message full condition. During Playback the $\overline{OVF}$ pin pulses LOW for approximately 6 microseconds when overflow is reached. The $\overline{EOM}$ pin does not go LOW at overflow unless an EOM bit is set in last row of the analog memory. After the initial $\overline{OVF}$ pulse goes LOW, the $\overline{OVF}$ pin will track the $\overline{CE}$ input as long as the device remains in overflow. This pin is normally used to cascade multiple ISD2500 devices together.

The original short $\overline{OVF}$ pulse may be detected using the microcontroller's external interrupt input. An alternative technique would be to hold $\overline{CE}$ LOW, even during Playback. The $\overline{OVF}$ pin will now go LOW and stay LOW at overflow and may be detected by polling. In this example, a falling $\overline{EOM}$ must be detected and used to force $\overline{CE}$ back HIGH. $\overline{CE}$ must go back HIGH before $\overline{EOM}$ goes HIGH. If $\overline{EOM}$ goes HIGH with $\overline{CE}$ still LOW, the set EOM bit will be skipped and the device will continue on playing back the next message.

MESSAGE CUEING "FAST FORWARD" OPERATION

Some applications may require the use of the Message Cueing M0 Operational Mode. This mode allows the user to "fast forward" through the message space of the device (see the section on Operational Mode). When operating in this mode, the ISD2500's internal timing is sped up by a factor of 800. The $\overline{EOM}$ pulse width now may be as small as 11 ms. (A general discussion of Message Cueing timing may be found in the section on Operational Modes.) This timing is too short to allow for polled operation in most microcontrollers. The external interrupt should be used to detect $\overline{EOM}$ in this instance.

Pin count is often a factor when using a microcontroller. The designer may not want to tie up 8 pins for address plus PD, $\overline{CE}$, P/$\overline{R}$, $\overline{OVF}$ and $\overline{EOM}$. This is a total of 13 pins. An alternative approach is to use the Message Cueing M0 Operational Mode with the M4 consecutive addressing mode. This application requires the connection of only 6 pins to the microcontroller: PD, $\overline{CE}$, P/$\overline{R}$, $\overline{OVF}$, $\overline{EOM}$ and M0. M4, A8 and A9 are permanently tied HIGH and all the rest of the address pins are tied LOW. Sequential recordings of multiple messages of random length and the playback of those messages in any order are possible in the following sequences.

Sequential Recording

1. M0 is left LOW throughout record.
2. Change the PD pin to LOW and delay T_{PUD}.
3. Change P/$\overline{R}$ to LOW.
4. Hold $\overline{CE}$ low to begin the first record. Bring $\overline{CE}$ back HIGH to end record.
5. Additional record operations may be done using sequence 4. Each recording will be appended to the end of the previous with an EOM flag bit set at the end of each messages.
6. $\overline{OVF}$ will go LOW if the device overflows during record.
7. At the end of the record sequence, PD is taken HIGH to power down the device and to reset the internal address counter.

Playback of Messages in Any Order

To playback message "N," perform the following sequence:

1. Change the PD pin to LOW and delay T_{PUD}.
2. Change P/$\overline{R}$ to HIGH.
3. If N = 1 (the first message), then A0 = 0, and pulse $\overline{CE}$ LOW. The first message will play then stop.
4. If N is greater than 1, you must first execute N-1 A0 Message Cueing Operational Mode cycles by doing the following:
   - **a.** Change A0 to HIGH.
   - **b.** Pulse $\overline{CE}$ LOW for less than 10 μs.
   - **c.** Either watch for a LOW $\overline{EOM}$ (may be as short as 11 μs) or pause for approximately 100 ms.
   - **d.** Each time you find an EOM, you have reached the end of a message. You will have moved silently through a message at 800 times normal speed.
   - **e.** Subtract 1 from N. If N does not equal 1, proceed to sequence (a) and do it again.
5. If N has been subtracted down to 1, then change A0 to 0 and pulse $\overline{CE}$ LOW. The Nth message will play at normal speed.

NOTE *The timings above are approximate. See the Operational Modes for a general discussion of Message Cueing Timing.*

PUSH-BUTTON MODE OPERATION

The ISD2500 series device includes a new Operational Mode called "Push-Button Mode." This M6 Operational Mode changes the functionality of the $\overline{CE}$, PD and $\overline{EOM}$ pins. The operations of these pins are fully explained in the Operational Mode section. A microcontroller may be used with this mode to gain several important extra features. Push-Button Mode allows the user to sequentially

playback several messages then change to record and add additional messages at the end of those already played. This also allows the designer to power-down the device between sequential record operations, an important feature in battery powered applications.

Sequential Record with Power-Down in Between

In the following sequences, M4, M6, A8 and A9 of an ISD2560 are tied together and to a pin of the microcontroller. The A0 Message Cueing Operational Mode is used as indicated. All the other address pins are tied LOW. It is only necessary to use 6 pins from the microcontroller, PD (Stop/Reset), $\overline{CE}$ (Start/Pause), $\overline{EOM}$ (run), P/$\overline{R}$, A0 and the combined M4, M6, A8 and A9. These combined pins will be called Op Mode Control. $\overline{EOM}$ is tied to the microcontroller's external interrupt pin. The microcontroller should be set up for a negative edge triggered interrupt. $\overline{OVF}$ is not needed as explained below.

To achieve flexible message control, the microcontroller must keep track of the number of messages recorded and played back. This count will be used with the A0 Message Cueing "fast forward" function to record messages sequentially and play them back in any order.

NOTE *A false interrupt is generated each time a control operation causes the $\overline{EOM}$ to fall. These interrupts should be ignored by the microcontroller. The $\overline{EOM}$ pin will go LOW and generate a wanted interrupt under two circumstances: during Playback or Message Cueing when a set EOM bit is encountered and during record when the device goes into overflow. This also allows the designer to determine when overflow is reached without looking at the overflow pin.*

---

1. The sequence begins with PD HIGH, P/$\overline{R}$ HIGH, $\overline{CE}$ HIGH and Op Mode control LOW.
2. Set up to record of the first message by taking PD LOW, P/$\overline{R}$ LOW, and Op Mode control HIGH.
3. When the OP Mode control pin goes HIGH, the $\overline{EOM}$ pin (which becomes the active HIGH run pin in Push-Button Mode) pin will go LOW to indicate the operation has not yet started. This will cause an interrupt in the microcontroller that should be "discarded."
4. To begin record, pulse $\overline{CE}$ LOW (a pulse begins and ends record in Push-Button Mode). The $\overline{EOM}$ pin will go HIGH to indicate an operation in progress. When recording is finished, pulse $\overline{CE}$ LOW to end the record cycle. The $\overline{EOM}$ pin will go LOW and generate another false interrupt.
5. After the completion of the record, change the Op Mode control pin to HIGH, and take PD HIGH. This powers down the ISD2560 device to typically 1 microamp.
6. To record the second message, take PD HIGH (T_{PUD} delay), P/$\overline{R}$ HIGH, and Op Mode control HIGH (false interrupt). We are now positioned at the beginning of the first message. Take A0 HIGH and pulse $\overline{CE}$ LOW. This puts the device into Message Cueing "fast forward" and jumps to the end of the first message. The $\overline{EOM}$ pin will go HIGH and then LOW to indicate the end of the first message has been found. The $\overline{EOM}$ interrupt may be used by the microcontroller to process this.
7. A0 may now be taken LOW, P/$\overline{R}$ changed to LOW, and a new record cycle begun. A unique feature of Push-Button Mode keeps the internal address pointer of the ISD2560 from being reset during the change of P/$\overline{R}$ from HIGH to LOW. Recording of the second message will begin at the end of the first message. The set EOM bit at the end of the first message will remain. The device may again be powered down.
8. Subsequent recordings may be made using additional A0 Message Cueing operations.

Playback Operations

Playback of any message may be achieved using the Push-Button and A0 Operational Modes.

1. The sequence begins with PD HIGH, P/$\overline{R}$ HIGH, $\overline{CE}$ HIGH and Op Mode control LOW.
2. Change PD to LOW (T_{PUD}), and Op Mode control HIGH (false interrupt).
3. Take A0 HIGH and execute N-1 Fast Forward operations.
4. Take A0 LOW and pulse $\overline{CE}$ LOW to begin playback of the desired message.
5. A falling $\overline{EOM}$ indicates an end of message has been found.
6. Take Op Mode control LOW and PD HIGH to power-down the device.

OTHER NOTES

A continuous LOW on the interrupt input of some microcontrollers may interfere with other types of interrupts. The reason that the device is taken out of Push-Button Mode after each operation is to make the $\overline{EOM}$ pin go HIGH in the static state. This frees up the microcontroller's interrupt structure.

All Push-Button Mode operations will be slowed by the debounce timer built into this function. A delay of T_{DB} will occur with each Push-Button Mode operation.

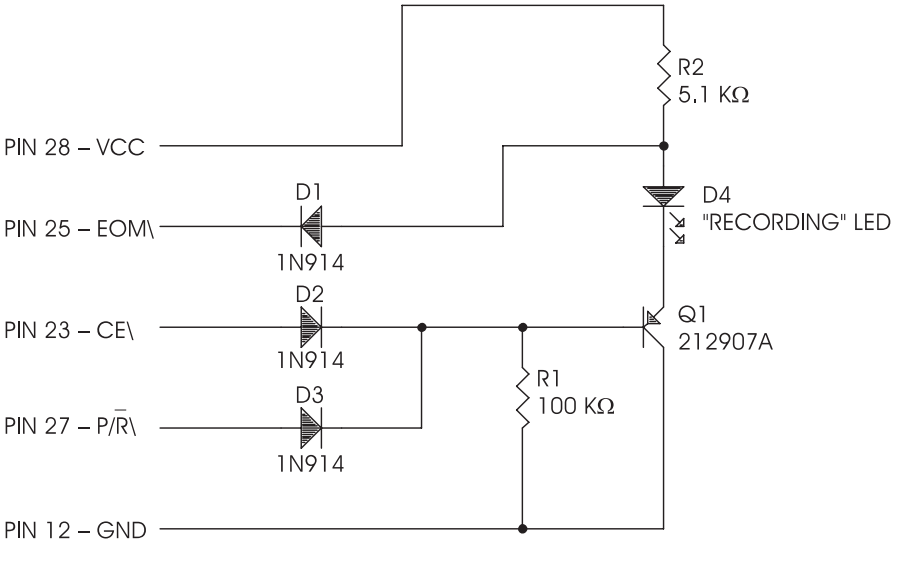
CONCLUSION

The above explanations show one of many possible ways to control the ISD2500 series device with a microcontroller. The designers should review this information and apply their unique perspective to the application they are designing.

RECORDING INDICATOR LIGHT

The circuit shown in Figure 9 is a simple method of using an LED to indicate when a record operation is in progress with an ISD1000A series device.

Figure 9: Recording Indicator Light for ISD1000A

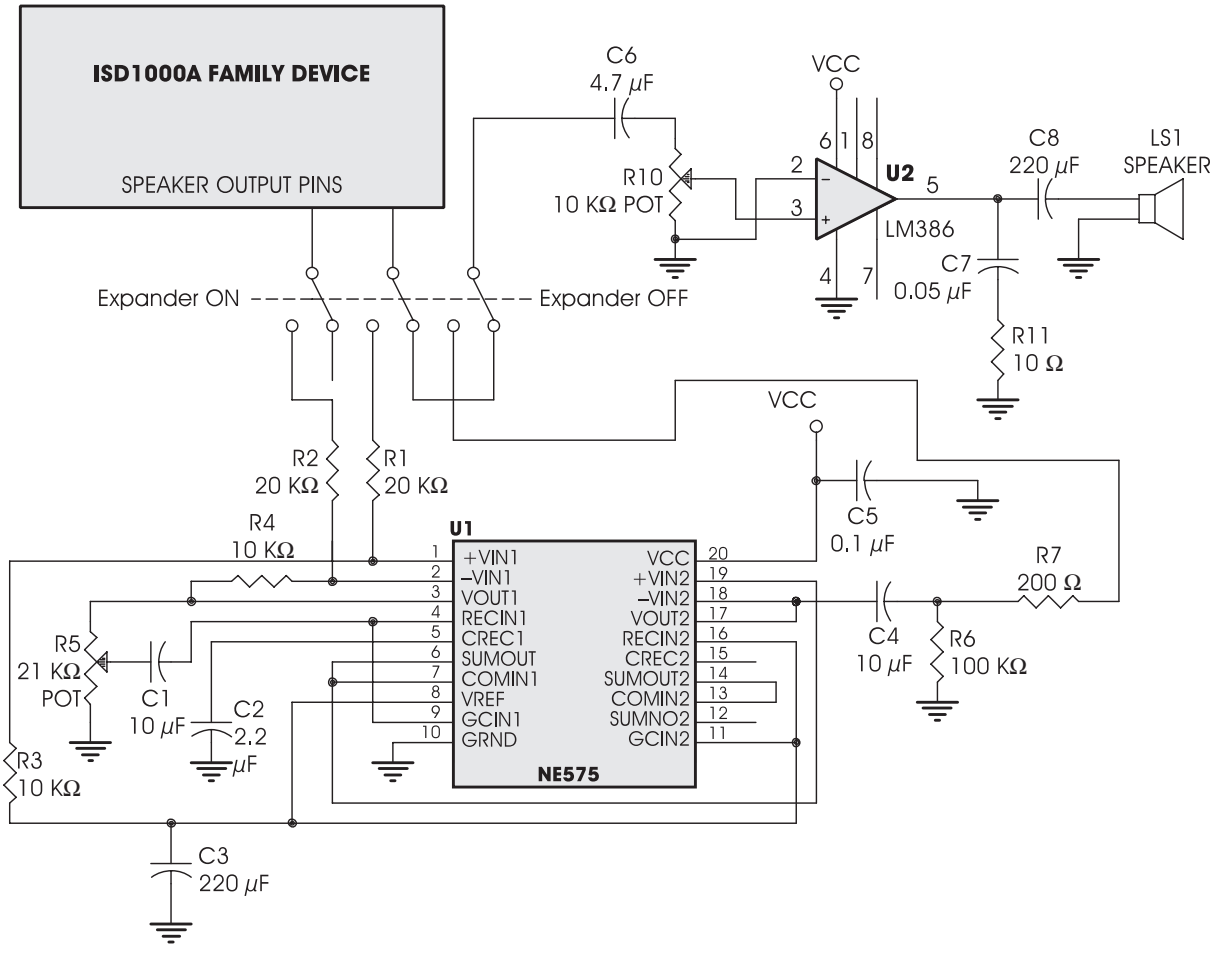


NOTE: *This circuit will turn on the LED only when actually recording. It requires a valid record selection (P/$\overline{R}$ LOW), and $\overline{CE}$ LOW to turn on. At the end of the time in the chip, EOM goes LOW and turns off the LED.*

CIRCUIT EXPLANATION

This circuit uses a PNP transistor to cause an LED to light only during a record operation and only when the ISD1000A device is not in overflow. The logic is very simple: when $\overline{CE}$ is LOW and P/$\overline{R}$ is LOW the PNP transistor conducts unless $\overline{EOM}$ is LOW.

Figure 10: Expander Circuit for Low Noise Playback



NOTE: *V_{CC} = 5 volts plus or minus 10 percent.*

EXPANDER CIRCUIT FOR IMPROVED NOISE PERFORMANCE

The circuit in Figure 10 was developed to provide an enhanced signal to noise ratio in applications where the output of the ISD device would be amplified considerably. A public address system or warning device in a high noise environment could benefit from the lower "effective noise" provided by this circuit.

The Expander circuit was assembled to illustrate the difference between the direct SNR and the SNR through the NE575 device. Although the ISD device will drive the 16 Ω speaker directly, the NE575 cannot. It is designed for 600 Ω applications so the LM386 audio amplifier had to be added to drive the speaker.

The circuit is adjusted so that the peak audio level from the ISD device is the same direct to the LM386 or through the NE575 to the LM386. Then, when the NE575 is switched in, the noise floor is "pushed down" to an inaudible level.

The result is that a public address system will not have an audible "hiss" when playing a message.

The result can be dramatically demonstrated during playback by moving the switch between the two positions and listening carefully in the pauses between syllables.

The Phillips/Signetics NE575 is one of a group of compander circuits used in telecommunications. Normally one half of the chip compresses incoming audio by 2:1 to transmit over the communications channel. The other half takes the received audio and expands it back to its original dynamic range. It is this half that is used in Figure 10. The compressor is not used. The audio in the ISD1000A has already been "compressed" to a degree by the AGC of the microphone preamplifier. If the ANA IN pin were used for recording, then perhaps the compressor half of the NE575 would be used.

The NE575 is a 20-pin version but there are smaller, less expensive versions such as the NE576 or NE577. These are all fully described in the Phillips RF Data Book. The applications include cordless and cellular phones, wireless microphones, and consumer audio devices such as automotive CD players.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Circuit Examples for ISD1100, ISD1200 and ISD1400 Products

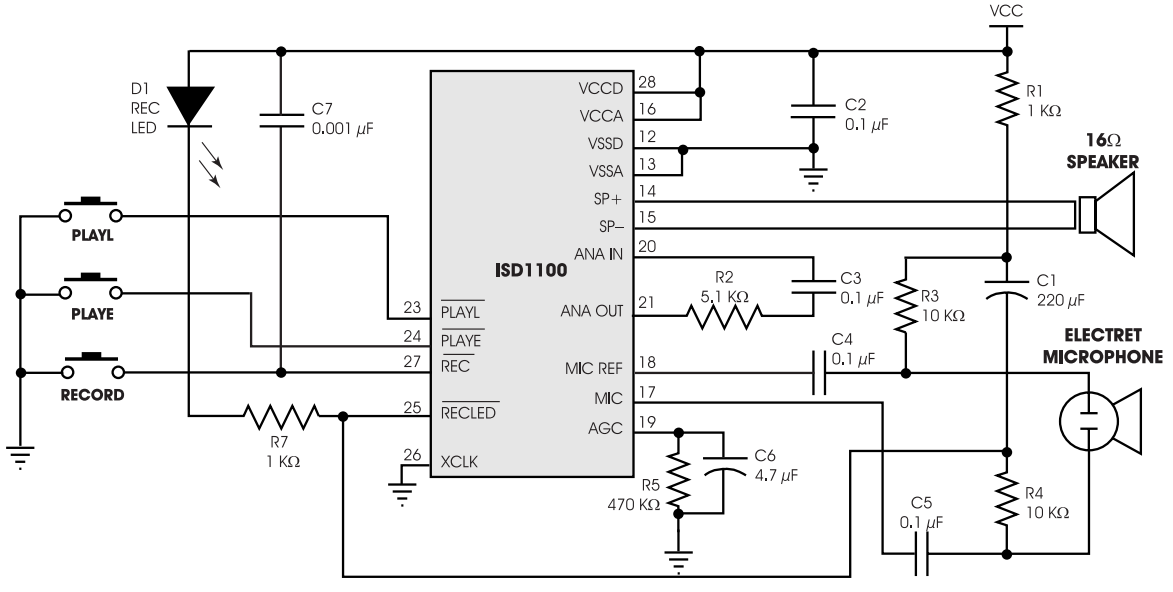
This chapter provides various applications for the ISD1100, ISD1200, and ISD1400 series of products. Most of these applications can use the ISD1200 or ISD1400 series interchangeably. In some cases the ISD1100 series may also be used. See Application Brief 3 for a discussion of the differences between the ISD1200 and the other two device series.

MINIMUM PARTS COUNT ISD1100 APPLICATION

An ISD1100 series device may be used to make a very low power record and playback system with automatic power down. An added difficulty arises for the designer, however, due to the continuous current drain of the electret microphone bias circuit. Figure 1 shows a schematic diagram that neatly solves this problem by using the $\overline{\text{RECLED}}$ output of the ISD1100 to provide the ground for the microphone bias circuit only during the time recording is active. Since $\overline{\text{RECLED}}$ only goes LOW during record, it shuts off current to the microphone bias circuit when recording is complete. C1 supplies filtering for the microphone bias circuit.

Another feature of this circuit is the differential use of the electret microphone. The microphone is connected directly between MIC and MIC REF on the ISD1100. Since R3 and R4 are equal resistors, power supply noise will be a common mode signal and will be rejected by the ISD1100's microphone pre-amplifier.

Figure 1: Simple Application for ISD1100 Series Device



The $\overline{\text{REC}}$, $\overline{\text{PLAYL}}$, $\overline{\text{PLAYE}}$ and address inputs have on-chip pull-up or pull-down resistors. (For a complete discussion of the ISD1100's on-chip pull-up or pull-down resistors, see Application Brief 3). Simple push buttons or slide switches may be used with an ISD1100 series product. The device will draw approximately 50 μA while each push button is pressed.

RECORD

Press and hold the $\overline{\text{REC}}$ push-button. The $\overline{\text{REC}}$ LED will illuminate to indicate recording is in progress. If overflow is reached, or the button is released, the LED will go out and the ISD1100 will automatically power-down. Since the $\overline{\text{RECLED}}$ output is now at V_{CC}, no current will be drawn by the microphone bias circuit.

PLAYBACK WITH A SINGLE PRESS OF A BUTTON

Press and release the $\overline{\text{PLAYE}}$ push-button. The message contained in the device will playback until it reaches a set EOM bit or OVF. Playback will then cease and the device will power down.

PLAYBACK USING A SLIDE SWITCH OR CONTINUOUS PRESS OF A BUTTON

Press and hold the push button or close the slide switch to begin and continue playback. If overflow is reached, the push button is released or the slide switch is opened, the device will end playback and automatically power down.

NOTE *If the push button is held down or the slide switch remains closed, the on-chip pull-up resistor will continue to draw approximately 50 μA of current.*

MINIMUM PARTS COUNT ISD1200/1400 APPLICATION

A minimum ISD1100/ISD1200 application is similar to the above ISD1100 application. The differences are caused by the lack of on-chip pull-up and pull-down resistors on the ISD1200/ISD1400 series devices. All inputs to the ISD1200/ISD1400 must be strapped to V_{CC} or V_{SS} or pulled up (or down) with external resistors. A representative circuit is shown in Figure 2. The operation of these devices is identical to that described in the above ISD1100 application.

AUTOMATIC POWER-UP LOOPING

There is one circuit function the ISD1000A device can do that the ISD1100, ISD1200, and ISD1400 cannot, which is power-up in looping playback. The ISD1100, ISD1200, and ISD1400 series all power-up with the input pins "locked out" and remain in that state until an internal power up delay time is satisfied. These new products include a playback looping Operational Mode. Unfortunately, the on-chip built-in power up delay ends the ability to automatically power up with the looping function enabled.

The circuit in Figure 3 shows an alternative way to accomplish this function. C1 rapidly pulls the $\overline{\text{PLAYE}}$ pin to V_{CC} when voltage is applied to the circuit. After the power up delay time is satisfied, the voltage decay caused by R1 allows the $\overline{\text{PLAYE}}$ to drop below its "ON" threshold and the device begins playback. Since the device is in Operational Mode (A6 and A7 are HIGH), and A3 is HIGH, playback loops on the first message contained in its memory. Playback looping will continue until power is removed from the device.

The designer should assume power up delay time of at least 25 ms before the $\overline{\text{PLAYE}}$ pin voltage level falls below minimum V_{IH} to ensure the circuit will correctly be put into looping mode.

Figure 2: Simple Application for ISD1200/ISD1400 Series Device

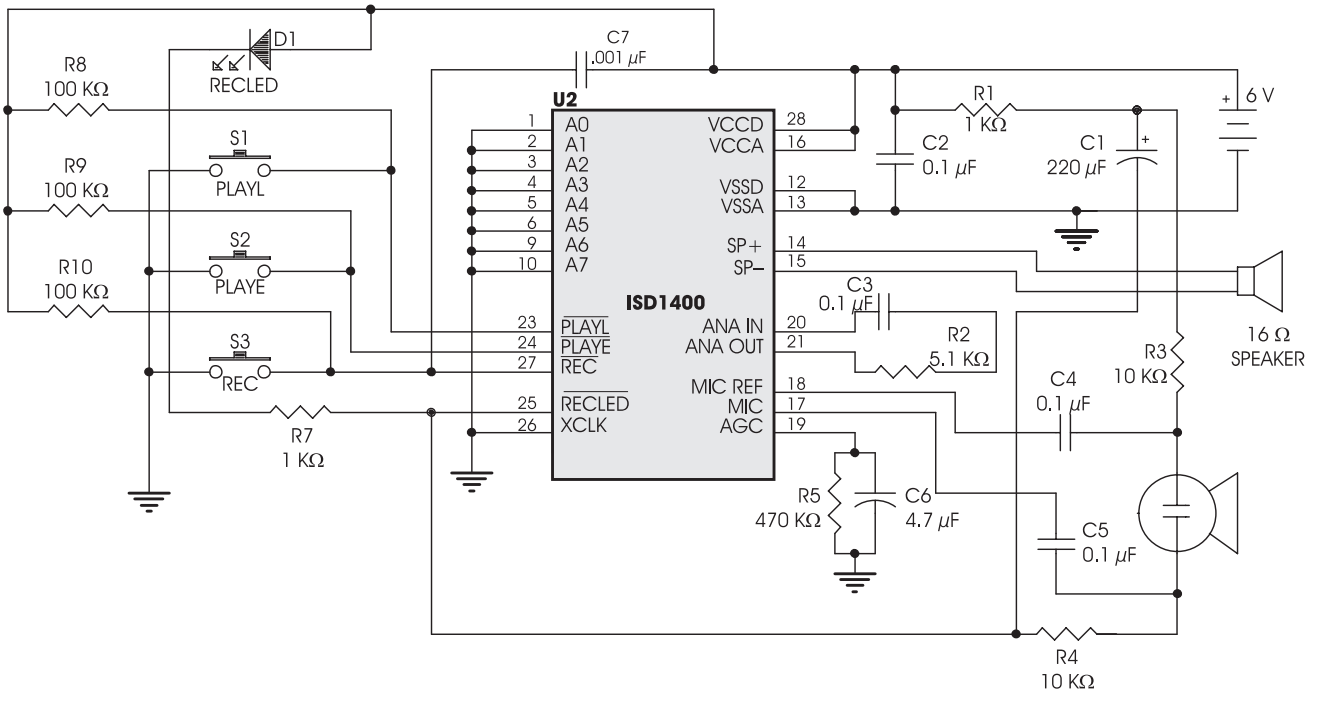
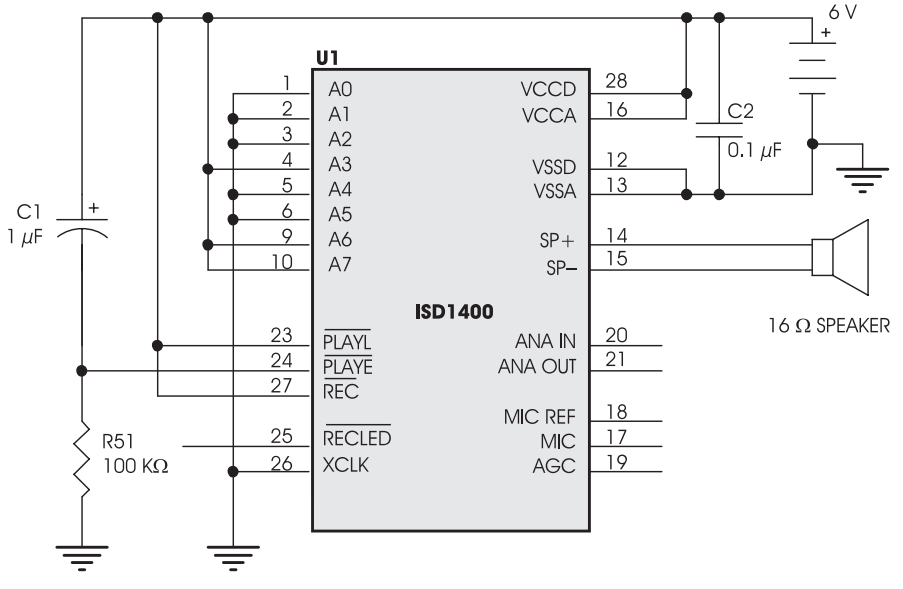


Figure 3: Automatic Power-up Looping



LOOPING AT ANY ADDRESS

The ISD1100, ISD1200, and ISD1400 products are recommended for new designs in the 10- to 20-second storage duration because of their simpler interface and automatic power-down capability. These devices include an Operational Mode (A3) that allows automatic looping at a message that starts at the beginning of memory or address "0." Some customers, however, want to loop on a message that begins at an address location other than "0." This allows them to store several messages in one device and select one of them for automatic looping.

Figure 2 under the section "Circuit Examples for ISD1000A and ISD2500 Products" shows a circuit that performs this function using the ISD1000A device. A slightly different circuit is required for the ISD1100, ISD1200, and ISD1400 series device. The diagram and explanation that follow demonstrate how this may be achieved.

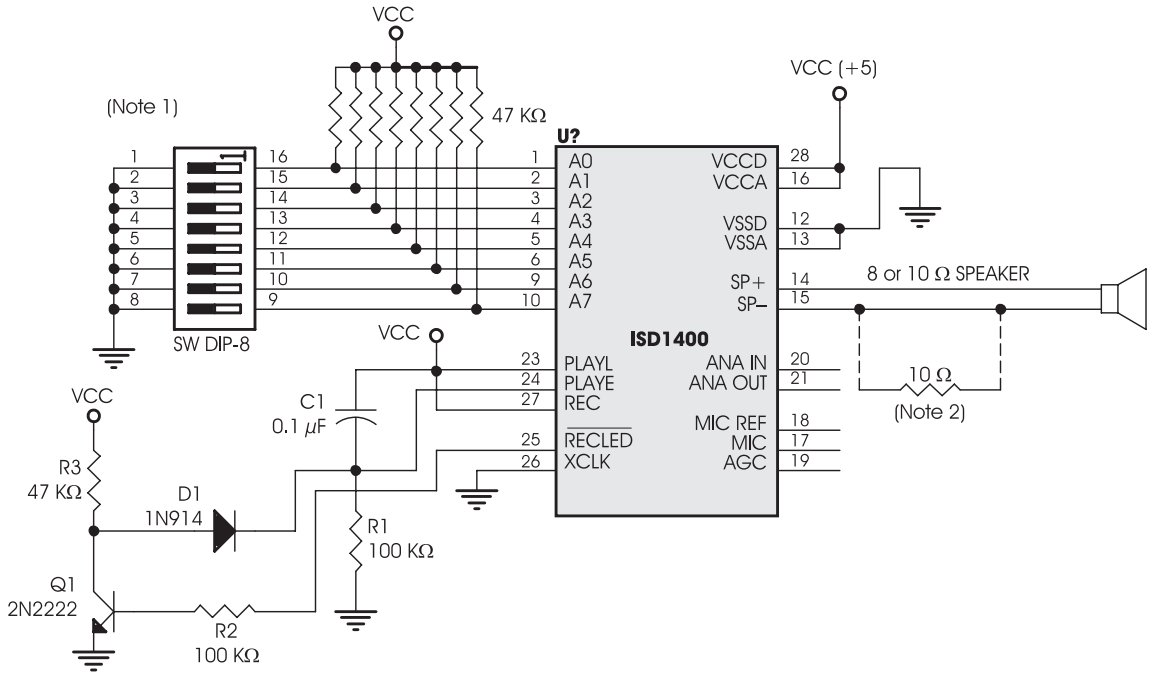
Figure 4 shows how the $\overline{\text{RECLED}}$ signal may be used to make the ISD1100, ISD1200, and ISD1400 device to loop on a message at an address other than "0." The R1-C1 combination causes the loop to automatically start at the address set by the dip switches when power is first applied to the circuit. If this is not desired, C1 should be replaced with a push button. A momentary closure of the push button will start the circuit to loop on the addressed message.

An unfortunate side effect of this circuit is a slight pop or "click" that occurs at the beginning of each loop. The circuit designer should evaluate their system requirements to determine whether or not this is a problem in their application.

FIXED MESSAGE AND RE-RECORDABLE MESSAGE SEGMENT EXAMPLE

Many applications require a fixed factory programmed message plus some capability for the end user to also program one or more messages. By manipulating the address and $\overline{\text{REC}}$ lines of the ISD1100, ISD1200, and ISD1400 series products, this capability may be easily achieved with few external parts. The following applications discussion and schematic show how this may be accomplished. While the ISD1400 is specifically mentioned, the ISD1100 and ISD1200 series may also be used in exactly the same way as long as the address and pull-up/pull-down resistor differences are understood.

Figure 4: Looping at Any Address[3]



1. *Only address 0 through 159 (decimal) are valid.*

2. *Add the 10 Ω resistor if an 8 Ω speaker is used.*

The applications schematic in Figure 5 shows a method for dividing the ISD1400 device into two messages.

- One of the messages is permanently recorded into the device by the manufacturer.
- The second message may be recorded (and erased and recorded again) in the field by the end user.

This design divides divide the device into a 4-second permanent message and a 16-second re-recordable message. The same techniques could be used to divide the memory into other combinations of permanent and recordable messages.

The permanent message (less than 4 seconds) is recorded at the OEM location at address "0" in the ISD1400. Recording of this message is explained below. Once recorded, there is no way to record over the analog memory at address "0" so the message cannot be erased.

RECORDING THE PERMANENT MESSAGE

The permanent message may be recorded into a packaged device before installing it into a circuit board. Once installed, the permanent message cannot be recorded over as long as JP1 is left intact.

The product may also be built using ISD1400 die. In this case, the permanent message is programmed by recording into the device before JP1 is installed. Simply press S2 and feed the audio to be recorded into the connection marked "Record In." Next install JP1 and the message is permanent.

NORMAL OPERATION

The normal operation of the device is simple. With S3 open, press S1 to playback the permanent message. With S3 closed, press S1 to playback the re-recordable message. Press S2 to record a message starting at the 4-second boundary.

CIRCUIT EXPLANATION

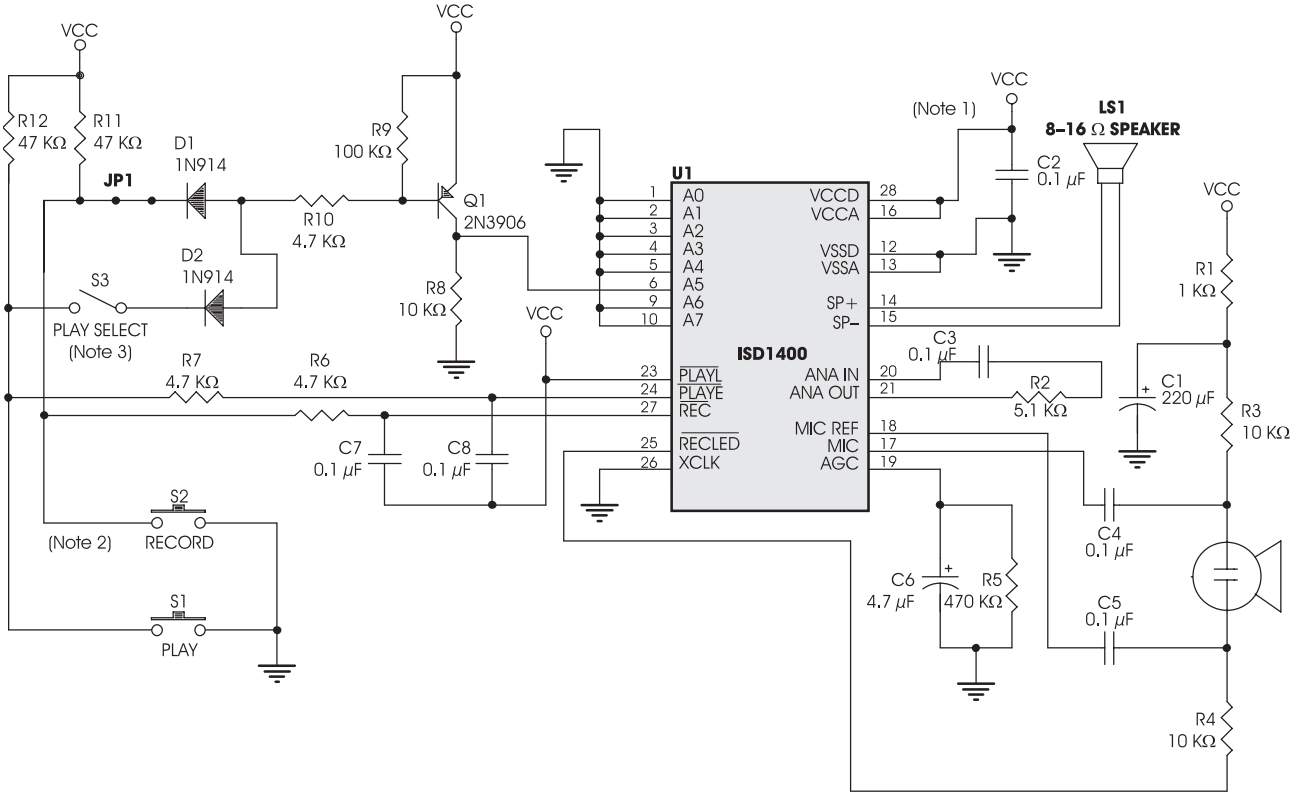
The PNP inverter transistor Q1 drives the address line A5 of the ISD1400. When S2 is pressed, D1 provides a base current path turning on Q1. Collector current through R8 brings A5 to a "1" level. The $\overline{REC}$ pin's LOW transition is delayed by the RC time constant set up by R6–C7 to satisfy the address set up time of the ISD1400. Record starts at address 0010 0000 of the device which equates to recording starting at the 4-second point in the memory.

When S1 is pressed with S3 closed, playback starts in a similar fashion at the 4-second point with the control signal coupled to Q1 through D2. R7–C8 provides the address set up delay.

When S1 is pressed with S3 open, playback then begins as address 0000 0000 of the ISD1400. This is the beginning of the device's memory.

On the analog side of the circuit, C4 and C5 have been changed from the ISD suggested value of 0.1 µF to 0.01 µF to roll off the low frequency response of the ISD1200 microphone amplifier. By reducing the lows, during playback more high frequency energy will be transferred to the speaker, making the sound seem louder and easier to hear.

Figure 5: Fixed and Re-recordable Message Segment Circuit Example



1. *V_{CC} = 4.5 to 6.5 volts.*
2. *Pressing S2 begins recording at 4-second boundary. Pressing S1 starts Playback at 0 or 4 seconds according to switch S3 setting.*
3. *S3 open, Playback begins at 0, S3 closed, Playback begins at 4 seconds.*

SIMPLE MULTIPLE MESSAGE APPLICATION WITH $\overline{\text{EOM}}$ DELETE AND ADDRESS RESET

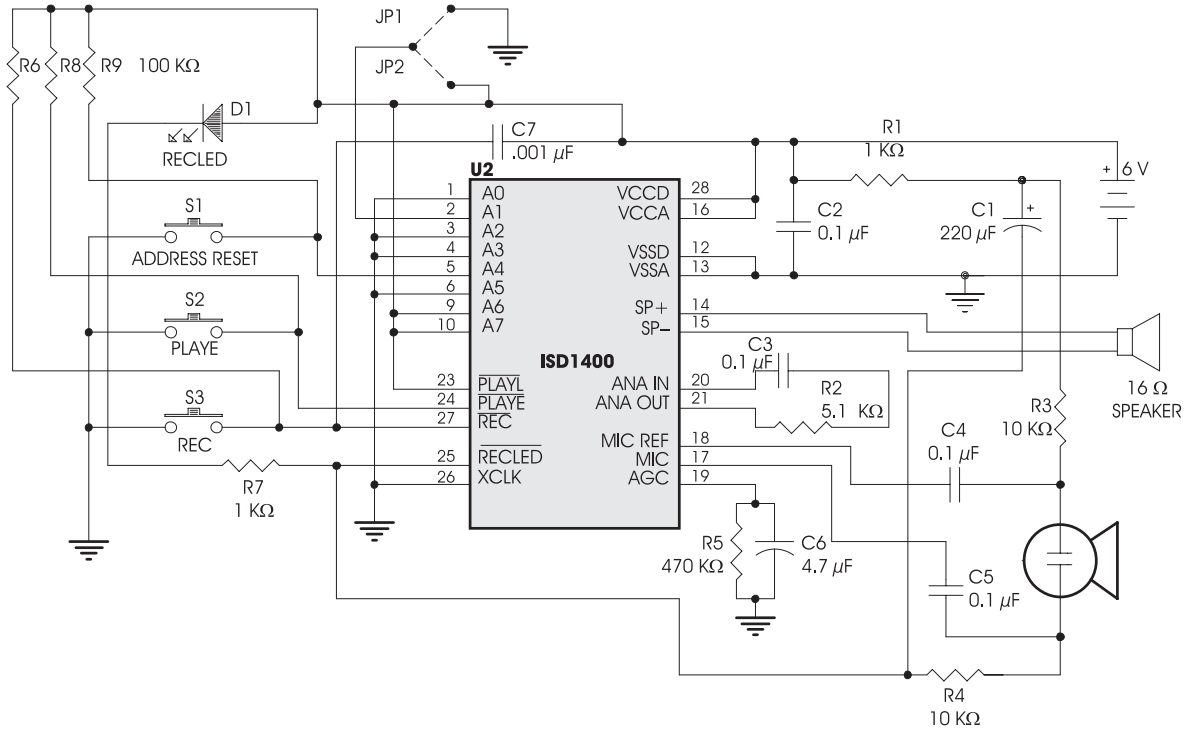
The ISD1100, ISD1200, and ISD1400 series include the A1 EOM Delete and A4 Consecutive Addressing Operational Modes found in the original ISD1000A device series. These modes allow the designer to produce a low cost product that can store multiple random length messages and play them back individually or all at once. When the Delete EOM Operational Mode is activated, playback starts at the beginning of memory and continues through all the messages just recorded without stopping. When Delete EOM is not activated, the messages are played back individually. The circuit diagram in Figure 6 and circuit explanation demonstrate these two applications.

CIRCUIT OPERATION – DELETE EOM ACTIVATED

The circuit is constructed as shown with JP2 installed. This straps A1 to a HIGH. Additionally, A6 and A7 are held HIGH to put the ISD1400 in Operational Mode. Also, R9 holds A4 HIGH unless the S1 push-button switch (Address Reset) is pressed.

Messages are recorded into the ISD1400 individually by pressing and holding the REC push- button for the length of the recording. The $\overline{\text{REC}}$ LED will illuminate during the recording. Additional messages may be recorded until the $\overline{\text{REC}}$ LED turns off. This indicates the device memory is full. The PLAYE push-button should not be pressed during this sequence. When the recording sequence is complete, a single momentary press of the PLAYE push-button will playback all the messages stored during the preceding Record sequence. A record sequence is ended by a playback operation, even if the memory is not full.

Figure 6: Multiple Message, EOM Delete, and Address Reset Application



NOTE: *Install JP2 for Delete EOM, install JP1 for normal operation.*

To start this playback sequence over, momentarily press the ADDRESS RESET push-button while the device is not playing back. This resets the internal address counter. The next press of PLAYE will start playback from the beginning of memory.

CIRCUIT OPERATION - DELETE EOM NOT ACTIVATED

The circuit is built exactly as the same with JP1 in and JP2 removed. The Delete EOM Operational mode is now disabled.

The recording sequence is performed as before. When the record sequence is complete, a single momentary press of the PLAYE push button will play the first message stored. A second press of the PLAYE push-button will play the second message stored. Messages will continue to playback in sequence, one message for each press of the PLAYE push-button.

As before, a momentary press of the ADDRESS RESET push-button will reset the ISD1400's internal address counter to enable the playback of the first message in the sequence.

USING THE SPEAKER OUTPUTS AS A PLAYBACK "RUN" INDICATOR IN THE ISD1100/1200/1400 SERIES DEVICES

Many applications require a signal to indicate when playback is occurring. An automatic announcement for a radio system, for instance, needs a signal to key the transmitter during the time the message is running. The ISD1100, ISD1200, and ISD1400 series of single-chip voice record/playback devices with their automatic power-down feature can provide this function using the speaker outputs.

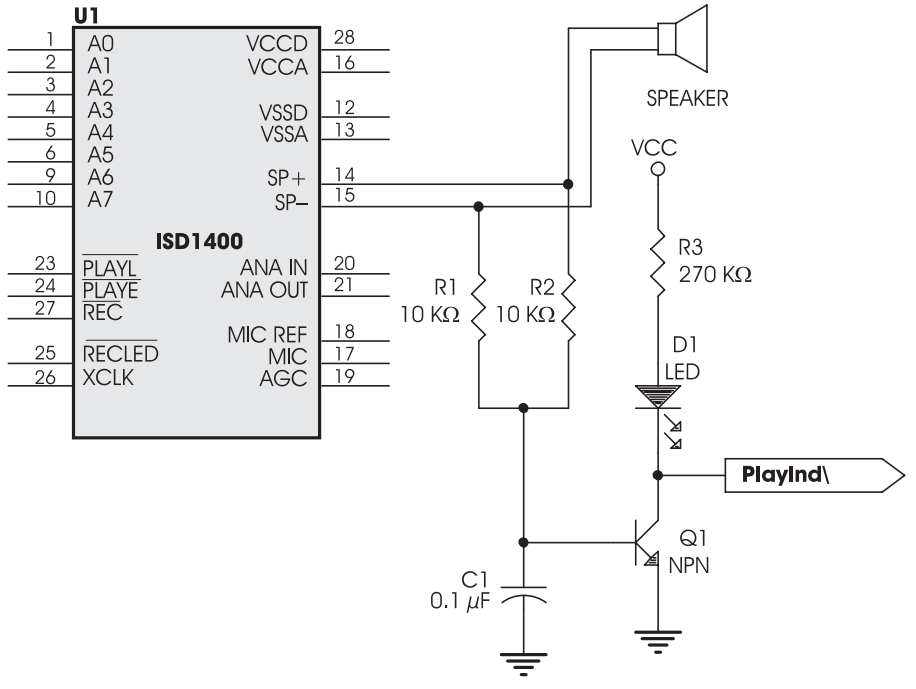
The speaker output pins of these ISD products power up to an average value of approximately 1.4 volts DC above the V_{SS} supply (which is usually at ground) during message playback. When the message stops at an End of Message location or the end of the analog memory space, the device automatically powers down, and the speaker output voltage falls to zero. This speaker bias voltage may be used to control an external circuit to provide a signal we may call PlayInd or PlayIndicator.

The circuit shown in Figure 7 exhibits one way this $\overline{\text{PlayInd}}$ signal may be derived. In this example R1 and R2 provide base current for Q1. Since the AC speaker voltage on SP+ is 180 degrees out of phase with the speaker voltage on SP–, the net result of the current flow into the base of Q1 will be as if a steady 1.4 volt signal were applied at each speaker pin. In Figure 7, each resistor will supply approximately 70 μA of base current or 140 μA total. If Q1 has a beta of 100 minimum, it can support at least 14 mA of collector current, enough to illuminate the LED as shown. Of course, a resistor may be substituted for the LED if a simple "1" and "0" switch is required. In this case, the signal at the collector of Q1 is the inversion of PlayInd or $\overline{\text{PlayInd}}$.

DETERMINING AN OVERFLOW CONDITION IN THE ISD1100, ISD1200, ISD1400 PRODUCT SERIES

The ISD1100, ISD1200, and ISD1400 product series do not have an overflow pin or other obvious indication of overflow status. In fact, it is not possible during playback to differentiate a normal EOM signal (present at the $\overline{\text{RECLED}}$ pin) from an EOM that results from the message stopping at the end of the device memory (overflow). It is possible in the A4 Operational Mode (A4, A6 and A7 HIGH), however, to determine if the device is at overflow by attempting a PLAY Edge operation and looking at the speaker pins.

Figure 7: Playback Run Indicator for ISD1100, ISD1200, and ISD1400 Series



NOTE: *Only speaker circuit shown to simplify diagram. Other components required for the circuit to record and playback.*

The previous heading described a method of deriving a $\overline{\text{PlayInd}}$ signal from an ISD1100, ISD1200, and ISD1400 series device. Using this circuit as an indicator, pulse the $\overline{\text{PLAYE}}$ pin and look at the $\overline{\text{PlayInd}}$ output. If the device is not in overflow, it will play the stored message and the $\overline{\text{PlayInd}}$ signal will be LOW for the duration of the message. If the device is in overflow, the $\overline{\text{PlayInd}}$ will pulse LOW for approximately 16 ms and go back HIGH.

It is also possible to determine an overflow condition from the $\overline{\text{PlayInd}}$ output when in Message Cueing Operational Mode (A0, A4, A6 and A7 HIGH, see the section "Operational Modes"). If the device "fast-forwards" through a message, the LOW-going $\overline{\text{PlayInd}}$ signal will be over 30 ms. If the device is in overflow, the $\overline{\text{PlayInd}}$ signal will be approximately 16 ms long.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Good Audio Design Practices

ISD products are very high-quality single-chip voice recording and playback systems. To get the full-quality voice capability of these devices, it is important to follow a few minimum guidelines when constructing your system. These suggested guidelines can help ensure satisfactory performance of your new recording system.

BASIC GUIDELINES

The guidelines are summarized as follows:

- Connect analog components (AGC resistors and capacitors, coupling capacitors, etc.) physically close to the ISD device. Use short component lead lengths.
- Use a quality microphone (see recommendations in "Microphone & Speaker Selection" under Application Information) and connect microphone ground to a low impedance analog ground return.
- Use either the differential electret circuit or the self biasing microphone, as demonstrated under the section on "Microphone and Speaker Selection."
- Provide high frequency decoupling capacitors at the analog and digital power pins, using low ESR (Effective Series Resistance) capacitors.
- Use a separate ground return to the power supply for the V_{CCD} (pin 28) decoupling capacitor.
- Use separate thick wire (#15 or better) or wide (>30 mils) power and ground routing lines.
- Use power supplies that do not introduce their own noise source (e.g., some switching supplies introduce noise into a recording.)

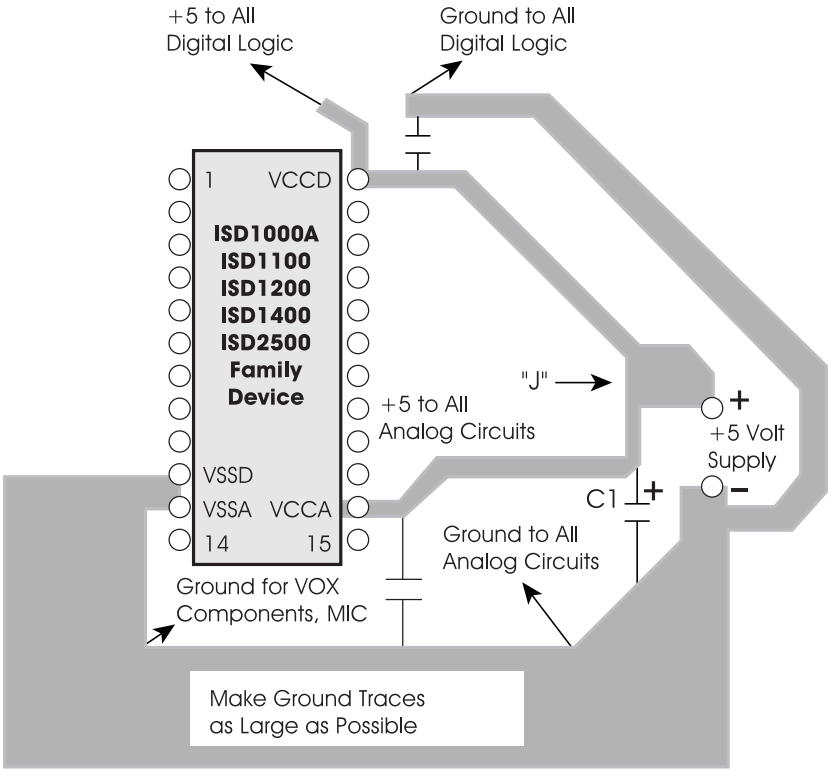
POWER SUPPLY AND GROUND DISTRIBUTION

There are two pin connections each for power and ground on the ISD devices. These separate connections are provided to minimize interference between the analog and digital portions of the circuits internal to the devices. It is highly recommended that this power separation be maintained in the manner shown on in the Figure 1 Power and Ground Connections diagram. Note in particular that V_{SSA} and V_{SSD} should be tied together right at pins 12 and 13.

CONNECTIONS TO THE ANALOG PATH

Components in the analog section of the ISD device should be physically located near the pins to which they are connected. Again referring to Figure 1, grounds and V_{CC} supplies for these components should be connected as indicated. In particular, capacitor C1 (low frequency voltage decoupling) should be as close to junction "J" as practicable. (Junction "J" separates V_{CCA} from V_{CCD}.) Components on the analog path should be tied as close as practicable to the device and be placed between C1 and the device. All digital control (addresses, control switches, etc.) should be tied to the appropriate V_{CC} or V_{SS} feed as shown at the top of the diagram.

Figure 1: ISD Device Power and Ground Connections



NOTE: *Address and control logic and audio connections not shown. Drawing is for power connections only.*

MICROPHONE AND SPEAKER

It is important to stress that the above guidelines are most effective if good quality microphones and speakers are used in the system. The user may want to experiment with a variety of microphones and speakers (and speaker enclosures) to get the optimum voice quality performance out of the system. The "Microphone and Speaker Selection" section contains several recommended microphones and speakers and "Using the Device" has a paragraph on audio amplification.

COMMENTS ON BATTERY OPERATION

The low operating power of the ISD series makes it ideal for use in portable battery operated environments. It should be noted, that as the battery approaches its end of life its output voltage will begin to drop. In addition, the effective series resistance of the battery at end of life increases substantially. As a result of these factors, the perceived voice quality of the ISD device will diminish. When this happens it is time to replace the battery. The device "tells" you when the battery is low.

STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Single-Chip Board Layout Diagrams

EXAMPLE PC BOARD LAYOUT

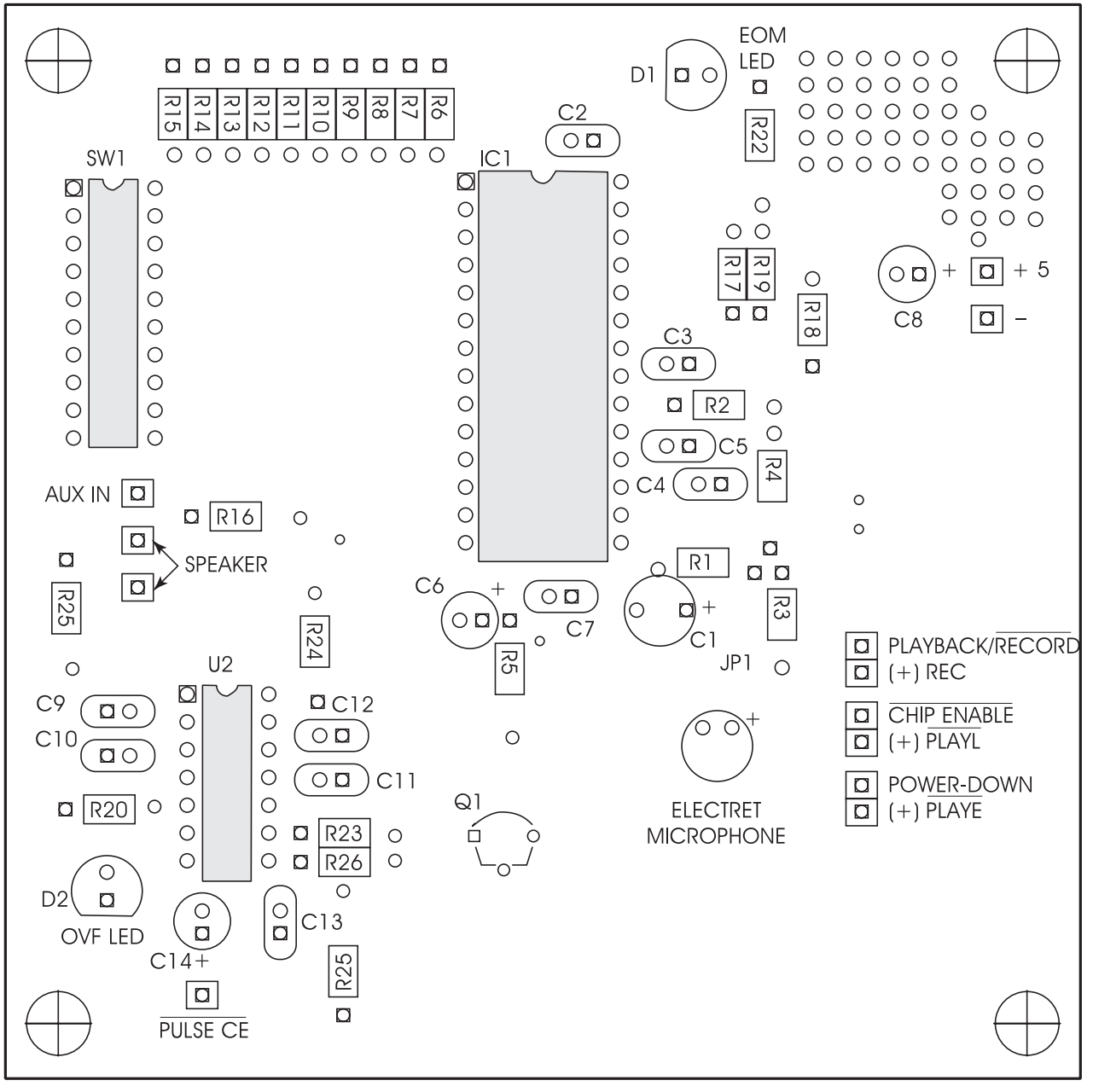
The printed circuit layout example in this chapter shows an implementation of the circuit shown in Figure 2 under the section "Circuit Examples for ISD1000A and ISD2500 Products." A dip switch (SW1) for addresses and pull-up resistors on the control inputs has been added. Additionally, two new address inputs and a pulse stretcher (U2A) for the overflow output (pin 22) have been added to the circuit so that this PC board will also work with the ISD2500 series. Also, one-shot pulse generator (U2B) adds the ability to generate short duration $\overline{CE}$ pulses for Message Cueing experimentation. The schematic of this board is shown in Figure 4, Single Chip Demo Board.

NOTE *The following PC board drawings are not to scale.*

The PC board layout incorporates the recommendations in "Good Audio Design Practices." Power feeds from the right-hand side of the board at the two points labeled "+" and "–". C8 is physically located at the branch of the V_{CC} traces that feed V_{CCD} on the top (going to pin 28) and V_{CCA} on the bottom (going to pin 16).

High-frequency ESR decoupling capacitors C2 and C7 are located adjacent to the supply pins they serve. C2, the decoupling cap for the V_{CCD} supply pin, has its own separate ground trace going directly back to the "–" input of the board. C7 picks up its ground from the major ground plane area on the "bottom" end of the board. The major power traces are greater than 30-mils wide and as direct as possible.

Figure 1: Single-Chip Demo Board Silk Screen



NOTE: *(*) = ISD2500 series devices only.*
(+) = ISD1100, ISD1200, and ISD1400 series devices only.

Figure 2: Single-Chip Demo Board Component Side PC Layout

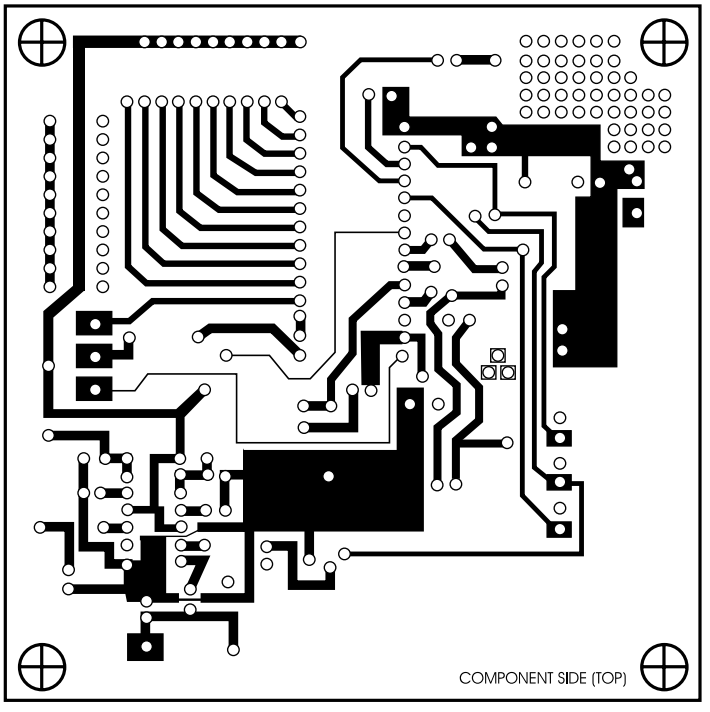


Figure not drawn to scale.

NOTE: *(*) = ISD2500 series devices only.*
(+) = ISD1100, ISD1200, and ISD1400 series devices only.
Figure not drawn to scale.

Figure 3: Single-Chip Demo Board Solder Side PC Layout

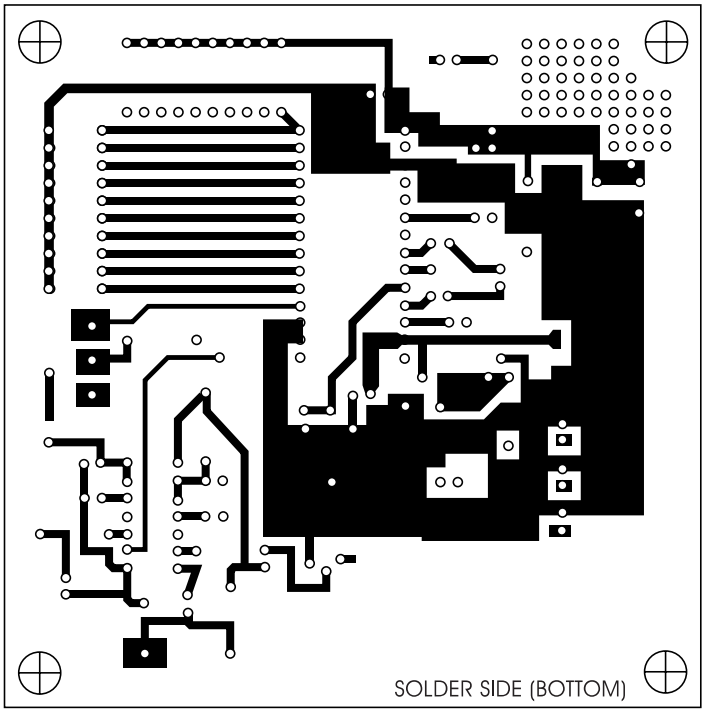
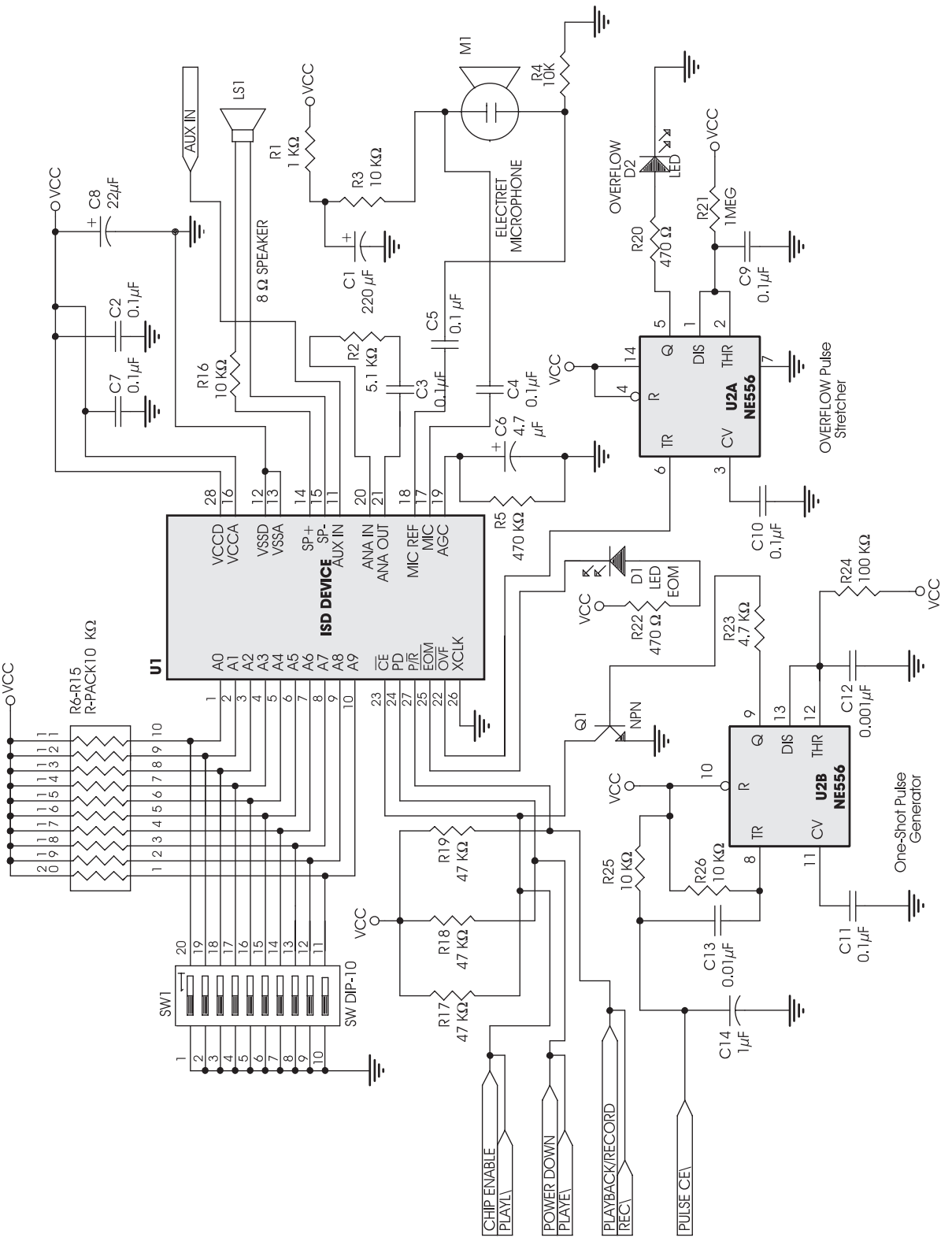


Figure not drawn to scale.

NOTE: *(*) = ISD2500 series devices only.*
(+) = ISD1100, ISD1200, and ISD1400 series devices only.
Figure not drawn to scale.

Figure 4: ISD2500 Single-Chip Demo Board Schematic



SERIAL INTERFACE PRODUCTS

Introduction and Circuit Examples

GENERAL DESCRIPTION

The ISD33000 ChipCorder series provides high-quality, 3-volt, single-chip record/playback solutions for 1- to 4-minute messaging applications which are ideal for cellular phones and other portable products. The CMOS devices include an on-chip oscillator, antialiasing filter, smoothing filter, AutoMute™ feature, audio amplifier, and high density, multilevel storage array. The ISD33000 series is designed to be used in a microprocessor- or microcontroller-based system. Address and control are accomplished through a Serial Peripheral Interface (SPI) or microwire serial interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Please refer to ISD33060/075/090/120-4 and ISD33120/150/180/240 data sheets for detailed description of the ISD33000 products.

Figure 1: ISD33000 Series Block Diagram

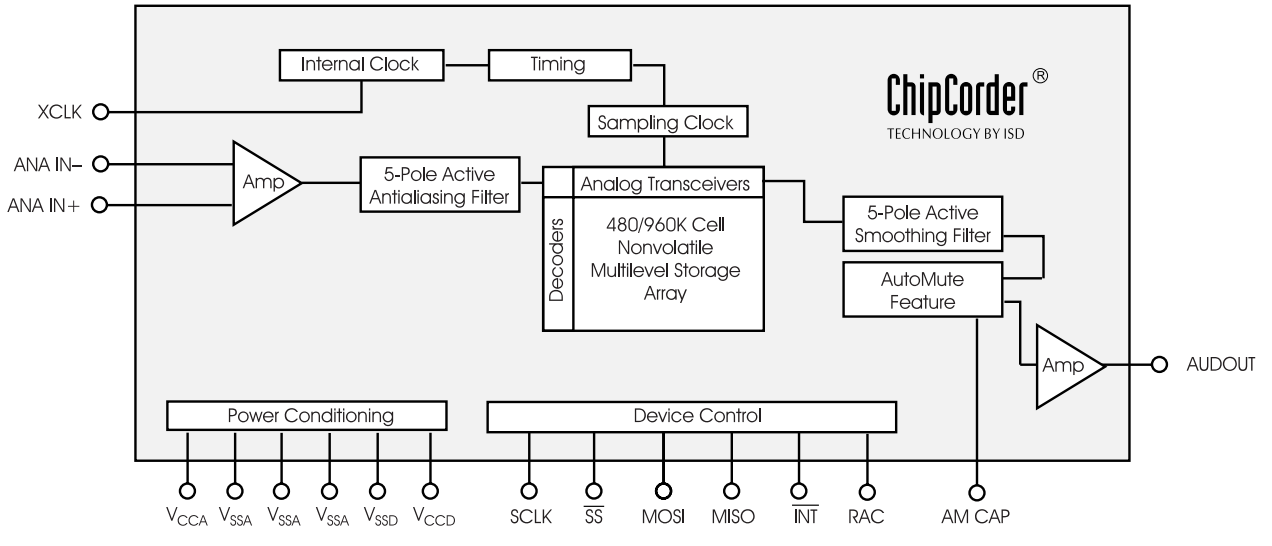


Table 1: ISD33000 Series Summary

Part Number	Duration	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD33060	60 sec	8.0	3.4
ISD33075	75 sec	6.4	2.7
ISD33090	90 sec	5.3	2.3
ISD33120-4	2.0 min	4.0	1.7
ISD33120	2.0 min	8.0	3.4
ISD331250	2.5 min	6.4	2.7
ISD33180	3.0 min	5.3	2.3
ISD33240	4.0 min	4.0	1.7

SERIAL INTERFACE PRODUCTS

Example Circuit: Minimum I/O Application for ISD33000 Products

Voltage Required: 3 volts

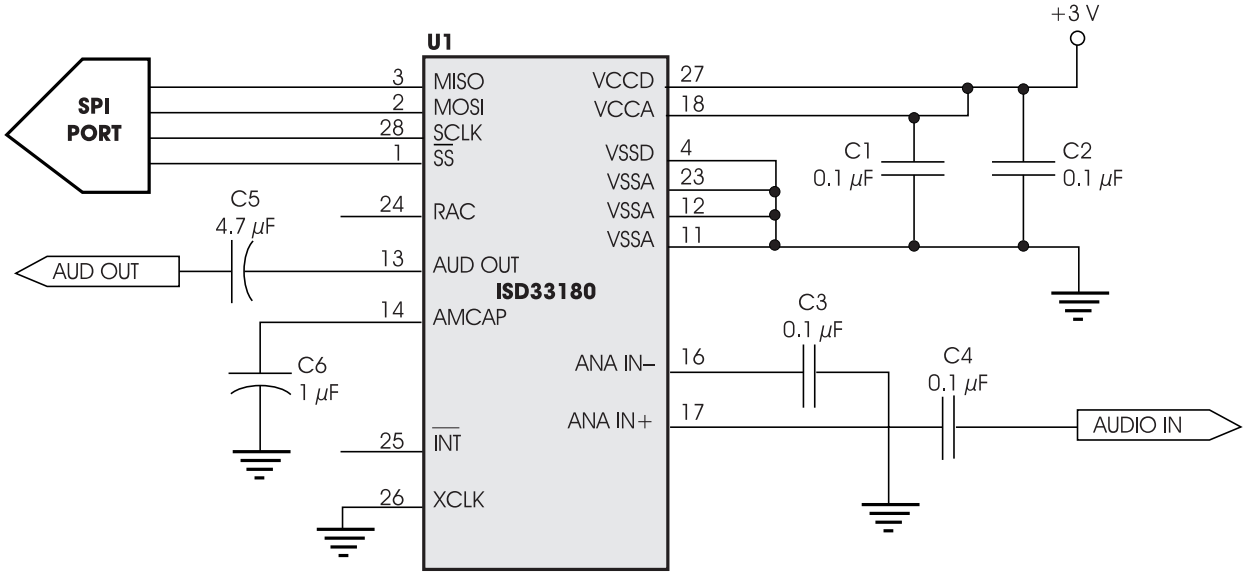
Number of I/O Pins: 4

Total Storage Time: 180 seconds (3 minutes)

Features: Multiple message Record and Play with message management.

NOTE *All messages are directly addressed. The internal address pointer may be read while playback is underway or during static or power-down conditions. The capability to change addresses "on the fly" enables full message management. Use of the RAC and/or $\overline{INT}$ pins may simplify some operations.*

Figure 1: Circuit Example



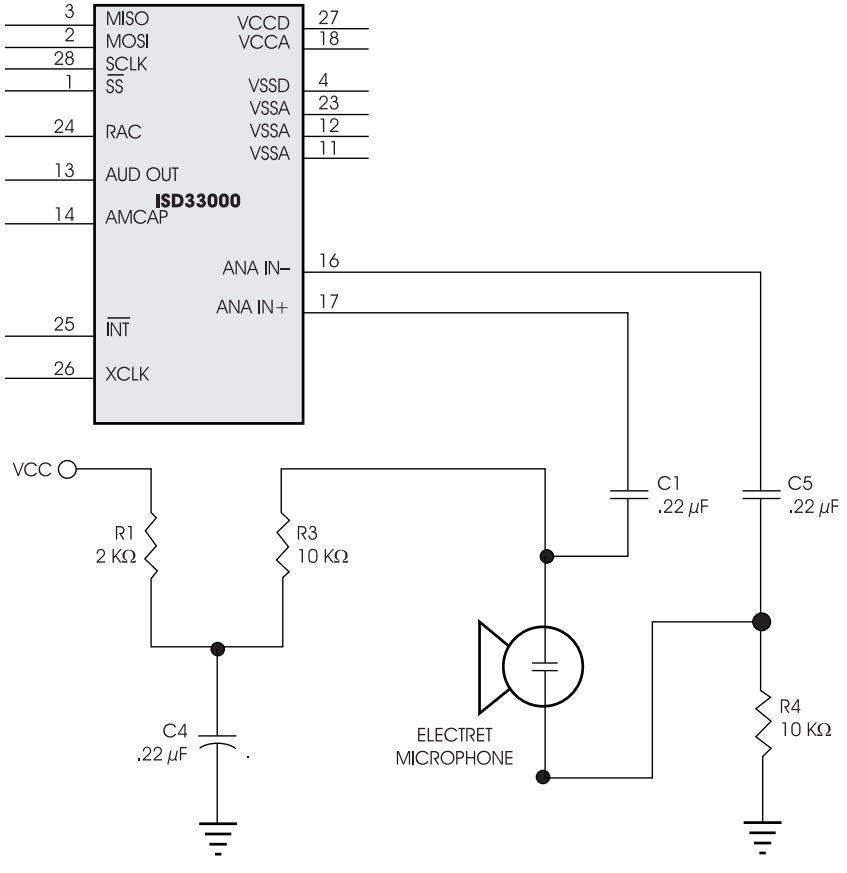
SERIAL INTERFACE PRODUCTS

Example Circuit: Microphone Circuit

This microphone circuit can be used for ISD33000 applications where there is no need for AGC. Applications such as memo recorders or toys are some examples. In many applications the performance of this circuit will be found adequate.

Please refer to "AGC Circuit for the ISD33000" for an AGC example.

Figure 1: Circuit Example



NOTE: *Only microphone connections are shown.*

Table 1: Passive Component Functions

Part	Function	Comments
R1, C4	Microphone power supply decoupling	Reduces power supply noise.
R3, R4	Microphone biasing resistors	Provide biasing for Microphone Operation.
C1, C5	Microphone DC-blocking capacitor low frequency cutoff	Decouples Microphone bias from the chip. Provides single-pole frequency cutoff and common mode noise rejection.

SERIAL INTERFACE PRODUCTS

Example Circuit: Single Transistor 3-Volt Speaker Driver

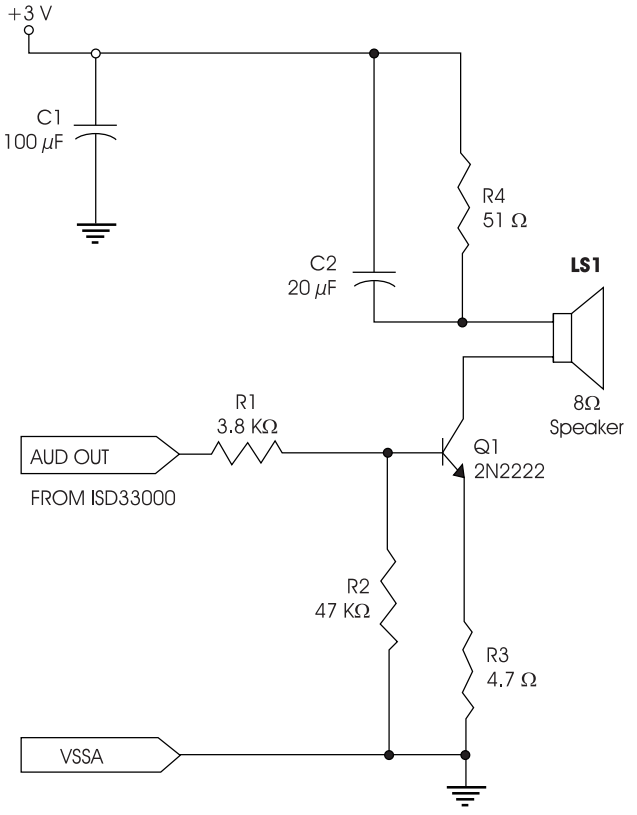
The ISD33000 series was designed for products which already have a speaker driver. This application brief shows a circuit diagram that will be acceptable for applications that may not already have a loud speaker driver. Applications such as memo recorders or toys are some examples.

The circuit in Figure 1 has a gain of almost 2:1. The single transistor 2N2222 along with some capacitors and resistors make a very cost effective 3 volt speaker driver.

The AUD OUT pin of the ISD33000 is designed to drive up to a 5 KΩ load. The AUDOUT pin is tri-state during record and it goes to 1.2 volts during playback. The R2 resistor turns off the Q1 transistor during record or standby, thus there is no power dissipation during record.

The R3 and R1 resistors can be varied to control the audio level for a specific speaker. The R1 resistor sets the biasing for the Q1 transistor. The speaker impedance and the R3 resistor set the gain. It is important that the R3 resistor does not go to zero ohms. That condition may damage the transistor

Figure 1: .Circuit Example



SERIAL INTERFACE PRODUCTS

Using the ISD33000 Device with 5-Volt Powered Processors

Today with the increased requirements for low voltage battery operation, many devices are offered that operate in the 3-volt range. The problem is the additional consideration that must be observed while using both 3-volt and 5-volt logic together. This brief assumes that the application requires a minimum of additional logic to interface the ISD33000 series powered at 3 volts to any microprocessor/controller powered at 5 volts.

The ISD33000 ChipCorder series provides high quality, 3-volt single chip record/playback solution for 1- to 4-minute message applications. Since the ISD33000 was designed to be used in conjunction with a microprocessor/controller, all addressing and control function are accomplished through a Serial Peripheral Interface (SPI) or microwire serial interface.

The I/O pads of the ISD33000 were designed without the need for the P channel device for ESD protection. Thus no level translation is required when connecting a 5-volt device to the inputs of the ISD33000. You may directly connect to any input on the ISD33000 from a 5-volt device.

All the outputs (except for MISO) are open drain, so if you would be connecting them to a device powered at 5 volt, simply pull up the output on the ISD33000 to the +5 volt supply of the microprocessor/controller.

The MISO output is the only exception on the ISD33000, and does include a P channel drive. At a +3 volt V_{CC} for the ISD33000, the specification will guarantee a minimum V_{OH} (output high voltage minimum) of $V_{CC} - 0.4$ or +2.6 volts. Most +5 volt devices require a VIH (input high voltage minimum) in the range of +4 volts. To meet the V_{IH} specification of the +5 volt device we must add a level translation.

If the application can tolerate this pin being inverted then Figure 1 can be used for the level translation, otherwise Figure 2 will perform the level translation but will not invert the MISO signal.

One word of caution, presently ISD Engineering has approved this solution. Applications has tested it, However, the absolute maximum rating for voltage applied to any pin presently indicates $V_{CC} + 0.3$, and this brief is violating that specification. The procedure to relax that specification is presently in process with ISD Product Engineering and QC departments. Until the complete sign off by these departments, and the authorized relaxation of this specification, the use of the interface described within this brief will remain the responsibility of the end-applications design engineer.

Figure 1: Inverted MISO

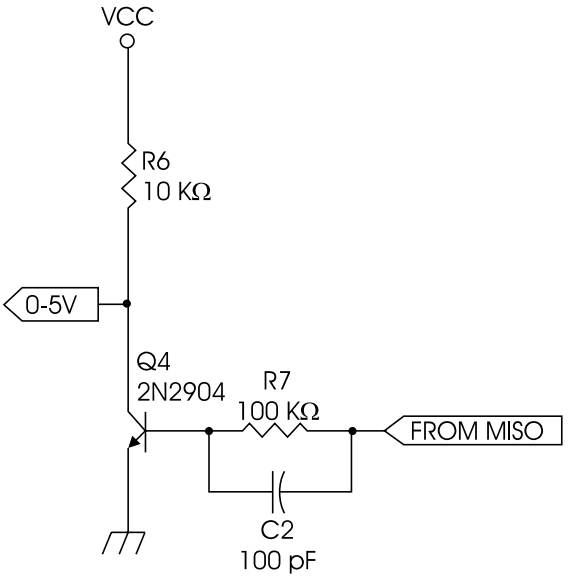
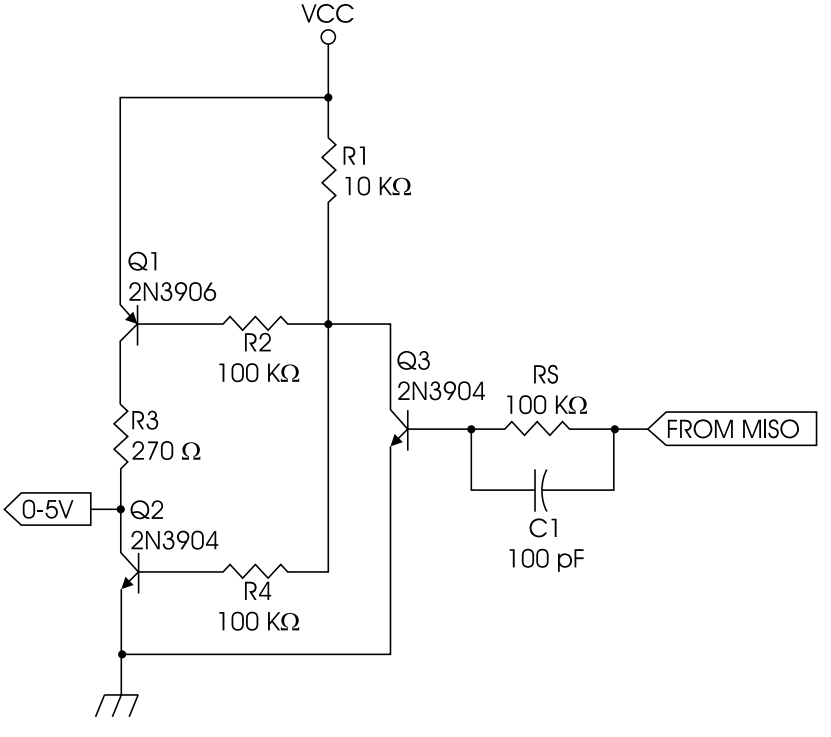
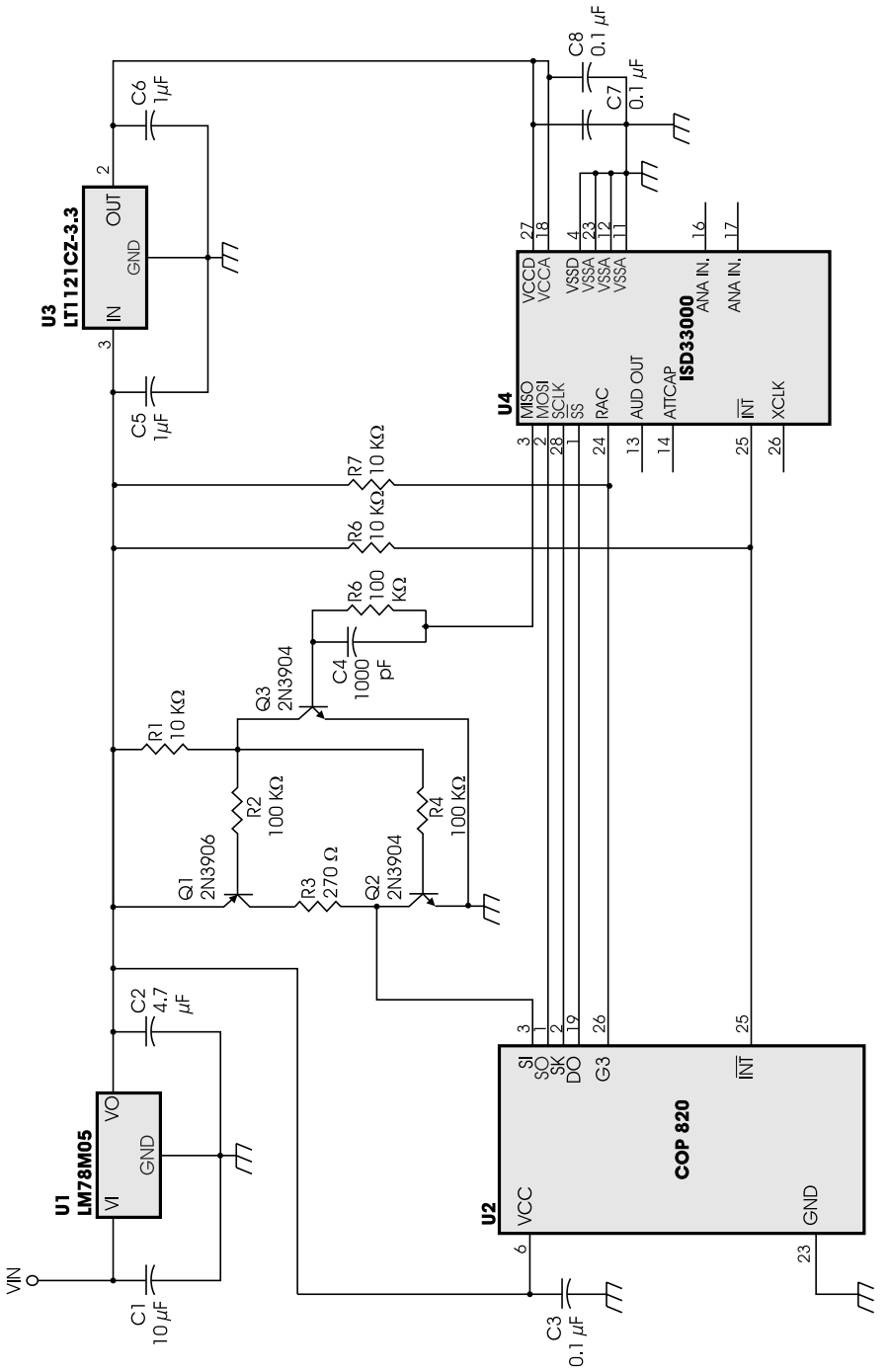


Figure 2: Non-Inverted MISO



The pseudo schematic outlined below demonstrates a typical interface between the ISD33000 powered at 3 volts and the microcontroller powered at 5 volts.

Figure 3: Typical Interface



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TECHNOLOGY BY ISD

SERIAL INTERFACE PRODUCTS

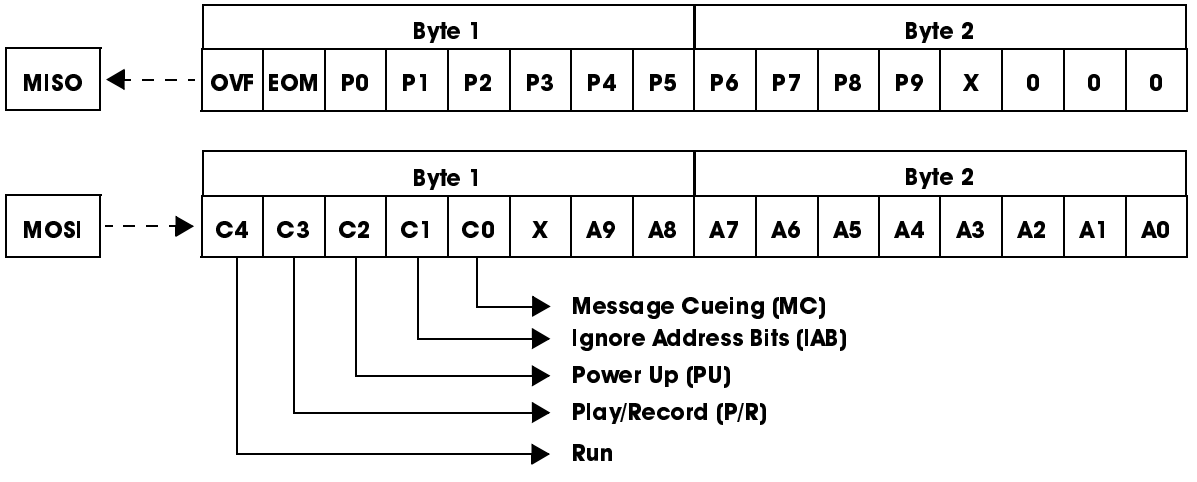
Operations, Tricks and Techniques in the ISD33000 Series

A simple but powerful command structure is built into the ISD33000 SPI control port. It's inherent flexibility allows the software programmer to direct the operation of the ISD33000 device with the minimum number of control cycles while allowing full use of the device's numerous modes. The following offers tips on the use of this port and suggest methods of simplifying various operations.

The MOSI (Master Out, Slave In) of the SPI port on the device is an input pin. The MISO (Master In, Slave Out) is an output pin. The ISD33000 operates as a "slave" device to the microcontroller running the system. The SPI port also includes a serial clock input called SCLK and a select input called $\overline{SS}$ (Slave Select). The $\overline{SS}$ is an active LOW signal.

The SPI command registers in the ISD33000 have the following composition:

Figure 1: SPI Command in the ISD33000 Series



All input command cycles in the ISD33000 series start with $\overline{SS}$ pin going LOW and end with $\overline{SS}$ pin returning HIGH. The bit position of the input data at the time the $\overline{SS}$ pin goes HIGH determines how the device reacts to the command. Any number of bits may be clocked into the SPI port on an input cycle. The last five bits input to the MOSI pin at the time the $\overline{SS}$ pin is HIGH determine the command sent in, even if several bytes were clocked into the port while the $\overline{SS}$ pin was LOW. Only the last 16 bits shifted into the SPI port are retained in the SPI port hardware.

The SCLK signal clocks the data into the ISD33000. The input data to the MOSI pin must be valid on the rising edge of the SCLK. The output data from the MISO pin changes following the falling edge of the SCLK pin. Consult the data sheet on the ISD33000 for the exact timing. The examples stated below assume the initial state of the SCLK pin is LOW when the $\overline{SS}$ pin goes LOW to start the command cycle but this is not required.

EXAMPLE ONE

Power Up the Device

The following is an example of a simple command to the ISD33000 SPI port. In this operation, the device powers up so that a record or playback cycle can start later. See Figure 1, which displays the bit positions of the five bits which compose the heart of the controls, (e.g. C0–C4). Use this diagram as a reference when reading the following:

1. The device powers up by setting the PU bit. That is, set bit C2 HIGH and bits C0, C1, C3 and C4 to LOW at the end of the command cycle. The five control bits in the SPI control register should then be set as <00100> as indicated in Figure 1.
2. In this example, an entire byte is shifted in since some hardware SPI ports can only operate on whole bytes. It is necessary, therefore, to shift in HEX address 20, <0010 0000> just to set the C2 bit. Note that the state of the A9, A8 and "X" bits during this operation do not matter. This is explained in more detail later.
3. The command cycle begins by setting $\overline{SS}$ to LOW, and then the MOSI pin LOW as well. The input byte, <0010 0000>, is clocked in, right to left. The first five bits clocked in, therefore, are all LOW. A single HIGH bit is then clocked in followed by two more LOW bits. The command ends with the $\overline{SS}$ pin returning to HIGH and then the ISD33000 will begin a power-up cycle. In T_{PUD}[1] time, the device will be powered up.

Table 1, Command Formats, displays the power-up bit data which is shifted from the command byte in the microcontroller into the MOSI pin of the ISD33000 and then into byte 2 of the input side of the SPI input port register. Note that the PU bit is shifted to the right out of the microcontroller and into the ISD33000 SPI port.

1. *T_{PUD} is the power-up delay time of the device. See the ISD33000 data sheet.*

Table 1: Command Formats

Shift #	Command Byte in Microcontroller	SPI Port in ISD33000 after "N" Shifts	Shift #	Command Byte in Microcontroller	SPI Port in ISD33000 after "N" Shifts
Initial condx.	<0010 0000>	<0000 0000>			
1	<0001 0000>	<0000 0000>	5	<0000 0001>	<0000 0000>
2	<0000 1000>	<0000 0000>	6	<0000 0000>	<1000 0000>
3	<0000 0100>	<0000 0000>	7	<0000 0000>	<0100 0000>
4	<0000 0010>	<0000 0000>	8	<0000 0000>	<0010 0000>

In this first example, the value of the address bits A0 through A9 were ignored. In fact, since the run bit, C4, was input as a LOW, only the HIGH PU bit effected the ISD33000. The state of C0, C1 and C3 also was irrelevant. ISD recommends that anytime data is shifted into a SPI port command register bit position that "does not matter" it should be set LOW for compatibility with possible future features that may be added to the device.

EXAMPLE TWO

Record at an Address

This second example assumes the ISD33000 is already powered up and that recording is to begin at a specific address. For this example, use address 92, or HEX address 5C, <00 0101 1100>. Each control bit in the input side of the command register of the device is set up as follows:

- C0—The MC bit must be LOW since a message cueing cycle is not desired.
- C1—The IAB bit must be LOW since the address is not being ignored.
- C2—The PU bit must remain HIGH since the device is already powered up and must remain powered up after this command cycle.
- C3—The P/R bit must be LOW since a record cycle is to be started.
- C4—The RUN bit must be HIGH since an active cycle is to be started.
- A0–A9—The address bits must be all be defined since the IAB bit is LOW.

1. The transfer of the two bytes of data is begun by changing the $\overline{SS}$ pin to a LOW. The bytes to be sent are: HEX address A0 5C, < 1010 0000> <0101 1100>.
2. Again, clock the bits in, right to left.[1] Therefore, the first bit clocked into the SPI port will be the A0 address bit which is set LOW, followed by A1 which is LOW, followed by A2 which is HIGH, and so forth.
3. The last of the 16 bits clocked into the SPI port will be the RUN bit which, of course, is HIGH.
4. The command cycle ends with the $\overline{SS}$ pin going HIGH. At this time, the record cycle starts at the address as specified by A0–A9.
5. Send an additional command so that the command cycle will proceed through the chip's memory as desired. The IAB bit in the command register must be set to enable the address sequencer internal to the ISD33000. Otherwise the device will do a looping record at the address specified by A0–A9. This second command cycle must be given before the chip reaches the end of the row where recording begins, thus allowing at least 150 ms to send the command.
6. The command byte to be input must be one that does not interrupt the record operation in progress but sets the IAB bit. Additional address information is not needed. If it is assumed that the SPI port of the microcontroller can input any number of bits in a control cycle, this operation only requires that five bits be input to the SPI port. The proper control bits to send are the same as originally sent in the first control operation with the exception that the IAB bit is now set. It is therefore necessary to only send <1011 0> to the SPI port.
7. Once again an SPI cycle is begun by taking $\overline{SS}$ LOW. The first bit shifted into the ISD33000 SPI port is C0, which is pulled LOW. The fifth and last bit shifted into the SPI port is C4, the RUN bit, which is set HIGH. The control sequence ends with the $\overline{SS}$ pin going HIGH and results in the recording proceeding through the memory in the ISD33000 row by row until manually halted.

---

1. *Note that some microcontrollers with hardware SPI ports can only proceed as left to right shifts. Consult the microprocessor data sheet for details. If this is the case, then invert the bit placement of the data shifted in. In this example, the A0 would become 05 and the 5C would become 3A. When inverting the bit placement, do not forget that two of the address bits fall in the "control byte" of the data sent into the device.*

NOTE *After each command cycle, the data shifted into the ISD33000 remains in the chip's SPI port hardware. As subsequent operations shift more data in, bits shifted to the right out of the 16-bit register space are lost. A record or play operation started with only a 5- or 8-bit input command, and with the IAB bit not set (i.e. set LOW) will cause the A0–A9 data at the end of the operation to be treated as an address pointer. This will, of course, be data input to the SPI port in the previous command cycle mostly from the C0–C4 bit positions and is probably not valid address data.*

EXAMPLE THREE

Playback at an Address

This example assumes the ISD33000 is already powered up and that playback will begin at a specific address. Here, use address 92, or HEX address 5C, <00 0101 1100>. Each control bit in the input side of the command register of the device is set up as follows:

- C0—The MC bit must be LOW since a message cueing cycle is not desired.
- C1—The IAB bit must be LOW since the address is not being ignored.
- C2—The PU bit must remain HIGH since the device is already powered up and must remain powered up after this command cycle.
- C3—The P/R bit must be HIGH since a playback cycle is to be started.
- C4—The RUN bit must be HIGH since an active cycle is to be started.
- A0–A9—The address bits must be all be defined since the IAB bit is LOW.

1. The transfer of the two bytes of data is begun by changing the $\overline{SS}$ pin to a LOW. The bytes to be sent are: HEX address E0 5C, < 1110 0000> <0101 1100>.
2. The first bit clocked into the SPI port will be the A0 address bit which is pulled LOW, followed by A1, also LOW, followed by A2 which is set HIGH.
3. The last of the 16 bits clocked into the SPI port will be the RUN bit which, of course, is HIGH
4. The command cycle ends with the $\overline{SS}$ pin returns to HIGH. At this time, the playback cycle starts at the address as specified by A0–A9.
5. Send an additional command so that the command cycle will proceed through the chip's memory as desired. The IAB bit in the command register must be set to enable the address sequencer internal to the ISD33000. Otherwise the device will do a looping record at the address specified by A0–A9. This second command cycle must be given before the chip reaches the end of the row where recording begins, thus allowing at least 150 ms to send the command.
6. The command byte input must be one which does not interrupt the playback operation in progress but sets the IAB bit. Additional address information is not needed. If it is assumed that the SPI port of the microcontroller can input any number of bits in a control cycle, this operation only requires that five bits be input to the SPI port. The proper control bits to send are the same as originally sent in the first control operation with the exception that the IAB bit is now set. It is therefore necessary to only send <1111 0> to the SPI port.
7. Once again an SPI cycle is begun by taking $\overline{SS}$ LOW. The first bit shifted into the ISD33000 SPI port is C0, set LOW. The fifth and last bit shifted into the SPI port is C4, the RUN bit, which is HIGH. The control sequence ends with the $\overline{SS}$ pin returning to HIGH and results in playback proceeding through the memory in the ISD33000 row by row until the ISD33000 is told to stop playback or a set EOM bit is encountered.

EXAMPLE FOUR

Stop Record or Playback and Power-Down the Device

This example assumes that a record or playback cycle is underway and that the operation is to be terminated. The device will also be powered down by this control cycle. The same command may be used to power-down in both the record and the playback cycles. In this example a full byte transfer is assumed.

1. A record or playback operation is terminated by clocking a command cycle into the SPI port with the RUN bit LOW. The PU bit must also be LOW, so that the device powers-down. The IAB bit must be HIGH at end of a record cycle to make sure the EOM is set in the correct place. The rest of the bits in the command byte do not matter, however, according to convention they are left LOW. The command byte needed to power-down a playback is, therefore HEX address 10<0001000) and the command byte to end power-down in a playback cycle is HEX address 00<00000000>.
2. Once again, the transfer of the command byte of data begins by changing the $\overline{SS}$ pin to LOW followed by the byte as described above.
3. Record or playback will end in approximately 50 ms (again, the data sheet will have exact information) followed by device power-down.

EXAMPLE FIVE

Address Jump During Record or Playback

One of the ISD33000's key features is its ability to seamlessly jump from one address to another during the course of a record or playback cycle. This function enables the message management operations described in "Message Management in the ISD33000." The following describes how this feature works:

The ISD33000 memory array may be thought of as an address map of x rows by y columns. The device is currently sold in two array sizes. Both versions have 1200 columns. The smaller device has 400 rows and the larger has 800 rows. Only the rows may be addressed. So, to begin an operation on a row at address "n", the device begins in column "0" and proceeds through the row to column 1199 (if not stopped by a command cycle along the way).

The internal address sequencer in the ISD33000 may be thought of as operating in one of two possible modes. As a record or playback operation proceeds through the device, at the end of each row, a decision must be made as to where to go next. If the IAB bit is set to "1" when the end of the row is reached, then the address sequencer increments by one count and record or playback proceeds to the next row in sequence. If the IAB bit is cleared to "0" when the end of the row is reached, then the address sequencer pulls the address from the SPI command register and record or playback proceeds at the row defined by this address. This transition from the end of one row to the beginning of some other row not in sequence is seamless. No samples are lost as one records or playbacks across boundaries.

Programmer Caution

An address jump from the last row in memory. Record or playback to the end of the last row in the memory[1] results in a device overflow (OVF) interrupt. The software which controls the ISD33000 must trap for this address and insure that this row is not used in a message management algorithm where an address jump might be necessary.

---

1. *Consult the data sheet for the device being used to determine the number of rows in the memory array.*

INTERRUPT SERVICE

The interrupt service structure of the ISD33000 may be read with only eight SPI clock cycles. The following example demonstrates how this is possible:

EXAMPLE SIX

Read Interrupt Status and Clear the Device Interrupt Condition

The ISD33000 device has only two interrupting conditions: (1) End Of Message (EOM) which signifies that a set EOM bit has been found during a playback cycle and (2) Overflow (OVF) which indicates that the end of device memory has been encountered during either a record or a playback cycle. Note that an overflow interrupt can only occur at the end of the last row in the device's memory.

Both of these conditions result from the end of device operation, (i.e., playback or record has ceased). Both conditions cause the $\overline{INT}$ pin[1] of the device to be pulled LOW. This pin will remain LOW until the next SPI cycle in the ISD33000 device.

As the interrupt condition is read and clocked out of the MISO pin, data is simultaneously being clocked into the MOSI pin. This input data will be interpreted as a control input and the device will react accordingly. It is necessary, therefore, to make sure this input data leaves the ISD33000 in a desired state. Since the interrupt always results from the end of an operation, shifting in a power-up command, as illustrated in Example One, is usually a safe response. In the example following, assume shifting in HEX address 20, <0010 0000> while the interrupt data is shifted out.

The following description explains how interrupt status may be read from the ISD33000:

1. The interrupt status read cycle begins with the $\overline{SS}$ pin of the device being changed to a LOW. At that time, the state of the OVF bit will be presented to the MISO output. This level is static. That is, it will remain low as long as the $\overline{SS}$ pin stays LOW and the SCLK pin is not clocked.
2. The first clock cycle of the input to the SCLK pin will now cause the state of the EOM bit to be presented to the MISO output.
3. Seven more clocks must be presented to the SCLK pin to insure the interrupt condition is properly cleared.
4. The interrupt status read is terminated by changing the $\overline{SS}$ pin back to a HIGH. When the $\overline{SS}$ pin goes HIGH, the INT pin output will be allowed to go back HIGH, pulled up by the external pull-up resistor.

The above examples demonstrate the ease of use of the ISD33000 family device. A record or playback cycle may be started and controlled with a minimum number of SPI clock cycles. Some short cuts exist that enable the device to be controlled with less than a full 8 bit transfer to the SPI control port. This translates into a voice record and playback system that requires very little overhead from the controller in the system.

1. *$\overline{INT}$ is an active LOW open drain output. If this output is to be used, a pull-up resistor must be installed to pull the pin up to the proper HIGH level.*

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SERIAL INTERFACE PRODUCTS

Using the ISD33000 Device with a Microcontroller

This application note describes how to use ISD33000 with a microcontroller. The purpose of this application note is to illustrate the ease of use of the ISD33000 series with any SPI compatible microcontroller.

Unlike other families of single-chip record and playback from ISD, the ISD33000 is a microcontroller slave peripheral device. It is controlled with a microcontroller either with an SPI compatible hardware already on the microcontroller or with I/O ports that emulate SPI protocol. For the ease of use and illustration a microcontroller with an SPI compatible serial interface is used in this application note.

SERIAL PERIPHERAL INTERFACE (SPI)

ISD33000 operates from an SPI serial interface. The SPI protocol is a synchronous serial data transfer protocol. The SPI interface has 4 control I/O pins.

1. Slave Select ($\overline{SS}$): This pin when low will select the ISD33000.
2. Master Out Slave In (MOSI): This is the serial input to the ISD33000.
3. Master In Slave Out (MISO): This is the serial input to the ISD33000.
4. Serial Clock (SCLK): This is the clock input to the ISD33000. The master microcontroller provides this clock.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on falling edge of the SCLK. On the ISD33000, data is clocked in on the MOSI input on the positive clock edge and data is clocked out on the MISO output on the negative clock edge.

All serial data transfers begin with the falling edge of $\overline{SS}$ pin. Slave Select is held low during all serial interface and it is held high between instructions. Each operation that ends in an EOM (End of Message) or an OVF (Overflow) from the ISD33000 will generate an Interrupt. The interrupt will be cleared the next time an SPI cycle is initiated. As the interrupt data is shifted out of the ISD33000 MISO pin, control and address data are simultaneously shifted into the ISD33000 MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. An operation begins with the RUN bit set and ends with the RUN bit reset. All operations begin with the rising edge of the $\overline{SS}$.

SPI CONTROL REGISTER

The SPI control register provides control of individual device functions such as play, record, stop/pause, message cueing (fast forward), power-up, power-down, start and stop operations and ignore address pointers.

There are five control bits associated with the ISD33000 that control the device. These bits are:

C0 = MC

When this bit is set to 1 during playback it starts a message cueing cycle (Fast forward to the next EOM). C0 operation is not defined during Record.

C1 = IAB

When this bit is set to 1, any address data shifted into the SPI MOSI shift register is ignored. A resulting Record, Playback or Message Cueing operation

will begin at the next address in the device memory at the end of the proceeding operation.

When IAB (Ignore Address Bit) is set LOW, a playback or record operation starts from address (A9–A0) and ends at the end of that row. If no other control data is input to the SPI port, the device will continue that operation over again at the same address and therefore "loop" on that row. To continue playback or record consecutively through the memory, a second SPI cycle should immediately be input with the IAB bit changed HIGH before the device reaches the end of a row. To stop an operation it is important to note that if the IAB bit is LOW, the data shifted into address bit locations will be transferred to the device's internal address register and the device's internal address prior to the stop instruction will be lost.

It is recommended to set IAB = HIGH when a stop/pause command is issued if address read back is desired.

C2 = PU

When this bit is set HIGH, the device powers-up and is ready for an operation after T_{PUD} (approximately 25 ms). Wait T_{PUD} before issuing an operational command. It is important to wait T_{PUD} after the power-up command is issued before sending another command; the device will not function properly if a record or playback command with power-up command is issued in the same SPI cycle. For example to record from address 00 the following program cycle should be used.

1. Send power-up command (00100<X-X)
2. Wait T_{PUD} (per device specification, approximately 25 ms)
3. Start recording (10100<A9–A0>)
4. Continue consecutive recording (10110 <X-X>)
5. C3 = P/R. When this bit is set HIGH, the device goes to playback mode and when it is LOW the device goes to record mode.
6. C4 = RUN. When this bit is pulled HIGH, the device begins an operation and when LOW, stops an operation.

SPI OPCODE FORMAT

The ISD33000 accepts either an 8-bit command or 16-bit command from a microcontroller through the SPI port. The opcode format is 5 control bits and 11 address bits for a 16-bit command. The opcode format is 5 control bits and 3 address bits for an 8 bit command with the 3 address bits being "don't care" bits.

EXAMPLES OF RECORD/PLAYBACK OPERATION

RECORD AT AN ADDRESS

Power Up the Device

Send 00100<xxxx> to the SPI

Wait T_{PUD}

Send 00100<xxxx> to the SPI

Wait 2 x T_{PUD}

Start Recording at <10 bit address >

Send 10100<x><10bit address> (note; IAB = 0)
Send 10110<xxxx> (note; IAB = 1)

Recording will continue until memory is full or a new SPI cycle with RUN = 0 is input or until the end of memory is reached (Overflow Interrupt).

Stop Record and Power down

Send 00000<xxxx> to the SPI

OR

Stop/Pause Record and Do Not Power-Down

Send 0 0110 <xxxx>

RECORD A MESSAGE AT THE NEXT AVAILABLE ADDRESS

If the Device is Not Powered Up

Send 00100<xxxx> to the SPI

Wait T_{PUD}

Send 00100<xxxx> to the SPI

Wait 2 x T_{PUD}

Record the Next Message

Send 10110<xxx>

Recording continues until ready to stop (or device runs out of memory space)

PLAYBACK AT AN ADDRESS

Power Up the Device

Send 01100<xxx> to the device.

Wait T_{PUD}.

Start Playback at <10 bit Address>

Send 11100<x><10 bit address>.

Send 11110<xxx> to continue playback.

Playback continues until memory overflows or ready to end (reaches EOM).

Stop playback and power down.

Send 01010<xxx>.

OR

Stop Playback don't power down.

Send 01110 <xxx>.

PLAYBACK AT THE NEXT MESSAGE

If the device is Not Powered Up

Send 01100<xxxx>

Wait T_{PUD}

Playback the next message

Send 11110<xxx>

Playback continues until an EOM is reached (or chip runs out of memory space)

PLAYBACK THE "3RD" MESSAGE (FAST FORWARD TO MESSAGE NUMBER 3 AND PLAY IT)

Power up the device

Send 01100<xxx>

Wait T_{PUD}

Start Message Cueing Cycle at "0" Address

Send 11101<x><00 0000 0000>

Send 11111<xxx>

Device runs at 800 times normal play speed, audio muted.

Device stops at next EOM, gives EOM interrupt, increments address counter 1 count, now the address pointers points to '2nd" Message. Execute second message cueing cycle at "next" message.

Send 11111<xxx>

Device runs at 800 times normal play speed, audio muted.

Device stops at next EOM, gives EOM interrupt, incumbents address counter 1 count, now the address pointers points to '3rd" message. Play "next" message.

Send 11110<xxx>

The third message will play at normal speed. When message ends EOM interrupt occurs

READ INTERRUPT STATUS BITS AND CURRENT ADDRESS

Clock in Instruction

Send <xxxxx><xxx>

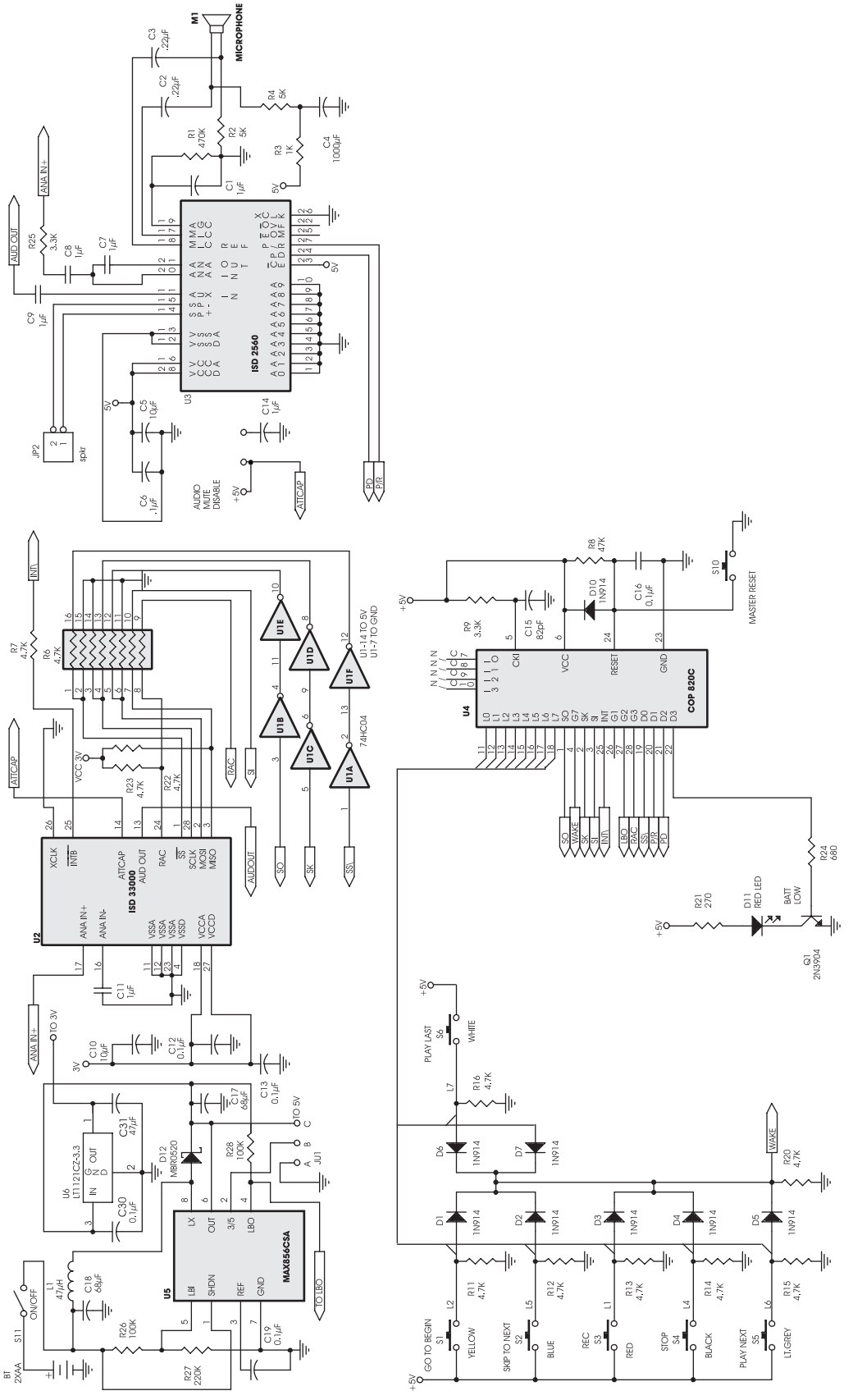
Device will execute the operation as specified by the instruction.

If there is no desire to change the status of the device, care should be taken that the command is compatible with current operation.

Send SPI 8 clocks to read the status bits (OVF and EOM)

Send SPI 16 clocks to read status and current address.

Figure 1: ES302 Schematic



NOTE: *L1 is a Sumida CD43-470. C17 and C18 are 10V Tantalum (SMD). D12 substitute 1N817 SCHOTTKY.*

APPLICATION EXAMPLE (ISD33000 DEMO BOARD)

The ISD-ES302 Demo Board is designed to enable listeners hear the voice quality of the 3-volt part and to demonstrate some of the features available through the SPI control bus.

FEATURES OF THE ISD-ES302 DEMO BOARD

- Record
- Play—last
- Play—next
- Stop/pause
- Go-to- beginning of memory
- Fast forward through messages.

HARDWARE

The three major integrated circuits on the board are the ISD33000 voice chip, U2, the NSC COP820C microcontroller, U4, and an audio chip, U3. The audio chip is an ISD2560 of which only the microphone preamplifier and the speaker driver are used. It is run on five volts whereas the ISD33000 is run on three volts. The audio chip would not normally be needed because the audio input and speaker output functions are already on the board in a cellular phone, for example. The board is powered by two AA cells. These cells drive a voltage converter to get the five volts for the audio chip and the microcontroller. This voltage is then regulated down to three volts (or 3.3 VDC) for the ISD33000 device.

SOFTWARE

COP8 is an 8-bit microcontroller from National Semi Conductor with 1 Kbytes of on-chip ROM and 64 bytes of on-chip RAM. The serial interface on-chip "microwire" is compatible with the ISD33000 SPI port.

The COP microcontroller provides the interface between the user's fingers on the keyboard and the ISD33000 device. It interprets the key strokes and issues the appropriate commands to the ISD33000. It also monitors the ISD33000 status registers and interrupt output to keep track of operations. The program also handles any interrupt that is generated by the ISD33000 during playback.

The following flowchart is used to create the demo software. The interrupt is a background routine. Every time an EOM or OVF is detected the ISD33000 will generate an interrupt. The microcontroller issues a stop command when EOM is detected and when an OVF is detected, the microcontroller re-initializes the address pointer to beginning of the memory in play mode followed by a stop command.

Figure 2: Demo Software Flowchart

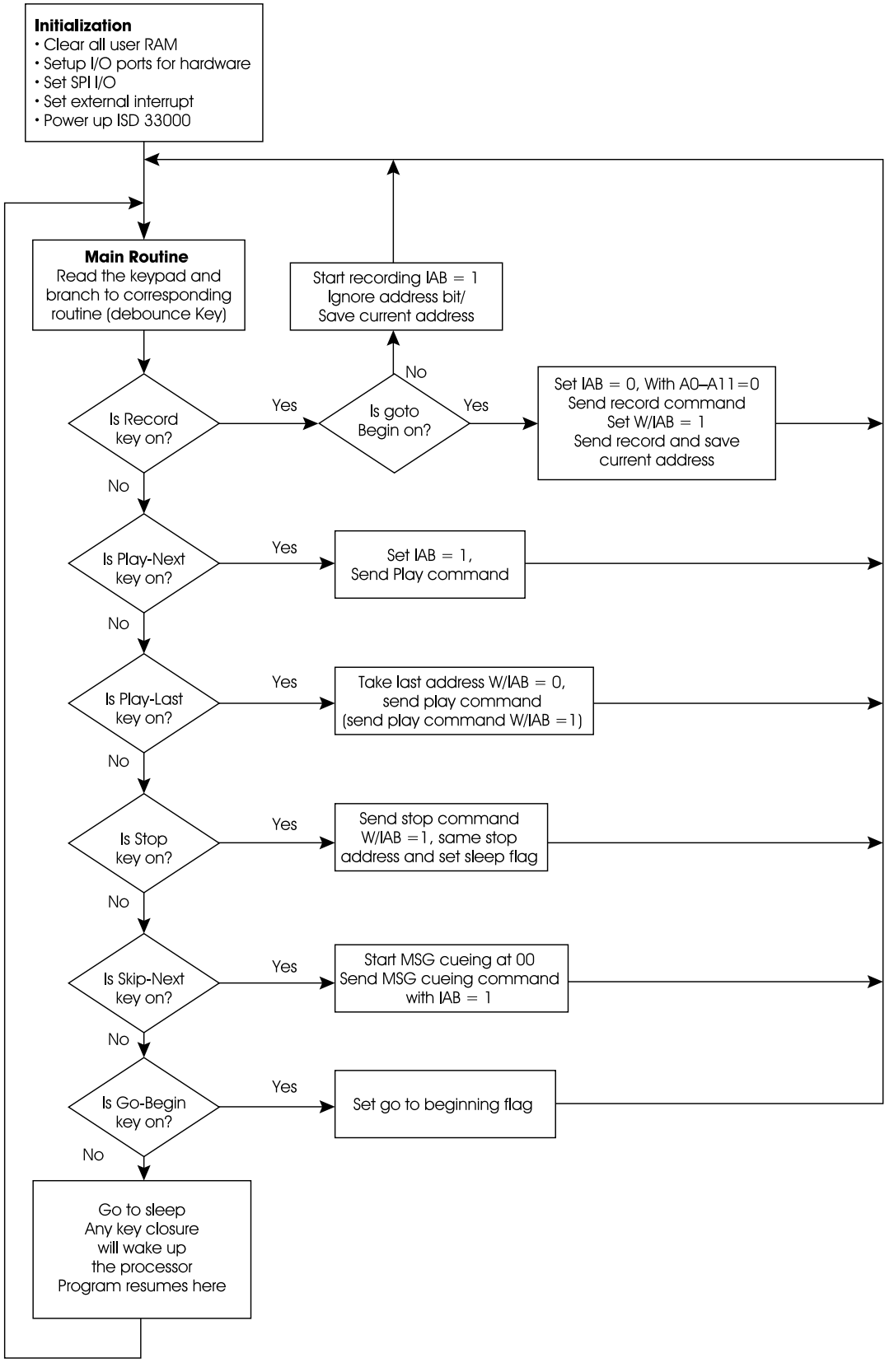
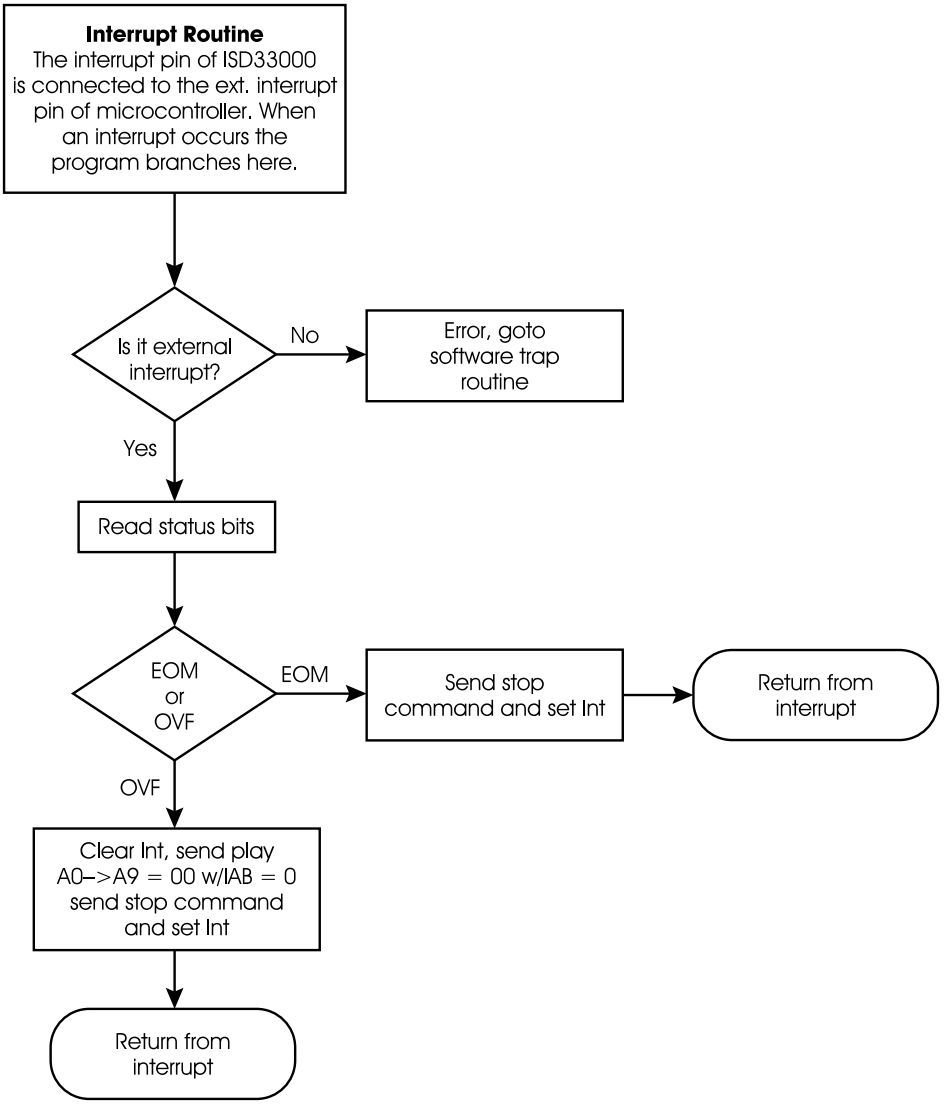


Figure 3: Interrupt Routine Flowchart



```
;**********************************************************************
;*   ISD33000  D E M O      P R O G R A M                             *
;*    S E C O N D   V E R S I O N                                      *
;*                                                                     *
;*    (C) 1996 I N F O R M A T I O N   S T O R A G E   D E V I C E S  *
;*                                                                     *
;*                                                                     *
;*      MICROCONTROLLER      : COP820C                                 *
;*      DATE OF LAST REVISION: 06.03.96                                *
;*      NAME OF SOURCE FILE  : demo.asm                                *
;*      CLOCK SPEED          : 2.8 - 2.2 MHz                           *
;;**********************************************************************
;**********************************************************************
.list 33
.INCLD COP820.INC     ;SYMBOLS USED FREQUENTLY BY COP820
.FORM
;Assignment For ISD33000 DEMO
;
;* CONSTANT DECLARATIONS
    SS      =       0       ; SLAVE SELECT
    D2      =       2       ; D PORT PIN 2
    D1      =       1       ; D PORT PIN 1
    LED     =       3       ; LED INDICTOR PIN
    LBO     =       2       ; LOW BAT DETECTOR
;**********************************************************************
;REGISTERS
;
    DELC2   =       0F0     ; COUNTER FOR SOFTWARE TIME LOOPS
    DELC1   =       0F1     ; COUNTER FOR SOFTWARE TIME LOOPS
    DBU     =       0F2     ; COUNTER FOR DEBOUNCE TIME
;   0FC                     ; RESERVED FOR X POINTER
;   0FD                     ; RESERVED FOR STACK POINTER
;   0FE                     ; RESERVED FOR B POINTER
;MEMORY
;**********************************************************************
    STAT    =       0C      ; STATUS REGISTER
    NEW     =       00      ; STOP OR COMPLETION
    OVF     =       01      ; OVERFLOW
    BEG     =       02      ; BEGGIN OF MEMORY
    HALT    =       03      ; OPERATION COMPLETED
    EOM     =       04      ; 1 END OF MESSAGE
    EOS     =       05      ; 1 EXTERNAL INTERRUPT PENDING
    EXTIN   =       06      ; 1=EXTERNAL INTERRUP PENDING
;---------------------------------------------------------------------
    ADDR0   =       001     ; BCD TO BINARY LOCATION BINARY IN [1,0] BCD IN [3,2]
    TDBUFF  =       002     ; TOP OF DATA BUFFER HOLDS STOP ADDRESS BYTE 1
    ADDR1   =       003     ; MEMORY LOCATION FORM TEMPORARY DATA
    TEMP    =       004     ; TEMPORARY REGISTER
    TDBUF1  =       005     ; TOP OF DATA BUFFER1 HOLDS STOP ADDRESS BYTE 2
    KEYBUF  =       006     ; COMMAND BUFFER
    KEYIN   =       007     ; HOLDS ADDRESS LOWER BYTE
    KEYIN1  =       008     ; HOLDS ADDRESS UPPER BYTE
    SAVEA   =       009     ; SAVE ACUMULATOR WHEN IN INTERRUPT
    SAVEB   =       00A     ; B REGISTER SAVE AREA
    SAVEX   =       00B     ; X POINTER SAVE AREA
```

```
;026.......02F; RESERVED STACK AREA
    STACK   =       02F     ; TOP OF STACK
;   ;
.FORM
;*************************************************************************
;       INTIALIZE REGISTERS
;       POWER UP AND PRESET ROUTINE
;*************************************************************************
.SECT CODE,ROM,ABS=0
CLRRAM:
    LD      B,#00   ; CLEAR ALL USER  RAM including I/O ports
    LD      X,#0FC  ; AND REGISTERS
DONE:CLR    A
    X       A,[B+]
    DRSZ    X
    JP      DONE
;START PROGRAM EXECUTION
REST:LD     SP,#02F DEFAULT STACK INITIALIZATION
    LD      B,#PORTLD; CONFIGURE L-PORT
    LD      [B+],#0FF
    LD      [B],#000; MAKE ALL L PINS INPUT
    LD      B,#PORTGD; CONFIGURE G PORT
    LD      [B+],#01F; IRQ LOW, PORTG DATA REGISTER
    LD      [B],#030; SET I/O FOR G POR & Microwire
    LD      PORTD,#07; initialize portd
;*************************************************************************
;ENABLE INTERRUPT
**************************************************************************
    LD      B,#CNTRL
    LD      [B+],#08C; CNTRL REGISTER SELECT MUIRE
    LD      [B],#003; INITIALIZE PSW
    LD      B,#0FF
;************ INITIALIZE ISD33000 *****************************
    LD      A,#000  ; INITIALIZE ADDRESS TO 00
    RBIT    SS,PORTD; ENABLE SPI
    JSR     SPIX    ; SEND OUT THE COMMAND
    LD      A,#000  ; POWER UP, USE INPUT ADDRESS REG.
    JSR     SPIX
    SBIT    SS,PORTD; DISABLE SPI
    LD      DELC1,#02; INITIALIZE DELAY COUNTER
    JSR     PWRUP   ; SEND POWER-UP COMMAND
;*****************  WAIT FOR AN INPUT HERE *******************************
;
;                   MAIN LOOP WAITING FOR A SWITCH CLOSER
;*************************************************************************
READ:
    IFBIT   LBO,PORTGP;IF LOW BATT PIN IS LOW GO TO WARNING ROUTINE
    JP      READ1   ;ELSE PROCEED
    JMP     WARNING ;GO TO WARNING ROUTINE
**************************************************************************
;BRANCH ACCORDING TO THE KEY PUSHED ON THE KEY PAD
;*************************************************************************
READ1:
    LD      PORTLC,#000; CONFIGURE L PORT AS INPUT PORT
    LD      PORTLD,#0FF; WEAK PULL-UP
```

```
    LD      A,PORTLP; READ PORT L
    LD      DELC1,#30; DE-BOUNCE THE SWITCH
    JSR     DELAY1
    AND     A,#0FF  ; SELECT THE  SWITCHES
    IFEQ    A,#040
    JP      PLAY    ; PLAY AT THE "NEXT" ADDRESS
    IFEQ    A,#02
    JP      REC     ; RECORD AT THE "NEXT" ADDRESS
    IFEQ    A,#010
    JP      STOP    ; STOP PLAYBACK OR RECORD
    IFEQ    A,#080
    JP      PLAY0   ; PLAY ADDRESS 0
    IFEQ    A,#008
    JP      REC0    ; RECORD AT ADDRESS 0
    IFEQ    A,#020
    JP      MSGCUE  ; DO A MESSAGE CUEING CYCLE
    IFEQ    A,#004
    JMP     GOTOB
    IFBIT   HALT,STAT; IF SLEEP MODE IS SET GO TO SLEEP ROUTINE
    JP      HALT1   ; GO TO SLEEP ROUTINE
    JP      READ    ; ELSE BACK TO MAIN
HALT1:
    RBIT    HALT,STAT; RESET SLEEP MODE FLAG
    SBIT    7,PORTGD; MICRO IS PUT TO SLEEP MODE FOR
    NOP     ; POWER SAVING
    NOP     ; THE PROGRAM RESUMES HERE WHEN A KEY
    NOP     ; RESET BUTTON IS PUSHED
    NOP
    JMP     READ    ; GO WAIT FOR AN INPUT
;*****************************************************************
;                         INITIALIZE ISD33000 Routine
;*****************************************************************
PWRUP:
    LD      A,#004  ; 00100 POWER UP ISD33000
    RBIT    SS,PORTD; SELECT ISD33000
    JSR     SPIX    ; SEND OUT THE POWER UP COMMAND
    SBIT    SS,PORTD; DISABLE SPI
    RET
;*****************************************************************************
;GENERIC DELAY ROUTINE  256TC X 256TC( TC= INSTRUCTION CYCLE )
;*****************************************************************************
DELAY1:LD   DELC2,#0FF
DELAY2:DRSZ DELC2   ; DELAY ROUTINE MAX LENGTH 256 LOOPS
    JP      DELAY2
    DRSZ    DELC1
    JP      DELAY1
    RET
;*********************************************************
                ;MESSAGE CUEING CYCLE
;*********************************************************
MSGCUE:
    SBIT    LED,PORTD; FLASH LED FOR 50MS TO INDICATE
    ; A MSG CUEING CYCLE
    LD      DELC1,#0F; DE-BOUNCE THE SWITCH
    JSR     DELAY1  ; USE DELAY1 ROUTINE
```

```
    RBIT    LED,PORTD; LED OFF
    LD      A,#01F  ; SEND MESSAGE CUEING COMMAND ;
    ; WITH IAB = 1
    RBIT    SS,PORTD; ENABLE SPI
    JSR     SPIX    ; SEND OUT THE COMMAND
    SBIT    SS,PORTD; DISABLE SPI
    JMP     READ    ; DONE GO TO MAIN ROUTINE
.FORM
*******************************************************************************
    *BEGIN INTERRUPT ROUTINE
 .=X'00FF
;*******************************************************************************
;INTERRUPT SERVICE ROUTINE , THE PROGRAM BRANCHES HERE WHEN THE PROCESSOR IS INTERRUPTED
;*******************************************************************************
INT1:
    IFBIT   IPND,PSW; CHECK  IF EXTERNAL INTERRUPT PENDING
    JP      EXT     ; GO SERVICE EXT. INTERRUPT
    JMP     CLRRAM  ; ELSE ILLEGAL CONDITION  RESET PROCESSOR
EXT:
    JSR     PUSH    ; SAVE REGISTERS
    RBIT    IPND,PSW; RESET EXTERNAL INTERRUPT PENDING
    JSR     STOPX   ; ISSUE A STOP COMMAND IF END OF MESSAGE
    IFBIT   07,TDBUFF; CHECK IF OVERFLOW ?
    JSR     OVFPO   ; YES GO TO OVERFLOW RECOVERY ROUTINE
    JSR     POP     ; RETURN FROM INTERRUPT
    RETI
;********************* END INTERRUPT ROUTINE**************************
*******************************************************************************
;RECORD AT "LAST" ADDRESS
;*******************************************************************************
REC:
    IFBIT   BEG,STAT; IF BEG OF MEMORY GO RECORD FROM 0
    JMP     REC0\   ; ELSE
    LD      A,#000  ; READ THE ADDRESS POINTER
    RBIT    SS,PORTD        ;
    JSR     SPIX    ;
    LD      A,KEYBUF        ; READ THE OUTPUT DATA
    X       A,KEYIN         ; SAVE IT IN KEY IN
    LD      A,#00D          ;
    JSR     SPIX    ; GET THE DATA FROM THE INCOMING BUFFER
    LD      A,KEYBUF; READ THE OUTPUT DATA
    X       A,KEYIN1; SAVE SECOND BYTE
    SBIT    SS,PORTD;
    SBIT    NEW,STAT        ; INDICATE A NEW RECORDING CYCLE
    RBIT    D2,PORTD        ; POWER AMPS ON
    RBIT    D1,PORTD        ; RECORD MODE
    SBIT    LED,PORTD       ; REC OPERATION IN PROGRESS
    JMP     READ    ; DONE WAIT FOR ANOTHER COMMAND OR OVF
;******************** SPI ROUTINE*****************************************
;
;THIS ROUTINE SENDS ANY GIVEN COMMAND AND RETURNS THE ADDRESS
;POINTER ONE BYTE AT THE TIME SAVES THE RETURN ADDRESS IN KEYBUF
;BE AWARE THAT ANY UN READ KEYBUF WILL BE LOST WITH THE NEXT SPI
;COMMAND
;*******************************************************************************
```

```
SPIX:
    X       A,SIOR  ; LOAD THE SPI SHIFT REGISTER
    SBIT    #BUSY,PSW; ENABLE THE SPI SHIFT REGISTER
WAIT:IFBIT  #BUSY,PSW; IF IN THE MIDDLE OF TRANSMISSION
    JP      WAIT    ; WAIT until done
    X       A,SIOR  ; READ SPI SHIFT REGISTER
    X       A,KEYBUF; SAVE THE STATUS IN KEYBUF
    RET
;*****************************************************************
; STOP WITH IAB=1
STOP:JSRSTOPX; SEND A STOP COMMAND
    JMP     READ
;*****************************************************************
;                   STOP ROUTINE
;*****************************************************************
STOPX:RBIT  LED,PORTD; LED OFF
    SBIT    D2,PORTD; DISABLE POWER AMPS
    LD      A,#000  ; SET THE STOP COMMAND WITH POWER UP BIT
    RBIT    SS,PORTD; DISABLE SPI
    JSR     SPIX
    LD      A,KEYBUF; GET THE ADDRESS FROM THE BUFFER
    X       A,TDBUFF; SAVE IT IN TDBUFF MEMORY LOCATION
    LD      A,#00E  ; SET THE STOP COMMAND WITH POWER UP BIT
    ; IN PLAY MODE WITH IAB = 1
    JSR     SPIX    ;
    LD      A,KEYBUF;
    X       A,TDBUF1; SAVE THE 2ND BYTE
    SBIT    SS,PORTD; DISABLE SPI
    SBIT    HALT,STAT; GO TO SLEEP MODE
    RET
;*****************************************************************
;   IGNORE ADDRESS BITS
;   ; PLAY AT "LAST" ADDRESS   ROUTINE
;*****************************************************************
PLAY:
    RBIT    D2,PORTD
    SBIT    D1,PORTD; UT ISD1000A IN PLAY MODE
    SBIT    LED,PORTD; INDICATE PLAY IN PROGRESS
    IFBIT   BEG,STAT; CHECK IF PLAY FROM BEG OF MEMORY
    JMP     PLAY2   ; YES, RESET ADDRESS TO 00 AND PLAY
PLAYN:
    LD      A,#00E  ; PLAY IAB = 1, PU =1, P/R =1 RUN =0
    RBIT    SS,PORTD;
    JSR     SPIX    ;
    SBIT     SS,PORTD;
    LD      A,#00F  ; PLAY IAB = 1, PU =1, P/R =1 RUN =1
    RBIT    SS,PORTD;
    JSR     SPIX    ;
    SBIT    SS,PORTD;
    JMP     READ    ; DONE GO WAIT FOR ANOTHER COMMAND
PLAY2:LD    A,#000  ; PLAY IAB = 1, PU =1, P/R =1 RUN =0
    RBIT    SS,PORTD;
    JSR     SPIX    ;
    LD      A,#007  ; PLAY IAB = 1, PU =1, P/R =1 RUN =1
    RBIT    SS,PORTD;
```

```
    JSR     SPIX    ;
    SBIT    SS,PORTD;
    RBIT    BEG,STAT; RESET BEG OF MEMORY FLAG
    JMP     PLAYN   ; GO CONTINUE
;*********************************************************************
;GO TO BEGINNING OF MEMORY  THIS ROUTINE ONLY FLASHES AN LED AND SETS
; A FLAG TO INDICATE THE BEG OF MEMORY BUTTON IS PUSHED
;*********************************************************************
GOTOB:
    SBIT    LED,PORTD; LED ON
    SBIT    BEG, STAT;
    LD      DELC1,#0F; DE-BOUNCE THE SWITCH
    JSR     DELAY1
    RBIT    LED,PORTD; LED OFF
    LD      DELC1,#0F; DELAY
    JSR     DELAY1  ;
    SBIT    LED,PORTD; LED ON
    LD      DELC1,#0F; DELAY
    JSR     DELAY1  ;
    RBIT    LED,PORTD; LED OFF
    JMP     READ    ; DONE WAIT FOR ANOTHER COMMAND
;*********************************************************************
;START PLAY AT ADDRESS 0 IGNORE ADDRESS BITS
;*********************************************************************
PLAY0:JSR   PLAY1   ; USE THE PLAY1 ROUTINE
    JMP     READ    ; DONE GO WAIT FOR ANOTHER COMMAND
PLAY1:
    RBIT    D2,PORTD; PD PIN TO 0
    SBIT    D1,PORTD; PUT ISD1000A IN PLAY MODE (P/R)
    SBIT    LED,PORTD;
    IFBIT   NEW,STAT; IF THERE IS NO NEW RECORD SKIP
    JMP     PLAYNW  ;
    JMP     PLAYA   ; PLAYA  ELSE
PLAYNW:
    LD      TEMP,#00; THIS ROUTINE READS THE ADDRESS POINTER
    IFBIT   5,KEYIN ; PREPARES IT FOR SPI REGISTER
    SBIT    7,TEMP  ; SAVE THE FISRT BYTE IN KEYIN AND SECOND
    IFBIT   4,KEYIN ; BYTE IN KEYIN1 MEMORY LOCATIONS
    SBIT    6,TEMP
    IFBIT   3,KEYIN
    SBIT    5,TEMP
    IFBIT   2,KEYIN
    SBIT    4,TEMP
    IFBIT   1,KEYIN
    SBIT    3,TEMP
    IFBIT   0,KEYIN
    SBIT    2,TEMP
    LD      A,TEMP
    X       A,KEYIN
    LD      A,KEYIN1
    X       A,TEMP
    IFBIT   7,TEMP
    SBIT    1,KEYIN
    IFBIT   6,TEMP
    SBIT    0,KEYIN
```

```
    LD      A,#00
    X       A,KEYIN1
    IFBIT   5,TEMP
    SBIT    7,KEYIN1
    IFBIT   4,TEMP
    SBIT    6,KEYIN1
    RBIT    NEW,STAT
PLAYA:
    LD      A, KEYIN; READ THE KEYIN BUFFER
    RBIT    SS,PORTD; SEND OUT THE ADDRESS
    JSR     SPIX
    LD      A,#007  ; PLAY IAB = 0, PU =1, P/R =1 RUN =1
    OR      A, KEYIN1;
    JSR     SPIX    ;
    SBIT    SS,PORTD; DISABLE SPI
    RBIT    SS,PORTD
    LD      A,#00E  ; PLAY IAB = 1, PU =1, P/R =1 RUN =0
    RBIT    SS,PORTD
    JSR     SPIX    ;
    SBIT    SS,PORTD;
    RBIT    SS,PORTD;
    LD      A,#00F  ; PLAY IAB = 1, PU =1, P/R =1 RUN =1
    RBIT    SS,PORTD;
    JSR     SPIX    ;
    SBIT    SS,PORTD;
    RET     ;
;*********************************************************************
                ;RECORD AT ADDRESS 0
;*********************************************************************
REC0:
    RBIT    D2,PORTD; POWER AMPS OFF
    RBIT    D1,PORTD; RECORD MODE
    SBIT    LED,PORTD
    LD      A,#000  ; INITIALIZE ROWS =000
    RBIT    SS,PORTD; ENABLE SPI
    JSR     SPIX    ;
    LD      A,#005  ; REC IAB = 0, PU = 1, P/R =0 RUN =1
    JSR     SPIX    ;
    SBIT    SS,PORTD; DISABLE SPI
    LD      A,#00D  ; REC IAB = 1, PU = 1, P/R =0 RUN =1
    RBIT    SS,PORTD;
    JSR     SPIX    ;
    SBIT    SS,PORTD;
    RBIT    BEG,STAT;
    JMP     READ
;*********************************************************************
;PUSH AND POP ROUTINES FOR SAVING REG. DURING INTERRUPT
**********************************************************************
POP:
    LD      A,SAVEX
    X       A,X
    LD      A,SAVEB
    X       A,B
    LD      A,LCDPTR
    X       A,PORTLD
```

```
    LD      A,SAVEA
    RET
;
PUSH:
    X       A,SAVEA
    LD      A,B
    X       A,SAVEB
    LD      A,X
    X       A,SAVEX
    LD      A,PORTLD
    X       A,LCDPTR
    RET
WARNING:
    SBIT    LED,PORTD
    LD      DELC1,#50; DE-BOUNCE THE SWITCH
    JSR     DELAY1
    RBIT    LED,PORTD
    LD      DELC1,#50; DE-BOUNCE THE SWITCH
    JSR     DELAY1
    JP      WARNING
;*********************************************************************
;                   OVERFLOW RECOVERY ROUTINE
; INITIALIZE ADDRESS POINTERS TO 00 IN PLAY MODE AND IMMEDIATELY STOP THE OPERATION.
;*********************************************************************
OVFPO:
    RBIT    SS,PORTD
    LD      A,#000  ; POWER UP, USE INPUT ADDRESS REG.
    JSR     SPIX    ;
    LD      A,#007  ; PLAY MODE WITH IAB = 0
    JSR     SPIX
    SBIT    SS,PORTD
    LD      A,#000  ; POWER UP, USE INPUT ADDRESS REG.
    RBIT    SS,PORTD
    JSR     SPIX
    LD      A,#006  ; STOP MODE WITH IAB = 0
    JSR     SPIX
    SBIT    SS,PORTD
    RET
 .ENDCLRRAM
;******************END OF PROGRAMM*********************************
```

INSTRUCTIONS

Six of the 9 push-buttons are labeled on the PCB. Pushing the yellow "GO_TO_BEG" button will reset the address pointer to the front of the chip or address 000. There will be a double flash of the LED, D11, in the bottom left corner of the PCB to indicate that this has been done.

Pushing the red "RECORD" button will turn on the red LED to indicate that the chip is now recording anything it hears at the microphone M1 near the top center of the board. The board will continue to record until the end of the chip is reached or the black "STOP" button is pressed. At that time, the LED will go out and the board will stop recording.

Pushing the white "PLAY_LAST" button will playback what was just recorded. The message will play through to its end or stop when the black "STOP" button is pressed.

Pushing the yellow "GO_TO_BEG" button and then the white "PLAY_NEXT" button will play messages from the beginning of memory through to the end or stop/pause when the black "STOP" button is pressed. To resume playback after pause, push PLAY_NEXT again. To play the next message, press PLAY_NEXT.

The blue "SKIP_TO_NEXT" button bypasses a message and plays the one after. For example, if three message are recorded beginning at the front of the chip, after the last message press the white "PLAY_NEXT" button to play the first message, press the blue "SKIP_TO_NEXT" button to bypass the second message and then press the white "PLAY_NEXT" to play the third message.

SERIAL INTERFACE PRODUCTS

Using the ISD33000 Device with a Low-Cost Motorola Microcontroller

ISD application note "Using the ISD33000 with a Microcontroller," described code written for the COPS family of microcontrollers to do basic record and playback in the ISD33000 device series. The ISD-ES302 demo board uses that microcontroller and runs the listed software in that application note.

This application note describes how the Motorola 6805 series of microcontrollers may be used to perform the same function. Specifically, the attached code runs in a MC68HC705J1A 20 pin device and plugs into the ISD-ES302 demo board via an adapter board. Only one change was made on the ISD-ES302 board; the addition of a diode. The adapter board and ISD-ES302 modification are described following the software discussion. Much of this design is covered in the section "Using the ISD33000 with a Microcontroller," refer to it for the main board schematic and related explanations. The flow chart for the software is essentially the same for both notes and will not be repeated.

The main difference between the code in the previous application note and this one is that the COPS processor has a hardware SPI port and the MC68HC705J1A Motorola microcontroller does not. This software, therefore, has routines written to replace the hardware SPI port.

MAJOR SOFTWARE ROUTINES

The list file of this software will be broken up into pieces and each routine described. Many notes can also be found in the software listing itself. An unassembled source file of this software is available as an E-mail attachment from ISD Applications Department. Send a request to apps@isd.com and ask for the Applications Note No. 3 Source code.

Program Set Up and Listing Header

This software was assembled using a 6805 cross assembler purchased from 2500 A.D. Software.

```
2500 A.D. 6805 Macro Assembler—Version 4.01b
              ------------------------------------------------
                      Input  Filename : DEMO1.ASM
                      Output Filename : DEMO1.obj
    1      LIST ON
    2      PL 120
    3*************************************************************
    4*This Software is Copyright 1996 by Information Storage Devices
    5*
    6  * ISD
    7*
    8*
    9*
   10*
```

```
11*  *****        ********   *     *         *****
12*  *     *      *          **    **       *      *
13*       *      *     *          * *   * *      *      *
14*      *      *     *****      *  *  *  *     *      *
15*     *      *     *          *   * *   *    *      *
16*    *      *     *          *    **    *   *      *
17*   *******      ********   *     *     *    *****
18*
19*
20*
21*
22*
23*
24;*************************************************************************
25;*   ISD33000  D E M O       P R O G R A M                                 *
26;*                                                                         *
27;*                                                                         *
28;*    (C) 1996 I N F O R M A T I O N   S T O R A G E   D E V I C E S      *
29;*                                                                         *
30;*                                                                         *
31;*      MICROCONTROLLER      : MC68HC705J1A                                *
32;*      DATE OF LAST REVISION: 06.03.96                                    *
33;*      NAME OF SOURCE FILE  : demo1.asm                                   *
34;*      CLOCK SPEED          : 3.579545 MHz                                *
35;*
36;*************************************************************************
37;*************************************************************************
38
39                          *
40                          *
41                          *
42                          *
43                          *
44                                 LIST ON
45
```

Microcontroller pin out and I/O definition, register definition: The following shows the pin out of the microcontroller and defines the device I/O. It also defines the memory map and interrupt vectors as well as the control registers used in the device.

```
46   0000                        .ABSOLUTE
47                          ************************************************************
48                              *Port Definitions       MC68HC705J1A DIP or SOIC Package
49                              *PORT A
50                          ************************************************************
51           0000               porta    equ     0
52           0040               portaDDR equ     %01000000
53
54           0000               L2       equ     $00     pin 18 - Go to Begin pushbutton
55           0001               L5       equ     $01     pin 17 - Skip to Next pushbutton
56           0002               L6       equ     $02     pin 16 - Play Next pushbutton
57           0003               L1       equ     $03     pin 15 - REC pushbutton
58           0004               L4       equ     $04     pin 14 - STOP pushbutton
59           0005               RAC      equ     $05     pin 13 - Row Address Clock Input
```

```
 60          0006            LOWBAT  equ     $06     pin 12 - LED control output
 61          0007            L7      equ     $07     pin 11 - Play Last pushbutton
 62                          *
 63                        ************************************************************
 64                          *PORT B
 65                        ************************************************************
 66          0001            portb    equ     1
 67          001F            portbDDR equ     %00011111
 68
 69          0000            PD      equ     $00     pin 8  - PD pin to ISD2500
 70          0001            PLAREC  equ     $01     pin 7  - PLAY/REC pin to ISD2500
 71          0002            SSBAR   equ     $02     pin 6  - Slave Select SPI Output
 72          0003            SK      equ     $03     pin 5  - SPI Clock output
 73          0004            SO      equ     $04     pin 4  - Serial Out
 74          0005            SI      equ     $05     pin 3  - Serial In
 75                          *
 76                        ************************************************************
 77                          * Other Pin definitions
 78                        ************************************************************
 79                          *Pin 10 = VSS (GND)
 80                          *Pin 20 = RESET\ (active low)
 81                          *Pin 19 = IRQ\ ISD33000 Interupt output
 82                          *Pin  9 = VCC (+5)
 83                          *Pin  1 = OSC1
 84                          *Pin  2 = OSC2
 85
 86                          *SOFTWARE ASSUMES A 3.579545 MHz Crystal
 87                         *PERIOD IS .279365 uSEC, OR INTERNAL CLOCK OF .55873 uSEC PER
 88                          *CYCLE.                                          ------
 89                          *
 90                          *
 91                        ************************************************************
 92                          *area definitions
 93                         ************************************************************
 94          00C0            RamArea         equ     $00C0
 95          00FF            StkTop          equ     $00FF
 96          0300            RomArea         equ     $0300
 97          07F8            IntVects        equ     $07F8
 98                          *
 99
100                         ************************************************************
101                          *Vector area
102                        ************************************************************
103   07F8                        org     IntVects
104   07F8   0300                 fdb     TIMESVC
105   07FA   0302                 fdb     extsvc
106   07FC   0301                 fdb     swisvc
107   07FE   0324                 fdb     reset
108                         *
109                         *
110
111                         ************************************************************
112                          *Control Register Definitions
113                         ************************************************************
114 0008    TSCR    equ     $8      TIMER STATUS AND CONTROL REG
```

```
115          0009            TCR             equ     $9      TIMER COUNTER REGISTER
116          000A            ISCR            equ     $A      IRQ STATUS AND CONTROL
117          0010            PDRA            equ     $10     PULL DOWN REGISTER A
118          0011            PDRB            equ     $11     PULL DOWN REGISTER B
119          07F1            MOR             equ     $07F1
120          07F0            COPR            equ     $07F0
121
122
```

Flag Registers and System Equates: The following listing shows the definition of the RAM area in the microcontroller as well as locations of flags, registers and equates. Note that there are two bytes reserved for flags when only one was necessary. Since this program was well within the memory boundaries of the microcontroller, it was not necessary to eliminate this unneeded byte.

```
123                         ************************************************************
124                           *Ram flags and registers
125                         ************************************************************
126
127
128   00C0                                  org     RamArea
129                         ************************************************************
130   00C0                    R00             rmb     1
131                           ***************************
132 0000    PLAYING equ     $00     Indicates we are Playing back
133 0001    RECDING equ     $01     Indicates we are Recording
134 0002    MAKEIT0 equ     $02     Make it zero flag
135 0003    OPERATE equ     $03
136                           ****** equu$04
137                           ****** equu$05
138                           ****** equu$06
139                           ****** equu$07
140                           ***************************
141   00C1                    R01             rmb     1
142                           ***************************
143                           ******          equ     $10
144                           ******          equ     $11
145                           ******          equ     $12
146                           ******          equ     $13
147                           ******          equ     $14
148                           ******          equ     $15
149                           ******          equ     $16
150                           ******          equ     $17
151                           ***************************
152
153                           ***************************
154                           *NOW SET UP THE REGISTERS USED IN THE PROGRAM
155                           ******************************************
156   00C2STRTREGS
157   00C2ADDRLrmb 1        Address reg LOW
158   00C3ADDRHrmb 1        Address reg HIGH
159   00C4RECADDLrmb1       holds addr of last record (LOW)
160   00C5RECADDHrmb1       holds addr of last record (HIGH)
161   00C6SPIONErmb1        SPI Low byte - with control bits
162   00C7SPITWOrmb1        SPI High byte - address
```

```
163   00C8SEQCNTrmb1      Real Time Interrupt counter
164   00C9TOFCNTrmb1      Timer Overflow Flag counter
165   00CATEMPrmb  1      USED FOR VARIOUS STUFF
166   00CBTEMP1rmb 1      USED IN DELAY TIMERS
167   00CCTEMP2rmb 1      USED only in 16.879 mSEC TIMER
168   00CDTEMPOUTrmb1     Store of acc during SPI activity
169   00CETEMPINrmb1      Store of acc during SPI activity
170                        *
171   00CFENDREG
172                        *
173           *NOTE THAT THIS POINT CANNOT GO PAST $ WITHOUT LOOKING AT THE STACK USAGE
174                        ************************************************************
175                          *Define equates and other things
176                        ************************************************************
177          0004            DDR             equ     4
178          0020            POWRERUP        equ     $20
179          00A0            SETREC          equ     $A0
180          0000            STOPPWRDN       equ     $10(IAB also set)
181          0030            STOP            equ     $30     (IAB also set)
182          00E0            SETPLAY         equ     $E0
183          00B0            REC             equ     $B0
184          00E8            SETMC           equ     $E8
185          00F8            MC              equ     $F8
186          00F0            PLAY            equ     $F0
187          0030            RINT            equ     $30     (IAB also set)
188          0070            READADR         equ     $70     (no RUN, IAB set)
189
190
191                          *
```

Interrupt Routines: The interrupt routines are defined below. Note that the timer interrupt service routine (TIMESVC) and the software interrupt service routine (SWISVC) are not needed in this software. An accidental interrupt to those routines results in an immediate return from interrupt instruction (rti).

The external interrupt routine shuts off the ISD2500 device on the board that is used as a microphone preamp and speaker driver. It also sends a STOP opcode to the ISD33000 that is probably not needed because an interrupt from the ISD33000 always results from the end of an operation. The external interrupt routine then checks to see that the interrupt has been cleared, i.e., that the INT pin of the ISD33000 is back HIGH. If it is not, then an early chip revision of the ISD33000 is in the system and the device is in the overflow interrupt state. To insure compatibility with this early revision device, the routine then sends a SETPLAY opcode with an address of zero and then a STOP opcode to clear the address counter in the ISD33000 and clear the overflow interrupt.

```
192                        ************************************************************
193 *Interrupt servce routines and subroutine
194                        ************************************************************
195   00CF.CODE
196   00CF.RELATIVE
197   0300org     RomArea
198                          *
199                          *
200   0300                   TIMESVC
201                          *
```

```
                          *NOTE:  Fop=.5587302 uSec (for a color burst xtal)
                          *
                          *

  0300
  0300   80                  rti
  0301
  0301swisvc
  0301   80                  rti
                          *

*-------------------------------------------------------
* START OF EXTERNAL INTERRUPT SERVICE ROUTINE
*-------------------------------------------------------
*

*The external int comes from the ISD33000. We first execute a
*STOP command to try to clear the interrupt.
  0302extsvc
  0302   10 01bsetPD,portbpower down ISD2500 audio chip

  0304   1D 00bclrLOWBAT,portaturn off the LED
  0306   17 C0bclrOPERATE,R00clear the OPERATE flag

  0308   A6 30lda#STOP
  030A   CD 04 5EjsrSPI_8stop the operation

  030D   CD 04 C7jsrTPBNdelay

*We should have a cleared int by now.  If it's not cleared,
*we must be in Overflow.

  0310   2F 11bihENDINTBranch if interrupt line is HIGH

*We in Overflow. Start play at zero then immediately stop it.
*This should clear the interrupt in a beta ISD33000 device

  0312   3F C2clrADDRL
  0314   3F C3clrADDRH
  0316
  0316   A6 E0lda#SETPLAYset up to play message with addr
  0318   CD 04 2EjsrADDADDRadd the address to it
  031B
  031B   CD 04 6BjsrSPI_16start the playback

*Now do the STOP
  031E   A6 30lda#STOP
  0320   CD 04 5EjsrSPI_8stop the operation

  0323ENDINT
  0323   80rti
  0324

*
```

```
256 *-------------------------------------------------------------257* END OF EXTERNAL
INTERRUPT SERVICE ROUTINE
258 *-------------------------------------------------------------259*
260 ;
261
```

Initialization: The reset initialization routine begins at address 324 (all address references are in hexadecimal). Note that the Mask Option Register (MOR) programming is shown for completeness but is "dummied out" so that this otherwise useless code is not executed. The mask option register must be programmed by the EEPROM programmer and must be set up manually in most programmers. Note also that the STOP command in line #321 is dummied out; the sleep instruction of the microcontroller is not used in this program.

```
262 ;*****************************************************************************
263    ;       INITIALIZE REGISTERS
264   ;       POWER UP AND PRESET ROUTINE
265 ;*****************************************************************************
266
267   0324reset
268 *
269   0324   A6 40USERlda#portaDDRset up to read push buttons
270   0326   B7 04staporta+DDR
271   0328   A6 1Flda#portbDDR
272   032A   B7 05staportb+DDR
273
274 *       lda     #$20
275 *       sta     MOR     enable Port A IRQs, no COP, enable
276 *       pull down resistors, enable OSC res.
277
278
279   032C   A6 00lda#$00Turn the LED off
280   032E   B7 00staporta
281
282   0330   A6 07lda#$07SI=LOW+SO=LOW+SK=LOW+SSBAR=HIGH+
283 *       PLAYREC=HIGH + PD=HIGH
284   0332   B7 01staport b
285
286   0334   A6 FClda#$FC
287   0336   B7 10staPDRAenable pull-down res PA0 & PA1
288   0338   A6 3Flda#$3F
289   033A   B7 11staPDRBenable no pull downs on port B
290   033C   3F C0clrR00
291   033E   3F C2clrADDRL
292   0340   3F C3clrADDRH
293   0342   3F C4clrRECADDL
294   0344   3F C5clrRECADDH
295   0346   3F CAclrTEMP
296
297   0348   5Fclrx
298
299   0349   A6 0Clda#$0CClear and disable timer int.
300   034B   B7 08staTSCR
301
```

```
302
303                 ;************ INITIALIZE ISD3300 ****************************
304   034D
305   034D   A6 20lda#POWRERUP
306   034F   CD 04 5EjsrSPI_8power up the ISD33000
307
308   0352   A6 20lda#POWRERUP
309   0354   CD 04 2EjsrADDADDRadd pwr up info to the addr info
310   0357
311   0357   CD 04 6BjsrSPI_16send in an address of all zeros
312
313   035A   CD 04 A1jsrFLASH1blink the led once
314
315   035D   9Crspreset the stack pointer
316   035E   9Aclienable interrups and GO!
317   035F
318
319   035FSTOPPIT
320
321 *       stop
322
323
```

Main Loop: The main loop simply looks for push-button closures on six switches. When a switch is closed, the routine branches to the proper point down in the code to execute the indicated operation. The microcontroller spends most of its time in this loop waiting for a switch closure.

```
324 ************************************************************************
325    *               TOP OF THE LOOP.  EVERYTHING STARTS FROM HERE           *
326    *                                                                       *
327 ************************************************************************
328    ********************  WAIT FOR AN INPUT HERE *******************************
329    *
330    *               MAIN LOOP WAITING FOR A SWITCH CLOSURE
331    ************************************************************************
332 * Read the pushbuttons and branch if they are "alive".
333   035READ
334   035F   00 00 11brsetL2,porta,GOTOBEG
335   0362   02 00 1EbrsetL5,porta,SKIP2NXT
336   0365   04 00 3EbrsetL6,porta,PLAYNXT
337   0368   06 00 60brsetL1,porta,RECIT
338   036B   08 00 0FbrsetL4,porta,STOPITX
339   036E   0E 00 0FbrsetL7,porta,PLAYLASX
340
341   0371   20 ECbraREAD
342
343
```

GOTOBEG: The "Go To Beginning" routine only sets the flag bit MAKIT0 (for Make It Zero) located in the R00 flag register. The MAKIT0 bit will be used to indicate to other routines that record or playback should start from address zero of the ISD33000 when next executed. After setting the flag bit, this routine branches to the READX routine which runs a debounce timer. The READX routine is executed after any push-button

sequence to effectively debounce the push buttons.

Also, in each of the next three routines, SKIP2NXT (Skip to the Next message), PLAYNXT (Play the Next message) and RECIT (Record a message) look at the MAKIT0 bit to see if the address counter should be first be cleared to all zeros before executing the operation. Thus the RECIT routine will be told to begin at zero if the GOTOBEG push button was pressed before the RECIT routine is called. If the push button was not pressed, RECIT will record starting at the end of the last record or play operation without resetting the address counter.

```
344   ****************************** GO TO Beginning ****************************
345
346 *The Go To Beginning Button is pushed
347   0373GOTOBEG
348   0373   06 C0 53brsetOPERATE,R00,READZ
349   0376   14 C0bsetMAKEIT0,R00
350
351
352   0378   CD 04 ACjsrFLASH2blink the led twice
353
354   037B   20 4CbraREADZ
355   ***************************************************************************
356
```

Misc: A couple of the branches are too long. An intermediate jump is needed.

```
357   037DSTOPITX
358   037D   CC 03 F9jmpSTOPIT
359
360   0380PLAYLASX
361   0380   CC 04 05jmpPLAYLAST
362
```

SKIP2NXT: This routine sends a SETMC[1] opcode to the ISD33000 with an address of zero if the MAKIT0 bit is set or sends a MC opcode if it is not set. This routine does not start a record or play operation, but merely causes the address counter in the ISD33000 to be modified so that it is left pointed at the "next" message in the device.

```
363 ****************************** Message Cueing *****************************
364
365          *Now do a message cueing cycle . . . but first, do we do it from zero?
366   0383SKIP2NXT
367   0383   06 C0 43brsetOPERATE,R00,READZ
368
369   0386   05 C0 13brclrMAKEIT0,R00,NOCUE0if this flag clear,
370 *       no cue from zero
371
372 *We do a message cueing cycle from address zero
373   0389   15 C0bclrMAKEIT0,R00
```

1. *See the "Opcode Summary" in the ISD 33000 Data Sheet for an explanation of the instructive opcodes.*

```
374   038B
375   038B   3F C2clrADDRL
376   038D   3F C3clrADDRH
377   038F
378   038F   CD 04 A1 jsrFLASH1blink the LED once
379
380   0392   A6 E8lda#SETMCset up to do a msg cue + addr
381   0394   CD 04 2EjsrADDADDRadd the address to it
382   0397
383
384   0397   CD 04 6BjsrSPI_16do msg cue (but don't play)
385
386
387   039A   20 2DbraREADZdebounce and leave
388
389 *we do a message cueing cycle from the last address
390   039CNOCUE0
391   039C   CD 04 A1jsrFLASH1blink the LED once
392
393   039F   A6 F8lda#MC
394   03A1   CD 04 5EjsrSPI_8do msg cue (but don't play)
395
396   03A4   20 23braREADZdebounce and leave
397
398 ********************************************************************************
399   03A6
400
401
```

PLAYNXT: This routine sends a SETPLAY opcode to the ISD33000 with an address of zero if the MAKIT0 bit is set. This causes playback to start at address zero. If the MAKIT0 flag bit is not set, a playback operation begins at whatever address is currently in the ISD33000's internal address pointer. While playback is occurring, only the STOP push button will be recognized by the software.

```
402 ***************************** Play Next Message ****************************
403
404 *Play the next message . . . unless Go to Beginning has been pressed
405   03A6PLAYNXT
406   03A6   06 C0 79brsetOPERATE,R00,READXcheck if we already oper.
407   03A9   16 C0bsetOPERATE,R00
408
409   03AB   12 01bsetPLAREC,portbPut the ISD2500 into Play
410   03AD   11 01bclrPD,portbPower up the ISD2500
411
412   03AF   05 C0 10brclrMAKEIT0,R00,NOPLA0if flag clear, no play fm zero
413
414                          *We play a message from address zero
415
416   03B2   15 C0bclrMAKEIT0,R00clear the makit it zero flag
417   03B4   3F C2clrADDRL
418   03B6   3F C3clrADDRH
419   03B8
420   03B8   A6 E0lda#SETPLAYset up to play a msg with addr
```

```
421   03BA   CD 04 2EjsrADDADDRadd the address to it
422   03BD
423   03BD   CD 04 6BjsrSPI_16start the playback
424
425   03C0   1C 00bsetLOWBAT,portaturn on the LED
426
427   *Now fall through from starting at zero and send 8 more bits to continue play
428
429 *we really play the "next message"
430   03C2 NOPLA0
431   03C2   A6 F0lda#PLAYload for play with IAB bit set
432   03C4   CD 04 5EjsrSPI_8start the playback
433
434   03C7   1C 00bsetLOWBAT,portaturn on the LED
435
436   03C9   20 57READZbraREADXdebounce and leave
437
438 ************************************************************************
439   03CB
440
441
```

RECIT: This routine sends a SETREC opcode to the ISD33000 with an address of zero if the MAKIT0 bit is set. This causes record to start at address zero. If the MAKIT0 flag bit is not set, a record operation begins at whatever address is currently in the ISD33000's internal address pointer. While record is occurring, only the STOP push button will be recognized by the software.

An additional function is performed during the RECIT routine and before recording begins. If the MAKIT0 bit is not set, i.e., the internal address is to be used for record, then this address is read out of the ISD33000 using the SPIIN subroutine (which will be explained later). This address is stored in a set of registers[1] so that the PLAYLAST routine can make use of it. If the MAKIT0 bit is set, then a zero is stored in these registers.

```
442 ************************** Record Next Message **************************
443
444              *Record the next message . . . unless Go to Beginning has been pressed
445   03CBRECIT
446
447   03CB   06 C0 54brsetOPERATE,R00,READXcheck to see if already oper
448   03CE   16 C0bsetOPERATE,R00
449
450   03D0   13 01bclrPLAREC,portbPut the ISD2500 into Record
451   03D2   11 01bclrPD,portbPower up the ISD2500
452
453   03D4   05 C0 16brclrMAKEIT0,R00,NOREC0if flag clear, no rec from 0
454
455
456 *We record message from address zero
457   03D7   15 C0bclrMAKEIT0,R00clear the makit it zero flag
458   03D9   3F C2clrADDRL
459   03DB   3F C3clrADDRH
460
```

1. *Since the ISD33000 family uses an address longer than 8 bits, it takes two 8-bit registers to share the address. In the software, these registers are called RECADDL and RECADDH.*

```
*Also clear the "record next" address bytes


  03DD   3F C4clrRECADDL
  03DF   3F C5clrRECADDH
  03E1
  03E1   A6 A0lda#SETRECset up to record a message with addr
  03E3   CD 04 2EjsrADDADDRadd the address to it
  03E6
  03E6   CD 04 6BjsrSPI_16start the recording

  03E9   1C 00bsetLOWBAT,portaturn on the LED
  03EB
  03EB   20 04braNOREC1

*Now send 8 more bits to continue record

*we really Record the "next message"
  03EDNOREC0
  03ED   A6 70lda#READADR
  03EF   AD 4CbsrSPIINgo read the current addr before rec


  03F1NOREC1
  03F1   A6 B0lda#REC
  03F3   AD 69bsrSPI_8start the recording

  03F5   1C 00bsetLOWBAT,portaturn on the LED

  03F7   20 29braREADXdebounce and leave

*******************************************************************************
  03F9


```

STOPIT: This routine sends a STOP opcode to the ISD33000. This interrupts any operation in progress. If a record operation is interrupted, an EOM flag bit is stored in the device to mark the end of the message.

```
************************ Stop Recording or Playing ************************

 *Stop whatever we are doing . . . but don't corrupt the address register
  03F9 STOPIT
  03F9   A6 30lda#STOP
  03FB   AD 61bsrSPI_8stop the operation

  03FD   1D 00bclrLOWBAT,portaturn off the LED

  03FF   17 C0bclrOPERATE,R00turn off the "Operate" flag

  0401   10 01bsetPD,portbPower down the ISD2500

  0403   20 1DbraREADX


```

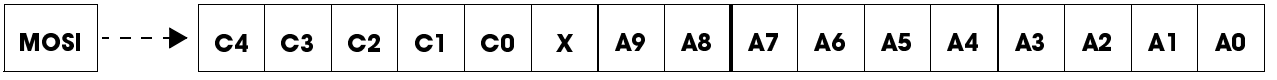
```
511 ********************************************************************************
512   0405
513
```

PLAYLAST: This routine retrieves the bytes that hold the address stored at the beginning of the last RECIT operation. It then sends a SETPLAY opcode and the address to the ISD33000 so that playback now begins at the address where the "last" recording started from.

```
514
515 ***************************** Play Next Message ****************************
516
517  *Play the last message we recorded
518   0405 PLAYLAST
519   0405   06 C0 1A brsetOPERATE,R00,READXcheck if we already oper
520   0408   16 C0 bsetOPERATE,R00
521
522   040A   12 01bsetPLAREC,portbPut the ISD2500 into Playback
523   040C   11 01bclrPD,portbPower up the ISD2500
524
525
526 *Go get the address we stored off just before we recorded (It's in
527 *RECADDH + RECADDL).  Put it in the address registers and GO!
528
529   040E   B6 C4ldaRECADDL
530   0410   B7 C2staADDRL
531
532   0412   B6 C5ldaRECADDH
533   0414   B7 C3staADDRH
534
535   0416   A6 E0lda#SETPLAYset up to play a message with addr
536   0418   CD 04 2EjsrADDADDRadd the address to it
537   041B
538   041B   CD 04 6BjsrSPI_16start the playback
539
540   041E   1C 00bsetLOWBAT,portaturn on the LED
541
542   0420   20 A0braNOPLA0Send 2nd command to set IAB bit
543
544 ********************************************************************************
545   0422
546
547
548 *after doing any and all the stuff,you arrive here to debounce the switches
549   0422   B6 00READXldaporta
550   0424   A4 9Fand#$9Fonly look at the push buttons
551   0426   26 FAbneREADXloop until the button is released
552
553 *OK, the button has been released
554   0428   CD 04 C7jsrTPBNgo wait for awhile
555   042B   CC 03 5Fjmp READ
556
557
558
```

559

ADDADDR Subroutine: Whenever we do any of the "SET" operations, we have to add a 10 bit address to the 5 bit ISD33000 opcode. The address starts with A0 in the LSB of the 16 bit word, with the opcode in the left-most 5 bits of the word. Graphically this looks like:

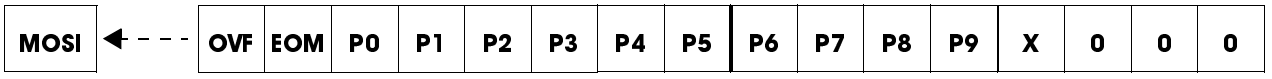


The two bytes to be shifted into the SPI port must be loaded such that the first bit shifted in is A0, the second is A1, etc. with the very last bit shifted into the SPI port being the C4 RUN bit. At that point the Slave Select pin will go HIGH to end the data input and start the operation as indicated by the bytes just shifted in.

In the ADDADDR subroutine, the accumulator brings in the opcode and the address is defined by the data in the ADDRL and ADDRH bytes. ADDRL contains A7–A0 and ADDRH holds A9 and A8 in the two LSB locations. This subroutine uses an AND and an OR operation to combine the opcode with bits A9 and A8 of the address and load SPIONE with this data. ADDRL is next written to SPITWO. SPIONE and SPITWO are the two byes that will be sent out of the SPI port of the micro.

```
560    ************************************************************
561    ************************************************************
562    *   SUBROUTINES START HERE!
563    ************************************************************
564    ************************************************************
565
566
567    ************************************************************
568    *SUBROUTINE ADDADDR
569    ************************************************************
570                       *This Subroutine adds the address to the control bits already
571                        *present in SPIONE. In doing so, it adds a second byte for
572                        *16 bit transfers into the ISD33000. This subroutine is
573                        *called with a control byte in the accumulator.
574
575   042EADDADDR
576   042E   B7 C6staSPIONEput the accumulator into SPI one
577
578   0430   B6 C3ldaADDRHget the upper byte of the address
579   0432   A4 03and#$03
580   0434   BA C6oraSPIONE
581   0436   B7 C6staSPIONE
582   0438
583   0438   B6 C2ldaADDRLGo get the lower byte
584   043A   B7 C7staSPITWO
585
586   043C   81rts
587
588
589
```

SPIIN Subroutine: This subroutine is used to read the address data out of the ISD33000 MISO pin before starting a record operation. This saves the "current address" so that a "play last record" operation is possible. Graphically the output side of the ISD33000 SPI port (MISO) looks like:



The OVF bit is presented to the MISO pin as soon as the Slave Select pin goes LOW. The first clock input to the ISD33000 SPI shifts the EOM to the MISO pin, and subsequent clocks shift the address data out, LSB first. Since we only read the MISO pin after the clock cycle, the OVF bit gets thrown away automatically. Note that the SHIFTIT routine (explained later) shifts the data into TEMPIN byte left to right. This causes the sense of the data to be inverted so that the EOM bit will be in the LSB position of the byte.

After the data is shifted out of the MISO pin, we are left with a byte holding P6–P0 plus the EOM bit and a second byte holding P9, P8 and P7. One more linked shift to the right of these two bytes dumps the EOM bit and positions the 10 bit address correctly for later use in the PLAYLAST routine.

It should be noted that whenever you read the ISD33000's SPI port data, you also are shifting data into the device. Accordingly, the calling routine must make sure the data written does not inadvertently start an unwanted operation, or interrupt an operation in progress. When SPIIN is called, the accumulator brings in the 5 bit opcode into the subroutine that is to be written to the MOSI port of the SPI. This routine assumes that an address will not be written into the SPI port at this time. Consequently the first byte written will be all zeros, followed by the second byte containing the opcode.

```
590                          ************************************************************
591 *SUBROUTNE SPIIN
592                          ************************************************************
593 * Read the SPI data from the chip, throw out the OVF and EOM
594 * bits, and store the address just retrieved in RECADDL and
595 * RECADDH. The accumulator comes in with the proper 5 bits
596 * of control so that nothing is disturbed.
597
598
599   043DSPIIN
600   043D   17 01bclrSK,portbMake sure the clock starts LOW
601   043F   15 01bclrSSBAR,portbDrop Slave Select
602
603   0441   B7 C6staSPIONESave the accumulator for later
604
605                           *we shift zeros in first
606
607   0443   3F CAclrTEMPput all zeros in temp
608   0445   AD 39bsrSHIFTIT
609
610   0447   B6 CEldaTEMPINget the data just shifted in
611   0449   B7 C4staRECADDL
612
613                           * note that EOM bit is still in RECADDL. We will
614                           * fix this later.
615
```

```
616   044B   B6 C6ldaSPIONEgo get the original accumulator
617   044D   B7 CAstaTEMP
618
619   044F   AD 2FbsrSHIFTITgo do the second byte
620
621
622 * TEMPIN now has upper 3 bits of the address in it. We will
623 * shift 1 of those bits into RECADDL. The last 2 bits remain
624 * in TEMPIN and this becomes RECADDH.
625
626   0451   34 CElsrTEMPIN
627   0453   36 C4rorRECADDL
628
629   0455   B6 CEldaTEMPIN
630   0457   B7 C5staRECADDH
631
632   0459   14 01bsetSSBAR,portbSlave Select goes HIGH to end
633                         *cycle
634   045B   19 01bclrSO,portbLeave this LOW when finished
635   045D   81rts
636
637
```

SPI_8 Subroutine: This subroutine is used to shift 8 bits into the MOSI pin of the ISD33000. The accumulator brings in the byte to be shifted. The SHIFTIT subroutine does the actual shifting of the data.

```
638                         ************************************************************
639 *SUBROUTNE SPI_8
640                         ************************************************************
641                          *SPI driver subroutine - outputs 8 bits. This routine sends
642 *the SPIONE byte out the bit banged SPI port.
643
644   045ESPI_8
645   045E   17 01bclr    SK,portb        Make sure the clock starts LOW
646   0460   15 01bclr    SSBAR,portb     Drop Slave Select
647
648   0462   B7 CAsta     TEMP
649   0464   AD 1Absr     SHIFTIT
650
651   0466   14 01bset    SSBAR,portb     Slave Select goes HIGH to end
652 *       cycle
653   0468   19 01bclr    SO,portb        Leave this LOW when finished
654   046A   81rts
655
656
```

SPI_16 Subroutine: This subroutine is used to shift 16 bits into the MOSI pin of the ISD33000. The SPITWO byte is shifted in first and the SPIONE bit is shifted in second. The SHIFTIT subroutine does the actual shifting of the data.

```
657                         ************************************************************
658                           *SUBROUTNE SPI_16
659                         ************************************************************
```

```
660                        *SPI driver subroutine - outputs 16 bits. This routine sends
661 *the SPIONE and SPITWO bytes out the bit banged SPI port.
662
663   046B SPI_16
664   046B   17 01bclr    SK,portb        Make sure the clock starts LOW
665   046D   15 01bclr    SSBAR,portb     Drop Slave Select
666
667   046F   B6 C7lda     SPITWO
668   0471   B7 CAsta     TEMP
669
670   0473   AD 0Bbsr     SHIFTIT
671
672   0475   B6 C6lda     SPIONE
673   0477   B7 CAsta     TEMP
674
675   0479   AD 05bsr     SHIFTIT
676   047B
677   047B   14 01bset    SSBAR,portb     Slave Select goes HIGH to end
678                          *cycle
679   047D   19 01bclr    SO,portb        Leave this LOW when finished
680   047F   81rts
681
682
683
```

SHIFTIT Subroutine: This subroutine does all the shifting of data into and out of the SPI port of the ISD33000. The TEMP register brings in the 8 bit data to be shifted out and the TEMPIN register brings data out of the routine. SHIFTIT talks directly to the ports of the microcontroller.

```
684 ************************************************************
685 *SUBROUTNE SHIFTIT
686 ************************************************************
687 *This subroutine shifts out 8 bits from the SPI Port
688
689   0480SHIFTIT
690   0480   A6 08lda#8
691   0482   B7 CBstaTEMP1put an 8 count into temp 1
692
693   0484   B6 CAldaTEMP
694
695   0486   44OUTAGNlsrashift the LSB into carry bit
696   0487   24 04bccOUTZERO
697
698   0489   18 01OUTONEbsetSO,portboutput a "1"
699   048B   20 02braCONTSPI
700
701   048D   19 01OUTZERObclrSO,portboutput a "0"
702
703
704 *Now toggle the clock to shift the data
705   048F   16 01CONTSPIbsetSK,portb
706   0491   17 01bclrSK,portb
707
708 *now look at incoming data
```

```
709
710   0493   0A 01 03brsetSI,portb,INONE
711   0496   98clcit's a 0, clear carry bit
712   0497   20 01braCONTIN
713
714   0499   99INONEsecit's a 1, set the carry bit
715
716   049A   36 CECONTINrorTEMPINbring the bit into the acc
717
718   049C   3A CBdecTEMP1
719   049E   26 E6bneOUTAGN
720   04A0
721   04A0   81rts
722
```

FLASH1 Subroutine: The FLASH1 subroutine blinks the LED once.

```
723                        ************************************************************
724                           *SUBROUTNE FLASH1
725                        ************************************************************
726                           *This subroutine flashes the LED once
727
728   04A1FLASH1
729   04A1   1C 00bsetLOWBAT,portaturn on the LED
730   04A3
731   04A3   A6 96lda#150
732   04A5   B7 CBstaTEMP1use 150 at the delay
733
734   04A7   AD 22bsrKEYDLYdelay
735   04A9   1D 00bclrLOWBAT,portaturn off the LED
736   04AB   81rts
737
738
739
```

FLASH2 Subroutine: The FLASH2 subroutine blinks the LED twice.

```
740                        ************************************************************
741                           *SUBROUTNE FLASH2
742                        ************************************************************
743                           *This subroutine flashes the LED twice
744   04AC                    FLASH2
745   04AC   1C 00bset    LOWBAT,porta    turn on the LED
746
747   04AE   A6 96lda     #150
748   04B0   B7 CBsta     TEMP1           use 150 at the delay
749
750   04B2   AD 17bsr     KEYDLY          delay
751   04B4   1D 00bclr    LOWBAT,porta    turn off the LED
752
753   04B6   A6 96lda     #150
754   04B8   B7 CBsta     TEMP1           use 150 at the delay
755
```

```
756   04BA   AD 0Fbsr     KEYDLY          delay
757   04BC   1C 00bset    LOWBAT,porta    turn on the LED
758
759   04BE   A6 96lda     #150
760   04C0   B7 CBsta     TEMP1           use 150 at the delay
761
762   04C2   AD 07bsrKEYDLYdelay
763   04C4   1D 00bclrLOWBAT,portaturn off the LED
764   04C6   81rts
765
766
767
```

TPBN Subroutine: This subroutine is used to generate delays in the program. Calling TPBN directly gives approximately a 1/4 second delay. KEYDLY can also be called as a subroutine. In this case, the accumulator brings in a variable that initiates a delay shorter than TPBN.

```
768 ************************************************************
769 *SUBROUTNE TPBN
770 ************************************************************
771 *USED FOR TIMING VARIOUS STUFF IN THE PROGRAM
772 *
773
774 *TPBN IS THE PUSH BUTTON DELAY IN PUSH BUTTON MODE
775   04C7A6 FA TPBNlda   #250    DELAY 250 MILLISECONDS (approx)
776   04C9   B7 CBstaTEMP1
777
778   04CB   B6 CBKEYDLYldaTEMP1(3)
779   04CD   27 0AbeqFINDLY(3)
780   04CF   3A CBdecTEMP1(5)
781
782
783
784                        ************************************************************
785                        *WAIT1    GENERATES A DELAY (1.154 mSEC)
786                        ************************************************************
787 *WAIT1 GENERATES A 1.154 MILLISECOND DELAY.  IT DOES NOT DISTURB THE
788 *ACCUMULATOR. FROM A BSR (CALLING THIS ROUTINE) THROUGH THE RTS (ENDING
789 *THIS ROUTINE, IT TAKES 2065 CYCLES x 4.3656 uSEC = 1.154 MSec. THIS THING
790                          *LOOPS 256 TIMES.
791
792   04D1   3F CC WAIT1clrTEMP2(5)
793   04D3   3C CC WAIT2incTEMP2(5)
794   04D5   26 FCbneWAIT2(3)
795
796   04D7   20 F2bra KEYDLY(3)
797
798   04D9   81FINDLYrts
799
800
801
802 *
803
```

```
804
805
806
807
808
809 * NOTE: THE LAST USABLE ADDRESS IS $7CF
810
811
812
813
814
815
```

Push Button Operation Notes

```
816       *Instructions:
817       *Six of the 9 push-buttons are labeled on the PCB. Pushing the Yellow
818       *"Go_to_Beg" button will reset the address pointer to the front of the
819       *chip or address 000. The indication that this has been done will be a
820       *double flash of the LED, D11, in the bottom left corner of the PCB.
821       *
822       *Pushing the Red "Record" button will turn on the Red LED to indicate
823       *that the chip is now recording anything it hears at the microphone M1
824       *near the top center of the board. The board will continue to Record
825       *until the end of the chip is reached or the Black "Stop" button is pressed.
826       *At that time the LED will go out and the board will stop Recording.
827       *
828       *Pushing the White "Play_Last" button will playback what you have just
829       *recorded. This message will play through to its end or stop when you
830       *press the Black "Stop" button
831       *
832       *Pushing the Yellow "Go_to_Beg" button, and then the White "Play_Next"
833       *button will play messages from the beginning of memory through to its
834       *end or stop/pause when you press the Black "Stop" button. To resume
835       *playback push play-next again if playback is paused. To play the next
836       *message press play next again.
837       *
838       *The Blue "Skip_to_Next" button will let you bypass a message and play
839       *the one after that message. For example, had you recorded three messages,
840       *beginning at the front of the chip, and gone back to the beginning after
841       *the last message then you could press the White "Play_Next" button to play
842       *message #1, press the Blue "Skip_to_Next" button to bypass message #2 and
843       *then Press the White "Play_Next" to play message #3.
844
845
846
846
```

Cross Reference Listing

```
Defined Symbol NameValueReferences
575 ADDADDR 042E     243 309 381 421 468 536
158 ADDRH   00C3     240 292 376 418 459 533 578
157 ADDRL   00C2     239 291 375 417 458 530 583
Pre CODE    00C0     195
716 CONTIN  049A     712
705 CONTSPI 048F     699
```

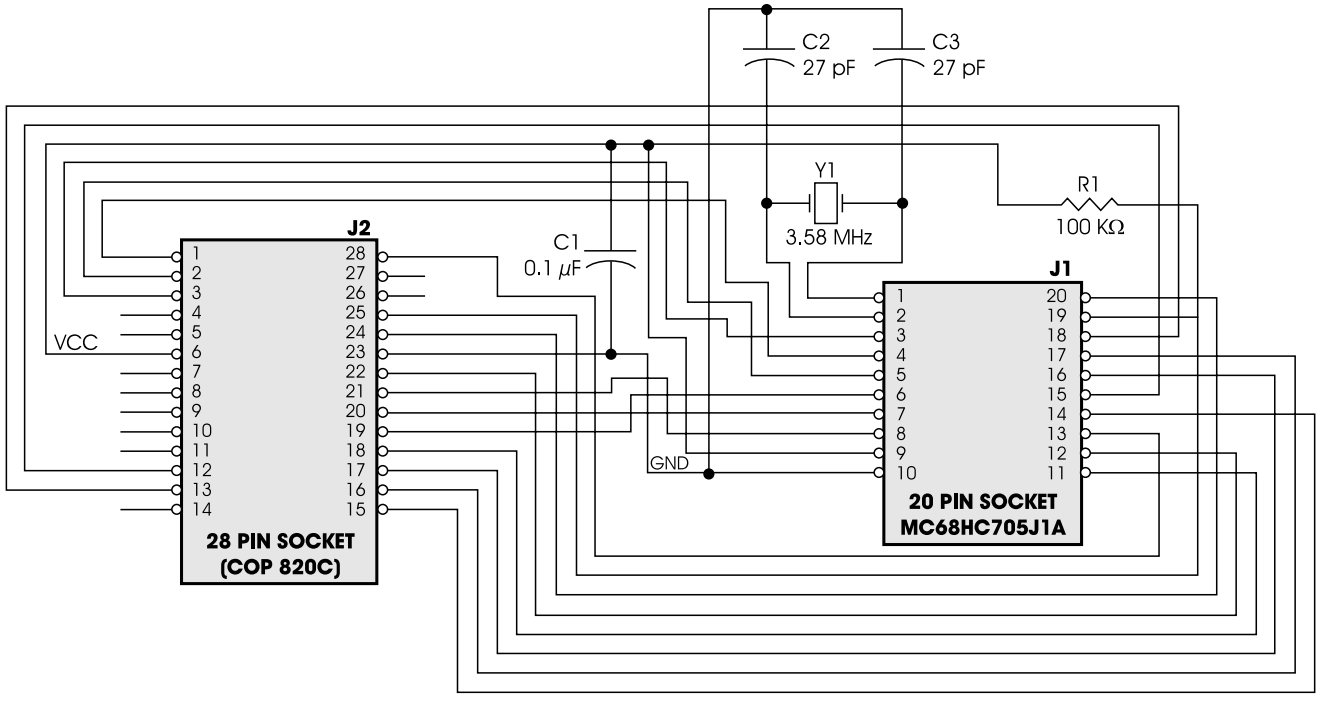
```
120 COPR    =  07F0
Pre DATA    0000
177 DDR     =  0004     270 272
251 ENDINT  0323     234
171 ENDREG  00CF
798 FINDLY  04D9     779
728 FLASH1  04A1     313 378 391
744 FLASH2  04AC     352
347 GOTOBEG 0373     334
714 INONE   0499     710
116 ISCR    =  000A
 97 IntVects=  07F8     103
778 KEYDLY  04CB     734 750 756 762 796
 57 L1      =  0003     337
 54 L2      =  0000     334
 58 L4      =  0004     338
 55 L5      =  0001     335
 56 L6      =  0002     336
 61 L7      =  0007     339
 60 LOWBAT  =       0006    223 425 434 472 488 503 540 729 735 745
    751 757 763
134 MAKEIT0 =  0002     349 369 373 412 416 453 457
185    MC=  00F8393
119    MOR=  07F1
804    MSGTABL04DA
390    NOCUE0 039C369
430    NOPLA0 03C2412 542
479    NOREC0 03ED453
484    NOREC1 03F1474
135    OPERATE =0003224 348 367 406 407 447 448 505 519 520
695    OUTAGN0486719
698    OUTONE 0489
701    OUTZERO048D696
Pre    PAGE00000
 69    PD=  0000221 410 451 507 523
117    PDRA=  0010287
118    PDRB=  0011289
 70    PLAREC=  0001409 450 522
186    PLAY=  00F0431
132    PLAYING=  0000
518    PLAYLAST0405361
360    PLAYLASX0380339
405    PLAYNXT03A6336
178    POWRERUP=  0020305 308
806    PTTABL04DA
130    R0000C0224 290 348 349 367 369 373 406 407 412
    416 447 448 453 457 505 519 520
141    R0100C1
 59    RAC=  0005
333    READ035F341 555
188    READADR=  0070480
549    READX0422406 436 447 490 509 519 551
436    READZ03C9348 354 367 387 396
183    REC =  00B0485
160    RECADDH00C5294 465 532 630
159    RECADDL00C4293 464 529 611 627
```

```
133    RECDING=  0001
445    RECIT03CB337
187    RINT=  0030
 94    RamArea =  00C0128
 96    RomArea=  0300197
163    SEQCNT00C8
184    SETMC=  00E8380
182    SETPLAY=  00E0242 420 535
179    SETREC                          =  00A0     467
689    SHIFTIT                            0480     608 619 649 670 675
 74    SI                              =  0005     710
 72    SK                              =  0003     600 645 664 705 706
366    SKIP2NXT                           0383     335
 73    SO                              =  0004     634 653 679 698 701
599    SPIIN                              043D     481
161    SPIONE                             00C6     576 580 581 603 616 672
162    SPITWO                             00C7     584 667
663    SPI_16                             046B     245 311 384 423 470 538
644    SPI_8                              045E     227 249 306 394 432 486 501
 71    SSBAR                           =  0002     601 632 646 651 665 677
181    STOP                            =  0030     226 248 500
499    STOPIT                             03F9     358
357    STOPITX                            037D     338
319    STOPPIT                            035F
180    STOPPWRDN                       =  0000
156    STRTREGS                           00C2
 95    StkTop                          =  00FF
115    TCR                             =  0009
165    TEMP                               00CA     295 607 617 648 668 673 693
166    TEMP1                              00CB     691 718 732 748 754 760 776 778 780
167    TEMP2                              00CC     792 793
169    TEMPIN                             00CE     610 626 629 716
168    TEMPOUT                            00CD
200    TIMESVC                            0300     104
164    TOFCNT                             00C9
775    TPBN                               04C7     229 554
114    TSCR                            =  0008     300
269    USER                               0324
792    WAIT1                              04D1
793    WAIT2                              04D3     794
220    extsvc                             0302     105
 51    porta=0000  223 270 280 334 335 336 337 338 339 425
    434 472 488 503 540 549 729 735 745 751
    757 763
 52    portaDDR                        =  0040     269
 66 portb   =      0001    221 272 284 409 410 450 451 507 522 523
    600 601 632 634 645 646 651 653 664 665
                                                  677 679 698 701 705 706 710
 67    portbDDR                        =  001F     271
267    reset                              0324     107
209    swisvc                             0301     106
Lines Assembled :  846            Assembly Errors :  0
```

APPENDIX

Figure 1 is used to adapt the COPS socket on the ISD-ES302 demo board to the Motorola MC68HC705J1A microcontroller. Plug J2 plugs into the COPS socket and the Motorola MC68HC705J1A plugs into the J1 socket. Also, R7 (4.7 Ω), which connects to the Interrupt output of the ISD33000, must be shunted with a 1N914 signal diode with the cathode toward the ISD chip. The Motorola microcontroller cannot see interrupts unless this is done.

Figure 1: Adapter Board Schematic



SERIAL INTERFACE PRODUCTS

Message Management in the ISD33000 Series

Many types of products for sound record and playback require message management capabilities. They need to be able to record, play or erase an individual message as needed. Some technologies are not well suited for this, such as magnetic tape-based recording systems which are unable to erase a message in the tape's middle then reuse during a new random length recording. Because of message management features built into the ISD33000 SPI-controlled record and playback IC these problems are eliminated.

MESSAGE MANAGEMENT RECORD

In a typical application, several messages are initially recorded into the chip in sequence, for example: Message #1, Message #2, Message #3, and Message #4. Since the ISD33000 device is able to read back the internal message pointer at the conclusion of each recording, a simple message address table is constructed to save the address location of each message in a separate digital, nonvolatile memory. A specific message, number three, for instance, may be selected and played back when needed.

A more usual application of message management is deleting nonconsecutive messages and reusing the space for future recordings (for example deleting messages one and three). Because of the message address table earlier constructed, the device is aware of the beginning and ending of each message previously recorded. During record the End Of Message (EOM) flags that mark these messages are not accessible; these flags are used only during playback. The recording process erases any EOM previously written at the end of a message. An alternative method is therefore needed to determine that the end of old messages (messages one and three) is found in real-time during recording. Once at the end of these messages the device needs to "jump" to a new address space without losing any analog data. The following explain how this is accomplished.

Two special message addressing features are built into the ISD33000 device: the Row Address Clock (RAC) output as well as a special mode included in the address management logic of the chip. To understand how these features work, it is first necessary to understand the memory architecture of the device.

The ISD33000's memory consists of a number of rows of memory cells, each row consisting of 1200 columns. When addressing the device, select the start of a row to begin record or playback. It is not possible to address inside a row. All operations in a row begin at column 1. For example, in the 8 KHz sample rate device, the ISD33120, samples are taken at an interval of 125 μs (consult the ISD33000 data sheets for the timing of other members of the family). Thus, 125 μs times 1200 columns per row, then each row contains 150 ms of sound. That defines the address resolution of this device at 150 ms and each record or playback cycle begins at the start of these 150 ms "blocks" of audio memory. The ISD33120 has 800 rows of memory and therefore (800 x .150) 120 seconds total memory.

The RAC pin of the ISD33000 series indicateS that record or playback is near the end of a row of memory. Using the ISD33120 as an example, the RAC pin goes LOW 12.5 ms before the end of each row and goes back HIGH exactly at the end of each row. It therefore becomes a "row clock" which determines where the device is in memory during record or playback operations. This is a slow clock, with a period of 150 ms (in this example). In a microcontroller environment it is relatively easy to use software polling of the RAC pin to determine when the end of each row has been reached.

In the message example above, the length of Message #1 and #2 are known and therefore the number of rows in each message space is easily computed. If Message #1 is *n* rows long, simply count *n* – 1 rows and employ the second message management feature built into the ISD33000.

After *n* – 1 RAC cycles and after the RAC pin has returned to HIGH, the device is now recording on row *n*, the last available row in this block (the old Message #1 space) of memory. Once recording begins on a row, it is now possible to utilize the second major message management feature of the ISD33000 family: a forced address jump. In the example, recording a new message continues after using up the space previously taken up by the old Message #1. To jump to the beginning of the next available address space (the beginning of old Message #3), without losing Message #2, carry out the following sequence:

1. RAC goes HIGH after *n* – 1 RAC cycles. Indicating that we are now recording on the last row of the old message #1 address space.
2. A new SPI addressed record cycle is initiated with the IAB bit LOW. The address is the location of old Message #3's beginning. Since recording is already under way, this operation will be ignored until the end of the current row.
3. The final falling edge of the RAC signals the end of the last row of the old Message #1 is near. When the RAC pin returns to HIGH, recording continues at the new address with no loss of audio samples.
4. While recording proceeds, the microcontroller controlling the operation must erect a message address table describing the location of each segment of the now-fragmented message.
5. At this time another SPI control cycle is sent to the ISD33120 device with the IAB bit set HIGH. This causes recording to continue in sequence through the old message three space.
6. If recording continues long enough so that all of the old Message #3 space is used up, a new address must be input so that recording can continue at the appropriate place after Message #4.
7. When recording ends, a SPI STOP command causes an EOM bit to be set indicating the end of the current message.

MESSAGE MANAGEMENT PLAYBACK

Playback of this new message proceeds in the same manner as record. The message address table is used to calculate where and when each jump occurs during playback. Only one EOM will be set in the entire fragmented message space to indicate the final end of this message.

MESSAGE ADDRESS TABLE

The Message Address Table (MAT) is an important part of the message management structure. This table keeps track of the beginning address of each message as well as the beginning and ending address of each fragment of a message. Additionally, a more sophisticated MAT may also contain information about message numbers, message order and other factors such as whether or not the message has been listened to since it was recorded.

The MAT may be structured in a variety of ways. For example, every row of the ISD33000 device may be treated as an independent block of memory with an entry in the MAT to indicate it's relationship to the various messages stored in the device. This may require more memory than practical, however, as the members of the ISD33000 series have 400 to 800 rows of memory storage. Tracking 800 rows not only requires 800 memory locations in the MAT, but also a digital word larger than 8 bits. Consequently, such a MAT might need as many as 1600 digital bytes, which may not be cost effective in some applications.

It is more practical to work with multiple rows serviced together as a single, larger, memory block. An ISD33120 segmented into 100 blocks, each 8 rows long, could be serviced by a MAT as small as 100 bytes. The following discusses one method of accomplishing this.

THE MESSAGE ADDRESS TABLE—AN EXAMPLE

The ISD33120 requires 10 bits to address any of its 800 rows of memory. Assume that each sequential 8 row block of memory is addressed as a single block, the lower 3 bits of memory are not needed. They are always zero. Now, only 7 bits of address are required to access any of 100 blocks in the message memory of the device. In this example each block is 0.8 seconds long.

The MAT in this example is a memory stack of 100 bytes where each byte may be associated with one of the blocks of memory in the ISD33000 device. As messages are recorded and erased, the specific association may change. How this works will become more apparent later in this section.

The data in the MAT memory byte either indicates no association with a block of memory or the status of a specific block of memory in the ISD33000 device. Bit 7 of each MAT memory byte has a special function. A "1" in this bit indicates that this byte points to the first block of memory in a message. The remaining 7 bits of each byte contain the address of one of the blocks of memory. There are four possibilities:

1. The data in the byte is all zeros (0000 0000). This indicates that there is no association with any memory block in the ISD33000.
2. The data in the byte has a "1" in bit position 7 (the MSB) and a seven bit address in bits 0–6 (1xxx__xxxx). The 1 in bit position 7 indicates that this is the first block of a message. The seven bit address points to the location of the first block of memory in the message.
3. The data in the byte has a "0" in bit position 7 and a valid seven bit address in bits 0–6 (0xxx xxxx). The 0 indicates that this is not the first block of a message in memory. The valid seven bit address points to the current block of memory in the message.
4. A special case of number two above occurs when addressing the first block of memory in the ISD33000 device. By convention, the first block of memory will always be the start of a message. As proven in this example, this is always the case. The data in the byte has a "1" in bit position 7 and all "0"s in the rest of the byte (1000 0000).

BUILDING THE MAT

While recording several messages, the MAT will be built from the top of the table, down, as space in the ISD33000 is consumed. One byte of the MAT is employed as each block of memory in the IC is used. Bytes associated with a single message in the MAT will always be sequential. The block addresses in a single message made up of multiple MAT entries will always be in numerical order but may not be sequential.

After recording and erasing a number of messages, an example MAT might look like Table 1.

This memory currently holds four messages of varying lengths. Notice that Message #1 is composed of blocks 5, 6 and 9, and Message #2 of blocks 2 and 8. This 100-byte MAT applies only the first 12 bytes and leaves the remaining 87 bytes filled with zeros.

Table 1: MAT Example

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg No.
1000 0101		1	000 0101	5	
0000 0110		0	000 0110	6	One
0000 1001		0	000 1001	9	
1000 0010		1	000 0010	2	Two
0000 1000		0	000 1000	8	
1000 1010		1	000 1010	10	
0000 1011		0	000 1011	11	Three
0000 1111		0	000 1111	15	
1000 0111		1	000 0111	3	
0000 1100		0	000 1100	4	Four
0000 1101		0	000 1101	7	
0000 1110		0	000 1110	14	
0000 0000 (87 bytes follow, all zeros)					

PLAYBACK ALGORITHM

To demonstrate the playback algorithm, Message #3 will be played back. The microcontroller controlling the system begins at the top of the MAT and searches down for bytes with bit 7 set to a "1." In this playback example, the microcontroller will stop on the third occurrence of this condition, pointing at the first pointer byte for Message #3. From this byte, the microcontroller knows that block 10 is the beginning block of ISD33000 memory for Message #3. The playback of Message #3 starts with block 10 being addressed through the SPI port. Once playback of the message commences, a second SPI cycle is input without an address and the IAB bit set so that playback will continue sequentially through the 8 rows of memory in this first message block.

NOTE *An easy way for the microcontroller to compute the address for the ISD33000 is to first clear bit 7, if set then load the block address into a register and shift left 3 bits with "0" shifted into the LSB bit position. As bits are shifted out of the MSB bit position, they need to be saved in a second byte. The original 7-bit address will now be a 10-bit address that may be used to start message playback.*

While the current block of the message plays back, the microcontroller now starts polling the RAC pin of the ISD33000. This pin has the same period as one row of memory of the device, that is, 150 ms in the ISD33120. The RAC pin goes LOW for the last 12.5 ms of each row. It's high-going edge is synchronous with the end of the current row. The microcontroller polling, therefore must be fast enough to "catch" the RAC pin while it is in the LOW state. The microcontroller must count seven complete RAC cycles, at the conclusion of the seventh RAC cycle, the ISD33000 is playing back the last row (the eighth row) in the current block.

When the eighth row of the block starts playing back, the microcontroller must return to the MAT and pull the next byte from the table. In the case of Message #3, the next MAT byte is 0000 1011. This indicates that the next block to be played is 11. Since playback has already begun on the last row of the block, the SPI may now input data as if to begin a new playback at the new address, that is, the address of block 11. This new SPI cycle does not have an immediate effect. The new address is buffered up awaiting the end of the row.

In this specific case, playback continues to the next sequential block in the ISD33000 device, and hence, the next sequential row in the memory of the device. It is possible to design a "smart" algorithm which detects playback (or record) proceeding in sequence from block to block and to ignore this SPI cycle. This is not explained in this section.

When playback reaches the end of this last row of the first block of Message #3, it automatically jumps to the first row of block 11 and continues recording without losing a sample. When playback reaches this point, (after the start of row 1 of block 11), it is again necessary to input a second SPI playback cycle without an address and with the IAB bit set to 1. This causes playback to proceed sequentially through the 8 rows of block 11.

When row 8 of the second block is reached, another SPI cycle inputs the address of the third and final block of the message. MAT shows that this is block 15. As with the first and second block of the message, input an immediate second SPI cycle to set the IAB bit.

Playback is now proceeding through the third and final block of Message #3. Since this is the last block of the message, assume that an EOM bit is set in one of the block's 8 rows. When the EOM bit is encountered, an EOM interrupt occurs and playback ends. If this is not the case, the message was improperly recorded or this is the last row in the ISD33000's memory and playback was terminated with an overflow interrupt.

A third special case situation may exist: the message may stop at the end boundary with a completely full block. If this occurs, then the microcontroller will go to the MAT a fourth time and read a byte of data. The data it reads shows the start of a new message (bit 7 = 1) and a block address of 7. When the message start flag is detected, however, the microcontroller assumes that this must be the end of the message and does not input a new SPI cycle. The message ends with an EOM interrupt to signal that the message is finished.

If the last message in the MAT table is being played and the above situation occurs, the microcontroller will read an all-zero byte. It will treat this situation the same as in the above paragraph: that this is the end of the message.

The software in the microcontroller must also be intelligent enough to know when the 100th byte of the MAT is being read. In this record/playback algorithm demonstrates that this block must be the end of a message.

Cascaded ISD33000 devices are not covered in this example. In a cascade application, a bit (or bits) in the MAT are reserved to indicate which ISD33000 device contains which block of memory.

RECORD ALGORITHM

To demonstrate the record algorithm, we record a new message, Message #5, and assume there is a current MAT that looks like Table 2.

When recording begins, the microcontroller must find an unused block in the ISD33000 device. There are a number of ways to accomplish this. The easiest is for the microcontroller to start with block zero and search through the MAT to see if that block is already in use. If zero is already in use, it then searches for block 1 and does the same test, then block 2, and so on. When an unused block is located, recording begins on that block in the ISD33000.

Table 2: New Entry in MAT Message

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg. No.
1000 0101		1	000 0101	5	One
through					
0000 1101		0	000 1101	7	Four
0000 1110		0	000 1110	14	
1000 0000		1	000 0000	0	Five
0000 0000					
(86 bytes follow, all zeros)					

In the demonstration example, according to the MAT, block zero is available. The microcontroller starts recording at block zero by executing an SPI record cycle to the correct address (in this case, the address is zero). Recording begins immediately at the end of the SPI cycle. As in playback, a second SPI cycle must now immediately be input without an address and with the IAB bit set so that recording will proceed sequentially through the rows of block zero.

At the same time, the microcontroller must create a new entry in the MAT for Message #5. Since the message starts at block zero, the new MAT byte will be 1000 0000. Table 2 shows this new entry for Message #5.

After the new MAT table entry is entered, the microcontroller begins looking for another unused block of memory. A smart algorithm "remembers" that a search through the memory to the point where the first unused block was found already occurred. The algorithm begins at this point (block 1 in this example) and seeks the next unused block (block 1).

As in the playback algorithm, the microcontroller must count RAC cycles to determine when the eighth row of the block is reached. After recording on the eighth row starts (at the end of the seventh RAC cycle), the microcontroller enters a new SPI record cycle to record at block 1. When the row ends, recording will continue without stopping through to block 1.

Since recording has continued into the second message block, the microcontroller builds another MAT table entry and locates another available memory block. Table 3 shows the new MAT table entry. Referring back to Table 1 and remembering that blocks 0 and 1 were already used, the next available block must be 12.

Table 3: New MAT Table Entry

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg No.
1000 0101		1	000 0101	5	One
through					
0000 1101		0	000 1101	7	Four
0000 1110		0	000 1110	14	
1000 0000		1	000 0000	0	Five
0000 0001		0	000 0001	1	
0000 0000					
(85 bytes follow, all zeros)					

Two more blocks are recorded and then a STOP command is executed. The STOP command causes an EOM bit to be written into the ISD33000 memory. The MAT will resemble Table 4 when recording Message #5 is complete.

Table 4: Using the STOP Command

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg No.
1000 0101		1	000 0101	5	One
through					
0000 1101		0	000 1101	7	Four
0000 1110		0	000 1110	14	
1000 0000		1	000 00000		
0000 0001		0	000 0001	1	Five
0000 1100		0	000 1100	12	
0000 1101		0	000 1101	13	
0000 0000					
(83 bytes follows, all zero)					

ERASING A MESSAGE

To erase a message remove that message's entry from the MAT. For example, to erase the recently recorded Message #5 simply change its four table entries to all zeros.

It is more complicated to erase Message #3. Please refer to Table 1. Message #3 uses 3 bytes in the MAT to describe the location of its three message blocks of storage space. These 3 bytes are (from the top down) sequentially the sixth, seventh, and eighth bytes of the MAT stack. To erase Message #3, shift all the bytes in the stack below this message up three places, writing over the 3 bytes that used to refer to Message #3. Still referencing Table 1 after this action is complete, a new Message #3 composed of the MAT stack bytes that were Message #4. Message #3 has disappeared from the MAT and thus was "erased."

Table 5 demonstrates what the original Table 1 looks like after Message #3 is erased.

REORDERING MESSAGES

An additional advantage to this message management system is that the message order can be reordered by system requirements as needed. Again referring to Table 5, it is easier to interchange Message #1 and Message #3. To accomplish this, perform the following sequence:

1. Copy the three bytes of the Message #1 pointer to a temporary stack.
2. Shift all bytes of the MAT down 1 byte.
3. Copy the 4 bytes of the Message #3 pointer into the first 4 bytes of the MAT.
4. Copy the 3 bytes of the old Message #1 from its temporary stack to the location in the MAT below Message #2.
5. Message #1 has become Message #3 and vice versa.

The new MAT looks like Table 6.

Table 5: Erasing Messages

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg No.
1000 0101		1	000 0101	5	
0000 0110		0	000 0110	6	One
0000 1001		0	000 1001	9	
1000 0010		1	000 0010	2	Two
0000 1000		0	000 1000	8	
1000 0111		1	000 0111	3	
0000 1100		0	000 1100	4	Three
0000 1101		0	000 1101	7	
0000 1110		0	000 1110	14	
0000 0000 (90 bytes follow, all zeros)					

Table 6: Reordering Messages

Message Add. Table (MAT)	=	Bit 7	Block Address	Block Add (dec)	Msg No.
1000 0111		1	000 0111	3	
0000 1100		0	000 1100	4	One
0000 1101		0	000 1101	7	
0000 1110		0	000 1110	14	
1000 0010		1	000 0010	2	Two
0000 1000		0	000 1000	8	
1000 0101		1	000 0101	5	
0000 0110		0	000 0110	6	Three
0000 1001		0	000 1001	9	
0000 0000 (90 bytes, follow, all zeros)					

CONCLUSION

This Application Note has shown an easy method of message management in the ISD33000 voice playback and record integrated circuit. The ability to record, play or erase an individual message as required has been demonstrated. Additionally, messages can be reordered as needed by the application requirements.

ChipCorder®
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SERIAL INTERFACE PRODUCTS

A "C" Language Source Code Example to Use with the ISD33000 Series

This applications note provides an example to end-users of how to use the supplied memory management algorithm (please see the section "Device Operation" for a more detailed discussion of this algorithm) to effectively manage the ISD33000 device's memory. This program is written in "C" language and compiled for use on the 68HC705-C8A microcontroller. Only the play and record functions are detailed here. The complete software "C" language source code for the ISD-ES301 Evaluation Board is available on ISD's web-site at www.isd.com.

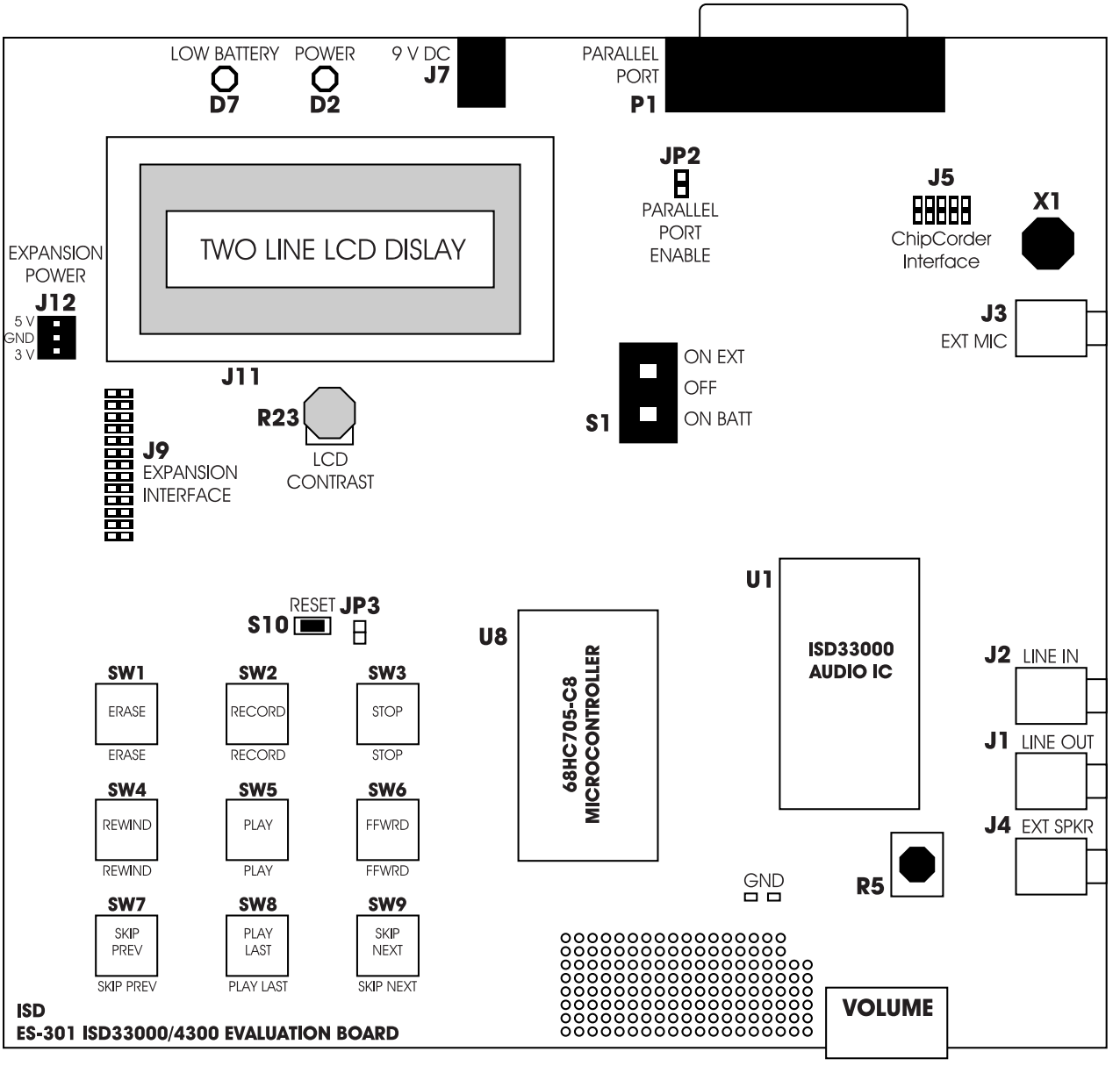
The ISD-ES301 is an evaluation and demonstration system which provides the user with the tools needed to evaluate ISD33000 analog ICs. This board can also function as a complete stand alone demonstration system. Some of the features incorporated in the software are; fast forward, rewind, skip to next message, skip to previous message, erase the current message, play, record and stop/pause a message.

The ISD-ES301 provides the following capabilities:

- Application development using the ISD33000 products
- User development of software for controlling the ISD33000 products
- Solder-in area on board for prototype installation
- Turn-key software for the Motorola microcontroller (68HC705-C8)
- Connection for SPI interface to off-board microcontroller

Figure 1, a board layout diagram, details the features of the ISD-ES301 accessible to or of importance to the user. The following Table 1 contains an alphabetical listing describing each of these features.

Figure 1: ISD-ES301 Front Panel



ISD-ES301 BOARD DESCRIPTION

The Table 1 lists all the features of the ISD-ES301 Audio Evaluation/Demo Board.

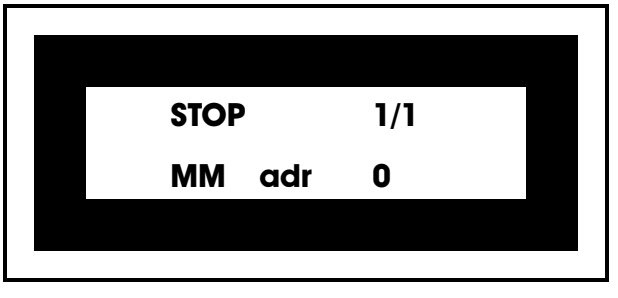
Table 1: ISD-ES301 Demo Board Feature

ID	Name	Description/Function
J1	Line Out	Direct Audio output of ISD33000 AUDOUT pin.
J2	Line In	Connection to ANA IN of ISD33000.
J3	Ext Mic	Connection for an external microphone.
J4	ext SPKR	Connection for an external speaker.
J5	chipcorder interface	Interface for external ChipCorder controller board.
J9	expansion interface	Connection for an external development board.
J11	two line lcd display	Two line LCD display for stand alone operation.
J12	expansion power	Test Points for 3 V, 5 V, and Ground
P1	parallel port	Printer cable connection to PC LPT1 port for PC operation.
R5	SCREW DRIVER ADJUST POT	Audio volume control.
R23	SCREW DRIVER ADJUST POT	LCD contrast control switch.
S1	Power switch	Power selection switch. [External Power or Internal Battery.]
S10	reset	Resets microcontroller (only).
SW1-9	keypad	Push-Button keys that make up the on board keypad.
U1	REMOVABLE ic socket	ChipCorder installation socket.
U8	microcontroller	68HC705-C8 microcontroller.
X1	Microphone	On board microphone.

MESSAGE MANAGEMENT EXAMPLE

Firmware written for the 68HC705-C8A microcontroller explains how to control the ChipCorder. The 68HC705-C8A interfaces to the ISD33000 device control I/O using the 68HC705-C8A SPI interface, interrupt, and I/O ports. A user interface consisting of nine push buttons and an LCD display is also supported by the firmware. When memory management mode is selected, the letters "MM" are displayed at the beginning of the lower line on the LCD display as shown in Figure 2.

Figure 2: Memory Management Mode



The LCD will display the following information on the first line:

- Status information such as play, record, pause, fast forward, rewind, and stop (shown)
- Number of messages in chip (1/1)
- Current message number being played (1/1)

The LCD will display the following information on the second line (messages use the entire line):

- Current Location in chip (adr 0)
- Chip overflow ("OVERFLOW")
- End of message reached ("END OF MESSAGE" or "NO MORE MESSAGES")

KEYPAD PUSH-BUTTON DESCRIPTION

The following lists the functionality of each push-button in the order they appear on the board, left to right, top to bottom.

ERASE

Erases one message at a time, starting with the last recorded message.

RECORD

In the memory management mode, pressing RECORD begins recording a new message at an address determined by the memory management system.

STOP (PAUSE)

If a message was playing, pushing this button will cause the current message to pause/stop. During record this button stops the recording process.

REWIND

In the memory management mode, REWIND decrements the row address counter 16 rows from the currently selected message.

PLAY

In memory management mode, playback begins at the "next" message in sequence. Play also resumes playing if PAUSE was previously selected.

FFWRD

In the memory management mode, FFWRD (fast forward) increments the row address counter 16 rows from the currently selected message.

SKIP PREV

In memory management mode, skips to the previous message.

PLAY LAST

Starts playing back from the beginning of the last played message, last recorded message, or last paused message.

SKIP NEXT

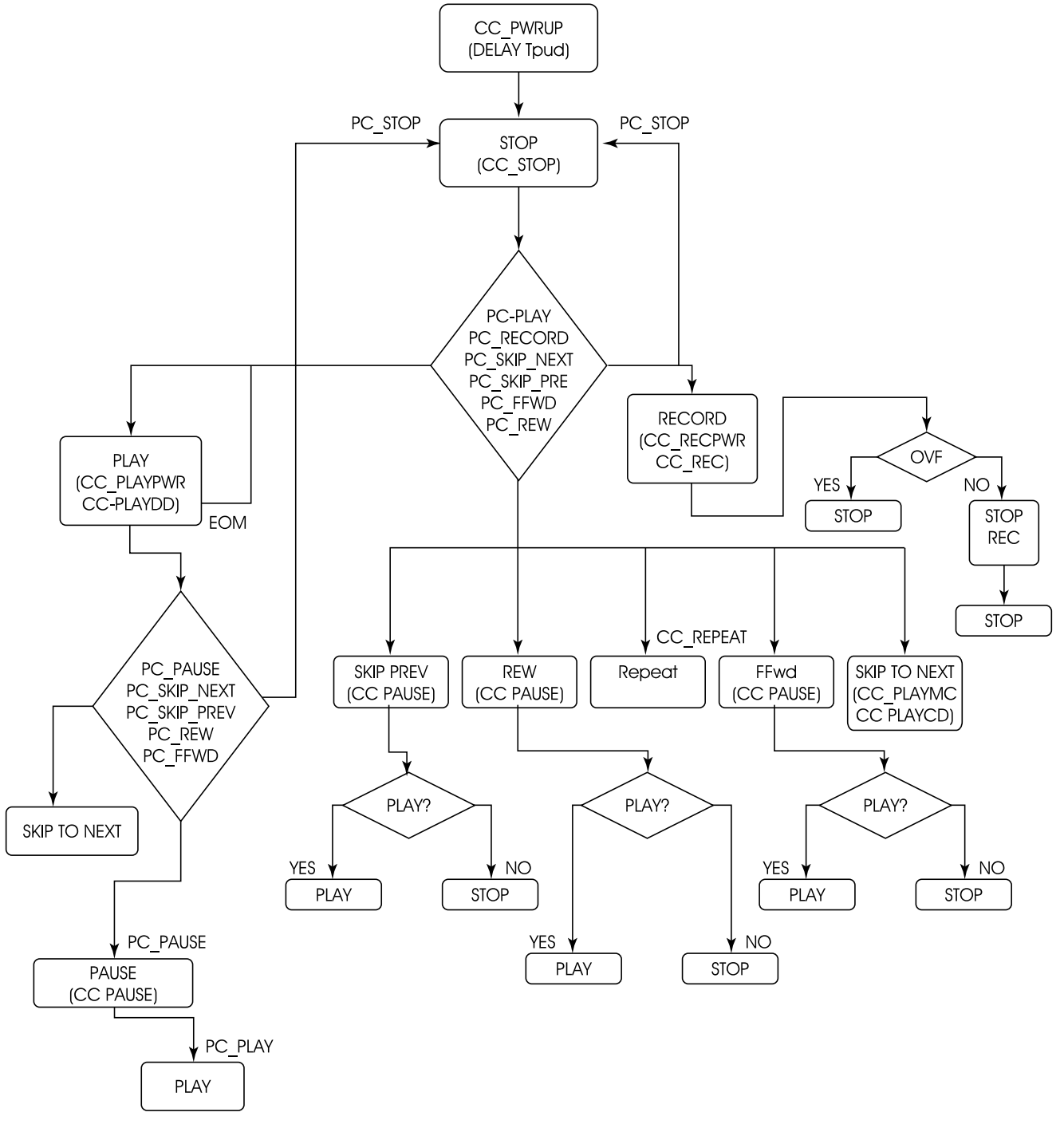
In memory management mode, skips to the next message. In manual mode, increments the row address counter 10 rows.

MEMORY MANAGEMENT MODE

This mode uses an algorithm (see "Message Management in the ISD33000 Series") which maintains a flexible message structure enabling messages to be re-recorded with different lengths while not affecting messages currently stored in the ChipCorder memory. This message structure is only maintained while the ISD-ES301 is powered up. In memory management mode the current address of the ISD33000 is updated every 16 memory rows at a time during record or playback operations. Current message number being played and the number of messages in the chip are displayed as well. Turning off power will erase the memory structure.

Figure 3 was used to write the demonstration software.

Figure 3: Push Button Control Flow Chart



```
/*----Initialize the memory address table----*/
  for ( index = 0; index < MAT_SIZE; ++index )
    MATEntry[index].All = 0x00;
   /*-----Initialize the mat structure variables-----*/
   MATStruct.EndPointer = -1;
   MATStruct.Index = 0;
/*--------------------All functions associated with Play-------------*/
void
StartPlayMessage( void )
{
   char tempStatus[ 9 ];
    /*-----if play is already running, don't re-spawn it-----*/
   if ( IsTaskRunning( RunPlayMessage ) )
      return;
   /*-----power up the isd chip-----*/
   PowerUp();
   /* ------System is in the memory management mode------ */
   {
      if ( !SystemData.NumberOfMessages )
      {
         /*----there are no messages yet in memory----*/
         SystemData.ErrorMessage ="NO MESSAGES     ";
         return;
      }
      /*----initialize reading of RAC----*/
      ReadRAC();
      /*----If the last key pressed was stop or repeat, need to
       get the BOM address,   otherwise just use the address
       in memory MemoryManagementData.Address----*/
      if ( ( KeyStatus == STOP ) || ( KeyStatus == REPEAT ) ||
      ( KeyStatus == NO_STATUS ) )
      {
         if ( SystemData.NumberOfMessages )
         {
            /*----Found messages in memory----*/
            if ( KeyStatus == REPEAT )
               /*----Set the message to be that of the last
               recorded one----*/
               SystemData.CurrentMessage = SystemData.LastRecordedMessage;
            /*----Find the address of the first block in the message----*/
            MemoryManagementData.Address =
            RetrieveBOMAddress( SystemData.CurrentMessage );
         }
         else
         {
            /*----there are no messages yet in memory----*/
            SystemData.ErrorMessage ="NO MESSAGES     ";
            return;
         }
      }
      /*----Play at the address specified by address----*/
      TransferMessageToChipCorder( CC_PLAYPWR, MemoryManagementData.Address );
      MemoryManagementData.RacCounter = 0;
      MemoryManagementData.GetAddress = TRUE;
   }
```

```
   /* ------Don't change the status if the key pressed was repeat------ */
   if ( KeyStatus != REPEAT )
      KeyStatus = PLAY;
   SpawnTask( RunPlayMessage );
   return;
} /*----StartPlay----*/
void
RunPlayMessage( void )
{
   if ( SystemMode == MEMORY_MANAGEMENT )
   {
      if ( MemoryManagementData.GetAddress )
      {
         /*----Test if time to retrieve the next address----*/
         MemoryManagementData.Address = RetrieveNextAddress( PC_PLAY );
         /*----clear get address flag----*/
         MemoryManagementData.GetAddress = FALSE;
      }/* if MemoryManagementData.GetAddress */
      if ( ReadRAC() )
      {
         /*----if RAC has changed then increment RAC counter----*/
         ++MemoryManagementData.RacCounter;
         /*----Test if the end of the block was reached----*/
         if ( MemoryManagementData.RacCounter == 1 )
            /*----Continue playing----*/
            TransferMessageToChipCorder( CC_PLAYDD, DONT_CARE );
         else if ( MemoryManagementData.RacCounter >= ROWS_PER_BLOCK )
         {
            if ( MemoryManagementData.Address <= SystemData.MaxRows )
            {
               /*----load the new block address and play at the address
               specified by address----*/
              TransferMessageToChipCorder( CC_PLAYPWR, MemoryManagementData.Address );
               /*----set GetAddress flag so next address will
               be retrieved----*/
               MemoryManagementData.GetAddress = TRUE;
               /*----Reinitialize the RAC Counter----*/
               MemoryManagementData.RacCounter = 0;
            }
          } /* else if */
      }/* if */
   }/* if MemoryManagement */
   ProcessInterrupts();
   /*----------test for end of message----------*/
   if ( SystemData.EOMFlag )
   {
      if ( InputMessage.Bit.RowPointer > ( SystemData.MaxRows - ROWS_PER_BLOCK + 1 ) )
      {
         SystemData.OVFFlag = TRUE;
         SystemData.ErrorMessage = "OVERFLOW        ";
      }
      else
         SystemData.ErrorMessage = "END OF MESSAGE  ";
      /*----Halt the playing of the message, even though it is most likely
      already stopped at this point because of the EOM flag----*/
```

```
      StopMessage();
   }
   return;
} /*----RunPlay----*/
void
StopPlayMessage( void )
{
   KillTask( RunPlayMessage );
   return;
} /*----StopPlay----*/
/*-------------------------------------------------------------------------*/
/*-----------------Retrieve Message Address for beginning of first address-----------
-----*/
uint
RetrieveBOMAddress( uint msgNumber )
{
   uint msgCounter=0;
   MATStruct.Index = 0;
   do
   {
      /* ------If at the beginning of a message------ */
      if ( MATEntry[ MATStruct.Index ].Bit.MessageIndicator )
      {
         ++msgCounter;
         ++MATStruct.Index;
      }
      else
      {
         /* ------The index has surpassed the end of the messages------ */
         if ( MATStruct.Index++ >= MATStruct.EndPointer )
         {
            /*----exit the loop...at the end of the array and haven't
            found the msg----*/
            SoftwareError( NO_MESSAGES );
            return ( SystemData.MaxRows + 1 );
         }
      }
   } while ( msgCounter < msgNumber );
   /* ------Shift the address left by three because there are really
   10 bits in the message, not 7------ */
   return ( ( MATEntry[ --MATStruct.Index ].Bit.BlockPointer ) << 3 );
}     /*----RetrieveBOMAddress----*/
/*--------------------Retrieve Message Address to continue play--------*/
uint
RetrieveNextAddress( uint key )
{
   if ( MATStruct.Index < MATStruct.EndPointer )
   {
      ++MATStruct.Index;
      if ( key == PC_FFWD )
      {
         /* ------If at the beginning of the message and not at the
         end of the messages------ */
         if ( ( MATEntry[ MATStruct.Index ].Bit.MessageIndicator ) &&
         ( SystemData.CurrentMessage < SystemData.NumberOfMessages ) )
```

```
         {
            /*----Found the beginning of the next message----*/
            ++SystemData.CurrentMessage;
         }
         /*----return the next block in the MAT----*/
         return ( uint )( ( MATEntry[ MATStruct.Index ].Bit.BlockPointer ) << 3 );
      }/* if key */
      else
      {
         /*-----key must be play or repeat-----*/
         if ( !( MATEntry[ MATStruct.Index ].Bit.MessageIndicator ) )
            /*----return the next block in the MAT----*/
            return ( uint )( ( MATEntry[ MATStruct.Index ].Bit.BlockPointer ) << 3 );
      }
   }
   /*----There is no more memory to play----*/
   return ( SystemData.MaxRows + 1 );
} /*----RetrieveNextAddress----*/
/*----------------All-functions associated with record------------------*/
void
StartRecordMessage( void )
{
   /*-----if record is already running, don't re-spawn it-----*/
   if ( IsTaskRunning( RunRecordMessage ) )
      return;
   /*-----power up isd chip-----*/
   PowerUp();
   /*----The mode is memory management----*/
   {
      /*----------Find the address of the next block in the message----------*/
      MemoryManagementData.Address =
      RetrieveRecordAddress( BOM );
      if ( MemoryManagementData.Address > SystemData.MaxRows || SystemData.OVFFlag )
      {
         /*----there must be no more blocks in this message----*/
         SystemData.ErrorMessage = "NO MORE MEMORY  ";
         KeyStatus = STOP;
         return;
      }
      /*---- Record at the address specified by address ----*/
      TransferMessageToChipCorder( CC_RECPWR, MemoryManagementData.Address );
      /*----------initialize reading of RAC----------*/
      MemoryManagementData.RacCounter = 0;
      /*----------clear get address flag----------*/
      MemoryManagementData.GetAddress = TRUE;
   }/* if MemoryManagement */
   SpawnTask( RunRecordMessage );
   return;
}
void
RunRecordMessage( void )
{
   if ( SystemMode == MEMORY_MANAGEMENT )
   {
      /*----------Test if time to retrieve the next address----------*/
```

```
      if ( MemoryManagementData.GetAddress )
      {
         MemoryManagementData.Address =
         RetrieveRecordAddress( NEXT_MSG );
         /*----------clear get address flag----------*/
         MemoryManagementData.GetAddress = FALSE;
      }
      if ( ReadRAC() )
      {
         /*----------if RAC has changed then increment RAC counter----------*/
         ++MemoryManagementData.RacCounter;
         /*----------Test if the end of the block was reached----------*/
         if ( MemoryManagementData.RacCounter == 1 )
            /*----------Record at the next avail. block----------*/
            TransferMessageToChipCorder( CC_RECD, DONT_CARE );
         else if ( MemoryManagementData.RacCounter >= ROWS_PER_BLOCK )
         {
            if ( MemoryManagementData.Address < SystemData.MaxRows )
            {
               /*-------load the new block address and record at the address specified
               by address----------*/
               TransferMessageToChipCorder( CC_RECPWR, MemoryManagementData.Address );
               /*----Reset the RAC Counter----*/
               MemoryManagementData.RacCounter = 0;
             /*----------set GetAddress flag so next address will be retreived----------*/
               MemoryManagementData.GetAddress = TRUE;
            }
            else
            {
               /*-----There's no more memory to record into, we've reached the
               end of the chip-----*/
              if ( InputMessage.Bit.RowPointer >= ( SystemData.MaxRows - ROWS_PER_BLOCK
) )
                  SystemData.ErrorMessage = "OVERFLOW        ";
               else
                  SystemData.ErrorMessage = "NO MORE MEMORY  ";
               SystemData.OVFFlag = TRUE;
               StopMessage();
               return;
            }//else
         }/* else if */
      }/* if */
   } /* if */
   ProcessInterrupts();
   /*----------test for overflow----------*/
   if ( SystemData.EOMFlag )
   {
      if ( InputMessage.Bit.RowPointer >= ( SystemData.MaxRows - ROWS_PER_BLOCK ) )
         SystemData.ErrorMessage = "OVERFLOW        ";
      else
         SystemData.ErrorMessage = "NO MORE MEMORY  ";
      /*-----There's no more memory to record into, we've reached the
      end of the chip-----*/
      SystemData.OVFFlag = TRUE;
      StopMessage();
```

```
   }/* if eomflag  */
   return;
}
void
StopRecordMessage( void )
{
   /*-----power down the isd chip-----*/
   PowerDown();
   KillTask( RunRecordMessage );
   return;
}
/*-------------------------------------------------------------------*/
/*------------------------Erase a message----------------------------*/
void
EraseMessage( void )
{
   /*----Assume the message exists----*/
   uchar index, numOfBlocksToErase=1;
   uchar x;
   if ( SystemMode == MEMORY_MANAGEMENT )
   {
      if ( !SystemData.NumberOfMessages )
      {
         SystemData.ErrorMessage = "NO MESSAGES     ";
         return;
      }
      /*----Need to get the BOM address so that the MATStruct.Index will
      be set to the corresponding entry----*/
      /* ------This is a dummy call, used only to set up the MATStruct.Index
      value to the correct one for the current message------ */
      RetrieveBOMAddress( SystemData.CurrentMessage );
      /*----save the position of the first block of the message----*/
      /* The index is pointing to the next block in memory,
      not the first block of the message, so we need to subtract 1 */
      index = MATStruct.Index;
      /*----find the number of blocks of memory that need to be erased----*/
      while ( ( !MATEntry[ ++MATStruct.Index ].Bit.MessageIndicator ) &&
      ( MATStruct.Index <= MATStruct.EndPointer ) )
         ++numOfBlocksToErase;
      /*----This is the new End pointer for the MAT----*/
      MATStruct.EndPointer -= numOfBlocksToErase;
      /*----If the current message is the last one, no messages
      need to be shifted----*/
      if ( SystemData.CurrentMessage != SystemData.NumberOfMessages )
      {
         /*---- Shift all the MAT Entries up numOfBlocksToErase to
         erase the message----*/
         do
         {
            MATEntry[ index ].All = MATEntry[ index + numOfBlocksToErase ].All;
            index++;
         } while ( ( index <= MATStruct.EndPointer ) && ( ( index + numOfBlocksToErase
) < MAT_SIZE ) );
      }
      else
```

```
         --SystemData.CurrentMessage;
      /*----place 0's in the remaining MAT entries after the EndPointer----*/
      for ( x = index; x < ( index + numOfBlocksToErase ); x++ )
      {
         if ( x < MAT_SIZE )
            MATEntry[ ( x ) ].All = 0x00;
      }
      /*----Decrement the number of total messages----*/
      --SystemData.NumberOfMessages;
      if ( SystemData.NumberOfMessages &&
      ( SystemData.CurrentMessage < SystemData.LastRecordedMessage ) )
         --SystemData.LastRecordedMessage;
      KeyStatus = ERASE_MSG;
      SystemData.OVFFlag = FALSE;
      if ( SystemData.NumberOfMessages )
         /*----find the BOM of the current message----*/
         MemoryManagementData.Address =
         RetrieveBOMAddress( SystemData.CurrentMessage );
      else
         MemoryManagementData.Address = 0;
      InputMessage.Bit.RowPointer = MemoryManagementData.Address;
   }
   return;
}/* EraseMessage */
/*-------------------------------------------------------------------------*/
/*-----------------Retrieve Message Address for Record---------------*/
uint
RetrieveRecordAddress( uchar bomFlag )
{
   uchar blockAddress=0;
   uchar tempIndex=0;
   if ( MATStruct.EndPointer < ( MAT_SIZE - 1 ) )
   {
      /*----If there's messages----*/
      if ( MATStruct.EndPointer >= 0 )
      {
         do
         {
            /*----Is the block Address in the MAT Table?----*/
            if ( MATEntry[ tempIndex ].Bit.BlockPointer == blockAddress )
            {
               /*----if yes, reset the index, then go look
               for the next block address----*/
               tempIndex = 0;
               ++blockAddress;
            }
            else
               /*----If the block address is not existent, make sure the
               end of the MAT has not been exceeded----*/
                  if ( ++tempIndex > MATStruct.EndPointer )
                     /*----exit the loop----*/
                     tempIndex = MAT_SIZE + 1;
         } while  ( tempIndex < MAT_SIZE );
      }
      if ( ++MATStruct.EndPointer < MAT_SIZE  )
```

```
      {
         MATEntry[ MATStruct.EndPointer ].Bit.BlockPointer = blockAddress;
         MATEntry[ MATStruct.EndPointer ].Bit.MessageIndicator = bomFlag;
         /*----Make sure that the index is pointing to the current entry----*/
         MATStruct.Index = MATStruct.EndPointer;
         return blockAddress << 3;
      }
   }
   /*----There is no more memory to record into----*/
   return ( SystemData.MaxRows + 1 );
} /*----RetrieveRecordAddress----*/
/*---------------------------------------------------------------------*/
/*--------------------------Interrupt routine-----------------------*/
#pragma TRAP_PROC SAVE_REGS
void
ExternalInterruptProc( void )
{
   /*-----tempByte, bit and i are used for the BitSwapMacro-----*/
   /*-----byteToSwap, tempInput2, tempInput1, tempByte2, and outputMessage
   are used for the TransferMessageToChipCorderMacro, -----*/
   uchar transfer, ccCommand;
   uchar bit, i;
   uint ccAddress;
   uint byteToSwap, outputMessage;
   uchar tempInput2, tempInput1;
   uchar tempByte2;
   /*-----This is to clear a dummy interrupt-----*/
   if ( SystemData.InterruptFlag )
      return;
   /*-----set the transfer flag to indicate to not send a command-----*/
   transfer = FALSE;
if ( SystemMode == MEMORY_MANAGEMENT )
   {
      switch ( KeyStatus )
      {
         case PLAY:
         case REPEAT:
             ++SystemData.RacCounter;
            /*----Test if the end of the first address was reached----*/
            if ( SystemData.RacCounter == 1 )
            {
               /*----Transfer Message to ChipCorder----*/
               (CC_PLAYDD, MemoryManagementData.Address);
            }
            /*-----test if the end of the block was reached-----*/
            else if ( SystemData.RacCounter >= ROWS_PER_BLOCK )
            {
               /*-----Means that there are more addresses in the message-----*/
               if ( MemoryManagementData.Address <= SystemData.MaxRows )
               {
                   /*----Transfer Message to ChipCorder----*/
               (CC_PLAYDD, MemoryManagementData.Address);
                  /*----set GetAddress flag so next address will
                  be retrieved----*/
                  MemoryManagementData.GetAddress = TRUE;
```

```
                  /*----Reinitialize the RAC Counter----*/
                  SystemData.RacCounter = 0;
               }
            }/* else if */
            break;
         case RECORD:
            ++SystemData.RacCounter;
            /*----Test if the end of the first address was reached----*/
            if ( SystemData.RacCounter == 1 )
            {
               /*----------Continue recording----------*/
               transfer = TRUE;
               ccCommand = CC_RECD;
               ccAddress = DONT_CARE;
            }
            /*-----test if the end of the block was reached-----*/
            else if ( SystemData.RacCounter >= ROWS_PER_BLOCK )
            {
               if ( MemoryManagementData.Address <= SystemData.MaxRows )
               {
                /*-------load the new block address and record at the address specified
                  by MemoryManagementData.Address----------*/
                  transfer = TRUE;
                  ccCommand = CC_RECPWR;
                  ccAddress = MemoryManagementData.Address;
                  /*----Reset the RAC Counter----*/
                  SystemData.RacCounter = 0;
                  /*----------set GetAddress flag so next address will be retreived---
-------*/
                  MemoryManagementData.GetAddress = TRUE;
               }
               else
               {
              if ( InputMessage.Bit.RowPointer >= ( SystemData.MaxRows - ROWS_PER_BLOCK
) )
                     SystemData.ErrorMessage = "OVERFLOW       ";
                  else
                     SystemData.ErrorMessage = "NO MORE MEMORY  ";
                  /*-----There's no more memory to record into, we've reached the
                  end of the chip-----*/
                  SystemData.OVFFlag = TRUE;
                  StopMessage();
               }/* else */
            }/* else if */
            break;
      } /* switch */
   }/* if MemoryManagement */
   else
   {
      if ( SystemData.RacCounter == 0 )
      {
         ++SystemData.RacCounter;
         if ( KeyStatus == RECORD )
         {
            /*---------Tranfer Message to ChipCorder----------*/
```

```
          cCC_RECD, DONT_CARE) ;
        }
        else if ( KeyStatus == PLAY || KeyStatus == REPEAT )
{
      TransferMessageToChipCorderMacro( ccCommand, ccAddress );
   }
}/* else */
return;
}/*-----ExternalInterruptProc-----*/
```

Figure 4: AGC Schematic

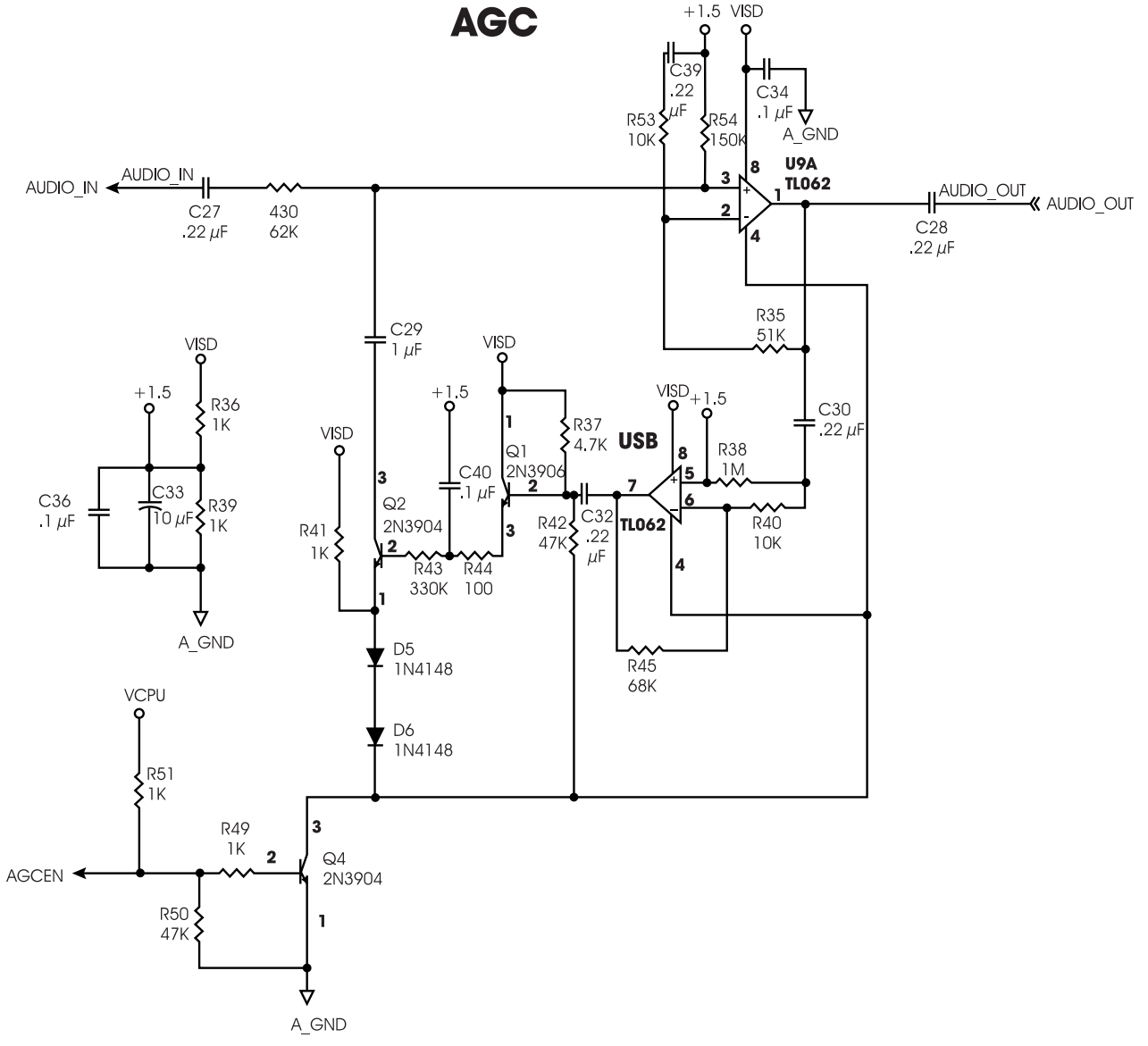


Figure 5: ISD-ES301

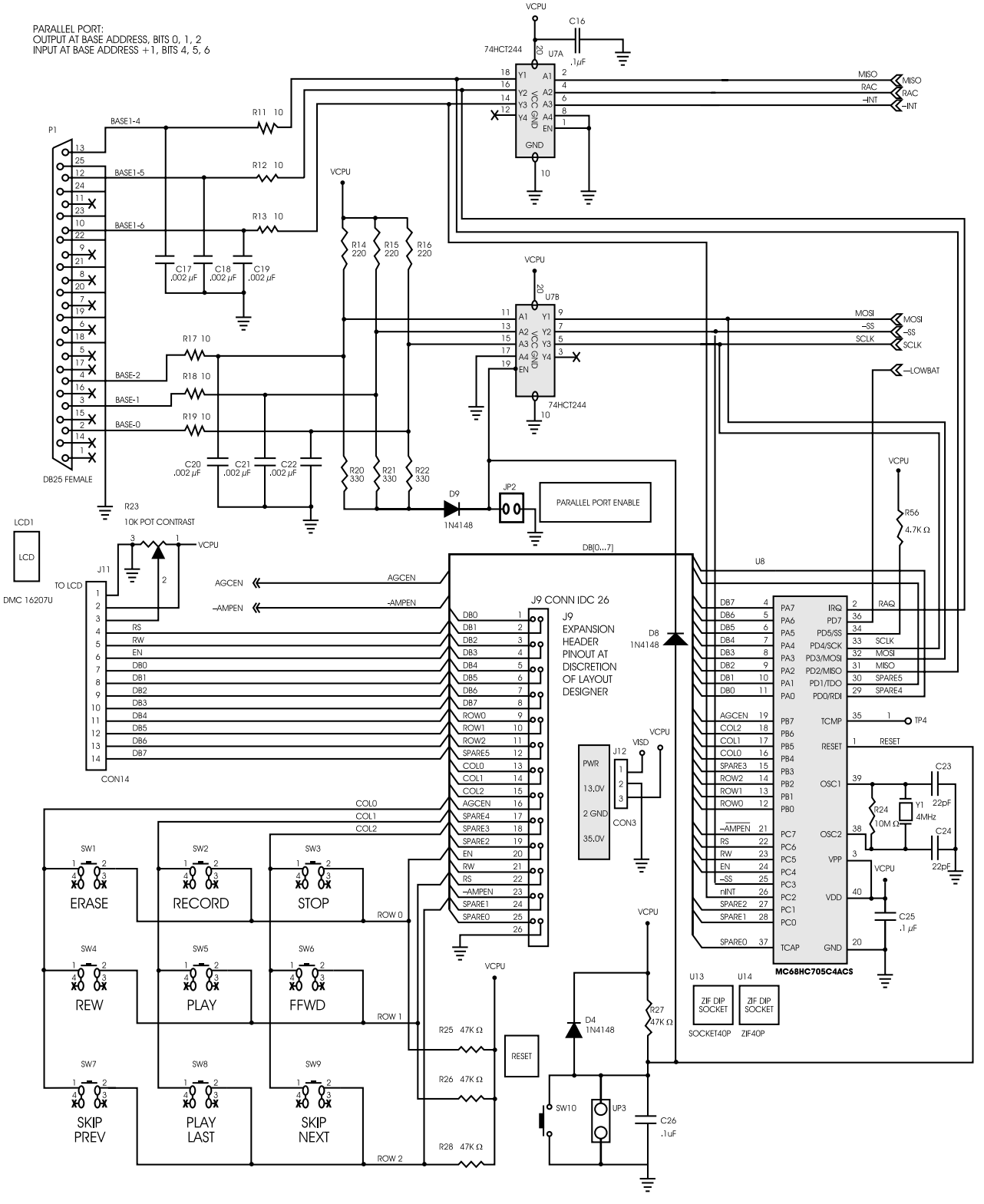
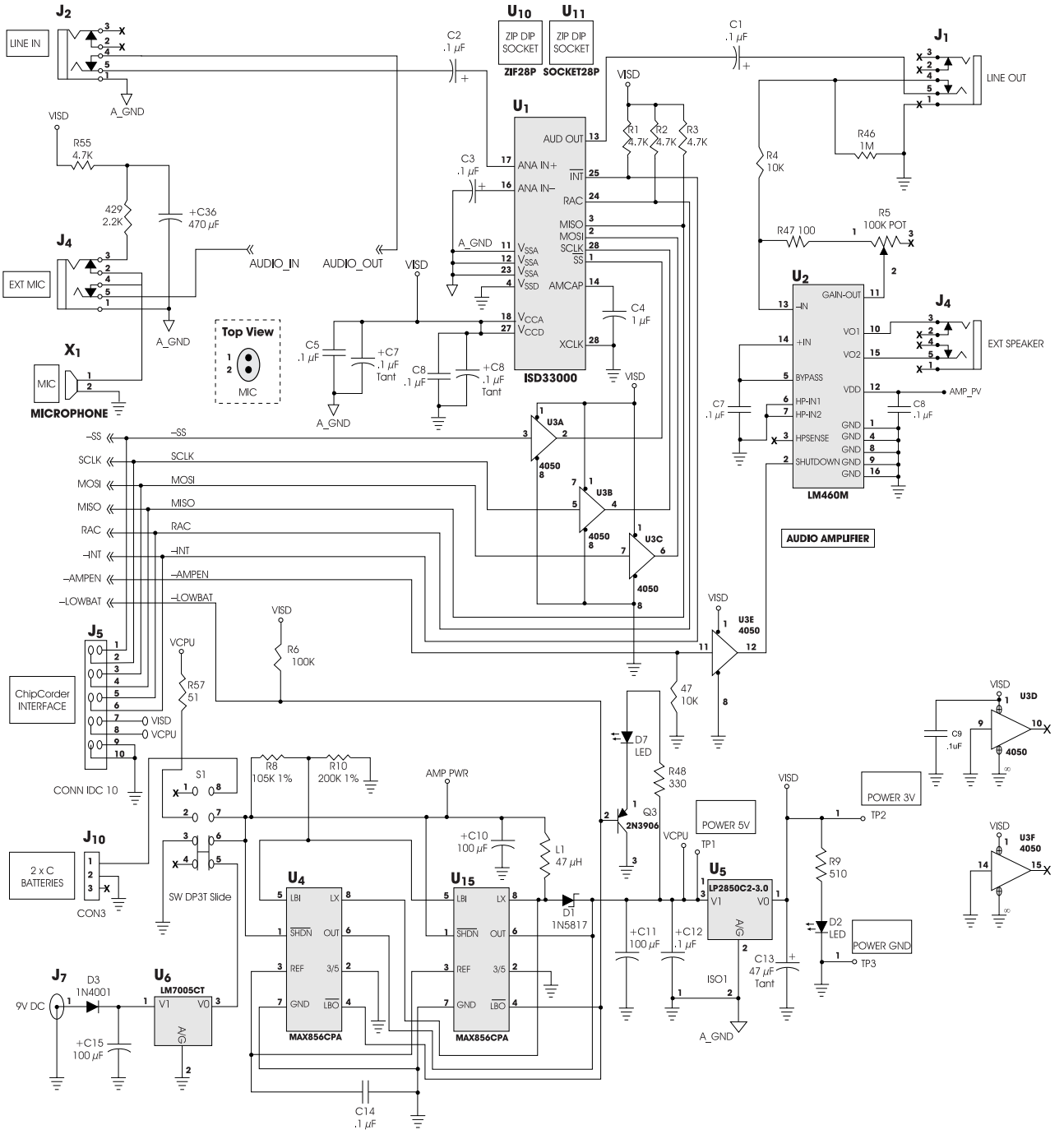


Figure 6: ISD-ES301



SERIAL INTERFACE PRODUCTS

AGC Circuit for ISD33000 Series

AGC CIRCUIT BLOCK

The ISD33000 series is intended to operate with systems that already include an input amplifier and a speaker driver. However, an 'off-the-shelf ' 3-volt microphone preamplifier with AGC is not a common item. Even if one is available, the device may not be economical for some applications. Fortunately, the ISD33000 has the building block in place to support a 3-volt microphone preamplifier and an AGC circuit using a handful of external components. This solution is made possible by utilizing part of the playback AUTOMUTE control circuitry during the record mode.

The circuit diagram in Figure 2 provides an overview of the solution. This AGC application requires one LM324 quad op amp, six carbon resistors, three capacitors, one "low noise" general purpose JFET, and an electret microphone. The circuit monitors the AMCAP voltage level and compares it to a known voltage reference level. The circuit generates the necessary gain factor to amplify the microphone's output level to within the ISD33000's dynamic range requirement.

The key to understanding how the circuit works lies in the AutoMute™ section. Figure 1 provides a simplified AutoMute block diagram. During the play operation, the array output signal is filtered and directed to the AutoMute circuitry. The filter output is also connected to the negative peak detector (NPDETL). The negative peak detector is a half wave rectifier. Therefore only the negative cycle of the signal is used to generate a DC level at AMCAP pin. This signal is then used to control the AutoMute gain level. The differential signal between ANA IN+ and ANA IN– is amplified, filtered and stored directly into the array during the record operation. The peak detector is also active in the record mode, thus the negative cycle of the input signal is rectified and a corresponding DC signal is generated. Figure 1 shows the input signal at the filter's output and AMCAP during a record operation. The signal at CHAN2 (AMCAP) increases with CHAN1's (VOICE) amplitude and decreases when there is no input (1).

Figure 1: Automute Block Diagram

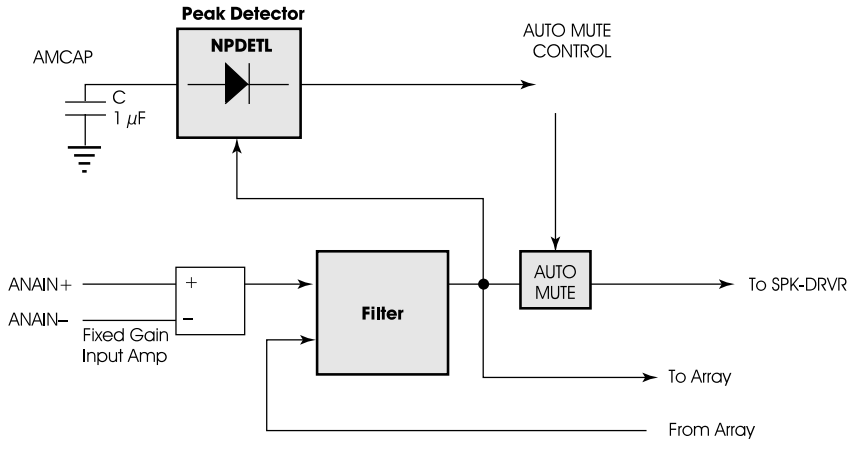
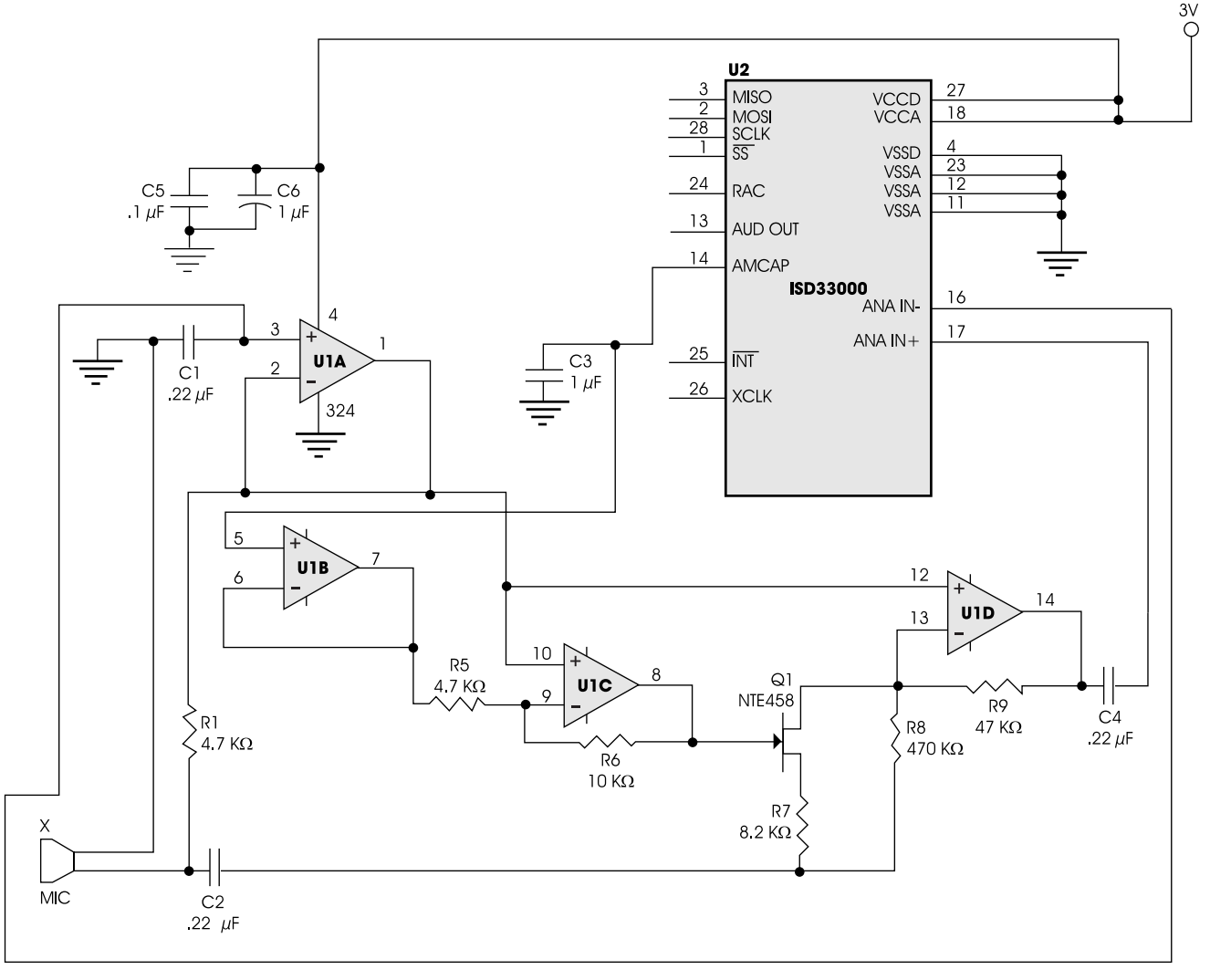
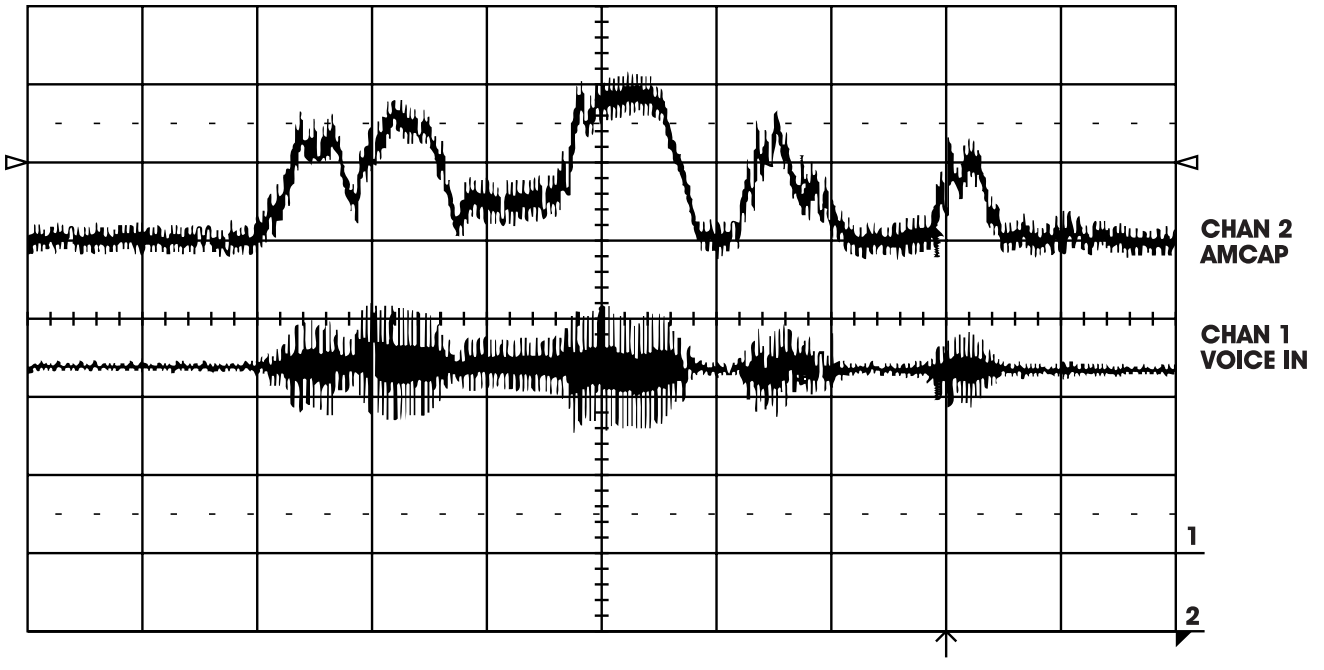


Figure 2: 3 Volt AGC Circuit Diagram



NOTE: *An alternative AGC circuit can be found in Figure 4 of the section "A 'C' Language Source Code Example to Use with the ISD33000 Series." This alternative AGC circuit requires more components but may provide superior performance.*

Figure 3: AMCAP Versus Voice In



The external circuitry uses CHAN2 signal to control ANA IN+ level. Figure 2 shows the components required to realize this function.

The circuit contains three major blocks:

1. Block One comprised of U1A and U1B

   U1A isolates and buffers the ANAIN– DC level for microphone biasing. This amplifier turns off the microphone circuit during power down thus reducing power consumption. The ANAIN- cannot bias the microphone without causing a large DC offset in the array. It reduces the usable dynamic range.

   U1B buffers the AMCAP level. The AMCAP pin is a high impedance node and any load > 1 mA changes the peak detector's rise and fall time. Such a load will prevent this node from tracking the input signal.

2. Block Two contains U1C, R5, R6. It forms the gain control function by subtracting the buffered ANAIN– level from the AMCAP signal.

   U1C's output signal has the following transfer function:

   VOUT= VANAIN – (VANAIN – VAMCAP) * (R6/R5) [1]

   VANAIN: DC level at ANAIN- terminal.

   VAMCAP: Signal at AMCAP terminal.

   CHAN2 in Figure 4 shows U1C's response to a typical voice pattern. When there is no voice (input signals flat) U1C is at it highest level. This signal becomes more negative when a voice pattern is present.

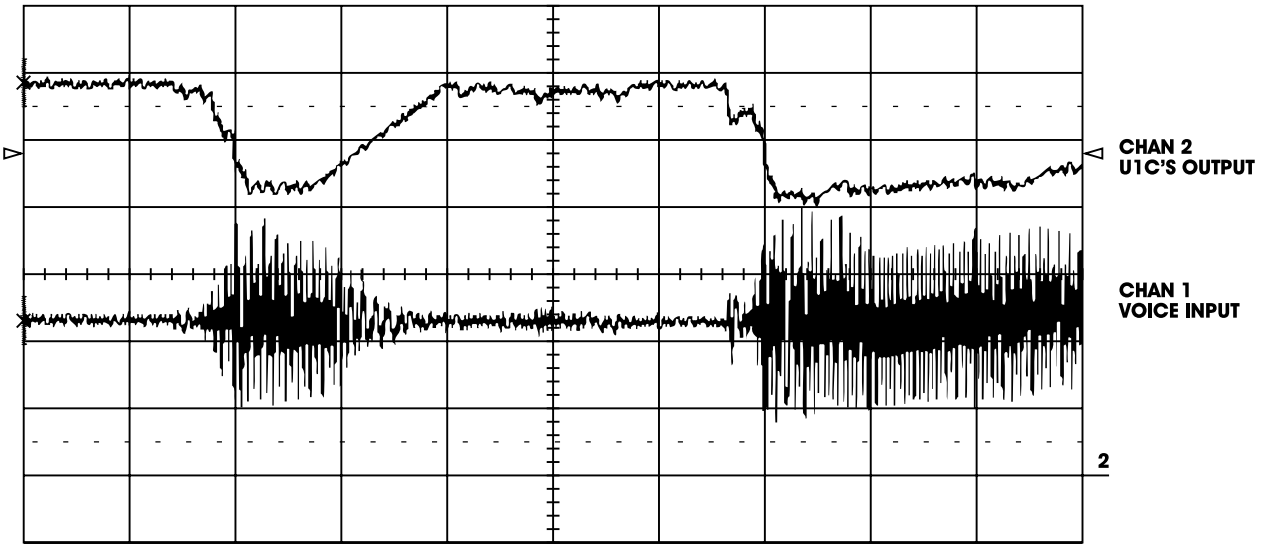
3. Block Three contains U1D, R9, R8, R7, Q1.

   It forms the variable gain stage for the microphone circuit. This block has three states:

   State1 is an attenuate state. This occurs when U1C output level equals (VANAIN – 0.5). During this period Q1's channel resistance is greater than R7. The output level is determined by:

   $VOUT = VMIC^{X}(–R9/R8)$ [2]

Figure 4: Input Signal Versus U1C's Output



- State Two is the full gain state. This condition exists when AMCAP voltage is equal to ANAIN– bias level. The gain is determined by R9/(R8//(R7+Q1rdson))). In practice Q1's rdson << R7 and R8 >> R7 so the output level can be estimated by:

  VOUT = VMIC^{X}(–R9/R7) [3]

- State3 is the variable gain state. The output level is controlled by the difference between U1C's output and ANAIN– bias voltage. The difference voltage sets the VGSoff which changes Q1's channel resistance. Therefore, the output level will range between equation[2] and equation[3] levels.

SETTING UP THE PROTOTYPE

It is highly recommended that the user prototype this circuit before committing to a PC board version. The prototype should be used to determine the best component values for the particular application. The user will need a low distortion 1 KHz sine wave source, an oscilloscope, and a DVM.

Figure 5 shows the modifications for the prototype circuit. In this circuit R1 and the microphone were replaced with R10, R11. This forms a 100:1 attenuator for the sine wave source. This is not necessary if the source can supply 0.5 mVrms and 20.0 mVrms. Connect the DVM's negative input to U1B-7 and the positive input to U1A-1. Replace R6 with R12, R7 with R13 (R12, R13 is a 10 KΩ trimpot). Set both trim pots to 5 KΩ before installing them.

This is a 2 step process.

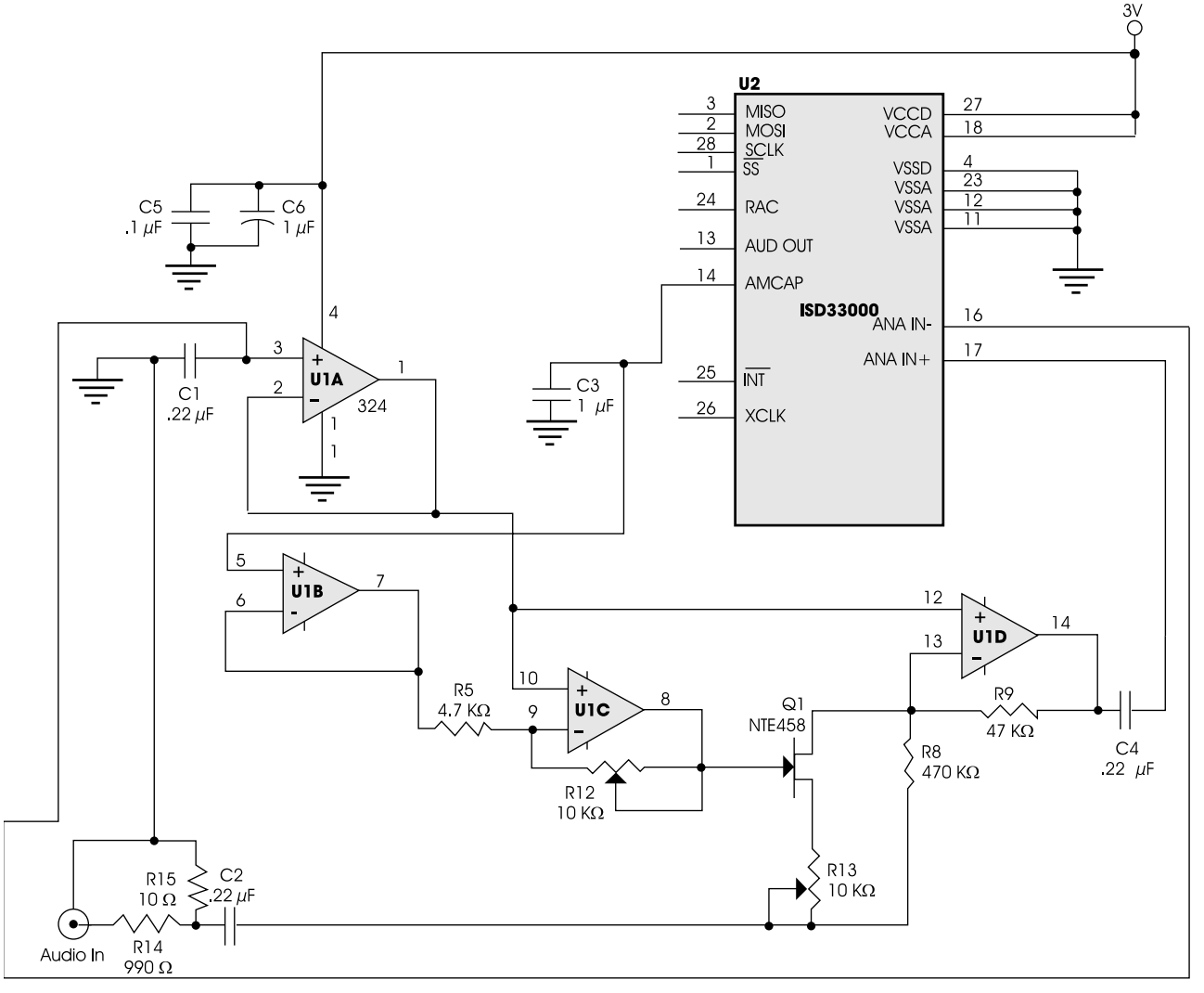
Step 1 determines a bias level for Q1 with maximum input level.

Set the sine wave source to 20 mVrms at input (C2). Adjust R12 until the DVM reads 250 mV DC.

Step 2 finds the gain setting for minimum signal level.

Set the sine wave source to 0.5 mVrms at C2. Adjust R13 until the DVM reads 250 mVdc. Remove R12, R13, measure their resistances and substitute with the nearest value fixed resistors. The minimum and maximum values were chosen to match the electret condenser microphone output with the Rbias = 4.7 KΩ and Vbias = 1.2 V. Other bias voltages and resistances may require readjustment of gain and attenuation level.

Figure 5: Prototype 3 Volt AGC Circuit



IMPROVEMENTS

Table 1 shows a typical component list. Although the LM324 worked at 3 volts, its output could not swing closer to ground than V_{SS} + 0.5 V. A low voltage CMOS op amp would be more suitable for this application. Q1 was shown as an NTE458 but another *N* channel JFET with VGSoff < 1.5 V could be used. R7 may have to be readjusted to match the new transistor's channel resistance vs. VGS characteristic. Lastly, the circuit draws less than 800 µA supply current. At this level, a typical microcontroller I/O pin can be used as power supply. This allows the circuit to be completely shut down when it is not used.

CONCLUSION

Until an integrated 3 volt microphone preamplifier/AGC IC becomes widely available and at a lower cost, the circuit described above provides a 'Low Cost' and serviceable alternative. Further information regarding the circuit is available from the ISD Applications Group.

Table 1: Bill of Materials for 3 Volt AGC Circuit

Item	Quantity	Reference	Part
1	3	C1,C2,C4	.22 µF
2	1	C3	1 µF
3	1	C5	.1 µF
4	1	C6	1 µF
5	1	Q1	NTE458
6	1	R1	4.7 KΩ
7	1	R5	4.7 KΩ
8	1	R6	10 KΩ
9	1	R7	8.2 KΩ
10	1	R8	470 KΩ
11	1	R9	47 KΩ
12	1	U1	LM324
13	1	U2	ISD 33000
14	1 X	Electret Condenser Microphone	