HEWLETT PACKARD

SERVICE MANUAL

HP MODELS 1650A AND 1651A

LOGIC ANALYZERS

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed: 2722A, 2801A, and 2814A

For additional information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section 1.

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Manual Part Number 01650-90901
Microfiche Part Number 01650-90801

PRINTED: 6 APRIL 1988

SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing)

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings) In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding) Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used Do not use repaired fuses or short circuited fuseholders To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply

SAFETY SYMBOLS

Instruction manual symbol The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met

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SECTION 1. GENERAL INFORMATION

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SECTION 1
GENERAL INFORMATION

1-1. INTRODUCTION

This service manual contains information on installing, testing, adjusting, and servicing the Hewlett-Packard Models 1650A and 1651A Logic Analyzers. This section of the manual includes instrument identification, description, options, accessories, specifications and other basic information.

A microfiche part number is listed under the manual part number on the title page of this manual. This number may be used to order 4 X 6-inch microfiche transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also contains the latest Manual Changes supplement as well as pertinent Service Notes.

1-2. INSTRUMENTS COVERED BY MANUAL

On the rear panel of the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is composed of two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments and changes only when a change has been made to the instrument. The suffix however, is assigned sequentially and is different for each instrument The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix different than those listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this instrument is accompanied by a yellow Manual Changes supplement. This supplement contains the necessary "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as accurate as possible, periodically request the latest Manual Change supplement for the instrument manual. The supplement for this manual is identified with the manual part number and print date, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

For information concerning a serial prefix number not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-3. INSTRUMENT DESCRIPTION

The HP 1650A is an 80-channel STATE/TIMING (25 MHz/100 MHz) logic analyzer, selectable in 16 channel groupings. The 1651A is a 32-channel STATE/TIMING logic analyzer, also selectable in 16 channel groupings. The user interface consists of a panel keyboard with an RPG knob and a nine-inch white phosphor, high resolution CRT for information display. A 3 1/2 inch Sony disc drive, for setup storage and retrieval, is integral to the analyzer. An RS-232-C port and external scope trigger are available on the rear panel. The RS-232-C port is used for printer hardcopy output or for analyzer control via a controller.

1-4. ACCESSORIES SUPPLIED

The following accessories are supplied with the HP 1650A/51A Logic Analyzers:

Probe Cables. Probe cables with a 40-pin connector on each end are supplied with each instrument. The probe cable is woven with 17 signal lines, 34 return lines, 34 chassis ground lines, and two power lines.

The power lines supply + 5 V for preprocessor power. Each cable supplies 600 milliamperes and the maximum power available from the HP 1650A/51A is 2 amperes. Five probe cables are supplied with the HP 1650A and two are supplied with the HP 1651A. *HP Part Number 01650-61608.*

Probe Tip Assemblies. Provides 16 data channels, 1 clock channel and 1 ground lead per pod assembly. Probe tip assemblies are supplied for direct probing and are removable for use with HP Model 10269C Probe Interface. The probe input specifications are listed in Table 1-1. Five Probe Tip Assemblies are supplied with the HP 1650A Logic Analyzer and two are supplied with the HP 1651A. *HP Part Number 01650-61607.*

Grabbers. Grabbers for the probe tip assemblies are supplied in packages of 20. 100 grabbers are supplied with the HP 1650A and 40 grabbers are supplied with the HP 1651A. *HP Part Number 5959-0288 (package of 20).*

One 2.3 metre (7.5 feet) **power cord.** See section 2 for available power cords.

One **Operating and Programming Manual Set.**

Two **Operating System Discs.**

One **Service Manual.**

One **RS-232-C Loopback Connector.**

1-5. ACCESSORIES AVAILABLE

The following accessories are available for use with the HP 1650A/51A:

HP Model 10269C Probe Interface. Used to interface the logic analyzer directly to a specific microprocessor.

Soft Carrying Case. *HP Part Number 1540-1066.*

HP Model 1008A Option 006 Testmobile.

HP Model 92192A 3.5" Microfloppy Discs *(box of ten).*

Rackmount Kit. *HP Part Number 5061-6175.*

1-6. SPECIFICATIONS

Table 1-1 is the list of specifications for the HP 1650A/51A Logic Analyzer. These specifications are the performance standards or limits against which the logic analyzer is tested.

1-7. OPERATING CHARACTERISTICS

Table 1-2 is a list of the operating characteristics of the HP 1650A/51A Logic Analyzer. The operating characteristics are a summary of performance capabilities of the HP 1650A/51A.

1-8. GENERAL CHARACTERISTICS

Table 1-3 is general characteristics of the HP 1650A/51A Logic Analyzer. The general characteristics are useful environmental operating conditions, shipping weights, and instrument dimensions.

1-9. RECOMMENDED TEST EQUIPMENT

Table 1-4 is a list of the test equipment required to test performance, make adjustments, and troubleshoot the HP 1650A/51A Logic Analyzer. The table indicates the critical specification of the test equipment and for which procedure the equipment is necessary. Equipment other than the recommended model may be used if it satisfies the critical specification listed in table 1-4.

Table 1-1. HP Model 1650A/51A Specifications

PROBES

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy:

Voltage Range	Accuracy
-2.0V to +2.0V	±150 mV
-9.9V to -2.1V	±300 mV
+2.1V to +9.9V	±300 mV

Dynamic Range: ± 10 volts about the threshold.

STATE MODE

Clock Repetition Rate:
Single phase is 25 MHz maximum. With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by >50 ns.

Clock Pulse Width: ≥10 ns at threshold

Setup Time: Data must be present prior to clock transition, ≥ 10 ns.

Hold Time: Data must be present after rising clock transition; 0 ns.

Data must be present after falling clock transition, 0 ns (HP 1651A); data must be present after falling L clock transition, 0 ns (HP 1650A); data must be present after falling J, K, M, and N clock transition, 1 ns (HP 1650A).

TIMING MODE

Minimum Detectable Glitch: 5 ns wide at the threshold.

Table 1-2. HP 1650A/51A Operating Characteristics

PROBES

Input RC: 100 KΩ ±2% shunted by approximately 8 pF at the probe tip.

TTL Threshold Preset: +1.6 volts.

ECL Threshold Preset: -1.3 volts.

Threshold Range: -9.9 to +9.9 volts in 0.1V increments.

Threshold Setting

Threshold levels may be defined for pods 1 and 2 individually (HP 1651A). Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5 (HP 1650A).

Minimum Input Overdrive: 250 mV or 30% of the input amplitude, whichever is greater

Maximum Voltage: ± 40 volts peak.

Maximum Power Available Through Cables:

2/3 amp @ 5V per cable; 2 amp @ 5V per HP 1650A/51A.

MEASURMENT CONFIGURATIONS

Analyzer Configurations:

Analyzer 1	Analyzer 2
Timing	Off
Off	Timing
State	Off
Off	State
Timing	State
State	Timing
State	State
Off	Off

Channel Assignment:

Each group of 16 channels (a pod) can be assigned to Analyzer 1, Analyzer 2, or remain unassigned. The HP 1650A contains 5 pods; the HP 1651A contains 2 pods.

Table 1-2. HP 1650A/51A Operating Characteristics (cont'd)

STATE ANALYSIS

MEMORY

Data Acquisition:

1024 samples/channel.

TRACE SPECIFICATION

Clocks:

Five clocks (HP 1650A) or two clocks (HP 1651A) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier:

The high or low level of four ORed clocks (HP 1650A) or one clock (HP1651A) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers:

Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. Eight pattern recognizers are available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on.

Range Recognizers:

Recognizes data which is numerically between or on two specified patterns (ANDed combination of 0s and/or 1s). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits and on a maximum of 2 pods.

Qualifier:

A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels:

There are eight levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first seven sequence levels.

Branching:

Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.

Table 1-2. HP 1650A/51A Operating Characteristics (cont'd)

Occurrence Counter:
Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.

Storage Qualification:
Each sequence level has a storage qualifier that specifies the states that are to be stored.

Enable/Disable:
Defines a window of post-trigger storage. States stored in this window can be qualified.

Prestore:
Stores two qualified states that precede states that are stored.

TAGGING

State Tagging:
Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4 X (10 to the 12th power).

Time Tagging:
Measures the time between stored states, relative to either the previous state or the trigger. Maximum time between states is 48 hours.

With tagging on, the acquisition memory is halved; minimum time between states is 60 ns.

SYMBOLS

Pattern Symbols:
User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit pattern can include 0s, 1s, and don't cares.

Range Symbols:
User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of 0s and 1s. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Pattern and Range Symbols: 100 per analyzer.

Symbols can be down-loaded over RS-232-C.

Table 1-2. HP 1650A/51A Operating Characteristics (cont'd)

TIMING ANALYSIS

TRANSITIONAL TIMING MODE

Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period:
10 ns.

Maximum Time Covered By Data: 5000 seconds.

Minimum Time Covered by Data: 10.24 μs.

GLITCH CAPTURE MODE

Data sample and glitch information stored every sample period.

Sample Period:
20 ns to 50 ms in a 1-2-5 sequence dependent on sec/div and delay settings.

Memory Depth:
512 samples/channel.

Time Covered by Data: Sample period X 512

WAVEFORM DISPLAY

Sec/div:
10 ns to 100 s; 0.01% resolution.

Delay:
-2500 s to 2500 s; presence of data dependent on the number of transitions in data between trigger and trigger plus delay (transitional timing).

Accumulate:
Waveform display is not erased between successive acquisitions.

Overlay Mode:

Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number Of Displayed Waveforms: 24

Table 1-2. HP 1650A/51A Operating Characteristics (cont'd)

TIME INTERVAL ACCURACY

Channel to Channel Skew: 4 ns typical.

Time Interval Accuracy:
± (sample period + channel-to-channel skew + 0.01% of time interval reading).

TRIGGER SPECIFICATION

Asynchronous Pattern:
Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high, or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.

Greater Than Duration:
Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is +0 ns to -20 ns. Trigger occurs at pattern + duration.

Less Than Duration:
Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is +20 ns to -0 ns. Trigger occurs at the end of the pattern.

Glitch/Edge Triggering:
Trigger on glitch or edge following valid duration of asynchronous pattern while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Table 1-2. HP 1650A/51A Operating Characteristics (cont'd)

MEASUREMENT AND DISPLAY FUNCTIONS

AUTOSCALE (TIMING ANALYZER ONLY)

Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

ACQUISITION SPECIFICATIONS

Arming:

Each analyzer can be armed by the run key, the other analyzer, or the external trigger in port.

Trace Mode:

Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

LABELS

Channels may be grouped together and given a six character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

INDICATORS

Activity Indicators:

Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers:

Two markers (X and 0) are shown as dashed lines on the display.

Trigger:

Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

MARKER FUNCTIONS

Time Interval:

The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Table 1-2. HP1650A/51A Operating Characteristics (cont'd)

Delta States (State Analyzer Only):

The X and 0 markers measure the number of tagged states between one state and trigger, or between two states.

Patterns:

The X and 0 markers can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The 0 marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics:

X to 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

RUN/STOP FUNCTIONS

Run:

Starts acquisition of data in specified trace mode.

Stop:

In single trace mode or the first run of a repetitive acquisition, STOP halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts acquisition of data and does not change current display.

DATA DISPLAY/ENTRY

Display Modes:

State listing; timing waveforms; interleaved, time-correlated listing of two state analyzers (time tagging on); time-correlated state listing and timing waveform display (state listing in upper half, timing waveform in lower half, and time tagging on)

Timing Waveform:

Pattern readout of timing waveforms at X or 0 marker.

Bases:

Binary, Octal, Decimal, Hexadecimal, ASCII (display only), and User-defined symbols.

Table 1-3. HP 1650A/51A General Characteristics

OPERATING ENVIRONMENT

Temperature

Instruments, 0° to 55 ° C (+32° to 131°F); probes and cables, 0° to 65°C (+32° to 149°F). Recommended temperature range for disc media, 10° to 50°C (+50° to 149°F).

Humidity

Instruments up to 95% relative humidity at +40°C; (104°F). Recommended humidity range for disc media, 8% to 80% relative humidity at +40°C (+104°F).

Altitude

To 4600 m (15,000 ft).

Vibration

Operation

Random vibration 5-500 Hz, 10 minutes per axis, ≈2.41 g (rms).

Non-operating

Random vibration 5-500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

Weight

10.0 kg (22 lbs) net; 18.2 kg (40 lbs) shipping.

Power

115V/230V, 48-66 Hz, 200 W max

Dimensions

Notes:

1. Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.

2. Dimensions are in millimetres and (inches).

Table 1-4. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
OSCILLOSCOPE	dual channel dc to 300 MHz	HP 54201A	P, T
PULSE GENERATOR	5 ns pulse width 20 ns period 1.3 ns risetime double pulse	HP 8161A/020	P
POWER SUPPLY	+ or - 10.2 V output current: 0 - 0.4 amperes	HP 6216B	P
POWER SPLITTER	50 ohms	HP 11549A	P
ADAPTER	Type N male to BNC female (qty 2)	HP Part Number 1250-0780	P
ADAPTER	Type N male to BNC male	HP Part Number 1250-0082	P
DMM	5.5 digit resolution	HP 3478A	A, T
RESISTOR	2 Ohms, 25 Watts	HP Part Number 0811-1390	T

* P=Performance Tests A=Adjustments T=Troubleshooting

SECTION 2. INSTALLATION

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SECTION 2
INSTALLATION

2-1. INTRODUCTION

This section of the manual contains information and instructions necessary for installing the HP 1650A/51A Logic Analyzer. Included in this section are inspection procedures, power requirements, hardware connections and configurations, and packaging information.

2-2. INITIAL INSPECTION

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Accessories supplied with the instrument are listed under Accessories Supplied in section 1 of this manual. The self test procedure is described in this section and electrical performance verification functions are described in section 5. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Self Test Performance Verification, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-3. OPERATING ENVIRONMENT

The operating environment for the HP 1650A/51A is described in table 1-2. Note the non-condensing humidity limitation. Condensation within the instrument cabinet can cause poor operation or malfunction. Protection should be provided against temperature extremes which cause condensation within the instrument.

2-4. STORAGE AND SHIPPING

This instrument may be stored or shipped in environments within the following limitations:

TEMPERATURE	-40° C TO 75° C
HUMIDITY	UP TO 90% AT 65° C
ALTITUDE	UP TO 15 300 METRES (50 000 FEET)

2-5. PACKAGING

2-6. Tagging for Service

If the instrument is to be shipped to a Hewlett-Packard office for service or repair; attach a tag to the instrument identifying owner, address of owner, complete instrument model and serial numbers, and a description of the service required.

2-7. Original Packaging

If the original packaging material is unavailable or unserviceable, materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for service, attach a tag showing owner, address of owner, complete instrument model and serial numbers, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-8. Other Packaging

The following general instructions should be followed for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of instrument to firmly cushion and prevent movement inside the container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

2-9. PREPARATION FOR USE

2-10. Power Requirements

The HP 1650A/1651A requires a power source of either 115 or 230 Vac, -22% to +10%; single phase, 48 to 66 Hz; 200 Watts maximum power.

CAUTION

BEFORE CONNECTING POWER TO THIS INSTRUMENT, be sure the line voltage switch on the rear panel of the instrument is set properly and the correct fuse is installed.

2-11. Line Voltage Selection

Before setting instrument power switch to ON position, verify that the fuse module is in the correct position for the line voltage.

The fuse module is located in the line filter/power switch module on the rear panel of the instrument.

If the arrow beside the voltage on the fuse module that is in-line with the filter arrow does not match line voltage to be used, it must be changed. To select the proper fuse for line voltage, gently pry out fuse module with a flat-blade screwdriver. To use other fuse in module, turn fuse module and reinsert into the line filter module.

2-12. POWER CABLE

WARNING

BEFORE CONNECTING THIS INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (Mains) power cord. The Mains plug must be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet does not provide an instrument ground.

This instrument is provided with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to figure 2-1 for power plugs and HP part numbers for the available plug configurations.

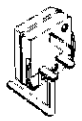
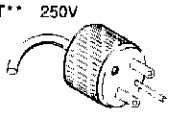
2-13. APPLYING POWER

When power is applied to the HP 1650A/51A, a power-up self test will automatically be performed. For information on the power-up self test, refer to section 3.

2-14. CLEANING REQUIREMENTS

Use MILD SOAP AND WATER to clean the HP 1650A/51A cabinet and front panel. Care must be taken not to use a harsh soap which will damage the water-base paint finish of the instrument.

Table 2-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 250V 900 	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 250V 901 	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia, New Zealand
OPT 250V 902 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So Africa, India (Unpolarized in many nations)
OPT** 125V 903 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Philippines, Taiwan,
OPT** 250V 904 	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 250V 905 	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals United States and Canada only
OPT 250V 906 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 220V 912 	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 250V 917 	8120-4600 8120-4211	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 100V 918 	8120-4753 8120-4754	Straight Mitl 90°	90/230 90/230	Dark Gray	Japan

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug
**These cords are included in the CSA certification approval of the equipment.
E = Earth Ground
L = Line
N = Neutral

Figure 2-1. Power Cord Plug Configurations

AC CABLES3

SECTION 3. PERFORMANCE TESTS

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SECTION 3
PERFORMANCE TESTS

3-1. INTRODUCTION

The procedures in this section test the instrument electrical performance by using the specifications of table 1-1 as the performance standards. All tests may be performed without access to the interior of the instrument.

3-2. EQUIPMENT REQUIRED

Equipment required for the performance tests in this section is listed in the Recommended Test Equipment table in Section 1. Any equipment that satisfies the critical specification listed in the table may be substituted for the recommended model.

3-3. TEST CONNECTOR

The performance tests and adjustments require connecting pulse generator outputs to probe pod inputs. Figure 3-1 is a test connector that may be built to allow testing of multiple channels (up to eight at one time). The test connector consists of a BNC connector and a length of wire. Connecting more than eight channels to the test connector at a time will induce loading of the circuit and true signal representation will degrade. Test results may not be accurate if more than eight channels are connected to the test connector.

The Hewlett-Packard part number for the BNC connector in figure 3-1 is 1250-1032. An equivalent part may be used in place of the Hewlett-Packard part.

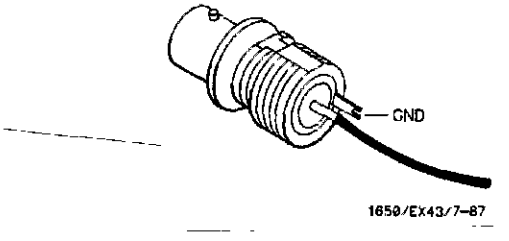

Figure 3-1. Test Connector

3-4. TEST RECORD

The results of the performance tests may be tabulated on the Test Record provided at the end of this section. The Test Record lists the performance tests and provides an area to mark whether the pod passed or failed the test. The results recorded in the table at incoming inspection may be used for later comparisons of the tests during periodic maintenance, troubleshooting, and after repairs or adjustments.

3-5. SELF TESTS

The power-up self test is automatically performed upon applying power to the logic analyzer. Since the performance tests require test equipment, self tests may be performed individually to provide a higher level of confidence that the instrument is operating properly. A message that the instrument has failed the test will appear if any problem is encountered during the test. The individual self tests may be performed for functions listed in the self test menu which is invoked via the I/O menu. The HP 1650A/51A self test is located on the operating system disc and is required to run the tests.

3-6. Power-up Self Test

The power-up self test is automatically invoked at power-up of the HP 1650A/51A Logic Analyzer. The revision number of the operating system firmware is given in the upper right of the screen during the power-up self test. As each test is completed, either "passed" or "failed" will be printed in front of the name of the test in this manner:

```
PERFORMING POWER-UP SELF TESTS

  passed  ROM test
  passed  RAM test
  passed  Interrupt test
  passed  Display test
  passed  Keyboard test
  passed  Acquisition test
  passed  Threshold test
  passed  Disc test

LOADING SYSTEM FILE
```

As indicated by the last message, the HP 1650A/51A will automatically load the operating system disc in the disc drive. If the operating system disc is not in the disc drive, the message "SYSTEM DISC NOT FOUND" will be displayed at the bottom of the screen and "NO DISC" will be displayed in front of disc test in place of "passed".

If the above message appears, turn off the instrument, insert the operating system disc into the disc drive, and again apply power.

3-7. Selectable Self Tests

Seven self tests may be invoked individually via the Self Test menu. The seven selectable self tests are:

HP 1650A Self Tests

* Data Acquisition
* RS-232-C
* External Trigger BNCs
* Keyboard
* RAM
* ROM
* Disc Drive
* Cycle through all tests

The required test is selected by moving the cursor to the test and pressing the front panel SELECT key. A pop-up menu appears with a description of the test to be performed. The self test does not begin until the cursor is placed on **Execute** and the front panel SELECT key is pressed.

After the test has been completed, either "Passed","Failed", or "Tested" will be displayed on the Self Test menu in front of the test. These tests are used as troubleshooting aids. Section 6 contains information on the individual tests used for troubleshooting.

3-8. CLOCK, QUALIFIER, AND DATA INPUTS TESTS

3-9. Clock, Qualifier, and Data Inputs Test 1

Description:

This test verifies maximum clock rate with counting mode for the HP 1650A/51A, and the setup and hold times for the falling edge of the HP 1650A L clock specification.

Specification:

Clock repetition rate: With time or state counting mode on, minimum time between states is 60 ns.

HP 1650A hold time: Data must be present after falling edge of L clock transition, 0 ns.

Setup time: Data must be present prior to clock transition, >=10ns.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1 Connect the HP 1650A/51A and test equipment as in figure 3-2.

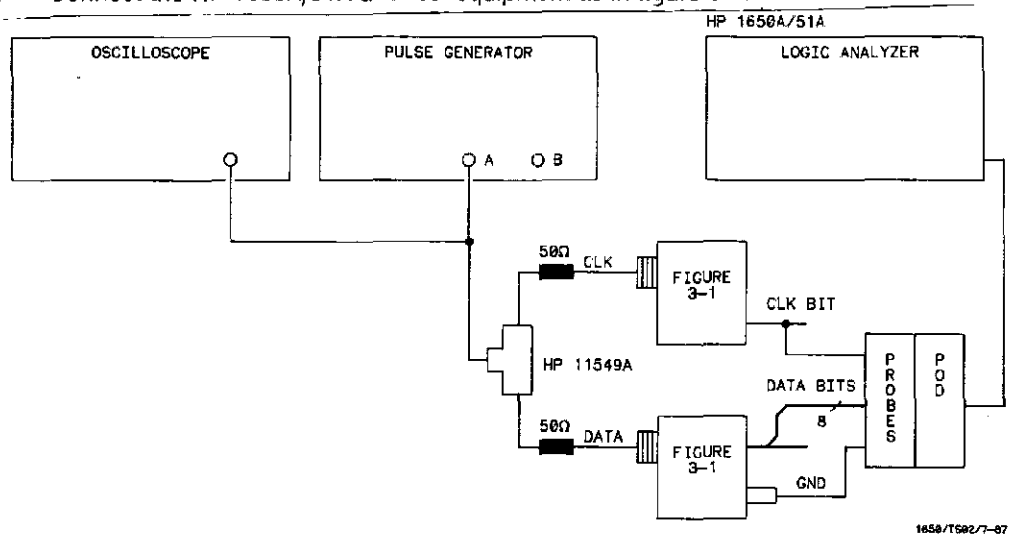

Figure 3-2. Setup for Clock, Qualifier, and Data Inputs Test 1

NOTE

In this setup, eight channels are connected to test eight channels at a time. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-3.

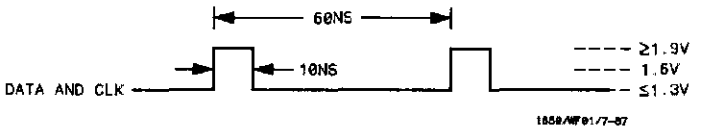

Figure 3-3. Waveform for Clock, Qualifier, and Data Inputs Test 1

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** menu as in figure 3-4. Refer to steps a through c below figure if unfamiliar with the menus.

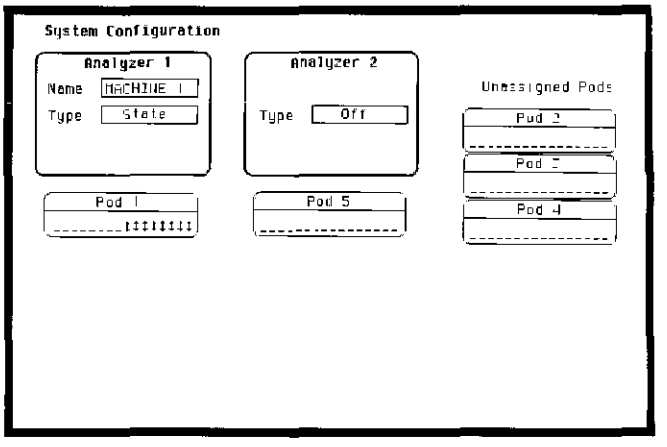

Figure 3-4. **System Configuration** *for Clock, Qualifier, and Data Inputs Test*

a. Move cursor to **Analyzer 1 Type** by using front-panel knob.

b. Select **State** as **Type** by using front-panel knob and SELECT key.

c. Assign pod under test to **Analyzer 1** by using front-panel knob and SELECT ke

Assign appropriate clock, edge, and channels of the pod under test to a label in the **STATE FORMAT SPECIFICATION** as in figure 3-5. Refer to steps a through c below figure if unfamiliar with the menus.

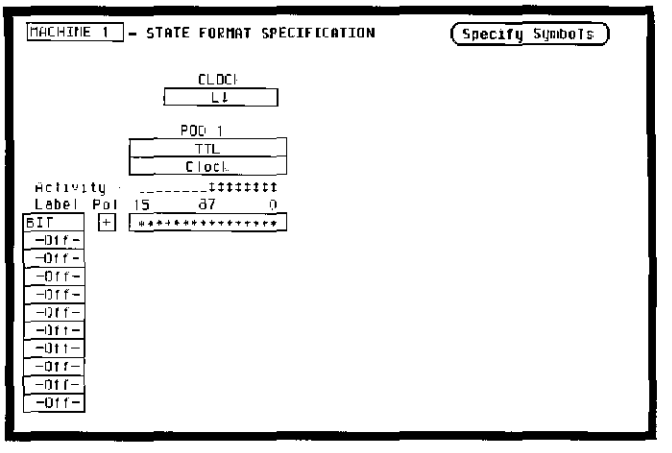

Figure 3-5. ***STATE FORMAT SPECIFICATION*** *for Clock, Qualifier, and Data Inputs Test 1*

a. Invoke **STATE FORMAT SPECIFICATION** by pressing front-panel FORMAT key.

b. Assign the falling clock edge of the pod under test by using the front-panel knob and SELECT key:

HP 1650A - Assign L clock for all pods.
HP 1651A - Assign J clock for Pod 1, Assign K clock for Pod 2.

c. Assign channels under test to label by using front-panel knob and SELECT key.

5. Set up the **STATE TRACE SPECIFICATION** menu for **Single Trace mode**, without sequencing levels and **Count States** as in figure 3-6. Refer to below figure if unfamiliar with the menus.

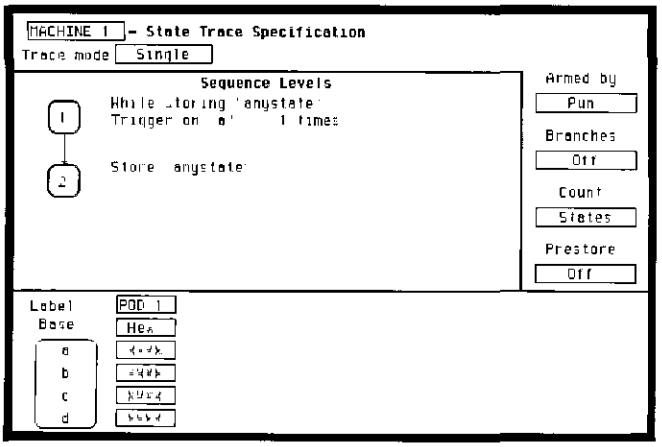

Figure 3-6. ***STATE TRACE SPECIFICATION*** *for Clock, Qualifier, and Data Inputs Test1*

a. Select **STATE TRACE SPECIFICATION** by pressing front-panel TRACE key.

b. Select **Single Trace mode** by using front-panel knob and SELECT key.

c. Select **Count States** by using front-panel knob and SELECT key. Pop-up menu will be displayed with selections of states to count.

d. Select **anystate** by pressing the SELECT key.

6. Press RUN. The **STATE LISTING** will be displayed as in figure 3-7 and will show F's for the channels under test.

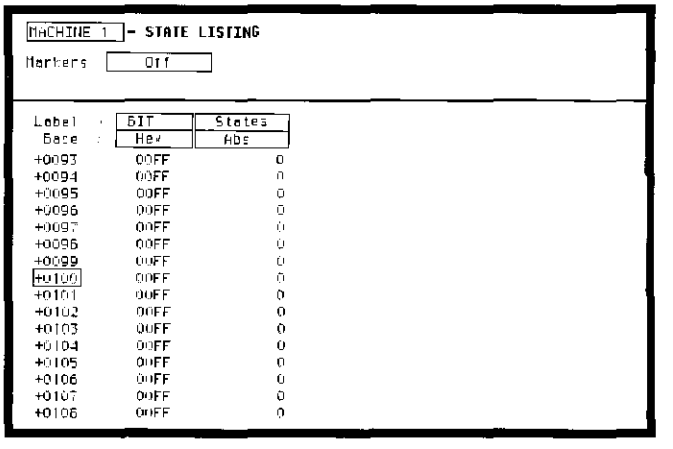

*Figure 3-7. **STATE LISTING** for Clock, Qualifer, and Data Inputs Test 1*

NOTE

To ensure consistent pattern of F's in listing, use front-panel ROLL keys and knob to scroll through State Listing.

7. Disconnect the channels under test from the test connector and connect the next eight channels to be tested.

8. Repeat step 6.

9. Disconnect the pod of channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all the pods have been tested.

    a. Move the cursor to **MACHINE 1** by using front-panel knob and SELECT key.

    b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-10. Clock, Qualifier, and Data Inputs Test 2

Description:

This performance test verifies the setup and hold time specification for the rising edg transition of all clocks on the HP 1650A/51A.

Specification:

Setup Time: Data must be present prior to clock transition, >= 10 ns.

Hold Time: Data must be present after rising clock transition, 0 ns.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1. Connect the HP 1650A/51A and test equipment as in figure 3-8.

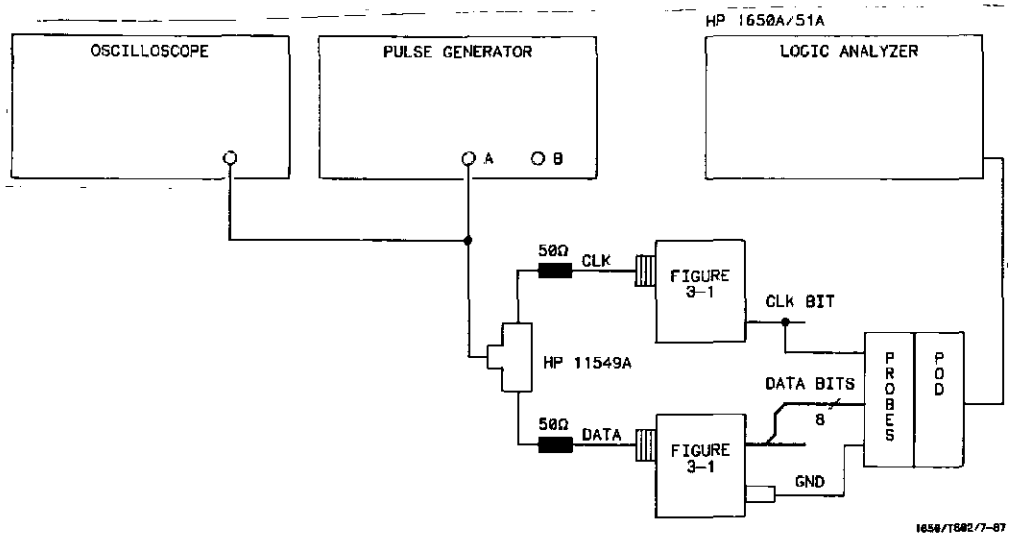

Figure 3-8. Setup for Clock, Qualifier, and Data Inputs Test 2

NOTE

In this setup, eight channels are connected to test half of the pod at a time. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for output in figure 3-9.

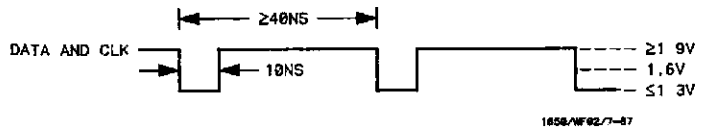

Figure 3-9. Waveform for Clock, Qualifier, and Data Inputs Test 2

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** menu as in previous test figure 3-4.

4. Assign appropriate clock, rising clock transition and all channels of the pod under test to label in the **STATE FORMAT SPECIFICATION** as in previous test figure 3-5.

5. Set up the **STATE TRACE SPECIFICATION** for **Single Trace mode**, without sequencing levels and **Count Off** as in figure 3-10.

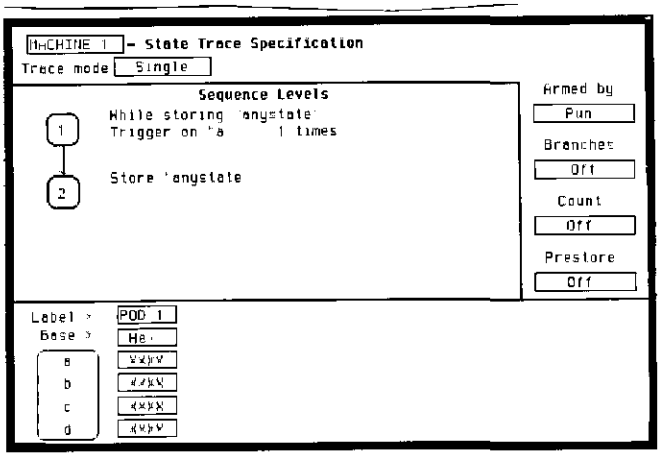

*Figure 3-10. **STATE TRACE SPECIFICATION** for Clock, Qualifier, and Data Inputs Test 2*

NOTE

This is the power-up default condition of this menu.

6. Press RUN. The **STATE LISTING** will be displayed and will list 0's for the channels under test as in figure 3-11.

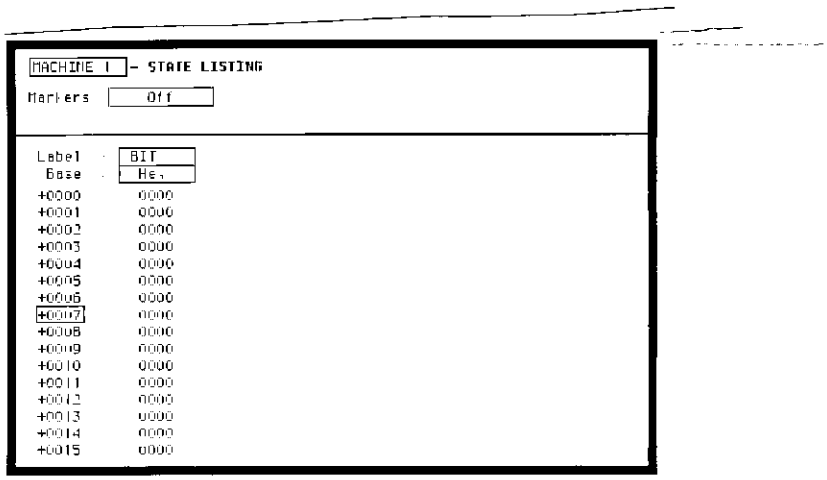

Figure 3-11. ***STATE LISTING*** *for Clock, Qualifier, and Data Inputs Test 2*

7. Disconnect the channels under test from the test connector and connect the remaining channels of the pod.

8. Repeat step 6.

9. Disconnect the pod of channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all pods have been tested with each clock.

    a. Move cursor to **MACHINE 1** by using front-panel knob.

    b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-11. Clock, Qualifier, and Data Inputs Test 3 (HP 1650A Only)

Description:

This performance test verifies the hold time specifications for the falling clock transition of the J, K, M and N clocks on the HP 1650A.

Specification:

HP 1650A Hold Time: Data must be present after falling J, K, M, and N clock transition, 1 ns.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1. Connect the HP 1650A and test equipment as in figure 3-12.

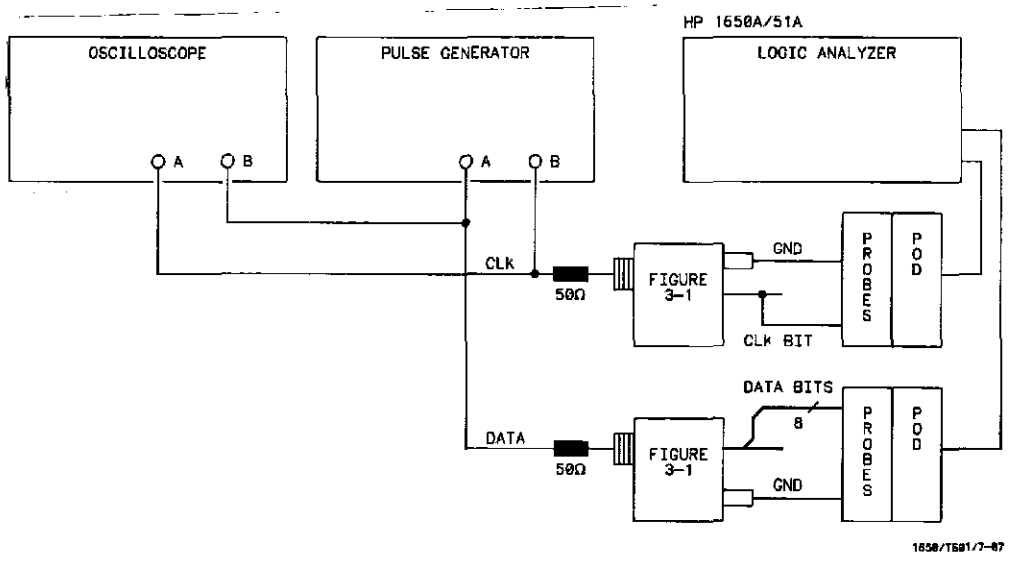

Figure 3-12. Setup for Clock, Qualifier, and Data Inputs Test 3

NOTE

In this setup, eight channels are connected to test half of the pod at a time. Ground lead must be grounded to ensure accurate test results.

2. Adjust the pulse generator for outputs in figure 3-13. Use double pulse mode of the pulse generator for the clock waveform.

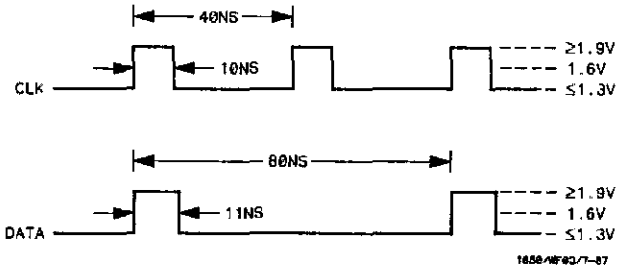

Figure 3-13. Waveform for Clock, Qualifier, and Data Inputs Test 3

3. Assign the pods under test to **Analyzer 1** in **System Configuration** as in previous test figure 3-4.

4. Assign the falling edge of the appropriate clock and all channels to label as in previous test figure 3-5, with the following pod clock assignments:

Pod 1-J clock, Pod 2-K clock,
Pod 3-any clock but L, Pod 4-M clock, Pod 5-N clock.

5. Set up the **STATE TRACE SPECIFICATION** for **Single Trace mode**, without sequencing levels and **Count Off** as in previous test figure 3-10.

6. Press RUN. The **STATE LISTING** will be displayed and alternate F's and 0's will be displayed as in figure 3-14.

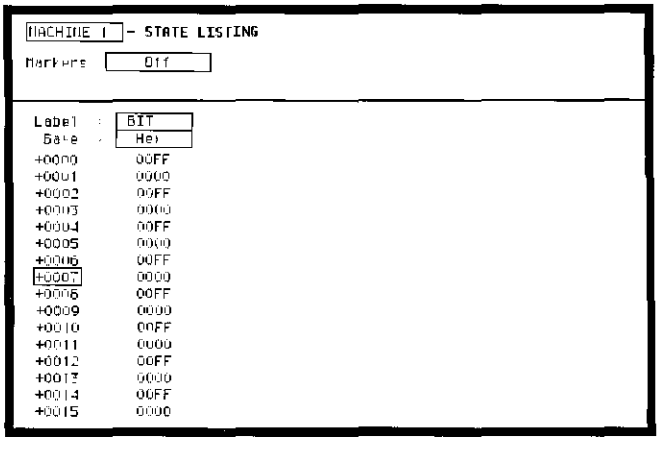

*Figure 3-14. **STATE LISTING** for Clock, Qualifier, and Data Inputs Test 3*

7. Disconnect the channels under test from the test connector and connect the remaining channels of the pod.

8. Repeat step 6.

9. Disconnect the pod of data channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

NOTE

When testing Pod 3, use any clock source but L clock.

10. Return to **System Configuration** and repeat steps 3 through 18 until all pods have been tested with each clock.

3-12. Clock, Qualifier, and Data Inputs Test 4

Description:

This performance test verifies the minimum swing voltages of the input probes a the maximum clock rate of the HP 1650A/51A when it is in single phase mode.

Specification:

Minimum swing: 600 mV peak-to-peak

Clock repetition rate: Single phase is 25 MHz maximum.

Clock pulse width: >= 10 ns at threshold.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1. Connect the HP 1650A/51A and test equipment as in figure 3-15.

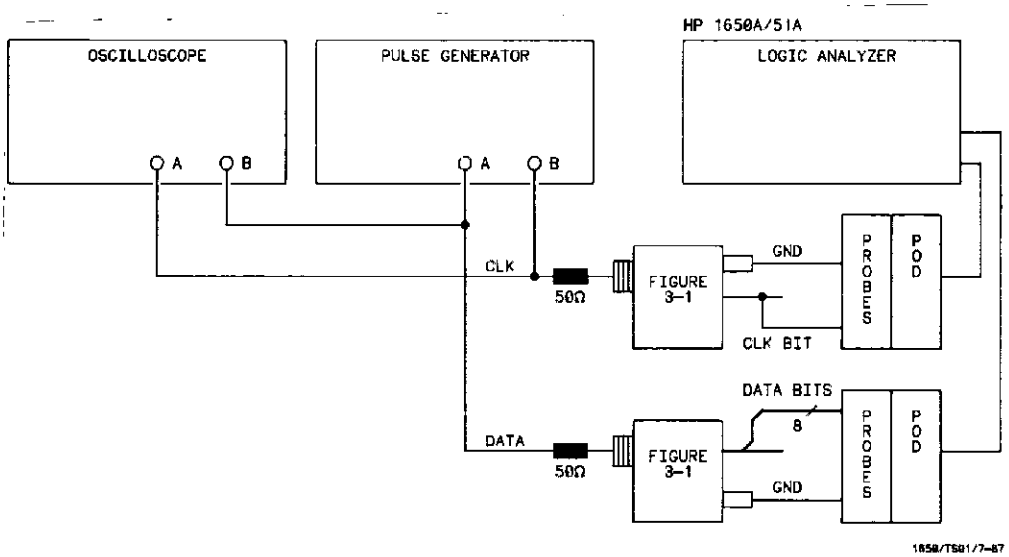

Figure 3-15. Setup for Clock, Qualifier, and Data Inputs Test 4

NOTE

In this setup, eight channels are connected to test half of the pod at a time. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-16. Use double pulse mode of the pulse generator for the clock pulse.

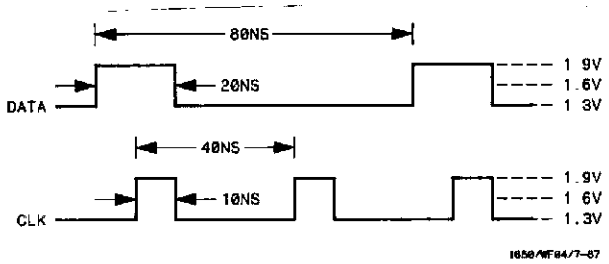

Figure 3-16. Waveform for Clock, Qualifier, and Data Input Test 4

3. Assign pod under test to **Analyzer 1** as in previous test figure 3-4.

4. Assign appropriate clock, rising clock transition and channels under test to label in **STATE FORMAT SPECIFICATION** menu as in previous test figure 3-5.

5. Set up the **STATE TRACE SPECIFICATION** for **Single Trace mode**, without sequencing levels, and **Count Off** as in previous test figure 3-9.

6. Press RUN. The **STATE LISTING** will be displayed showing alternate F's and 0's for the channels under test as in figure 3-17.

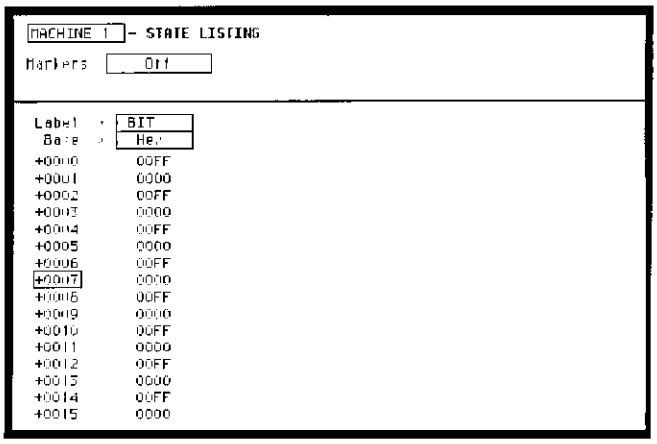

*Figure 3-17. **STATE LISTING** for Clock, Qualifier, and Data Inputs Test 4*

7. Disconnect the channels under test from the test connector and connect the remaining channels.

8. Repeat step 6.

9. Disconnect the pod of data channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all pods have been tested with each clock.

    a. Move cursor to **MACHINE** 1 by using front-panel knob.

    b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-13. Clock, Qualifier, and Data Inputs Test 5

Description:

This performance test verifies the maximum clock rate for mixed mode clocking during state operation of the HP 1650A/51A.

Specification:

Clock repetition rate: Single phase is 25 MHz maximum With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by > 50 ns.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1. Connect the HP 1650A/51A and test equipment as in figure 3-18 by connecting channels 0-3 and 8-11 of the pod under test to the test connector. On the slave clock transition the four bits of the lower byte are transferred to the logic analyzer, and on the master clock transition the four bits of the upper byte are transferred to the logic analyzer.

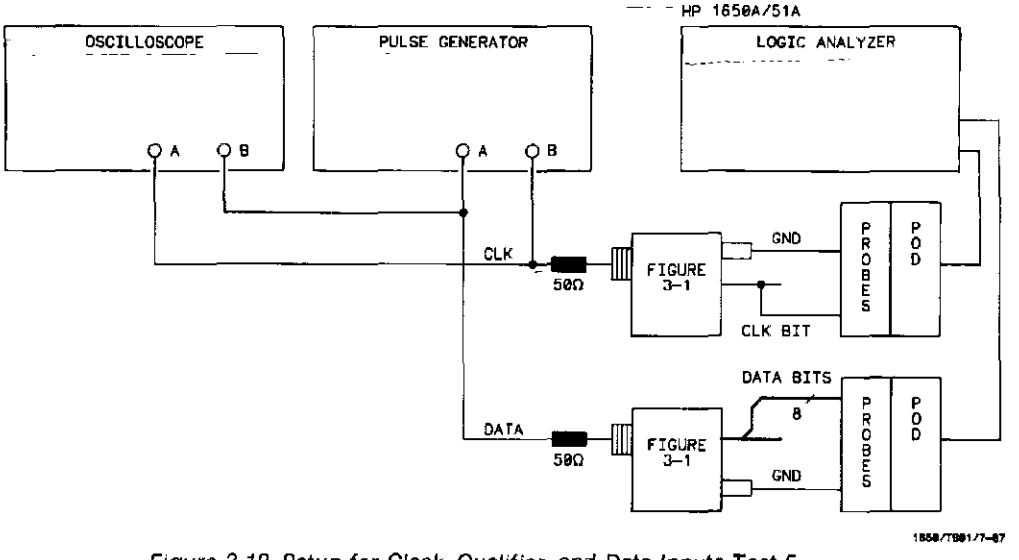

Figure 3-18. Setup for Clock, Qualifier, and Data Inputs Test 5

NOTE

In this setup, eight channels are connected to test half of the pod at one time. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-19. Use double pulse mode of the pulse generator for clock waveform.

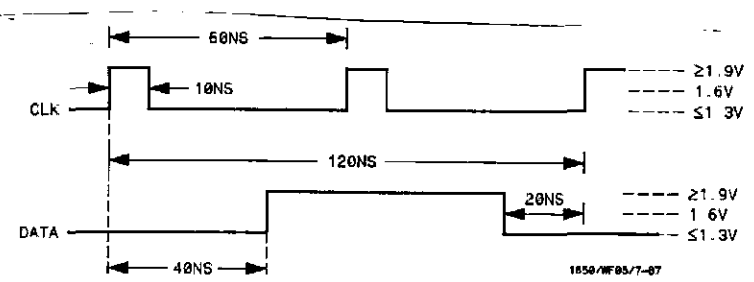

Figure 3-19. Waveforms for Clock, Qualifier, and Data Inputs Test 5

3. Assign the pods under test to **Analyzer 1** in **System Configuration** as in previous test figure 3-4.

4. Set up the **STATE FORMAT SPECIFICATION** as in figure 3-20, assigning the falling clock transition as master and the rising transition as slave Refer to steps below figure if unfamiliar with the menus.

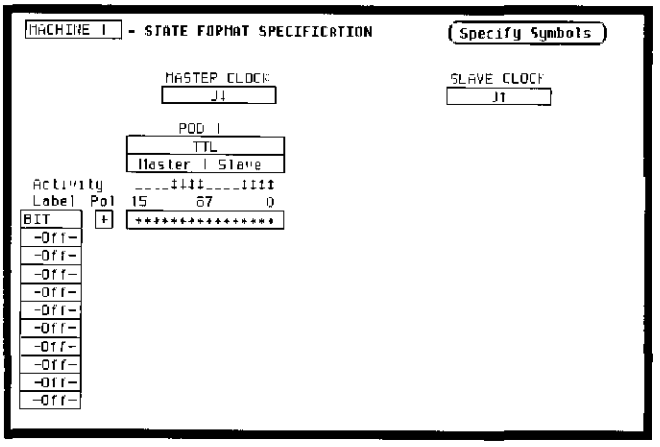

*Figure 3-20. **STATE FORMAT SPECIFICATION** for Clock, Qualifier, and Data Inputs Test 5*

a. Press front-panel FORMAT key.

b. Select **Mixed Clocks** mode by using the front-panel knob and SELECT key.

c. Assign falling clock transition to master clock and rising clock transition to slave clock.

d. Assign all channels to pod under test.

e. Assign all channels to pod under test by using front-panel knob and SELECT key.

5. Set up **STATE TRACE SPECIFICATION** for **Single Trace mode**, without sequencing levels, as in previous test figure 3-6, but with **Count Off**.

6. Press RUN. The **STATE LISTING** will be displayed as in figure 3-21.

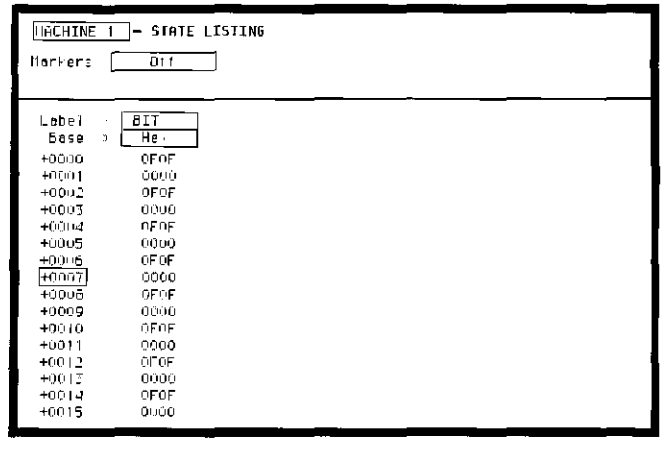

Figure 3-21. ***STATE LISTING*** *for Clock, Qualifier, and Data Inputs Test 5*

7. Disconnect the channels under test from the test connector and connect the remaining channels (4-7 and 12-15) of the pod.

8. Repeat step 6.

9. Disconnect the pod of data channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all pods have been tested with each clock.

a. Move cursor to **MACHINE 1** by using front-panel knob.

b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-14. Clock, Qualifier, and Data Inputs Test 6

Description:

This performance test verifies the maximum clock rate for demultiplexed clocking during state operation of the HP 1650A/51A.

Specification:

Clock repetition rate: Single phase is 25 MHz maximum. With time or state counting, minimum time between states is 60 ns Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by > 50 ns.

Equipment:

Pulse Generator
Oscilloscope
Test Connectors (figure 3-1)

Procedure:

1. Connect the HP 1650A/51A and test equipment as in figure 3-22 by connecting channels 0 - 7 of the pod under test to test connector.

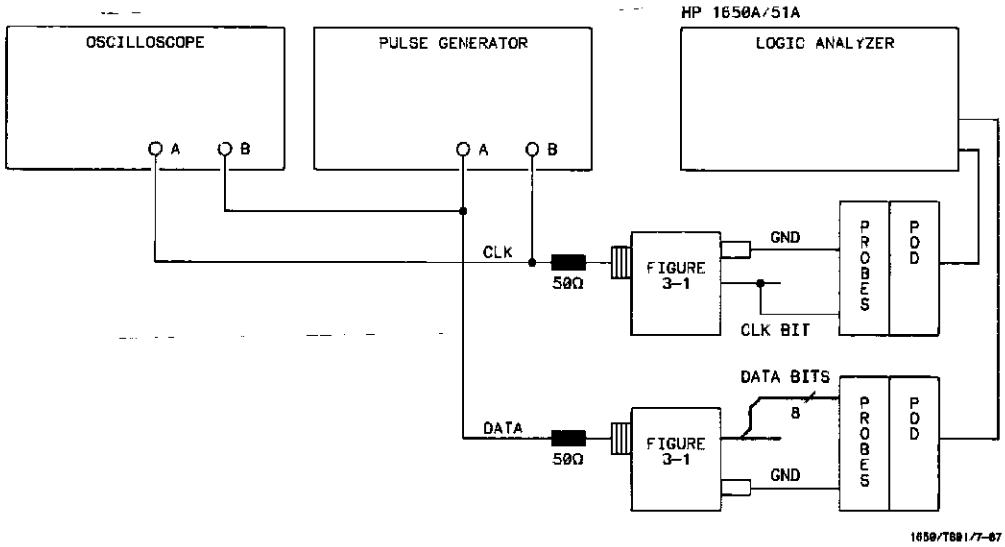

Figure 3-22. Setup for Clock, Qualifier, and Data Inputs Test 6

NOTE

In this setup, eight channels are connected to test half of the pod at one time. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-23. Use double pulse mode of pulse generator for clock waveform.

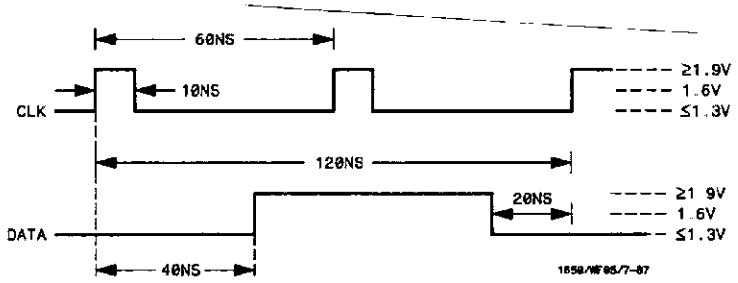

Figure 3-23. Waveforms for Clock, Qualifier, and Data Inputs Test 6

3. Assign the pods under test to **Analyzer 1** in **System Configuration** as in previous test figure 3-4.

4. Set up the **STATE FORMAT SPECIFICATION** as in figure 3-24, assigning the falling clock transition as master and the rising transition as slave. Refer to steps below figure if unfamiliar with the menus.

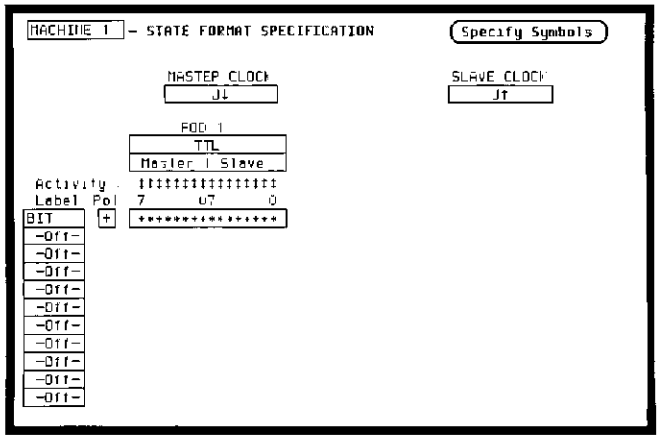

Figure 3-24. **STATE FORMAT SPECIFICATION** *for Clock, Qualifier, and Data Inputs Test 6*

a. Press front-panel FORMAT key.

b. Select **Demultiplex** clock mode by using the front-panel knob and SELECT key.

c. Assign falling clock transition to master clock and rising clock transition to slave clock.

d. Assign all channels to pod under test.

5. Set up **STATE TRACE SPECIFICATION** for **Single Trace mode**, without sequencing levels as in previous test figure 3-6 but with **Count Off.**

6. Press RUN. The **STATE LISTING** will be displayed as in figure 3-25.

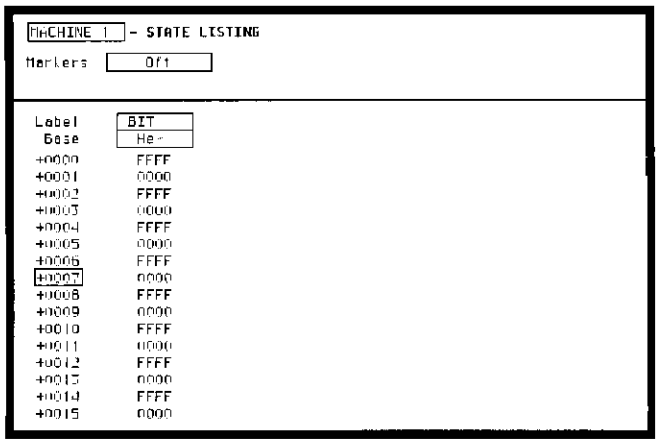

Figure 3-25. ***STATE LISTING*** for Clock, Qualifier, and Data Inputs Test 6

7. Disconnect the channels under test from the test connector and connect the remaining channels of the pod.

8. Repeat step 6.

9. Disconnect the pod of data channels under test from the probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all pods have been tested with each clock.

a. Move cursor to **MACHINE 1** by using front-panel knob.

b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-15. GLITCH TEST

Description:

This performance test verifies the glitch detection specification of the HP 1650A/51A.

Specification:

Minimum detectable glitch: 5 ns wide at the threshold.

Equipment:

Pulse Generator
Oscilloscope
Test Connector (figure 3-1)

Procedure:

1. Connect the test equipment as in figure 3-26. The clock input is not used for the glitch performance test.

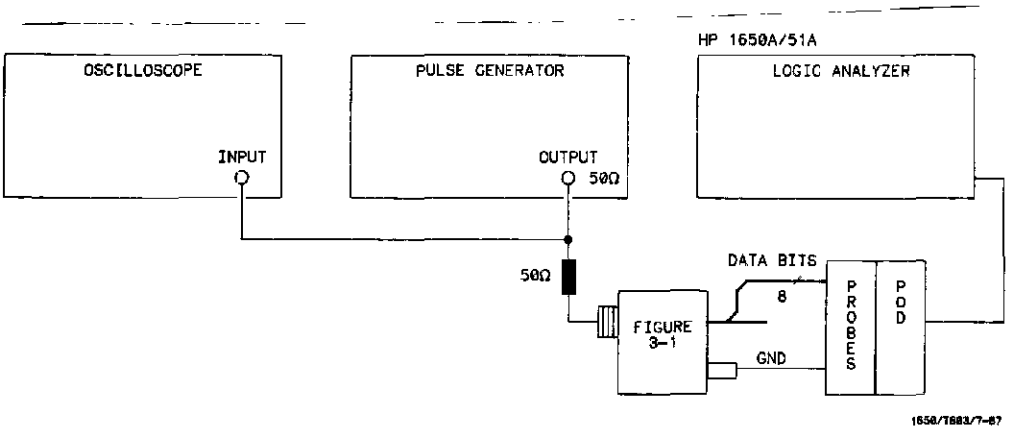

Figure 3-26. Setup for Glitch Test

NOTE

In this setup, eight channels are connected to test half of the pod at one time. Ground lead must be grounded to ensure accurate test results

2. Set pulse generator for output in figure 3-27.

Figure 3-27. Waveform for Glitch Test

3. Set up the **System Configuration** menu for assigning pod under test to **Analyzer 1** as in figure 3-28.

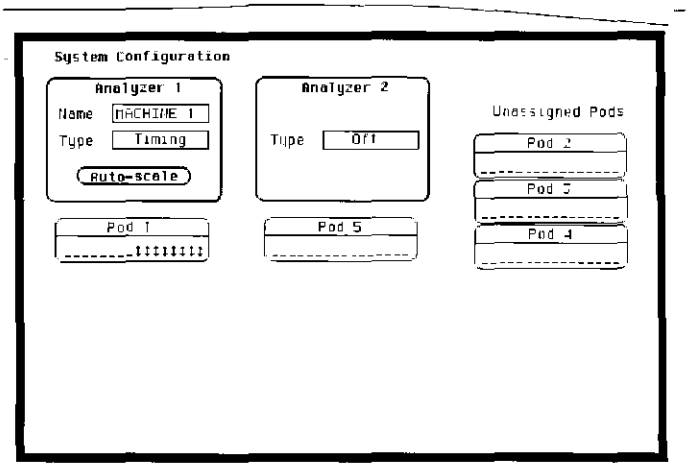

*Figure 3-28. **System Configuration** Menu for Glitch Test*

a. Select **System Configuration** menu. This is power-up default menu.

b. Set analyzer **Type** to **Timing**.

c. Assign pod under test to **Analyzer 1** by using front-panel knob and SELECT key.

Set up the **TIMING FORMAT SPECIFICATION** menu to assign all bits of pod under test to a label as in figure 3-29.

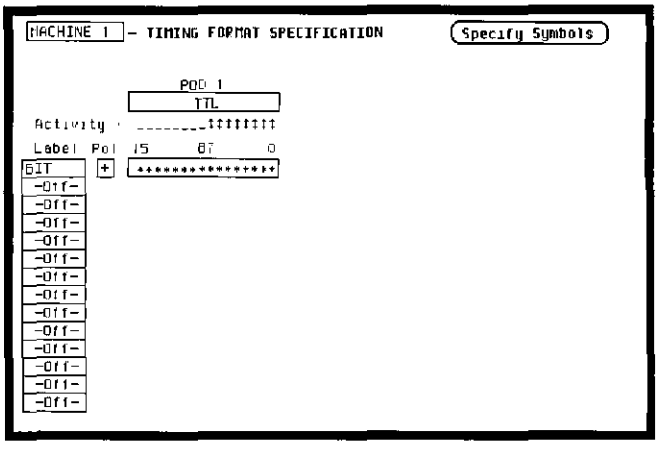

Figure 3-29. ***TIMING FORMAT SPECIFICATION*** *Menu for Glitch Test*

NOTE

This is the power-up default mode of this menu.

a. Turn on label for pod under test by using front-panel knob and SELECT key.

b. Assign all channels in pod under test to label by using front-panel knob and SELECT key.

5. Set up the **TIMING TRACE SPECIFICATION** menu as in figure 3-30.

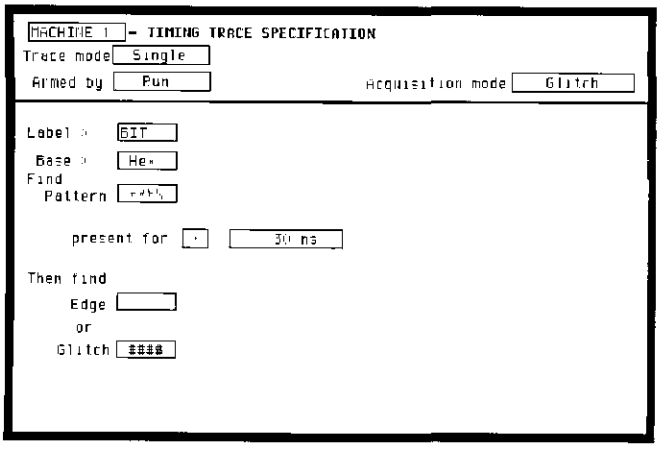

Figure 3-30 ***TIMING TRACE SPECIFICATION*** *Menu for Glitch Test*

a. Select **Single Trace mode.**

b. Set **Acquisition Mode** to **Glitch.**

c. Set **Find Pattern** to all DON'T CARE (X's) and **present for >30.00 r**

d. Set **Then find Glitch** on all channels.

6. Press RUN. The analyzer will acquire data and show glitches on channels under test as in figure 3-31.

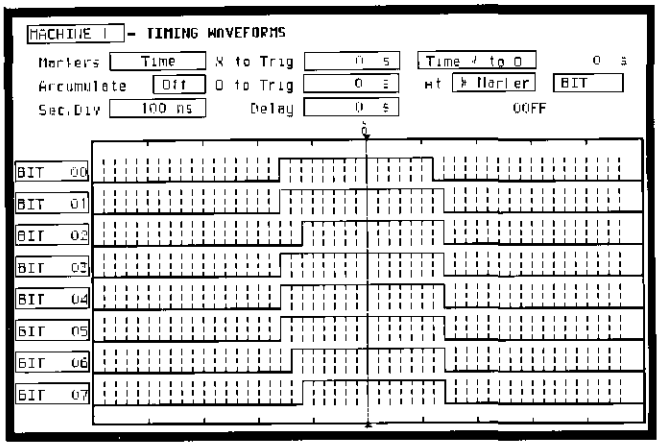

Figure 3-31. ***TIMING WAVEFORMS*** *for Glitch Test*

NOTE

If system clock and data synchronize, glitches may be displayed on the ***TIMING WAVEFORMS*** *menu as valid data transitions.*

7. Disconnect channels under test and connect remaining eight channels to be tested.

8. Repeat step 6.

9. Disconnect pod of data channels under test from probe tip assembly and connect the next pod of data channels to be tested.

10. Return to **System Configuration** and repeat steps 3 through 9 until all the pods have been tested.

    a. Move cursor to **MACHINE** 1 by using front-panel knob and SELECT key.

    b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-16. THRESHOLD ACCURACY TEST

Description:

This procedure verifies the threshold accuracy within the three ranges stated in the specification.

Specification:

Threshold accuracy: 150 mV accuracy over the range -2.0 to +2.0 volts; 300 mV accuracy over the ranges -9.9 to -2.1 volts and +2.1 to +9.9 volts.

Equipment:

Power Supply
Test Connector (figure 3-1)

Procedure:

1. Connect the test equipment as in figure 3-32.

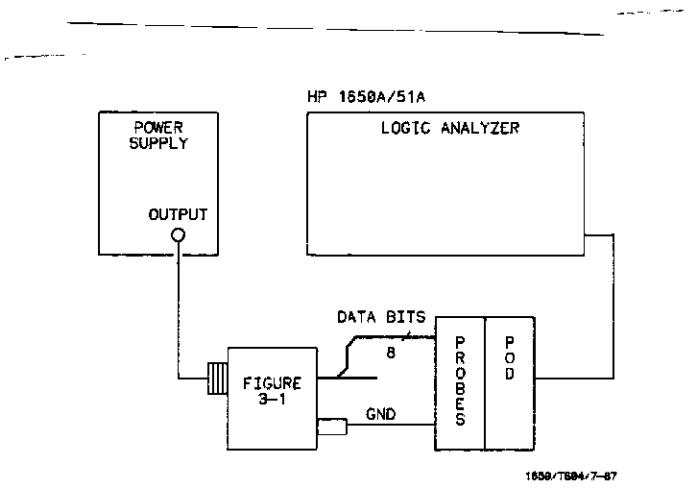

Figure 3-32. Setup for Threshold Accuracy Test

NOTE

In this setup, eight channels are connected to test half of the pod at a time. Ground lead must be grounded to ensure accurate test results.

2. Set up the **System Configuration** menu for assigning pod under test to **Analyzer 1** as in figu 3-33.

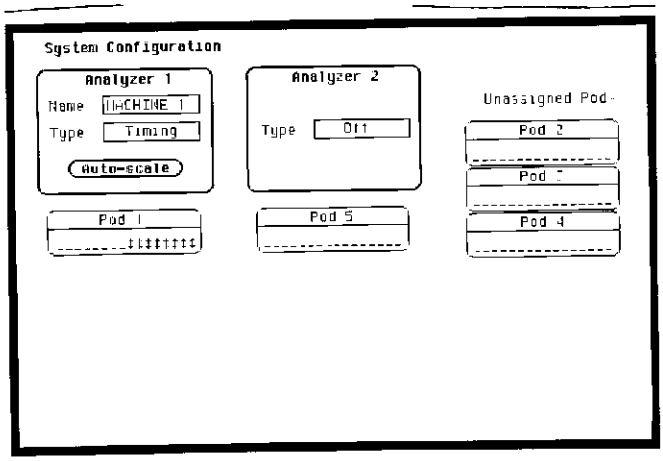

Figure 3-33. **System Configuration** *for Threshold Accuracy Test*

a. Select **System Configuration** menu. (This is the power-up default menu.)

b. Assign pod under test to **Analyzer 1** by using front-panel knob and SELECT key.

Configure the **TIMING FORMAT SPECIFICATION** menu for **User defined** pod threshold of **+0.0 V** for the pod under test and assign all bits of the pod to a label as in figure 3-34.

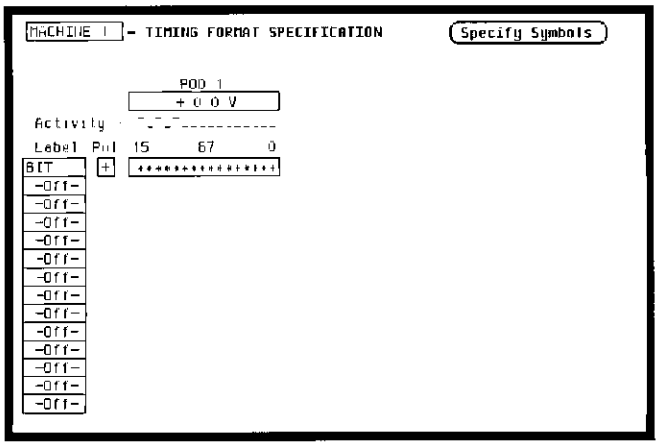

Figure 3-34. ***TIMING FORMAT SPECIFICATION*** *1 for Threshold Accuracy Test*

a. Select **TIMING FORMAT SPECIFICATION** menu by pressing front-panel FORMAT key.

b. Assign **User defined** pod threshold by using front-panel knob and SELECT key.

c. **Modify label** by using front-panel knob and SELECT key.

d. Assign all bits of pod under test to label by using front-panel knob and SELECT key.

4. Configure the **TIMING TRACE SPECIFICATION** menu for **Single Trace mode** and **Glitch Acquisition mode** as in figure 3-35.

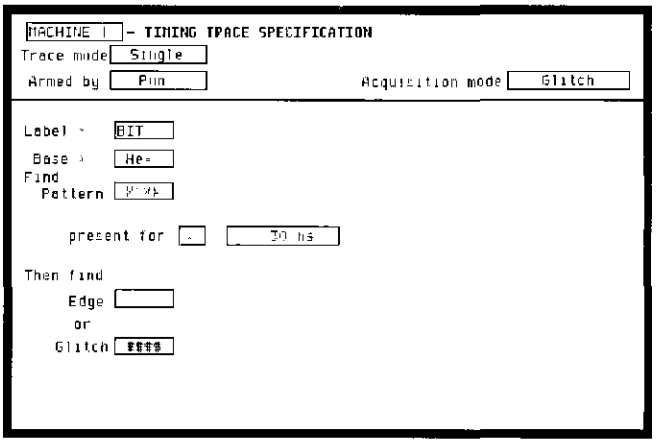

*Figure 3-35. **TIMING TRACE SPECIFICATION** for Threshold Accuracy Test*

a. Select **TIMING TRACE SPECIFICATION** menu by pressing front-panel TRACE key.

b. Assign **Single Trace mode** and **Glitch Acquisition mode** by using the front-panel knob and SELECT key.

c. Set **FIND Pattern** to all DON'T CARE (X's) and **present for >30.00 ns.**

d. Set **Then find Glitch** on all channels.

5. Adjust the power supply output for +150 mV.

6. Press RUN. Data displayed on **TIMING WAVEFORMS** will be all high for the pod under test as in figure 3-36.

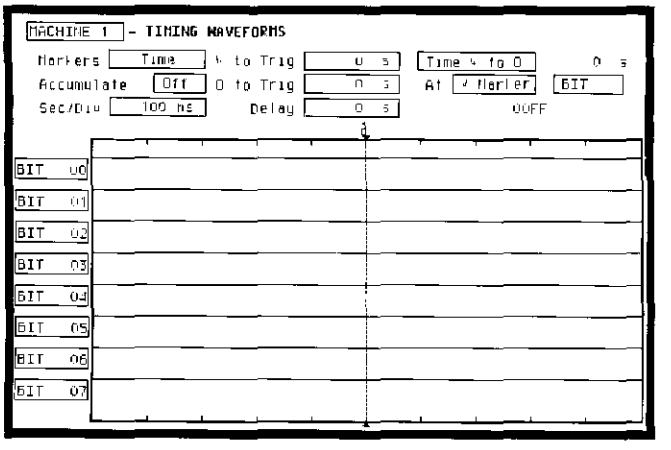

*Figure 3-36. **TIMING WAVEFORMS** 1 for Threshold Accuracy Test*

7. Adjust power supply for output of -150 mV.

8. Press RUN. Data displayed on the **TIMING WAVEFORMS** will be all low for the channels under test as in figure 3-37.

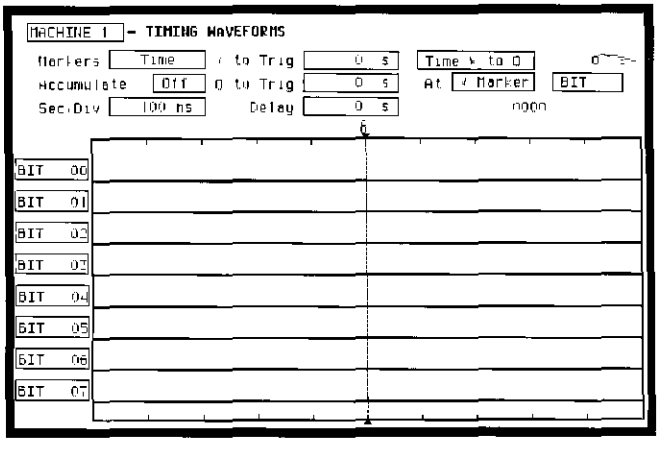

*Figure 3-37. **TIMING WAVEFORMS** 2 for Threshold Test*

9. Return to the **TIMING FORMAT SPECIFICATION** and change **User defined Pod Threshold** to **+9.9V** as in figure 3-38.

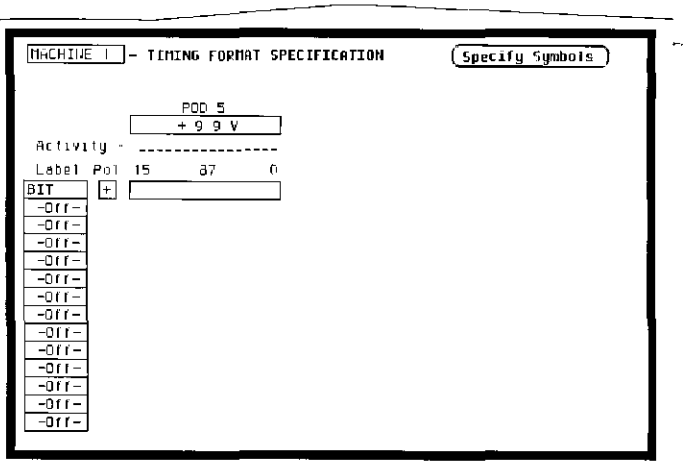

Figure 3-38. ***TIMING FORMAT SPECIFICATION*** *2 for Threshold Accuracy Test*

a. Select **TIMING FORMAT SPECIFICATION** menu by pressing front-panel FORMAT key.

b. Change pod threshold level assignment by using front-panel knob and SELECT key.

10. Adjust power supply for output of **+10.2 V**.

11. Press RUN. Data displayed on the **TIMING WAVEFORMS** will be all high for the pod under test as in previous figure 3-36.

12. Adjust power supply for output of **+9.6 V**.

13. Press RUN. Data displayed on the **TIMING WAVEFORMS** will be all low as in previous figure 3-37

14. Change the **User defined Pod Threshold** in the **TIMING FORMAT SPECIFICATION** to **-9.9 V** as in figure 3-39.

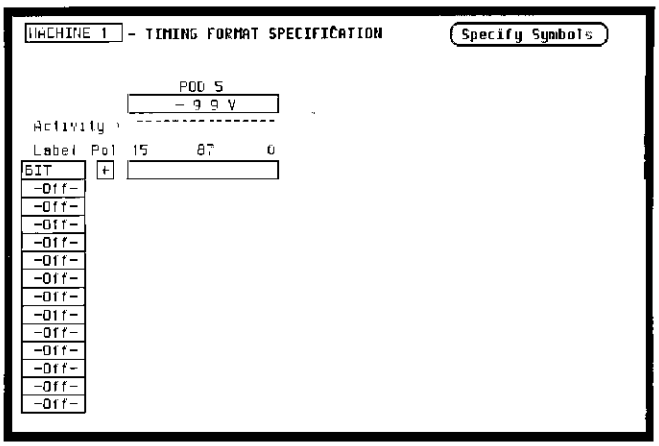

Figure 3-39. ***TIMING FORMAT SPECIFICATION*** *3 for Threshold Accuracy Test*

a. Select **TIMING FORMAT SPECIFICATION** menu by pressing front-panel FORMAT key.

b. Change pod threshold level assignment by using front-panel knob and SELECT key.

15. Adjust power supply for output of **-9.6 V.**

16. Press RUN. Data displayed in the **TIMING WAVEFORMS** will be all high for pod under test as in figure 3-36.

17. Adjust power supply for output of **-10.2 V.**

18. Press RUN. Data displayed in the **TIMING WAVEFORMS** will be all low for pod under test as in figure 3-37.

19. Disconnect the eight channels connected to test connector and connect remaining channels of pod to be tested.

20. Repeat steps 14 through 18 and then steps 3 through 13.

21. Disconnect pod of data channels under test from probe tip assembly and connect next pod of data channels to be tested.

22. Return to **System Configuration** and repeat steps 2 through 21 until all pods have been tested.

    a. Move cursor to **MACHINE 1** by using front-panel knob and SELECT key.

    b. Invoke **System Configuration** by using front-panel knob and SELECT key.

3-17. DYNAMIC RANGE TEST

Description:

This procedure verifies the dynamic range of the threshold of each pod.

Specification:

Dynamic Range: +/- 10 volts about the threshold.

Equipment:

Power Supply
Test Connector (figure 3-1)

Procedure:

1. Connect the test equipment as in figure 3-40.

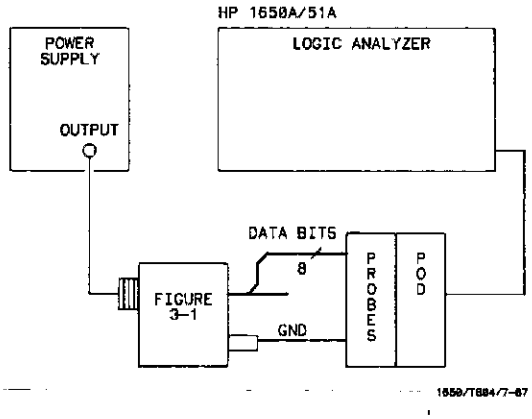

Figure 3-40. Setup for Dynamic Range Test

NOTE

In this setup, eight channels are connected to test half of the pod at a time. Ground lead must be grounded to ensure accurate test results.

2. Set up the **System Configuration** menu for assigning the pod under test to **Analyzer 1** as in figure 3-41.

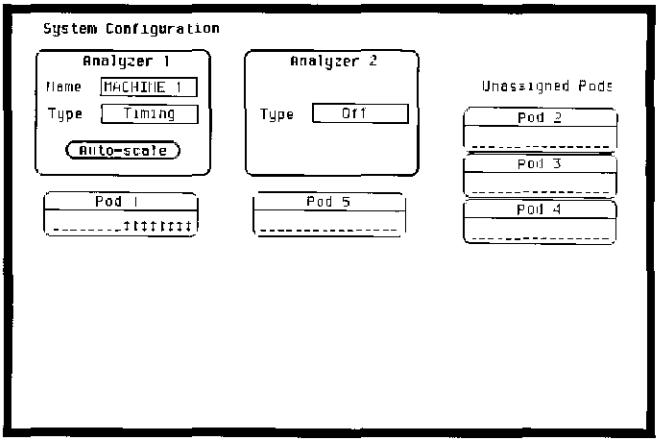

Figure 3-41. ***System Configuration*** *for Dynamic Range Test*

a. Select **System Configuration** menu. (This is the power-up default menu.)

b. Assign pod under test to **Analyzer 1** by using front panel knob and SELECT key.

Configure the **TIMING FORMAT SPECIFICATION** menu for **User defined** pod threshold of **-1.0 V** for the pod under test and assign all the bits of the pod to a label as in figure 3-42.

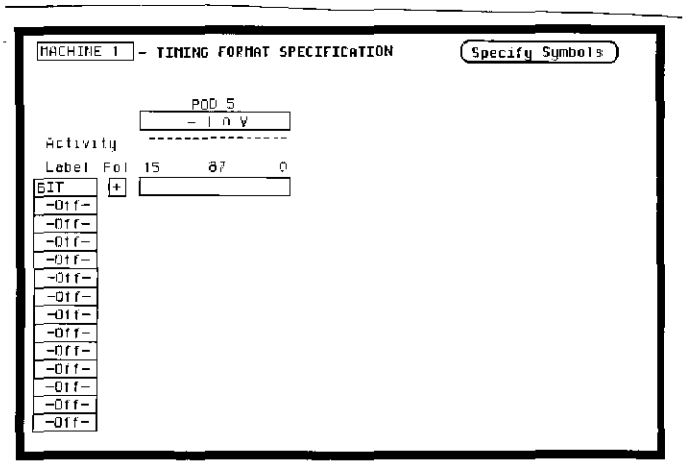

Figure 3-42. ***TIMING FORMAT SPECIFICATION*** *for Dynamic Range Test*

a. Select **TIMING FORMAT SPECIFICATION** menu by pressing front-panel FORMAT key.

b. Assign **User defined** pod threshold by using front-panel knob and SELECT key.

c. **Modify label** by using front-panel knob and SELECT key.

d. Assign all bits of pod under test to label by using front-panel knob and SELECT key.

4. Configure the **TIMING TRACE SPECIFICATION** menu for **Single Trace mode** and **Glitch Acquisition mode** as in figure 3-43.

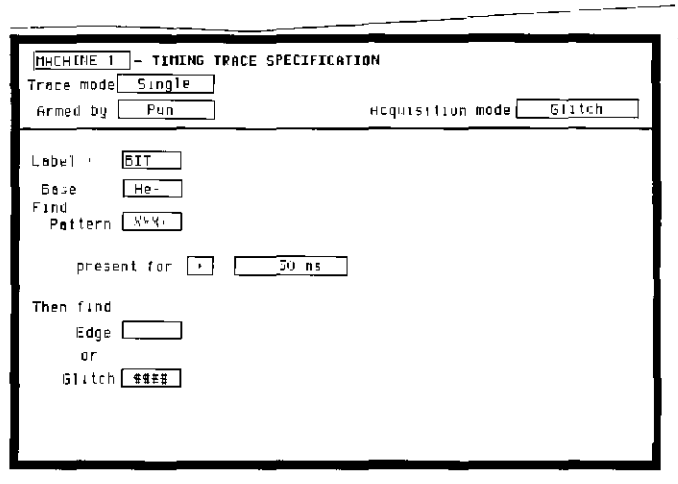

*Figure 3-43. **TIMING TRACE SPECIFICATION** for Dynamic Range Test*

a. Select **TIMING TRACE SPECIFICATION** menu by pressing front-panel TRACE key.

b. Assign **Single Trace mode** and **Glitch Acquisition mode** by using the front-panel knob and SELECT key.

c. Set **Find Pattern** to all DON'T CARE (X's) and **present for >30.00 ns.**

d. Set **Then find Glitch** on all channels.

5. Adjust the power supply output for +9.0 V.

6. Press RUN. Data displayed on **TIMING WAVEFORMS** will be all high for pod under test as in figure 3-44.

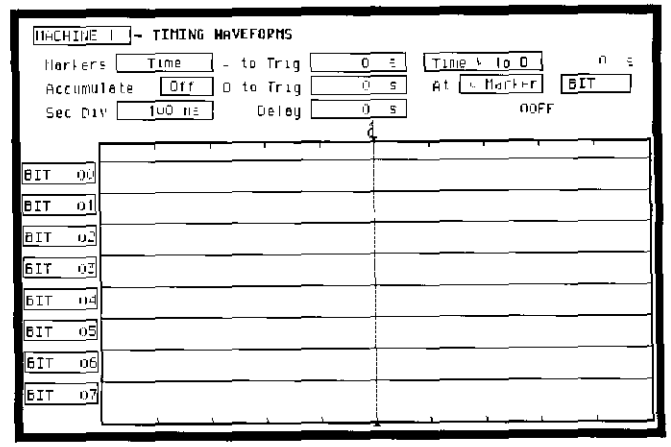

Figure 3-44. ***TIMING WAVEFORMS*** *1 for Dynamic Range Test*

7. Adjust power supply for output of -9.0 V.

8. Change **FORMAT SPECIFICATION** for threshold of **+1.0 V**. Refer to figure 3-41.

9. Press RUN. Data displayed on the **TIMING WAVEFORMS** will be all low for channels under test as in figure 3-45.

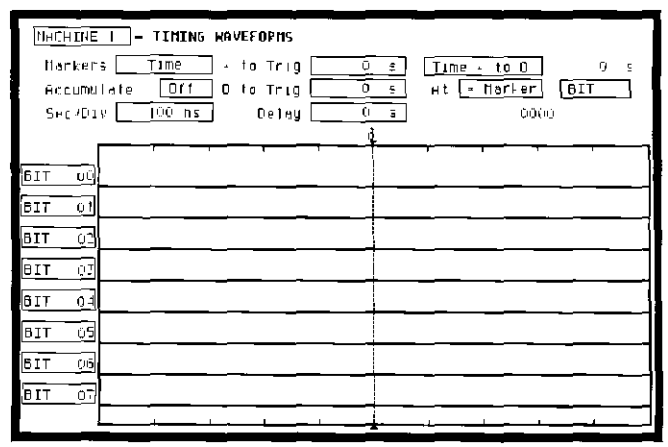

Figure 3-45. ***TIMING WAVEFORMS*** *2 for Dynamic Range Test*

6. Press RUN. Data displayed on **TIMING WAVEFORMS** will be all high for pod under test as in figure 3-44.

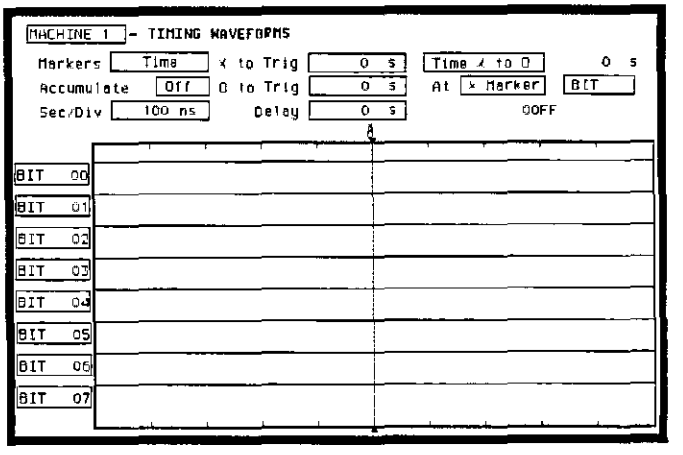

*Figure 3-44. **TIMING WAVEFORMS** 1 for Dynamic Range Test*

7. Adjust power supply for output of -9.0 V.

8. Change **FORMAT SPECIFICATION** for threshold of **+1.0 V**. Refer to figure 3-41.

9. Press RUN. Data displayed on the **TIMING WAVEFORMS** will be all low for channels under test as in figure 3-45.

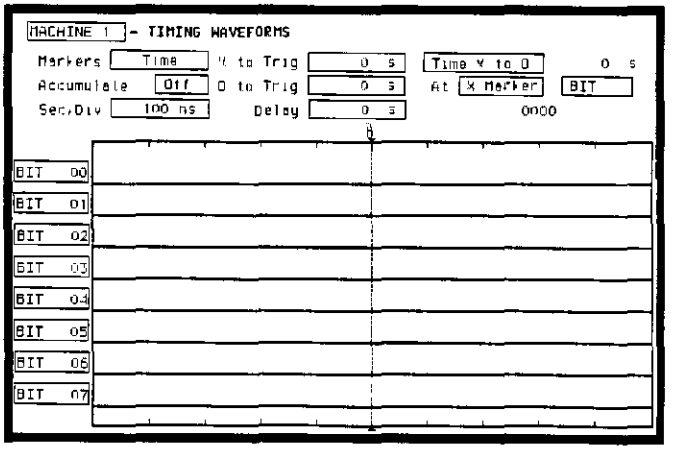

*Figure 3-45. **TIMING WAVEFORMS** 2 for Dynamic Range Test*

Table 3-1. Performance Test Record

Hewlett-Packard
Model 1650A/51A
Logic Analyzer

Serial
Number _____

Tested by _____

Work Order No. _____

Date Tested _____

Recommended Calibration
Interval 24 Months

PARAGRAPH	TEST	RESULTS	Passed	Failed
3-9	CLOCK, QUALIFIER, AND DATA INPUTS TEST 1	POD1		
		POD2		
		POD3		
		POD4		
		POD5		
3-10	CLOCK, QUALIFIER, AND DATA INPUTS TEST 2	POD1		
		POD2		
		POD3		
		POD4		
		POD5		
3-11	CLOCK, QUALIFIER, AND DATA INPUTS TEST 3	POD1		
		POD2		
		POD3		
		POD4		
		POD5		
3-12	CLOCK, QUALIFIER, AND DATA INPUTS TEST 4	POD1		
		POD2		
		POD3		
		POD4		
		POD5		
3-13	CLOCK, QUALIFIER, AND DATA INPUTS TEST 5	POD1		
		POD2		
		POD3		
		POD4		
		POD5		

Table 3-1. Performance Test Record (continued)

PARAGRAPH	TEST	RESULTS		
3-14	CLOCK, QUALIFIER, AND DATA INPUTS TEST 6		Passed	Failed
		POD1	_____	_____
		POD2	_____	_____
		POD3	_____	_____
		POD4	_____	_____
		POD5	_____	_____
3-15	GLITCH TEST	POD1	_____	_____
		POD2	_____	_____
		POD3	_____	_____
		POD4	_____	_____
		POD5	_____	_____
3-16	THRESHOLD ACCURACY TEST	POD1	_____	_____
		POD2	_____	_____
		POD3	_____	_____
		POD4	_____	_____
		POD5	_____	_____
3-17	DYNAMIC RANGE TEST	POD1	_____	_____
		POD2	_____	_____
		POD3	_____	_____
		POD4	_____	_____
		POD5	_____	_____

SECTION 4. ADJUSTMENTS

Table of Contents

SECTION 4
ADJUSTMENTS

4-1. INTRODUCTION

This section provides adjustment procedures for the HP 1650A/51A. The assemblies with adjustments are: the power supply, CRT monitor, and the system board. Figures in this section are the testpoint and adjustment locations for the HP 1650A/51A.

NOTE

An instrument warm-up of 15 minutes is recommended, but not required, before adjustment procedures are performed.

4-2. EQUIPMENT REQUIRED

Equipment required for adjustments is listed in the Recommended Test Equipment table in section 1 of this manual. Any equipment that satisfies the critical specification listed in the table may be substituted for the recommended model.

WARNING

Read the Safety Summary at the beginning of this manual before performing any adjustment procedures.

4-3. CALIBRATION INTERVAL

The recommended calibration interval for the HP 1650A/51A is two years. The adjustments are set at the factory on assemblies when they are tested. However, adjustments may be necessary after repairs have been made to the instrument. Usually the only assembly that may require adjustments is the assembly that has been replaced.

CAUTION

The adjustment procedures are performed with the top cover of the instrument removed. Take care to avoid shorting or damaging internal parts of the instrument.

4-4. POWER SUPPLY ASSEMBLY ADJUSTMENT

1. Disconnect power cord from HP 1650A/51A. Refer to figure 4-1 or 4-2, depending on the power supply assembly installed, for testpoint and adjustment locations.
2. Connect the negative lead of the voltmeter to Power Supply Assembly ground.
3. Connect the positive lead of the voltmeter to +5V on the Power Supply Assembly.
4. Connect the power cord to the HP 1650A/51A and put power switch in ON position.
5. Voltmeter should indicate voltage within the range of +5.050 V to +5.150 V.

6. If voltmeter reading is out of this range, adjust +5 ADJ on Power Supply Assembly to +5.100 V ± .050 V (+5.050 V to +5.150 V).

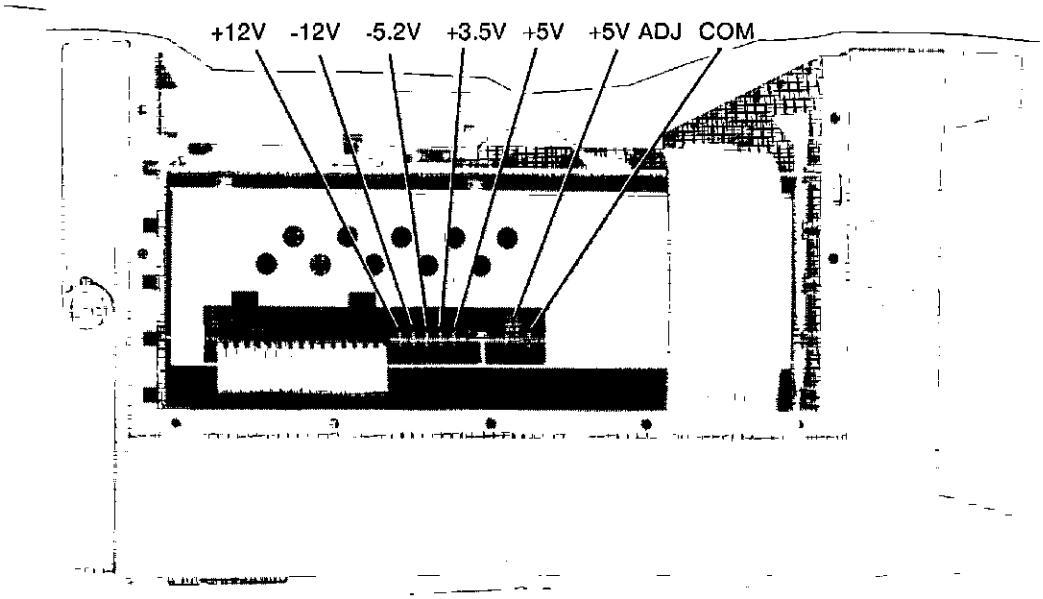

Figure 4-1. HP 1650A/51A Power Supply Assembly I Testpoints and Adjustment Location

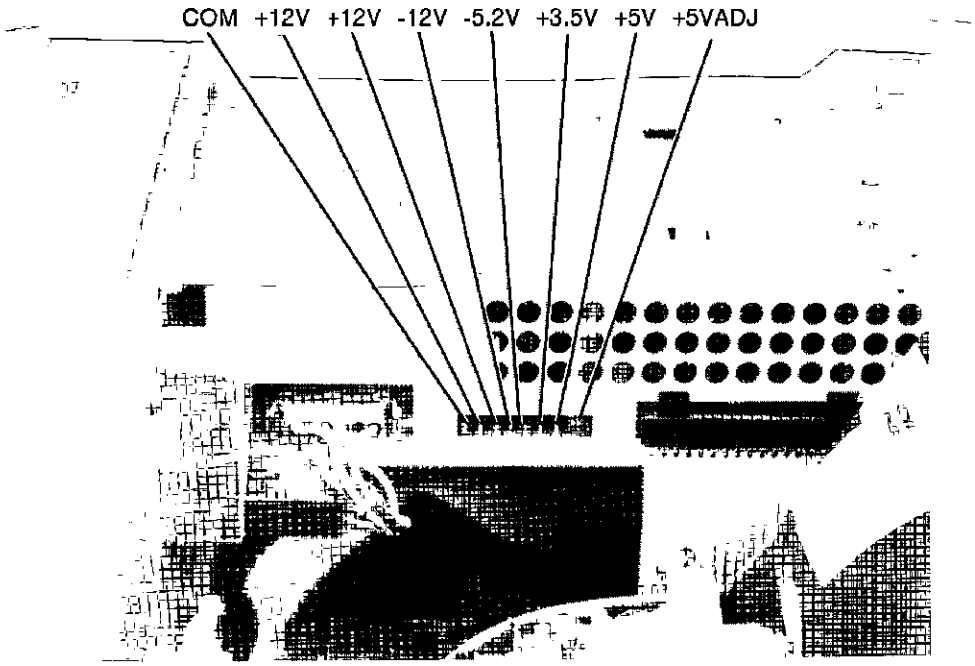

Figure 4-2. HP 1650A/51A Power Supply Assembly II Testpoints and Adjustment Location

4-5. CRT MONITOR ASSEMBLY ADJUSTMENTS

4-6. Intensity, Sub-bright, and Contrast Adjustment

1. Refer to figure 4-3 for adjustment locations.

2. Place **TIMING WAVEFORMS** menu on the screen of the HP 1650A/51A, by pressing front-panel Display key.

NOTE

This menu is used because it has characters throughout the screen which are watched during the procedures. Any other menu may be used; however, the adjustments may not be as accurate if characters and/or lines are not displayed throughout the screen.

3. Set rear-panel INTENSITY to the minimum setting.

4. Adjust sweep board Sub-bright control to the lowest setting of brightness where menu is visible on the CRT screen.

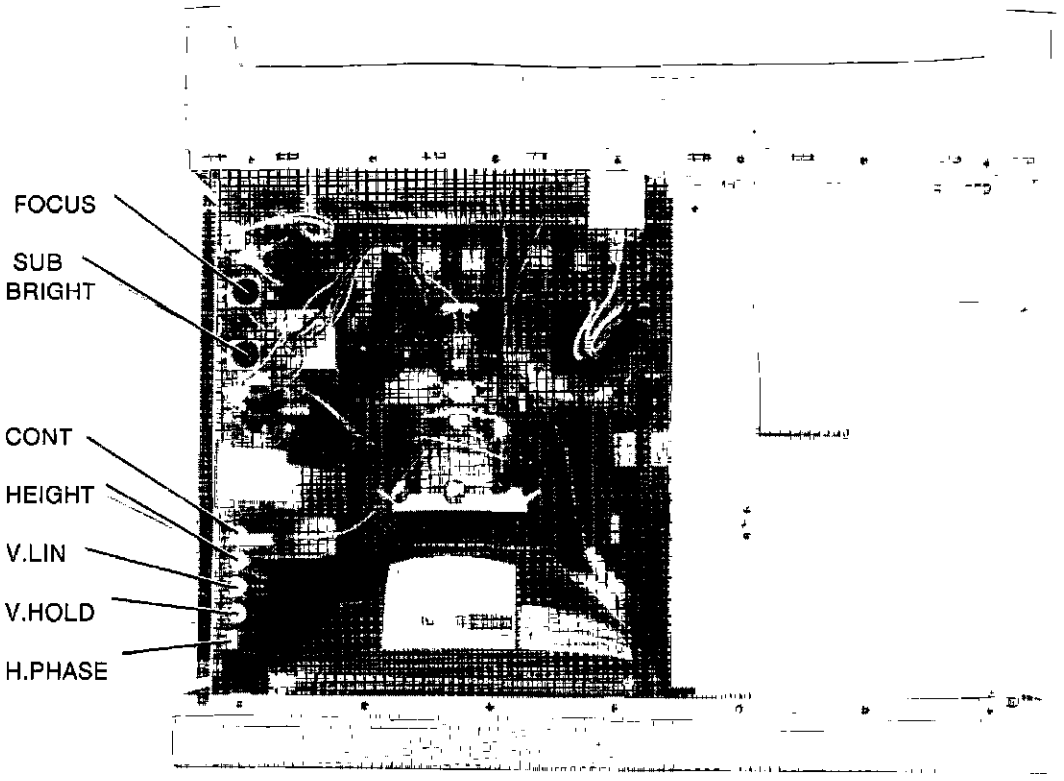

Figure 4-3. Adjustment Locations of HP 1650A/51A CRT Monitor Assembly

5. Turn rear-panel INTENSITY to bring up the intensity level on screen. Screen intensity should be at a comfortable viewing level and the position of both adjustments should be close to mid-range.

6. Press RUN and then STOP.

7. Adjust CONT so the error message is easily seen.

4-7. Focus Adjustment

1. Refer to figure 4-3 for adjustment locations.

2. Place **TIMING WAVEFORMS** menu on the screen of the HP 1650A/51A by pressing the front-panel DISPLAY key.

3. Adjust sweep board Focus control for sharp pixels in the center of the screen menu. Note Focus control position.

4. Adjust sweep board Focus for sharp pixels at the corners of the screen Note Focus control position.

5. Set sweep board Focus control for mid-position between the two positions noted in steps 3 and 4 for best over-all pixel focus.

4-8. Horizontal Phase, Vertical Linearity, and Height Adjustments

1. Refer to figure 4-3 for adjustment locations.

2. Place **TIMING WAVEFORMS** menu on the screen of the HP 1650A/51A by pressing front-panel DISPLAY key.

NOTE

This menu is used because it has characters and lines throughout the menu which are watched during the procedures. Any other menu may be used, however, the adjustments may not be as accurate.

3. Adjust sweep board H. PHASE to center the menu horizontally on the CRT screen.

4. Adjust sweep board V. LIN so top and bottom rows of text are equal in height. Text height should be approximately 1mm.

NOTE

The V. LIN and Height adjustments are interactive and may need to be repeated as necessary.

5. Adjust sweep board Height to give the screen menu top and bottom borders equal to the side borders of the menu.

6. Readjust steps 4 and 5 as necessary for a uniform display of the screen menu.

4-9. SYSTEM BOARD ASSEMBLY THRESHOLD ADJUSTMENT

1. Disconnect power cord from HP 1650A/51A.

2. Connect negative (-) lead of voltmeter to TP GND. Refer to figure 4-4 for testpoint and adjustment locations.

3. Connect positive (+) lead of voltmeter to HP 1650A **A1TP2**, or HP 1651A **A1TP3** on the System Board Assembly.

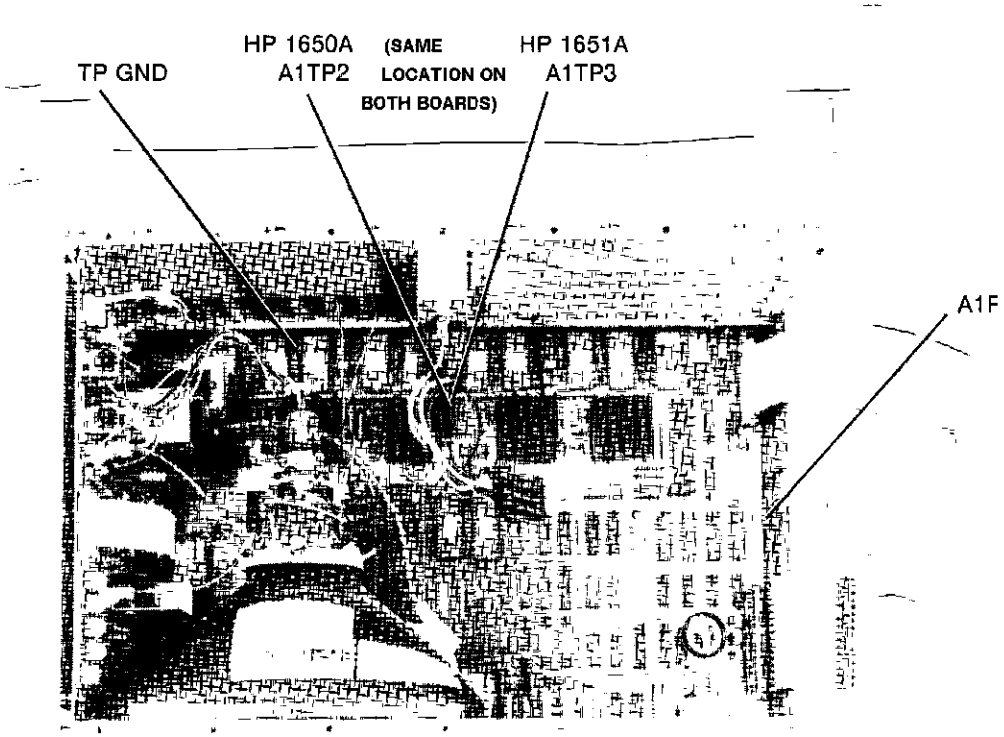

Figure 4-4. System Board Assembly Testpoint and Adjustment Locations

4. Connect power cord to logic analyzer and turn instrument power to ON.

5. Assign HP 1650A POD 3, or HP 1651A POD 2, to a machine in the **System Configuration** menu by using front-panel knob and SELECT key.

6. Set **User defined Pod Threshold** of the pod assigned in the previous step to **-9.9 V** in the Format Specification menu by using the following steps if unfamiliar with the menus.

   a. Press front-panel FORMAT key.

   b. Move cursor to **TTL** (threshold field) and press SELECT.

   c. Assign **User defined** threshold by using front-panel knob and SELECT key.

7. Voltmeter readout should indicate voltage within the range of -.975 V to -1.005 V (-.990 V ± .015 V).

8. Set **User defined Pod Threshold** of the pod assigned in the previous step to **+9.9 V** in the Format Specification menu.

9. Note voltmeter readout. Voltage reading should be within the range of +.975 V to +1.0005 V (+.990 V ± .015 V).

10. If either voltage reading is not within the given range, use the procedure below to adjust the threshold level.

    a. Set **User defined Pod threshold** of the pod assigned to **-9.9 V**.

    b. Adjust A1R57 for reading of -.9900 V ± .0005 V. Refer to figure 4-3 for adjustment locations.

    c. Set **User defined Pod threshold** to **+9.9 V**.

    d. Note the difference between this reading and +.9900 V.

    e. Adjust A1R57 so the difference in step d is halved, ± .0005 V.

    EXAMPLES:

    If reading is + .9952 V, the difference is .0052 V. Adjust A1R57 for +.9926 V ± .0005 V.

    If reading is + .9834 V, the difference is .0066 V. Adjust A1R57 for +.9867 V ± .0005 V.

SECTION 5. REPLACEABLE PARTS

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SECTION 5
REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists the abbreviations used in the parts list and throughout the manual. Table 5-2 lists all replaceable parts for the instrument. Table 5-3 contains the names and addresses corresponding to the code number of the manufacturer. The parts of the disassembled HP 1650A in figure 5-1 are the main replaceable assemblies in the HP 1650A/51A.

5-2. ABBREVIATIONS

Table 5-1 lists the abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviations are used, one in all capital letters, and one in partial or no capital letters. However, elsewhere in the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

5-3. PARTS LIST

Table 5-2 is a list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Electrical assemblies and their components in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. Reference designation.

b. Hewlett-Packard part number.

c. Part number Check Digit (CD).

d. Total quantity (QTY) in instrument or on assembly. The total quantity is given once and at the first appearance of the part number in the list.

e. Description of the part.

f. Typical manufacturer of part in an identifying five-digit code.

5-4. EXCHANGE ASSEMBLIES

Some parts used in this instrument have been set up for an exchange program. This program allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance-verified by the factory. The cost is significantly less than that of a new part. The exchange parts have a part number in the form XXXXX-695XX.

After receiving the repaired exchange part from Hewlett-Packard, a United States customer has thirty days to return the faulty assembly. For orders not originating in the United States, contact the local Hewlett-Packard service organization. If the faulty assembly is not returned within the warranty time limit, the customer will be charged an additional amount. The additional amount will be the difference in price between a new assembly and that of an exchange assembly.

5-5. ORDERING INFORMATION

To order a part in the material list, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part not listed in the material list, include the instrument part number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard Sales and Service Office.

5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum amount for parts ordered through a local Hewlett-Packard office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices.

So Hewlett-Packard can provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard office. Addresses and telephone numbers are located at the back of this manual.

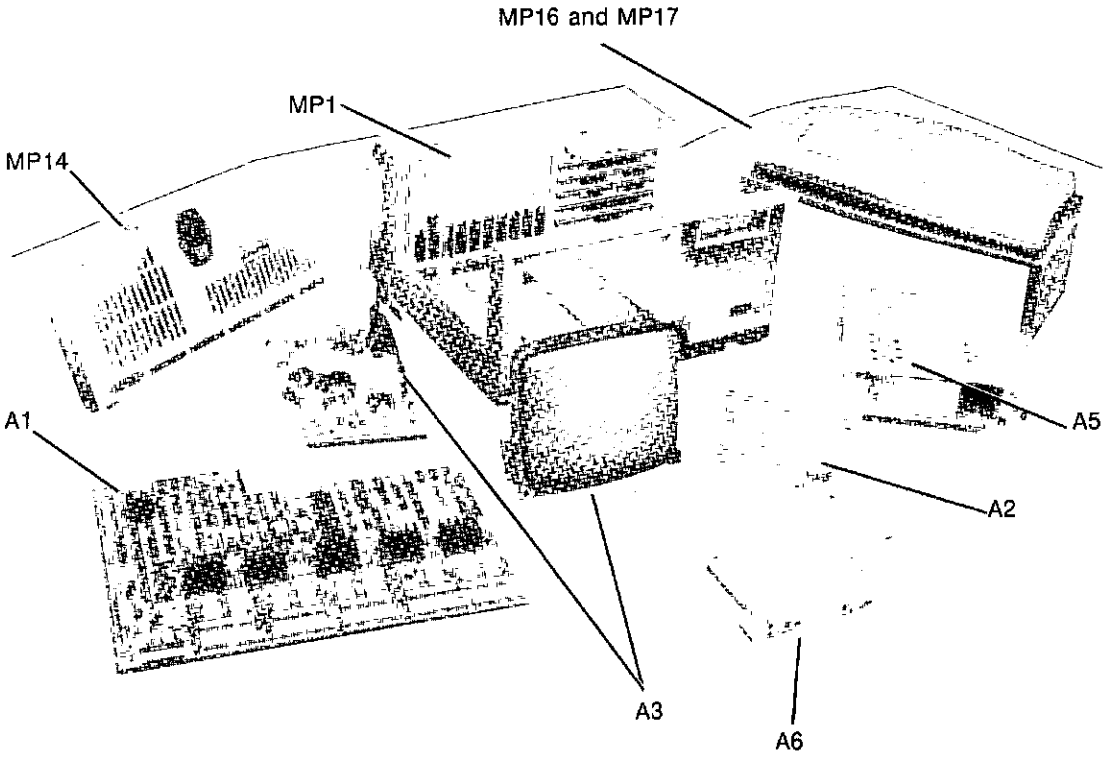

Figure 5-1. HP 1650A/51A Main Replaceable Parts

Table 5-1 Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	=assembly
B	=fan,motor
BT	=battery
C	=capacitor
CR	=diode;diode thyristor; varactor
DL	=delay line
DS	=annunciator;lamp;LED
E	=misc. electrical part
F	=fuse
FL	=filter
H	=hardware
J	=electrical connector (stationary portion);jack
L	=coil,inductor
MP	=misc. mechanical part
P	=electrical connector (moveable portion);plug
Q	=transistor;SCR; triode thyristor
R	=resistor
RT	=thermistor
S	=switch;jumper
T	=transformer
TB	=terminal board
TP	=test point
U	=integrated circuit, microcircuit
V	=electron tube, glow lamp
VR	=voltage regulator, breakdown diode
W	=cable
X	=socket
Y	=crystal unit(piezo-electric or quartz)

ABBREVIATIONS

A	=amperes
A/D	=analog-to-digital
AC	=alternating current
ADJ	=adjust(ment)
AL	=aluminum
AMPL	=amplifier
ANLG	=analog
ANSI	=American National Standards Institute
ASSY	=assembly
ASTIG	=astigmatism
ASYNCHRO	=asynchronous
ATTEN	=attenuator
AWG	=American wire gauge
BAL	=balance
BCD	=binary-code decimal
BD	=board
BFR	=buffer
BIN	=binary
BRDG	=bridge
BSHG	=bushing
BW	=bandwidth
C	=ceramic,cermet (resistor)
CAL	=calibrate,calibration
CC	=carbon composition
CCW	=counterclockwise
CER	=ceramic
CFM	=cubic feet/minute
CH	=choke
CHAM	=chamfered
CHAN	=channel
CHAR	=character
CM	=centimeter
CMOS	=complementary metal-oxide-semiconductor
CMR	=common mode rejection
CNDCT	=conductor
CNTR	=counter
CON	=connector
CONT	=contact
CRT	=cathode-ray tube
CW	=clockwise
D	=diameter
D/A	=digital-to-analog
DAC	=digital-to-analog converter
DARL	=darlington
DAT	=data
DBL	=double
DBM	=decibel referenced to 1mW
DC	=direct current
DCDR	=decoder
DEG	=degree
DEMUX	=demultiplexer
DET	=detector
DIA	=diameter
DIP	=dual in-line package
DIV	=division
DMA	=direct memory access
DPDT	=double-pole, double-throw
DRC	=DAC refresh controller
DRVR	=driver
DWL	=dowel
ECL	=emitter coupled logic
ELAS	=elastomeric
EXT	=external
F	=farads;metal film (resistor)
FC	=carbon film/ composition
FD	=feed
FEM	=female
FF	=flip-flop
FL	=flat
FM	=foam;from
FR	=front
FT	=gain bandwidth product
FW	=full wave
FXD	=fixed
GEN	=generator
GND	=ground(ed)
GP	=general purpose
GRAT	=graticule
GRV	=groove
H	=henries;high
HD	=hardware
HDND	=hardened
HG	=mercury
HGT	=height
HLCL	=helical
HORIZ	=horizontal
HP	=Hewlett-Packard
HP-IB	=Hewlett-Packard Interface Bus
HR	=hour(s)
HV	=high voltage
HZ	=Hertz
I/O	=input/output
IC	=integrated circuit
ID	=inside diameter
IN	=inch
INCL	=include(s)
INCAND	=incandescent
INP	=input
INTEN	=intensity
INTL	=internal
INV	=inverter
JFET	=junction field-effect transistor
JKT	=jacket
K	=kilo(10^3)
L	=low
LB	=pound
LCH	=latch
LCL	=local
LED	=light-emitting diode
LG	=long
LI	=lithium
LK	=lock
LKWR	=lockwasher
LS	=low power Schottky
LV	=low voltage
M	=mega(10^6),megohms; meter(distance)
MACH	=machine
MAX	=maximum
MFR	=manufacturer
MICPROC	=microprocessor
MINTR	=miniature
MISC	=miscellaneous
MLD	=molded
MM	=millimeter
MO	=metal oxide
MTG	=mounting
MTLC	=metallic
MUX	=multiplexer
MW	=milliwatt
N	=nano(10^{-9})
NC	=no connection
NMOS	=n-channel metal-oxide-semiconductor
NPN	=negative-positive-negative
NPRN	=neoprene
NRFR	=not recommended for field replacement
NSR	=not separately replaceable
NUM	=numeric
OBD	=order by description
OCTL	=octal
OD	=outside diameter
OP AMP	=operational amplifier
OSC	=oscillator
P	=plastic
P/O	=part of
PC	=printed circuit
PCB	=printed circuit board
PD	=power dissipation
PF	=picofards
PI	=plug in
PL	=plate(d)
PLA	=programmable logic array
PLST	=plastic
PNP	=positive-negative-positive
POLYE	=polyester
POS	=positive,position
POT	=potentiometer
POZI	=pozidrive
PP	=peak-to-peak
PPM	=parts per million
PRCN	=precision
PREAMP	=preamplifier
PRGMBL	=programmable
PRL	=parallel
PROG	=programmable
PSTN	=position
PT	=point
PW	=potted wirewound
PWR	=power
R-S	=reset-set
RAM	=random-access memory
RECT	=rectifier
RET	=retainer
RF	=radio frequency
RGLTR	=regulator
RGTR	=register
RK	=rack
RMS	=root-mean-square
RND	=round
ROM	=read-only memory
RPG	=rotary pulse generator
RX	=receiver
S	=Schottky-clamped; seconds(time)
SCR	=screw;silicon controlled rectifier
SEC	=second(time),secondary
SEG	=segment
SEL	=selector
SGL	=single
SHF	=shift
SI	=silicon
SIP	=single in-line package
SKT	=skirt
SL	=slide
SLDR	=solder
SLT	=slot(ted)
SOLD	=solenoid
SPCL	=special
SQ	=square
SREG	=shift register
SRQ	=service request
STAT	=static
STD	=standard
SYNCHRO	=synchronous
TA	=tantalum
TBAX	=tubeaxial
TC	=temperature coefficient
TD	=time delay
THD	=thread(ed)
THK	=thick
THRU	=through
TP	=test point
TPG	=tapping
TPL	=triple
TRANS	=transformer
TRIG	=trigger(ed)
TRMR	=trimmmer
TRN	=turn(s)
TTL	=transistor-transistor
TX	=transmitter
U	=micro(10^{-6})
UL	=Underwriters Laboratory
UNREG	=unregulated
VA	=voltampere
VAC	=volt,ac
VAR	=variable
VCO	=voltage-controlled oscillator
VDC	=volt,dc
VERT	=vertical
VF	=voltage,filtered
VS	=versus
W	=watts
W/	=with
W/O	=without
WW	=wirewound
XSTR	=transistor
ZNR	=zener
°C	=degree Celsius (Centigrade)
°F	=degree Fahrenheit
°K	=degree Kelvin

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01650-69501	4	1	SYSTEM BOARD ASSEMBLY (1650A-80 CHANNEL)	28480	01650-69501
A1	01651-69501	5	1	SYSTEM BOARD ASSEMBLY (1651A-32 CHANNEL)	28480	01651-69501
A2	01650-66503	0	1	KEYBOARD ASSEMBLY-ELASTOMERIC	28480	01650-66503
A3	2090-0204	9	1	CRT MONITOR ASSEMBLY	28480	2090-0204
A4	0960-0753	6	1	ROTARY PULSE GENERATOR	28480	0960-0753
A5	0950-1879	8	1	POWER SUPPLY ASSEMBLY	28480	0950-1879
A6	0950-1798	8	1	DISC DRIVE ASSEMBLY	28480	0950-1798
A7	01650-61606	6	1	INTENSITY ADJ ASSEMBLY	28480	01650-61606
A8	9135-0325	8	1	LINE FILTER/POWER/SWITCH/FUSE ASSEMBLY	28480	9135-0325
A9	01650-61608	7	5	PROBE TIP ASSEMBLY (1650A-80 CHANNEL)	28480	01650-61608
A9	01650-61608	7	2	PROBE TIP ASSEMBLY (1651A-32 CHANNELS)	28480	01650-61608
B1	3160-0521	3	1	FAN-TUBEAXIAL	28480	3160-0521
F1	2110-0003	0	1	FUSE 3A 110/120 V	28480	2110-0003
F1	2110-0043	8	1	FUSE 1.5A 220/240 V	28480	2110-0043
H1	0535-0113	8	10	TINNERMAN NUT	28480	0535-0113
H2	01650-00203	0	2	NUT PLATE (HANDLE)	28480	01650-00203
H3	0515-1035	0	22	FLATHD MS M3x8MM (FOOT)	28480	0515-1035
H4	0535-0056	1	4	LOCKNUT (CRT)	28480	0535-0056
H5	0515-0374	5	12	PANHD MS M3x10MM (FAN AND REAR PANEL)	28480	0515-0374
H6	0624-0530	3	8	SCREW 8-16 (BOTTOM-OUTSIDE)	28480	0624-0530
H7	2950-0001	8	1	NUTH 1/4x32x.093 (BNC)	28480	2950-0001
H8	0515-1135	7	4	FLATHD MS M3x25MM	28480	0515-1135
H9	0515-0372	2	2	PANHD M3x8MM	28480	0515-0372
H10	2190-0027	6	1	WASHER .256 .478 .02 (INT ADJ)	28480	2190-0027
H11	2950-0072	3	1	NUTH 1/4-32 .062	28480	2950-0072
H12	2190-0016	3	2	WASHER-IL .377 .507 .02 (BNC)	28480	2190-0016
H13	2950-0001	8	2	NUTH 3/8-32 .093 (BNC)	28480	2950-0001
H14	1400-0611	0	1	CLAMP-CABLE (DISC DRIVE)	28480	1400-0611
H15	01650-82401	1	2	SCREW-SHOULDER (HANDLE)	28480	01650-82401
MP1	01650-45201	1	1	CABINET-MOLDED PLASTIC	28480	01650-45201
MP2	01650-04901	2	1	HANDLE-BALE	28480	01650-04901
MP3	1460-1345	5	2	TILT STAND	28480	1460-1345
MP4	01650-47701	0	2	FOOT-MOLDED PLASTIC	28480	01650-47701
MP5	01650-01202	0	1	BRACKET-GROUND (CRT)	28480	01650-01202
MP6	01650-94301	5	1	LABEL-HP1650A IDENTIFICATION	28480	01650-94301
MP6	01651-94301	6	1	LABEL-HP1651A IDENTIFICATION	28480	01651-94301
MP7	01650-94305	9	1	LABEL-KEYBOARD	28480	01650-94305
MP8	01650-45204	4	2	KEYBOARD HOUSING	28480	01650-45204
MP9	01650-41901	0	1	KEYPAD-ELASTOMERIC	28480	01650-41901
MP10	01650-45205	5	1	KEYBOARD SPACER	28480	01650-45205
MP11				NOT ASSIGNED		
MP12	01650-46101	2	2	LOCKING PIN-PC BOARD	28480	01650-46101
MP13	5040-8823	2	1	KNOB GRAY	28480	5040-8823
MP14	01650-00201	1	1	REAR PANEL (1650A-80 CHANNEL)	28480	01650-00201
MP14	01651-00201	2	1	REAR PANEL (1651A-32 CHANNEL)	28480	01651-00201
MP15	5080-2054	3	1	LABEL CSA CERTIFICATION	28480	5080-2054
MP16	01650-04101	4	1	COVER-TOP	28480	01650-04101
MP17	01650-84501	6	1	POUCH (TOP COVER)	28480	01650-84501
MP18	01650-94303	7	1	LABELS-FIVE PROBES	28480	01650-94303
MP19	01650-29101	6	1	SPRING GROUND	28480	01650-29101
MP20	01650-25401	2	1	INSULATOR-DISC DRIVE	28480	01650-25401
P1	01650-63202	0	1	RS-232-C LOOPBACK CONNECTOR	28480	01650-63202
W1	01650-61601	9	1	CABLE-SWEEP	28480	01650-61601
W2	01650-61612	2	1	CABLE-DC POWER SUPPLY	28480	01650-61612
W3	01650-61604	2	1	CABLE-DISC DRIVE	28480	01650-61604
W4	01650-61605	3	2	CABLE-BNC-J11	28480	01650-61605
W5	01650-61605	3		CABLE-BNC-J12	28480	01650-61605
W6	01650-61602	0	1	CABLE-AC LINE FILTER	28480	01650-61602
W7	01650-61607	5	5	CABLE-PROBE 1650A-80 CHANNELS	28480	01650-61607
W7	01650-61607	5	2	CABLE-PROBE 1651A-32 CHANNELS	28480	01650-61607
W8	01650-61606	4	1	CABLE-INTENSITY ADJ	28480	01650-61606
W9	8120-1521	6	1	CABLE-POWER (STANDARD INSTRUMENT)	28480	8120-1521
W9	8120-1703	6	1	CABLE-POWER (OPTION 900-UK)	28480	8120-1703
W9	8120-0696	4	1	CABLE-POWER (OPTION 901-AUSTL)	28480	8121-0696
W9	8120-1692	2	1	CABLE-POWER (OPTION 902-EUR)	28480	8120-1692
W9	8120-2296	4	1	CABLE-POWER (OPTION 906-SWIT)	28480	8120-2296
W9	8120-2957	4	1	CABLE-POWER (OPTION 912-DEN)	28480	8120-2957
W9	8120-4600	8	1	CABLE-POWER (OPTION 917-AFRICA)	28480	8120-4600
A9	01650-61608	6		PROBE TIP ASSEMBLY	28480	01650-61608
A9A1	01650-82101	8	17	PROBE LEAD	28480	01650-82101

See introduction to this section for ordering information

Table 5-2 Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9A2	01650-82102	9	1	GROUND LEAD - LONG	28480	01650-82102
A9A3	01650-82103	0	2	GROUND LEAD - SHORT	28480	01650-82103

See introduction to this section for ordering information

Table 5-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
C0633	RIFA	BROMMA	SE	
S0167	FUJITSU LTD	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
1B546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92806
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	N V. PHILIPS-ELCOMA DEPARTMENT	EINDHOVEN	HL	02878
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52763	STETTNER ELECTRONICS INC	CHATTANOOGA	TN	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON	CA	92634
75915	LITTELFUSE INC	DES PLAINES	IL	60016

SECTION 6. SERVICE

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SECTION 6
SERVICE

6-1. INTRODUCTION

This section provides troubleshooting information for isolating a faulty assembly. Procedures are also provided for removing and installing the mainframe components of the HP 1650A/51A. Relative locations of the replaceable frame components are in figure 6-1, a top view of the HP 1650A/51A with the top cover removed.

6-2. SAFETY CONSIDERATIONS

Read the Safety Summary at the front of this manual before servicing the instrument. Before performing any procedure, review it for cautions and warnings.

WARNING

Maintenance should be performed by trained service personnel aware of the hazards involved (for example, fire and electrical shock). When maintenance can be performed without power applied, the power should be removed from the instrument.

6-3. LOGIC CONVENTION

Logic states are defined as follows:

0 — False, negated, inactive, or unasserted state.

1 — True, active, or asserted state.

Voltage levels representing logic states are as follows:

LOW (L) — The more negative of two voltage levels.

HIGH (H) — The more positive of two voltage levels.

Signals may be either HIGH true, or LOW true. The HP 1650A/51A contains both TTL and ECL ICs. Worst case voltage levels for troubleshooting and signature analysis are as follows (IC data sheet specifications may be more accurate):

TTL VOLTAGE LEVELS

Level	Voltage
LOW	less than 0.8 V
HIGH	greater than 2.0 V

ECL VOLTAGE LEVELS

Level	Voltage
LOW	less than -1.50 V
HIGH	greater than -1.10 V

Because ECL inputs are pulled down inside the IC, an unconnected ECL input is low. ECL outputs may be tied together the same way as open-collector TTL outputs. Thus, they may be wire-ANDed or wire-ORed.

CAUTION

Never remove or install any circuit board with the instrument power ON. Component damage may occur.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the display sweep board. To avoid electrical shock, the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and sweep boards to discharge before servicing this instrument.

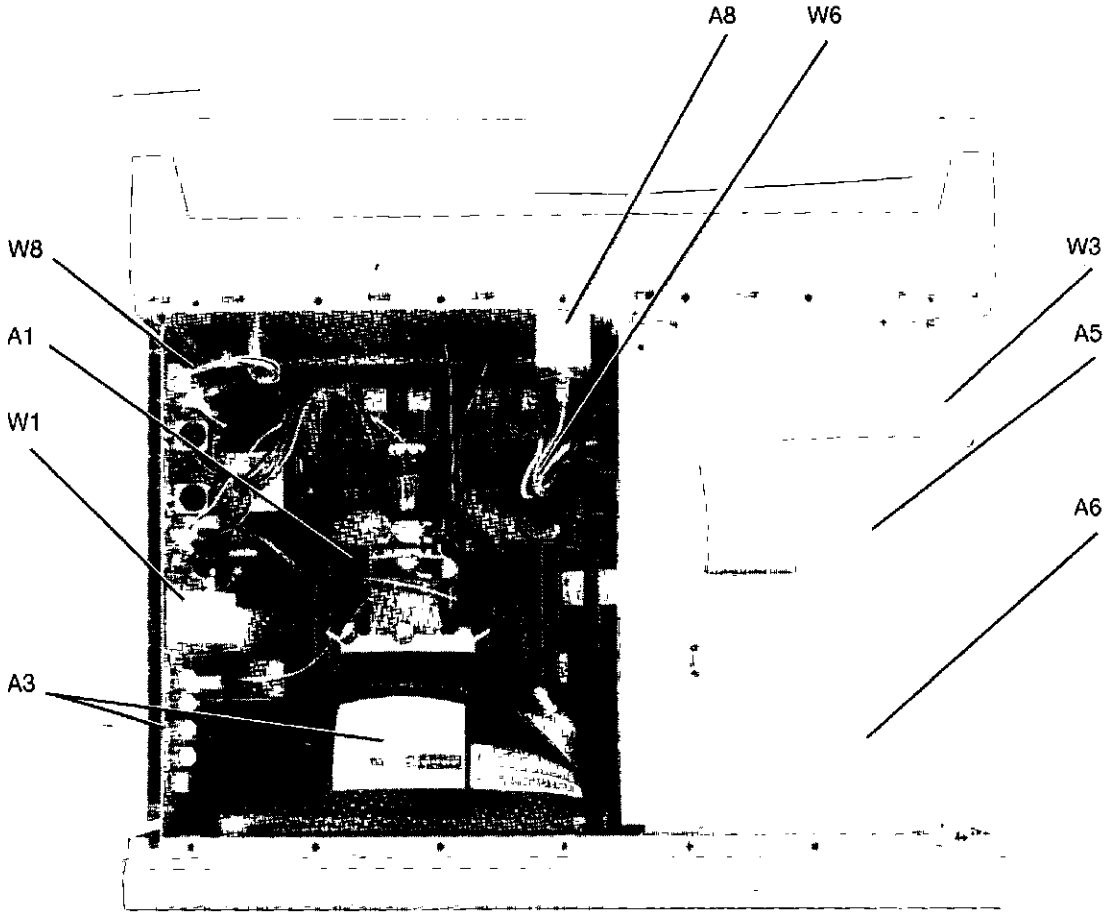


Figure 6-1. Replaceable Module and Cable Locations (Top Cover Removed)

6-4. BLOCK LEVEL THEORY OF OPERATION

The HP 1650A/1651A is an 80/32 channel state and timing logic analyzer. The human interface is a front-panel keypad and knob for instrument control and 9" (diagonal) white phosphor CRT for information display. Available on the rear panel is an RS-232-C port for communication to a printer or from a controller. Also on the rear panel are two BNCs for input or output of an external trigger.

The System Assembly Board is built around the 68000 microprocessor and powerful data acquisition ICs that probe, shape, store, and analyze data from a target system. An acquisition interface to the 68000 makes the data acquisition system fully compatible with the architecture of the 68000 microprocessor. The System Assembly Board contains the necessary circuitry to interface the keypad, CRT monitor, disc drive, and RS-232-C port

6-5. Data Acquisition

The data acquisition system consists of the data acquisition pods, acquisition ICs, and the interface to the 68000. The interface to the target system is through any of the data acquisition pods. There are five pods available on the HP 1650A (80 channels) and two pods available on the HP 1651A (32 channels). Each pod contains 16 input data probes and one external clock input for state mode measurements. The data probes can be used for state or timing measurements.

Each probe pod assembly consists of 17 twelve-inch twisted pairs of probe and tip assemblies that plug into a pod. This houses one end of a four and one-half (4.5) foot woven cable. The other end of the woven cable terminates at the rear panel of the logic analyzer. The woven cable consists of 17 nichrome signal lines, 34 signal return lines and 2 power supply lines All are woven together with polyaramid yarn.

Each probe input has an input impedance of 100 K ohms in parallel with approximately 6 pF. Probe can be grounded in two ways: with a common pod ground for state mode measurements, or a probe tip ground for higher frequency measurements.

The input signals are attenuated by a factor of 10 in the passive probe. The signals are applied to a comparator where they are compared against a voltage threshold to determine if the voltage level is above or below the threshold level. The comparator then shapes the single-ended signal and outputs it at an ECL level to the acquisition IC. The input data is then stored at the acquisition IC.

6-6. Arming Control

The two BNCs on the rear panel are J11 and J12 and are used for arming control of the HP1650A/51A acquisition ICs. An arm signal may be output from the ICs to the EXTERNAL TRIGGER OUTPUT, J12, or input to the ICs from EXTERNAL TRIGGER INPUT, J11.

6-7. Memory

The memory of the HP 1650A/1651A has three separate memories: one ROM and two RAM memories. The system (EP)ROM is 16K long by 8 wide and is used primarily for booting up the system and self-test storage. The system (D)RAM is 64K long by 4 wide and contains the operating system and the acquired data from the target system. Since the RAM is a volatile memory, the operating system is loaded at each power-up of the instrument via the built-in disc drive and a mini-floppy disc.

The display (D)RAM is 64K long by 4 wide and is cycle-shared between the 68000 and the display refresh circuitry. This is why the display bus is separate from the local bus. The two buses are separated by a set of address multiplexers and data buffers.

6-8. CRT Controller

The CRT controller provides the sync and timing signals needed by the CRT Monitor Assembly to drive the CRT.

The controller generates four signals: horizontal sync, vertical sync, display enable and a 6.25 kHz signal. The horizontal and vertical sync signals are applied to the CRT monitor assembly and to display PALs. The display PALs use the sync signals to generate the timing signals for the display RAM.

The CRT Monitor Assembly consists of the sweep board circuitry, a 9-inch white phosphor display CRT, and the CRT yoke. The assembly requires +5 and +12 volts, which it receives from the power supply via the System Board Assembly.

6-9. Disc Controller

The disc controller performs the necessary functions for reading or writing data to the built-in disc drive of the HP 1650A/51A. The disc controller interface to the 68000 is an 8-bit bidirectional bus for data, status, and control word transfers.

The built-in disc drive is a 3.5 inch double-sided Sony disc drive. Its main features are low power consumption, low height, and high reliability with simple mechanism and electronic circuitry.

6-10. Keypad and Knob Interface

The keypad and knob interface provide the circuitry to latch and send the keypad and knob data to the 68000.

The keypad of the HP1650A/51A is elastomeric and each key has a single function.

6-11. RS-232-C Interface

The controlling IC of the RS-232-C interface is a Signetics SCN2661 Enhanced Programmable Communications Interface (EPCI), a universal synchronous/asynchronous receiver/transmitter (USART) data communications IC.

The SCN2661 serializes parallel data from the 68000 for transmission. At the same time, it also receives serial data and converts it to parallel data characters for input to the 68000.

The IC contains a baud rate generator which can be programmed from the HP1650A/51A I/O menu for one of eight baud rates. Protocol, word length, stop bits length, and parity are also programmed via the I/O menu.

The DS14C88 and DS14C89 are line drivers/receivers used by the HP 1650A/51A for interface of terminal equipment with data communications equipment. Slew rate control is provided on the ICs eliminating the need for external capacitors.

6-12. Power Supply

The power supply is a 120W switching power supply. It has a dc output power connector and cable which connects to the System Board Assembly of the HP 1650A/51A. The ac input range to the power supply is 115V or 230V with the maximum power of 200W when operating at 48-66 Hz.

The power module supplies all necessary voltages to the System Board Assembly. The voltages necessary for operating the Disc Drive and Sweep/CRT/Yoke Assembly are also supplied by the power supply via the System Board Assembly

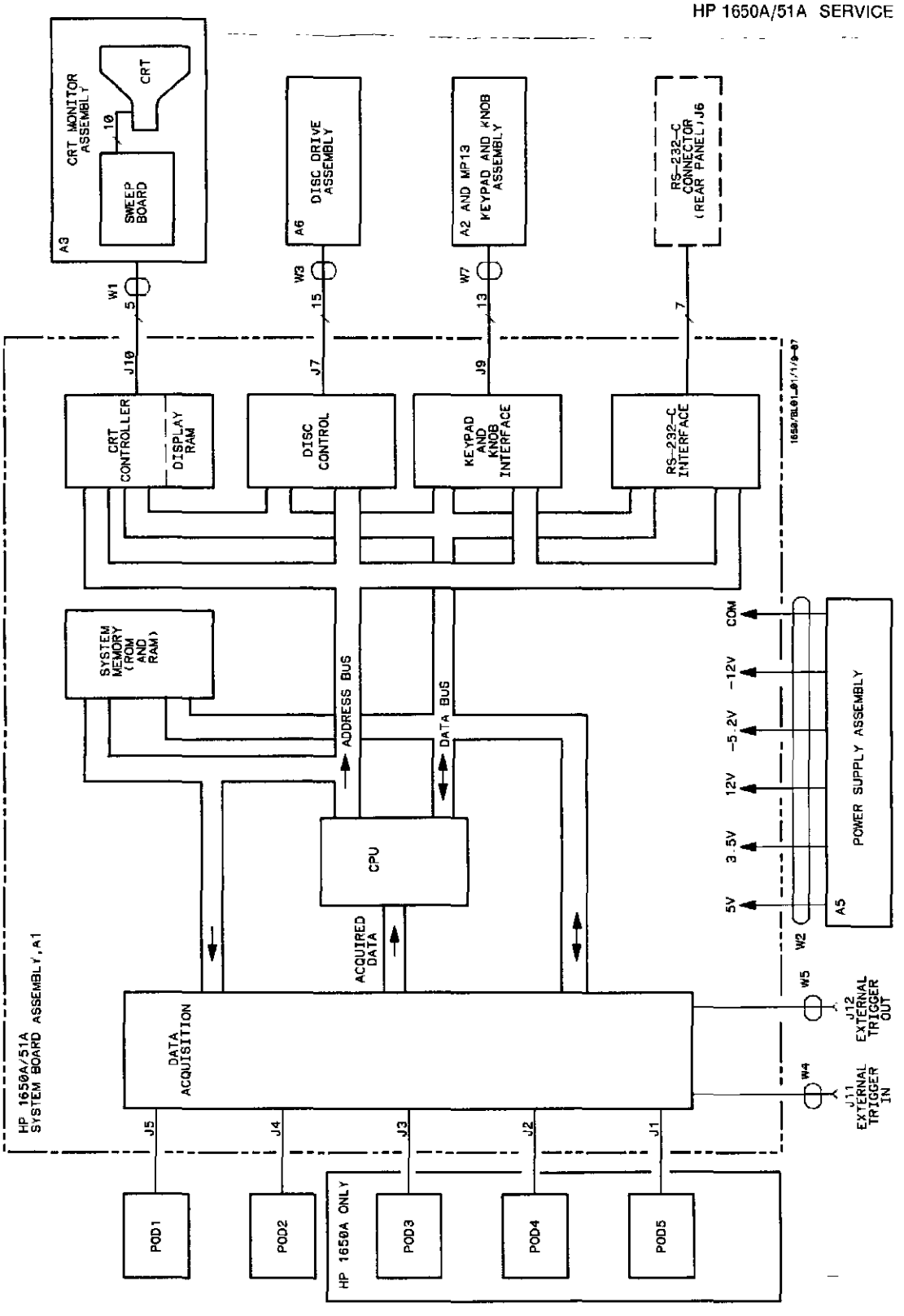


Figure 6-2. Overall Block Diagram for HP 1650A/51A

6-13. TROUBLESHOOTING

6-14. Troubleshooting Flowcharts

The troubleshooting flowcharts will help isolate trouble in the HP 1650A/51A to the module level. Several tables following, and the disassembly procedures preceding the charts, will help with troubleshooting. The circled numbers on the first chart indicate the entry point of the next flowchart for isolating a problem.

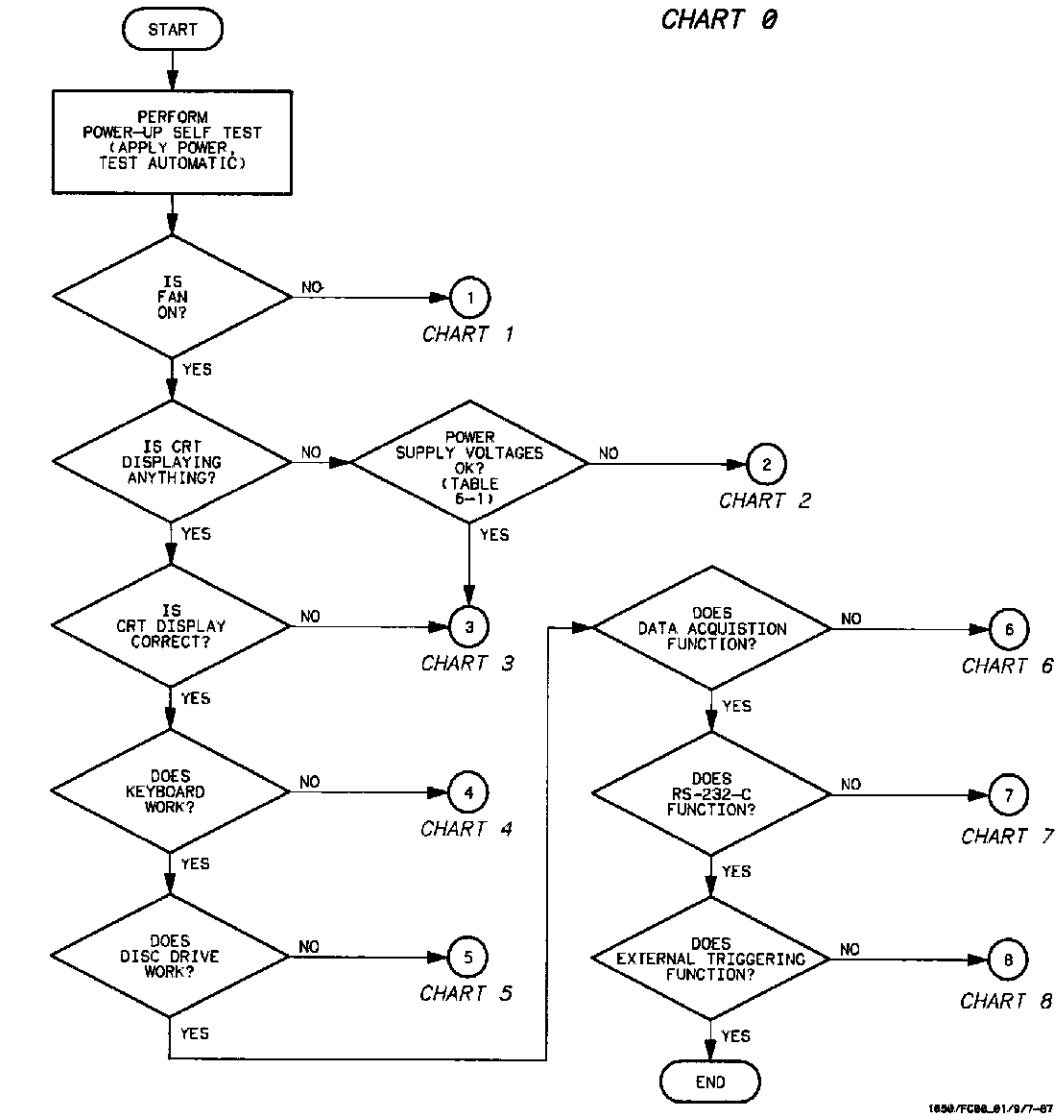


Figure 6-3. General Trouble Isolation Flowchart for HP 1650A/51A

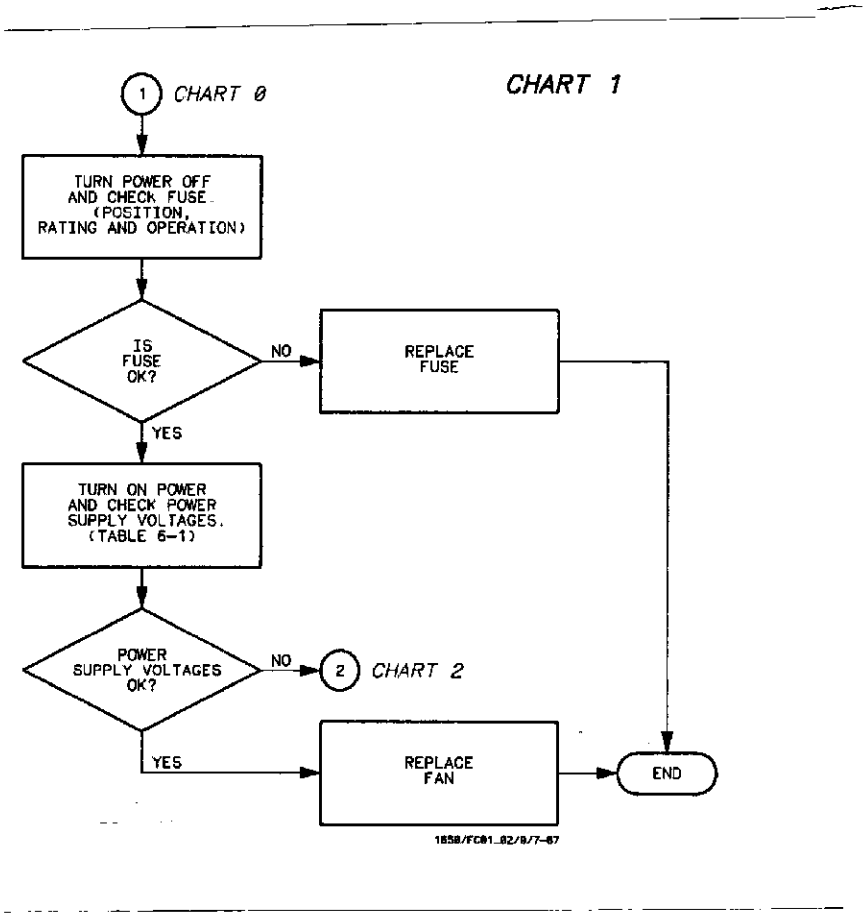


Figure 6-4. Trouble Isolation Chart for HP 1650A/51A Fan/Fuse

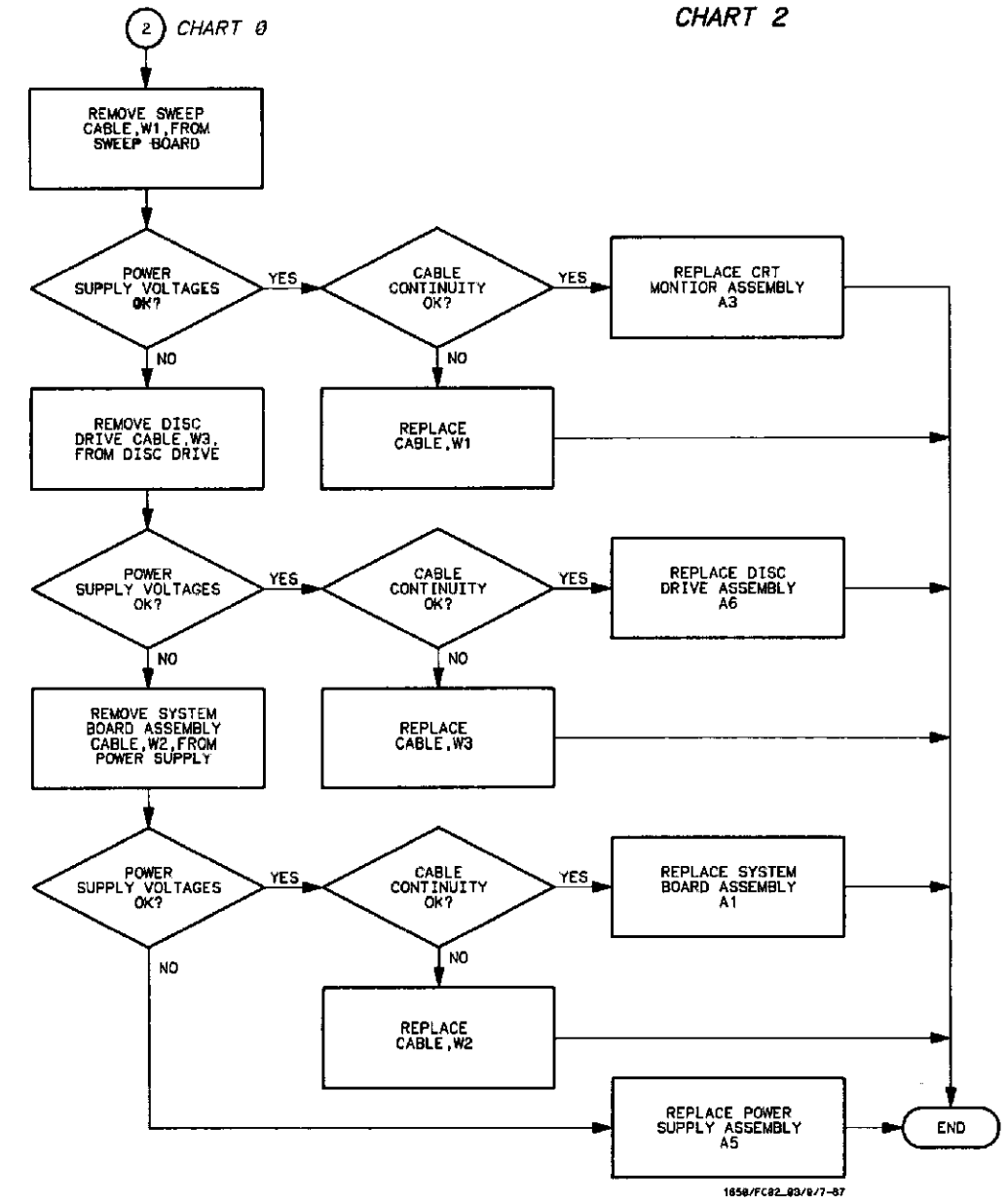
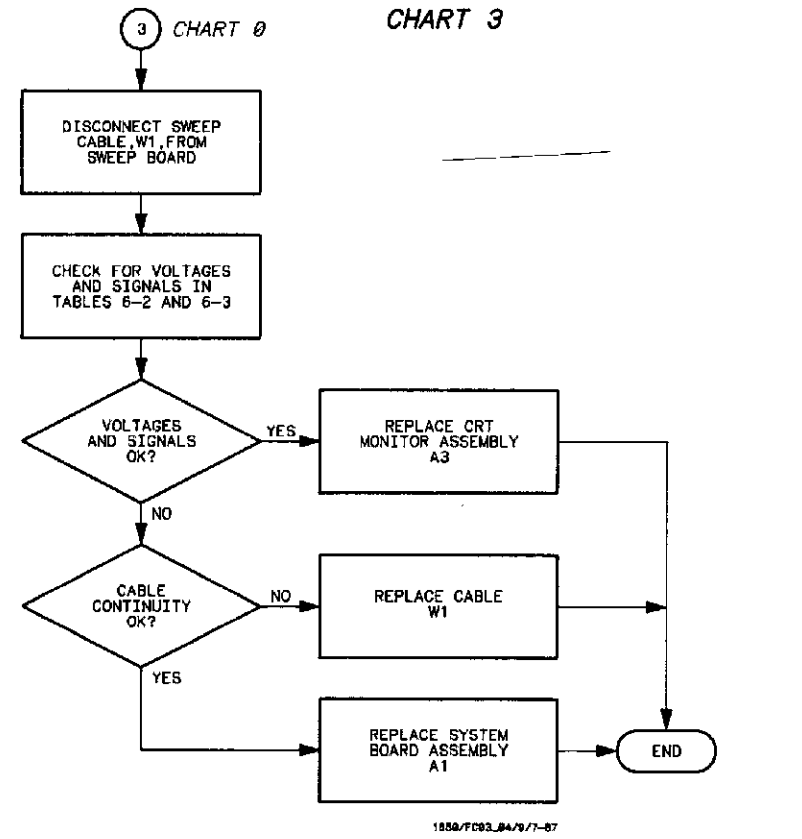


Figure 6-5. Trouble Isolation Flowchart for HP 1650A/51A Power Supply



e 6-6. *Trouble Isolation Flowchart for HP 1650A/51A CRT Monitor*

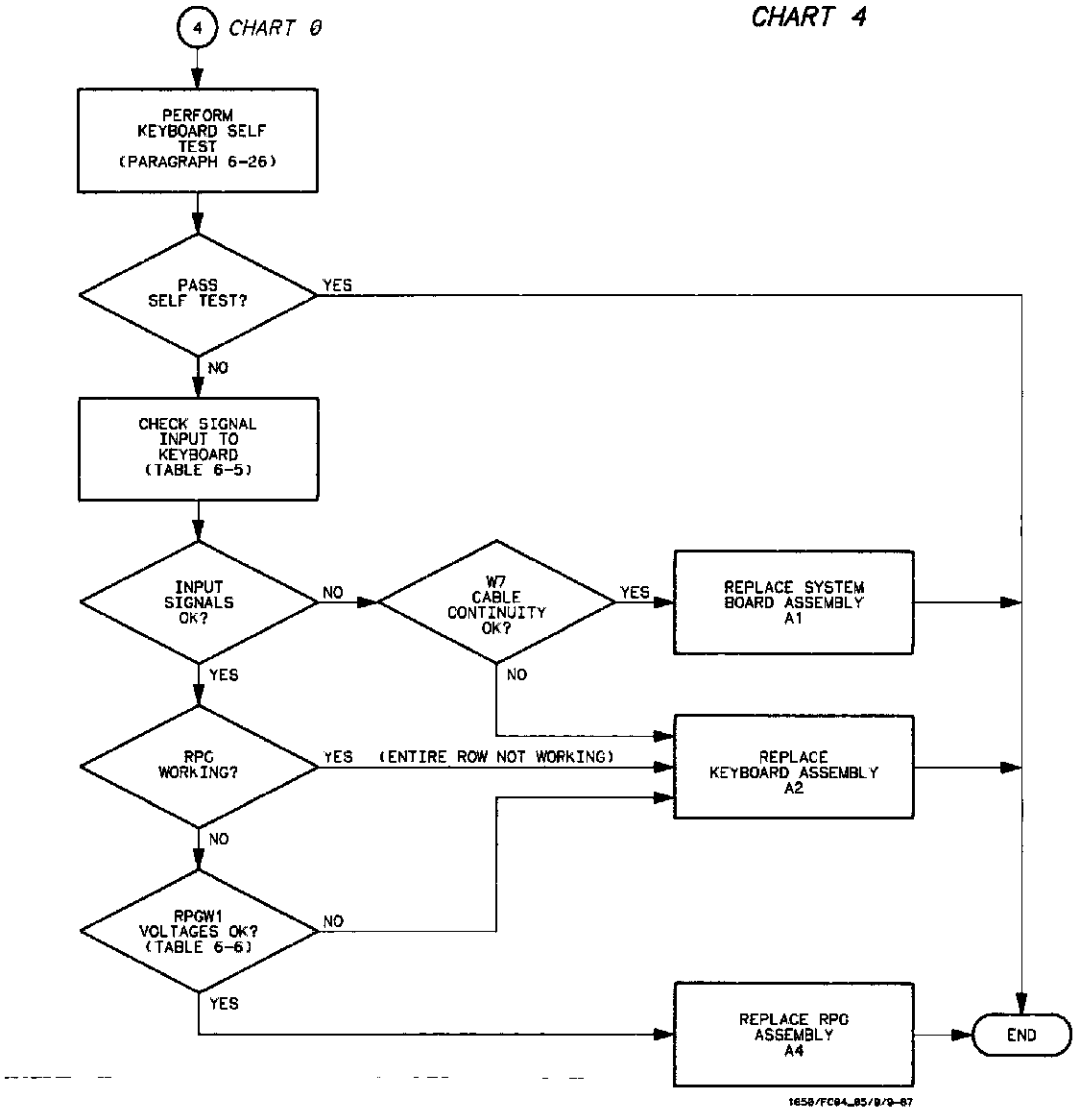


Figure 6-7. Trouble Isolation Flowchart for HP 1650A/51A Keyboard

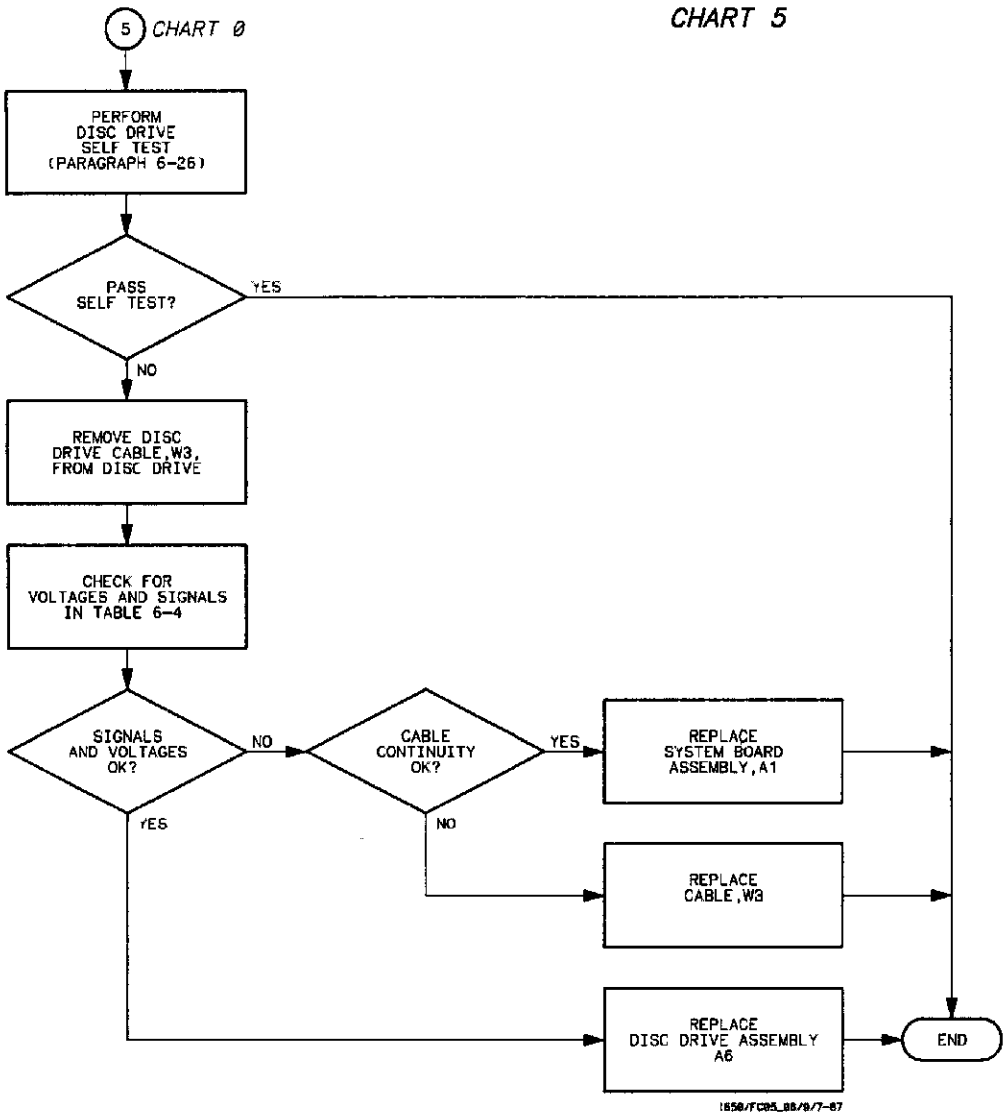


Figure 6-8. Trouble Isolation Flowchart for HP 1650A/51A Disc Drive

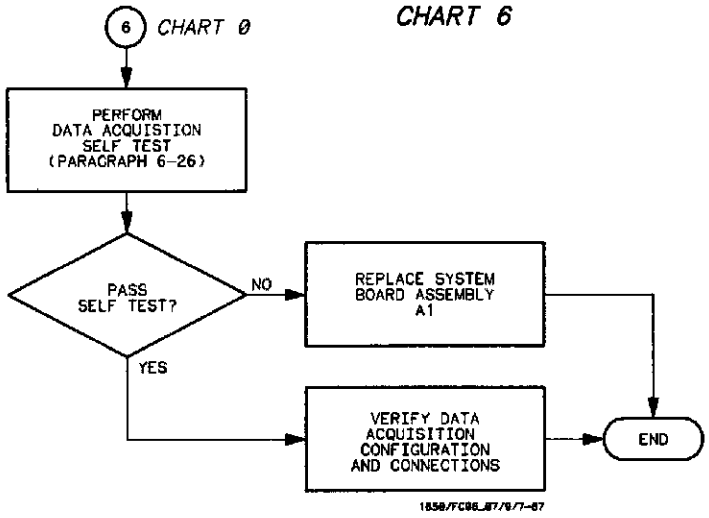


Figure 6-9. Trouble Isolation Flowchart for HP 1650A/51A Data Acquisitio

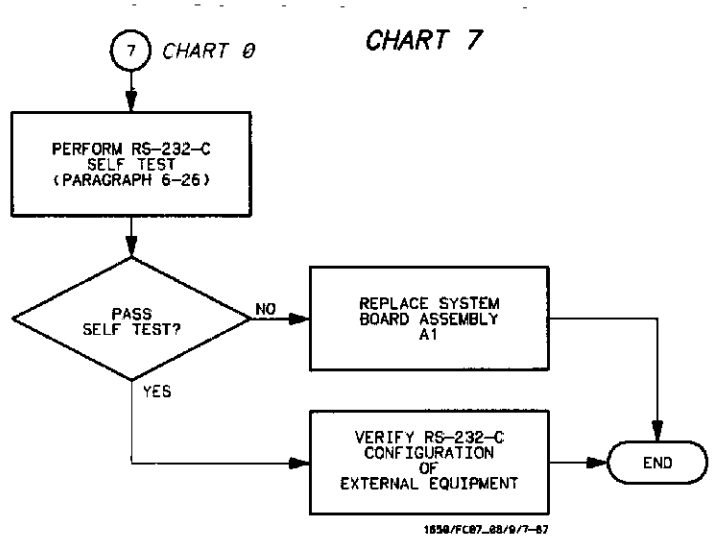


Figure 6-10. Trouble Isolation Flowchart for HP 1650A/51A RS-232-C

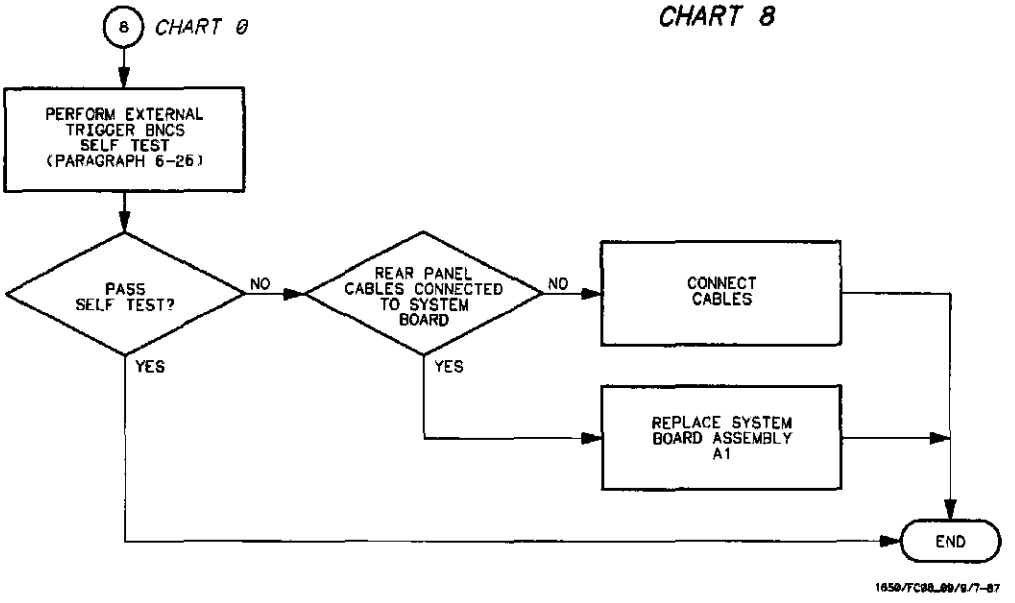


Figure 6-11. Trouble Isolation Flowchart for HP 1650A/51A Trigger BNCs

NOTE

For troubleshooting information for auxiliary power, refer to Auxiliary Power Supply in this section.

6-15. Power Supply Voltages Check

1. Remove top cover from instrument.
2. Refer to figures 6-12 and 6-13 for locations of power supply test points.
3. Check voltages on power supply test points for voltages printed on power supply PC board.
4. The power supply can be isolated to check output voltages with the following steps.

   a. Remove power cable from instrument.

   b. Disconnect cable W2 from power supply as in figure 6-12.

   c. Load +5 V supply with resistor (see Recommended Test Equipment in section 1). Use alligator clips to connect one end of the resistor to any pin 1-4, and the other end to any pin 5-8.

   d. Connect power cable and check for voltages in table 6-1.

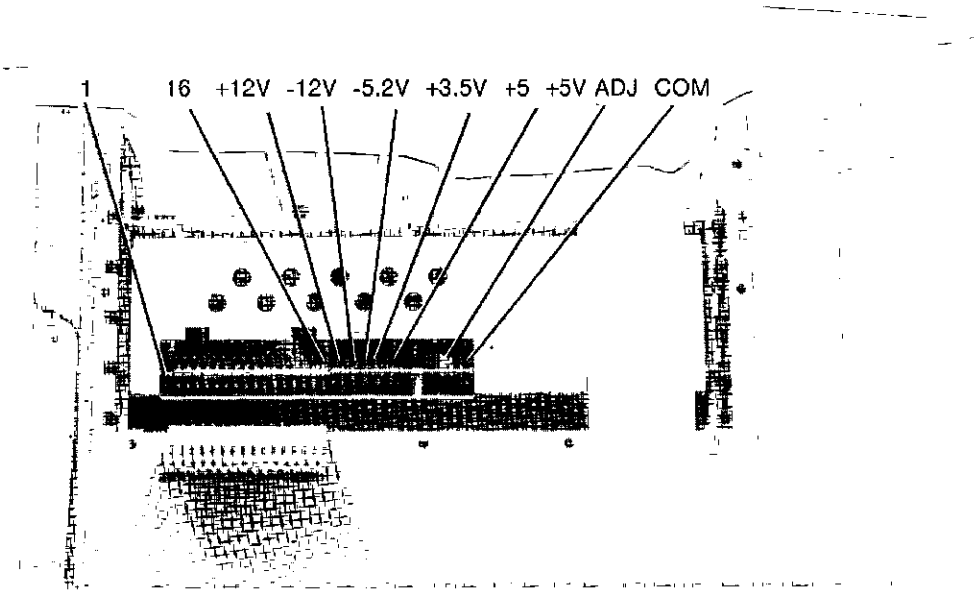


Figure 6-12 Location of Power Supply Assembly I Test Points

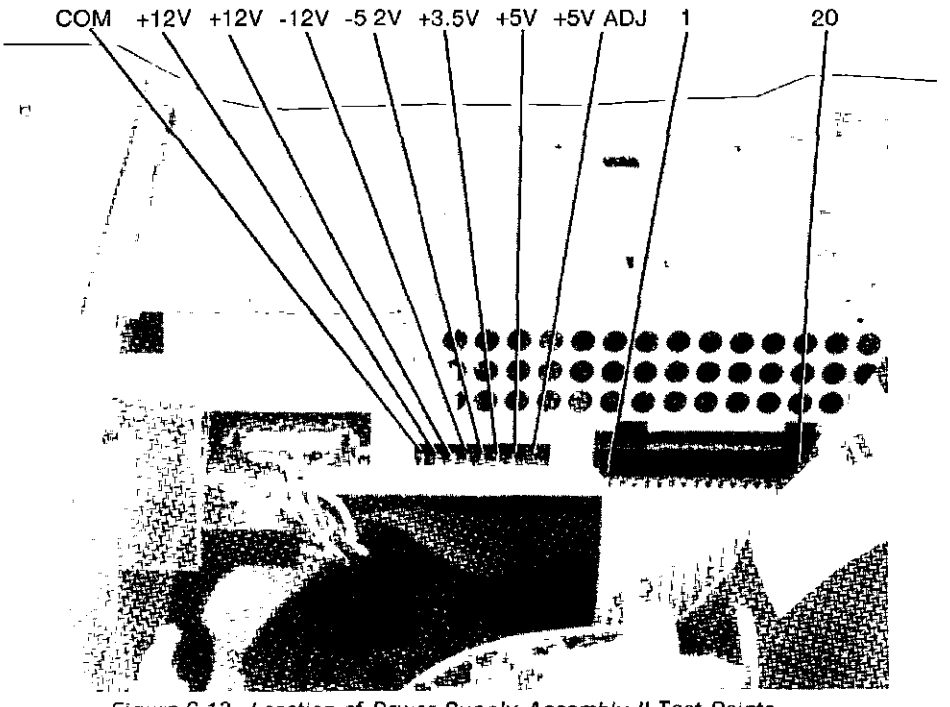


Figure 6-13. Location of Power Supply Assembly II Test Points

Table 6-1. Power Supply Voltages

PIN	SIGNAL	PIN	SIGNAL
1	+5.1 V	11	-5.2 V
2	+5.1 V	12	GROUND
3	+5.1 V	13	+12 V
4	+5.1 V	14	GROUND
5	GROUND	15	-12 V
6	GROUND	16	GROUND
7	GROUND	17	+12 V
8	GROUND	18	-5.2 V
9	+3.5 V	19	+15.5 V
10	GROUND	20	GROUND

6-16. CRT Monitor Signals Check

1. Remove top cover from instrument.

2. Check W1 for signals listed in table 6-2. Refer to figure 6-14 for cable location. The dynamic video signals HFB and HHB are single-ended TTL inputs. Check for activity these pins. Table 6-3 is the truth table for these signals.

Table 6-2. CRT Monitor Cable Pin Assignments

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	+5 V	2	+12 V
3	GROUND	4	GROUND
5	+12 V	6	GROUND
7	+12 V	8	GROUND
9	+12 V	10	HHSYNC
11	HVSYNC	12	+12 V
13	NC	14	NC
15	GROUND	16	HFB
17	GROUND	18	HHB
19	GROUND	20	+5 V

Table 6-3. HFB and HHB Truth Table

HFB	HHB	Video Output
0	0	Off
0	1	Half-bright
1	0	Full-bright
1	1	Full-bright

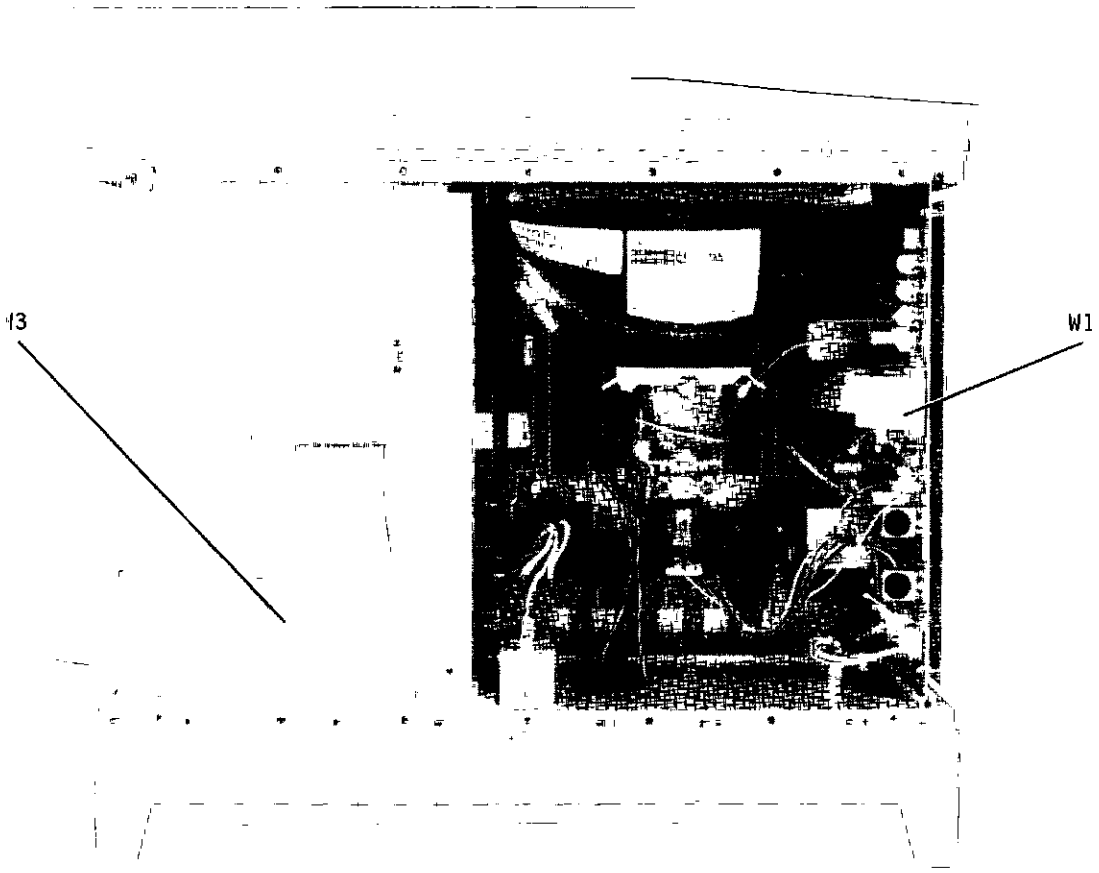


Figure 6-14. CRT Monitor Cable, W1, and Disc Drive Cable, W3, Locations

6-17. Disc Drive Voltages Check

1. Remove top cover from instrument.
2. Run repetitive disc drive self test. Refer to paragraph 6-26.
3. Remove disc drive cable from disc drive.
4. Check disc drive cable for voltages listed in table 6-4 Refer to figure 6-1 for cable l

Table 6-4. Disc Drive Cable Signals

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	CHANGE RESET (+5 V)	2	DISC CHANGE
3	+5 V	4	IN USE
5	+5 V	6	DRIVE SELECT3 (+5 V)
7	+5 V	8	INDEX
9	+5 V	10	DRIVE SELECTO
11	+5 V	12	DRIVE SELECT1
13	GROUND	14	DRIVE SELECT2 (+5 V)
15	GROUND	16	MOTOR ON
17	GROUND	18	DIRECTION
19	GROUND	20	STEP
21	GROUND	22	WRITE DATA
23	GROUND	24	WRITE GATE
25	GROUND	26	TRACK 00
27	GROUND	28	WRITE PROTECT
29	+12 V	30	READ DATA
31	+12 V	32	HEAD SELECT
33	+12 V	34	READY

CAUTION

The connector of the disc drive is marked with an arrow at pin 34 of connector. The end of disc drive cable is marked at pin 1 of cable. ***DO NOT MATCH ARROWS OF CABLE AND CONNECTOR WHEN CONNECTING DISC DRIVE CABLE TO DISC DRIVE. DISC DRIVE DAMAGE WILL OCCUR.***

6-18. Keyboard Signals Check

1. Remove top cover from instrument.
2. Refer to power supply disassembly procedure in this section and remove power supply.
3. Remove the four screws attaching the key board to the front panel.
4. Allow keyboard to fall forward from the front panel as in figure 6-15.
5. Replace power supply, reconnect power supply cables, and apply power to the instrument.

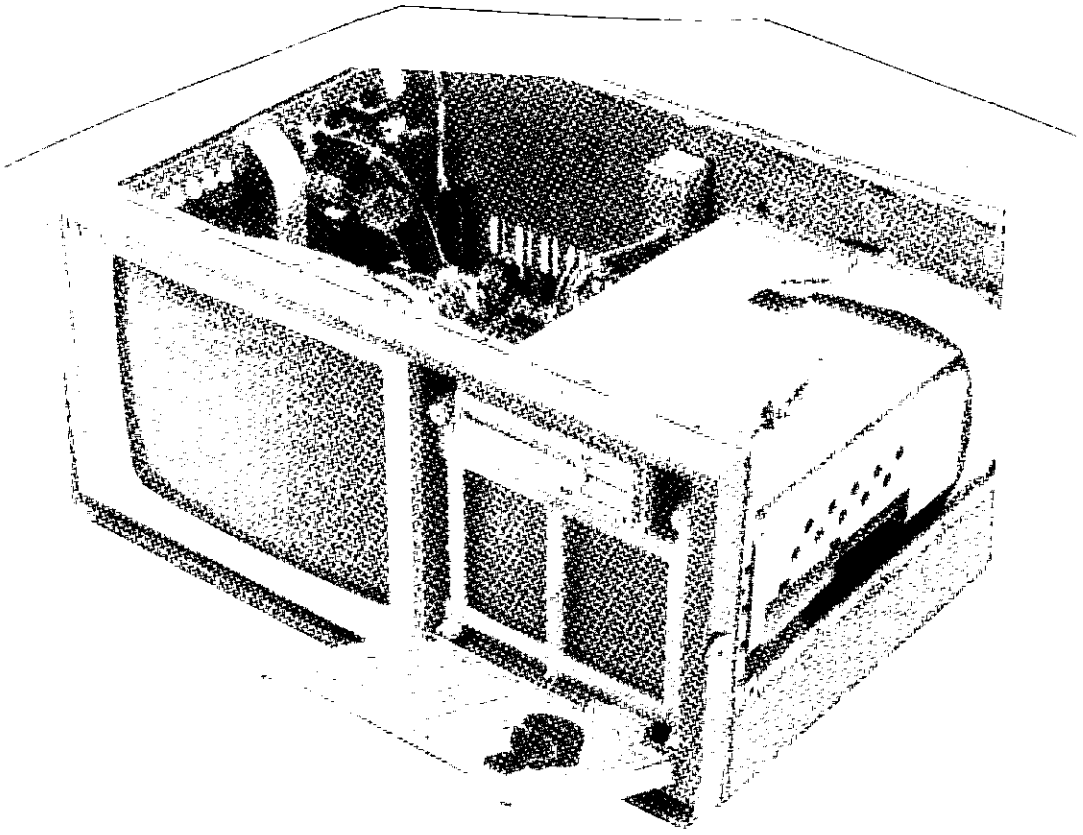


Figure 6-15. HP 1650A/51A Keyboard Position for Trouble Isolation

6. The row scan signal of 250 Hz is present at all times. This signal is found on pins 14 through 20 of keyboard cable connector. The same signal is on pins 3 and 9 through 13 only when a key is being pressed. Refer to table 6-5 for all signals going to and from the keyboard.

Table 6-5. Keyboard Cable Voltages and Signals

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	2	GROUND
3	COLUMN DATA*	4	+5 V
5	GROUND	6	RPG2
7	RPG1	8	NC
9	COLUMN DATA*	10	COLUMN DATA*
11	COLUMN DATA*	12	COLUMN DATA*
13	COLUMN DATA*	14	250 Hz
15	250 Hz	16	250 Hz
17	250 Hz	18	250 Hz
19	250 Hz	20	250 Hz

**** Row scan signal of 250 Hz is on these pins only when a key in the corresponding column is pressed.***

7. To determine whether keypad or keyboard is faulty when random key is not operting, short key (with paper clip or screwdriver) and look for signal on appropriate pin

8. Refer to table 6-6 for voltages on RPG connector.

Table 6-6. RPG Connector Voltages

PIN	VOLTAGE
1	TTL Pulse*
2	GROUND
3	TTL Pulse*
4	NC
5	+5 V

**** When RPG is rotated.***

6-19. EXTENDED SELF TESTS

The extended self tests are used for isolating problems in the HP 1650A/51A. The self tests may be invoked from any menu by pressing the front-panel I/O key. The pop-up I/O menu appears on-screen with the following choices:

* **Exit**
* **Print Screen**
* **Print All**
* **Disc Operations**
* **RS-232-C Configuration**
* **External BNC Configuration**
* **Self Tests**

1. Move the cursor to * **Self Tests** by using the front-panel knob and then press SELECT. Another pop-up menu will appear as in figure 6-16.

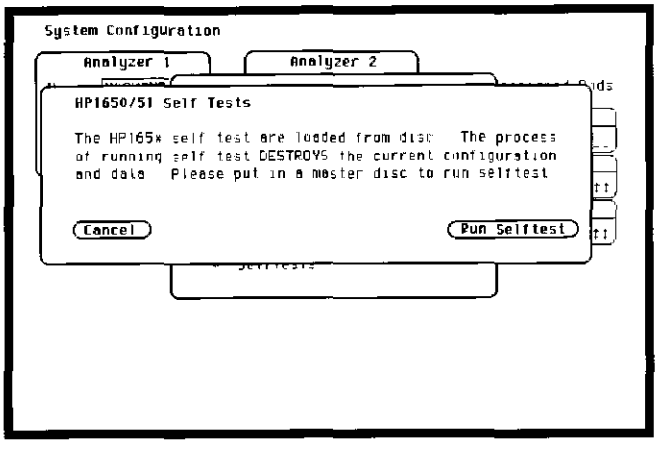


Figure 6-16. ***HP 1650A/51A Self Tests*** *Pop-up Menu*

NOTE

This is the initial menu of the self-tests which informs that all current configurations and data in the logic analyzer will be destroyed when the self tests are implemented. Because the self tests are contained on the operating system disc, the operating system disc (or a copy of it) must be inserted into into the disc drive before continuing.

2. Insert operating system disc (or copy of it) into disc drive.

3. Move cursor to **Run Selftest** or **Start Self Test** with front-panel knob and press SELECT. After loading the self tests, the **HP 1650A/51A Self Tests** menu will be displayed as in figure 6-17.

NOTE

A message will appear on-screen indicating the HP 1650A/51A is loading the test system file before the menu is displayed.

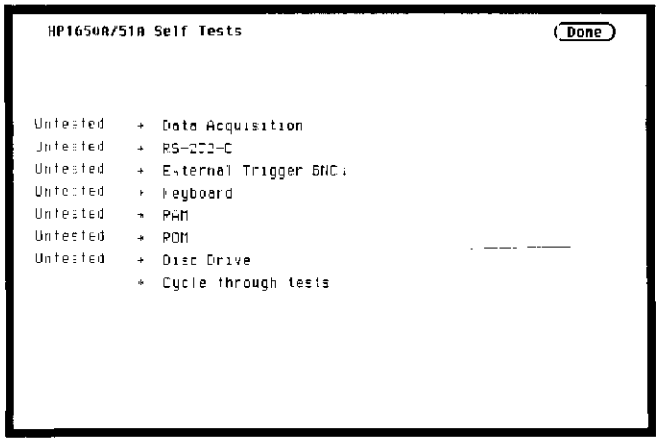


Figure 6-17. ***HP 1650A Self Tests*** *Menu*

4. To leave the **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT. The HP 1650A/51A will reload the operating system and display the default **System Configuration** menu.

NOTE

Operating system disc (or copy of it) must be in disc drive for reloading after extended self tests.

6-20. Data Acquisition Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **Data Acquisition** and press SELECT. Menu and description will be displayed as in figure 6-18.

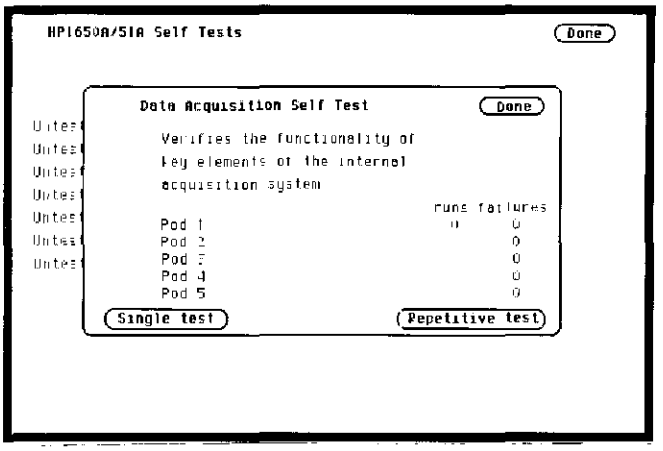


*Figure 6-18. **Data Acquisition Self Test** Pop-up Menu*

2. Move cursor to **Single test** or **Repetitive test** and press SELECT.

3. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed in the menu as in figure 6-19.

4. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

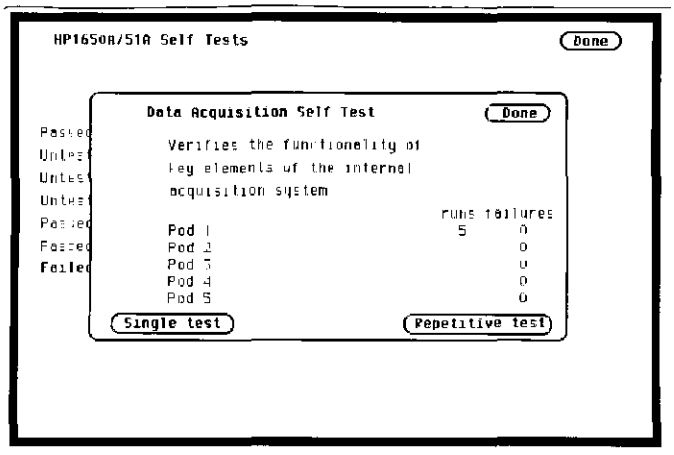


Figure 6-19. Runs and Failures of Repetitive Data Acquisition Self Test

6-21. RS-232-C Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **RS-232-C** and press SELECT. Menu and description will be displayed as in figure 6-20.

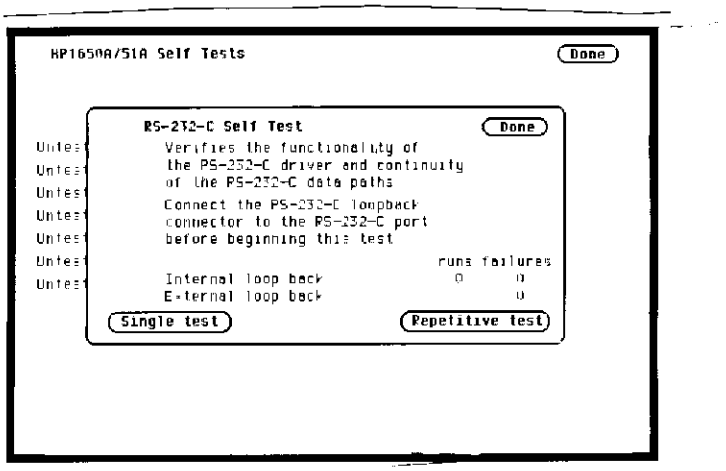


*Figure 6-20. **RS-232-C Self Test** Pop-up Menu*

2. Connect RS-232-C loopback connector to rear-panel RS-232-C receptacle.

NOTE

RS-232-C loopback connector is an accessory supplied with the HP 1650A/51A.

3. Move cursor to **Single test** or **Repetitive test** and press SELECT.

4. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed in the menu.

5. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

6-22. External Trigger BNCs Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **External Trigger BNCs** and press SELECT. Menu and description will be displayed as in figure 6-21

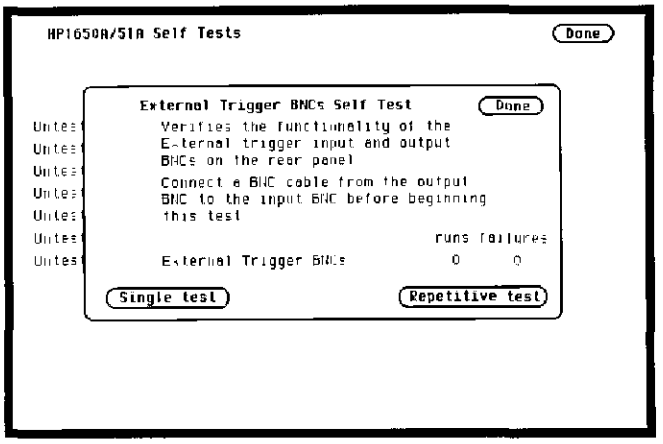


Figure 6-21. ***External Trigger BNCs*** *Pop-up Menu*

2. Connect rear-panel BNC connectors to each other with a BNC cable.

3. Move cursor to **Single test** or **Repetitive test** and press SELECT.

4. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed in the menu.

5. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

6-23. Keyboard Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **Keyboard** and press SELECT. Men description will be displayed as in figure 6-22.

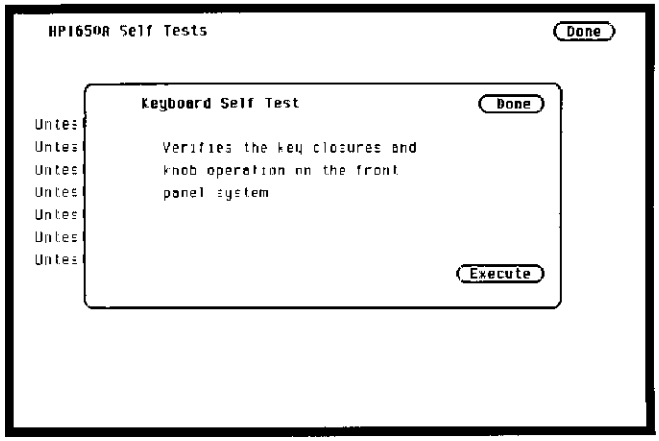


Figure 6-22. ***Keyboard Self Test*** *Pop-up Menu*

2. Move cursor to **Execute** and press SELECT.

3. Press all keys on keypad and rotate front-panel RPG knob to verify proper operation.

4. Press front-panel STOP key twice to return to **Keyboard Self Test** menu.

5. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

6-24. RAM Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **RAM** and press SELECT. Menu and description will be displayed as in figure 6-23.

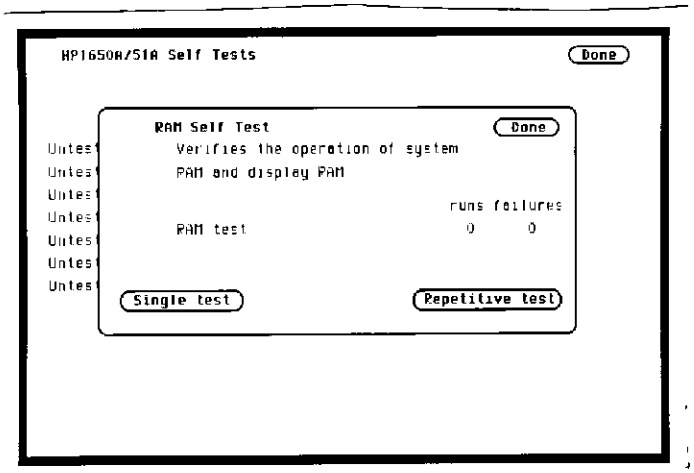


*Figure 6-23. **RAM Self Test** Pop-up Menu*

2. Move cursor to **Single test** or **Repetitive test** and press SELECT.

3. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed as in figure 6-24.

4. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

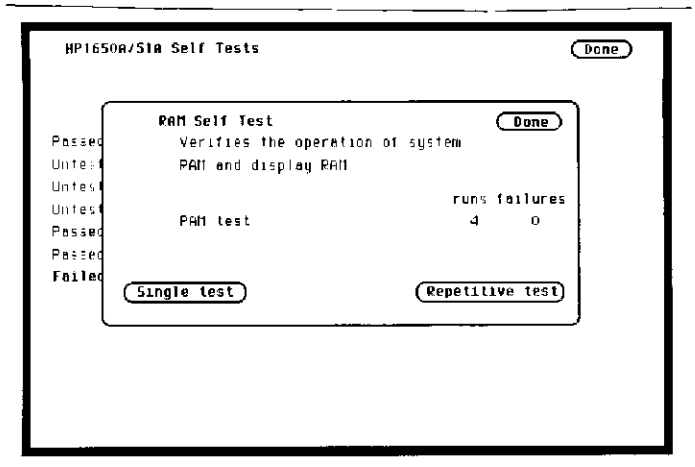


Figure 6-24. Runs and Failures of Repetitive RAM Self Test

6-25. ROM Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **ROM** and press SELECT. Menu and de scription will be displayed as in figure 6-25.

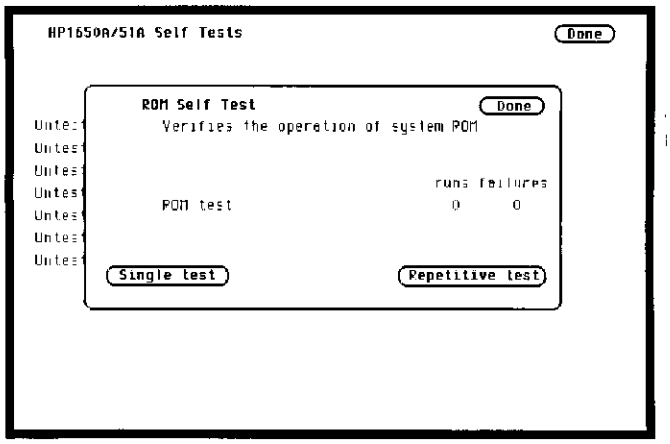


Figure 6-25. ***ROM Self Test*** *Pop-up Menu*

2. Move cursor to **Single test** or **Repetitive test** and press SELECT.

3. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed as in figure 6-26.

4. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

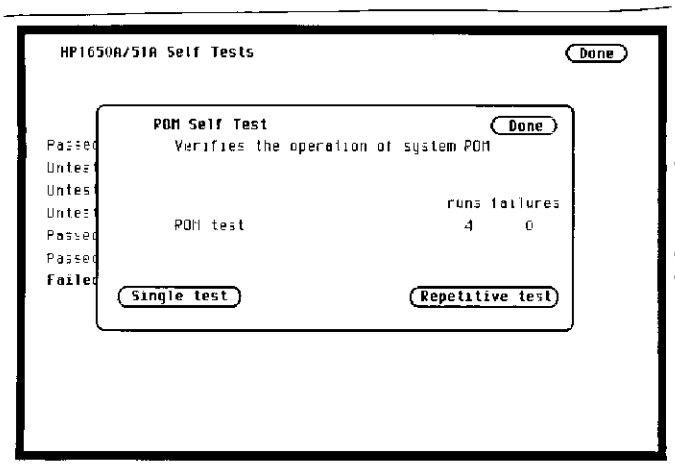


Figure 6-26. Runs And Failures of Repetitive ROM Self Test

6-26. Disc Drive Self Test

1. In **HP 1650A/51A Self Tests** menu, move cursor to **Disc Drive** and press SELECT. Menu and description will be displayed as in figure 6-27.

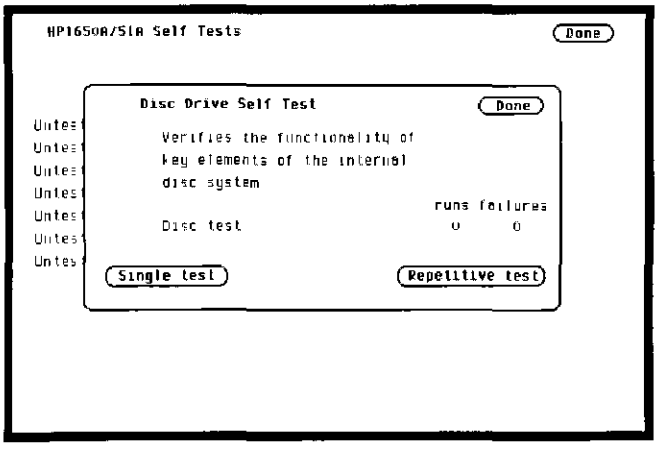


*Figure 6-27. **Disc Drive Self Test** Pop-up Menu*

2. Move cursor to **Single test** or **Repetitive test** and press SELECT.

3. If running repetitive test, press front-panel STOP key to end test. The number of runs and failures will be displayed as in figure 6-28.

4. To return to **HP 1650A/51A Self Tests** menu, move cursor to **Done** and press SELECT.

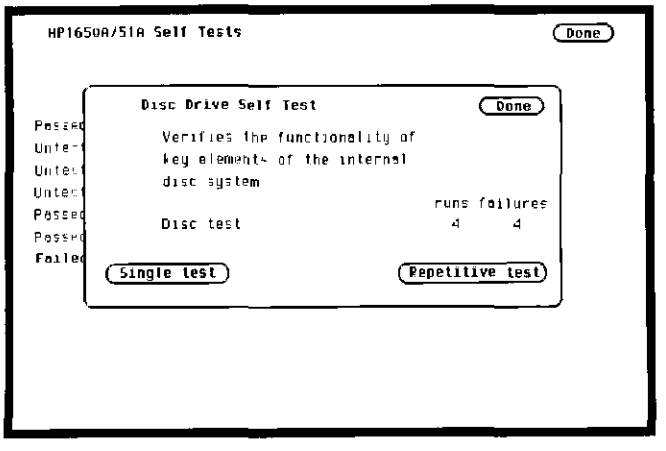


Figure 6-28. Runs and Failures of Repetitive Disc Drive Self Test

6-27. Cycle Through Tests

1. In **HP 1650A/51A Self Tests** menu, move cursor to **Cycle through Tests** and press SELECT.

   The following tests will run consecutively and continually until the front-panel STOP key is pressed.

   Data Acquisition Self Test
   RAM Self Test
   ROM Self Test
   Disc Drive Self Test

2. Press front-panel STOP key to end the continuous tests.

3. To see results of continuous test on data acquisition, move cursor to * **Data Acquisition** and press SELECT. The number of runs and failures of the continuous test will be displayed on the **Data Acquisition Self Test** menu as in previous figure 6-18.

4. Press SELECT to return to **HP 1650A/51A Self Tests** menu.

5. To see results of continuous test on RAM, move cursor to * **RAM** and press select. The number of runs and failures of the continuous test will be displayed on the **RAM Self Test** menu as in previous figure 6-20

6. Press SELECT to return to **HP 1650A/51A Self Tests** menu.

7. To see results of continuous test on ROM, move cursor to * **ROM** and press SELECT. The number of runs and failures of the continuous test will be displayed on the **ROM Self Test** menu as in previous figure 6-23.

8. Press SELECT to return to **HP 1650A/51A Self Tests** menu.

9. To see results of continuous test on disc drive, move cursor to * **Disc Drive** and press SELECT. The number of runs and failures of the continuous test will be displayed on the **Disc Drive Self Test** menu as in previous figure 6-27.

10. Press SELECT to return to **HP 1650A/51A Self Tests** menu.

6-28. AUXILIARY POWER SUPPLY

The HP 1650A/51A provides + 5 V through the probe cables for use with preprocessors. When the probe cables are connected to the preprocessor interface and a slow clock or no activity is seen on all the pods, the problem may be the +5 V supply to the pods. To check the supply voltage to the preprocessor interface, use the following steps.

1. Ground negative lead of voltmeter to rear panel and check for +5 V at either pin 1 or 39 with positive lead.

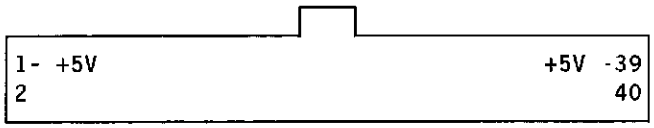


Figure 6-29. HP 1650A/51A Probe Cable Connector

2. If +5V is not at probe cable connector continue with the following steps.

   a. Remove HP 1650A/51A power cable.

   b. Remove all attached pod cables from rear panel.

   c. Remove the four top and the four bottom screws from the rear panel.

   d. Pull rear panel out far enough for power switch/line filter module to clear the inner panel of the instrument.

   e. Turn rear panel clockwise to expose the probe power fuse located on edge of System board Assembly, A1, behind the RS-232-C connector.

   f. Check fuse for continuity and replace if necessary.

   g. If fuse is good, replace System Board Assembly. Refer to disassembly procedure in this section.

3. If + 5 V is present at probe end, the problem must be with the preprocessor interface. Contact your nearest Hewlett-Packard Sales and Service Office for information for servicing the preprocessor interface.

6-29. ASSEMBLY REMOVAL AND INSTALLATION

This section contains the procedures for removal and installation of the logic analyzer system board, power supply, disc drive, CRT monitor assembly, and fan. Read the Safety Summary at the front of this manual before servicing the instrument. The relative location of the replaceable mainframe components are shown in figure 6-1, which is a top view of the logic analyzer with the top cover removed.

6-30. Removal and Installation of System Board Assembly

1. Disconnect power cable.
2. Remove the six screws from top and the two screws from each side of instrument.
3. Lift top cover off.
4. Detach AC power supply cable assembly, W5, from power supply.
5. Detach the pods from System Assembly Board (through rear panel).
6. Detach input/output trigger cables, MP14W1 and MP14W2, from System Board Assembly, A1.
7. Remove rear panel by removing the 8 screws securing it to instrument cabinet and lifting off.

NOTE

When reconnecting cables ensure the input/output trigger cables are connected to the correct rear-panel BNCs.

8. Remove the power supply. Refer to Removal and Replacement of Power Supply in this section, if necessary.
9. Detach the cables of the keyboard, sweep board, power supply, disc drive, fan and rear panel BNC cable assemblies from System Board Assembly.
10. Carefully place instrument in a front-panel-down position (or on its side) and remove the 8 screws securing System Board Assembly to bottom of instrument cabinet.
11. Slide System Board Assembly out of cabinet through rear panel of instrument.
12. Replace System Board Assembly by reversing this procedure.

6-31. Removal and Replacement of Disc Drive

1. Disconnect power cable.
2. Remove the six screws from top and the two screws on each side of instrument cabinet.
3. Remove top cover.
4. Remove the two screws securing disc drive to disc drive panel.
5. Detach disc drive cable assembly, W2, from disc drive.
6. Slide disc drive through front panel of instrument cabinet.
7. Replace disc drive by reversing this procedure.

6-32. Removal and Replacement of CRT Monitor Assembly

1. Disconnect power cable.
2. Remove the six screws from top and the two screws from each side of instrument cabinet.
3. Lift top cover off.
4. Connect a jumper lead between ground lug of CRT and shaft of a screwdriver. To discharge CRT, place screwdriver under protective rubber cap of post accelerator lead and momentarily touch screwdriver to metal clip of post accelerator lead.

CAUTION

Discharge the post accelerator lead to a grounding lug only. Components will be damaged if the post accelerator is discharged to other areas.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT before handling by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead.

5. Disconnect post accelerator lead from CRT by firmly squeezing rubber cap until metal clip disengages from CRT.
6. Detach intensity cable assembly from sweep board.
7. Detach sweep cable assembly, W1, from sweep board and CRT Monitor Assembly cables from CRT and sweep board.

8. Slide sweep board up and out of cabinet slot.

NOTE

When installing sweep board, it may be necessary to press on center of the outer shield of sweep board to allow the board to clear cabinet support rib.

9. Carefully place instrument in front-panel-down position.

10. To remove CRT, remove the four locknuts securing CRT to front panel. Remove CRT and ground bracket from front panel of instrument.

NOTE

When installing CRT, make certain that CRT yoke is properly aligned. THE GROUND BRACKET MUST BE INSTALLED BEFORE THE CRT.

11. To install CRT Monitor Assembly, reverse this procedure.

NOTE

After replacement of CRT Monitor Assembly, perform the CRT adjustment procedures detailed in section 4 of this manual.

6-33. Removal and Replacement of Power Supply

1. Disconnect power cable.

2. Remove the six screws from top and the two screws from each side of instrument cabinet.

3. Lift top cover off

4. Detach disc drive cable, W3, from disc drive.

5. Detach the System Board Assembly power supply cable assembly, W2, from power supply.

6. Detach AC line supply cable assembly, W5, from power supply.

7. Remove the two PCB retainers securing power supply from right front and rear corners of the instrument cabinet by pulling retainers up and out.

8. Slide power supply out through side of instrument cabinet.

9. To install power supply, reverse this procedure.

NOTE

When installing the power supply, make certain power supply connector is directed to outside.

6-34. Removal and Replacement of Fan

1. Disconnect power cable.
2. Remove the six screws from top and the two screws from each side of instrument.
3. Lift off top cover.
4. Detach fan cable assembly, B1W1, from System Board Assembly.
5. Detach AC line supply cable, W5, from power supply.
6. Remove pod cables from System Board Assembly through rear panel.

NOTE

When connecting cables, be sure input/output cables are connected to the correct rear-panel BNC.

7. Detach input/output trigger cables, MP14W1 and MP14W2, from System Board Assembly.
8. Remove rear panel by removing the eight screws securing rear panel to instrument panel.
9. Remove fan by removing the four screws securing it to cabinet.
10. To install fan, reverse this procedure.

NOTE

When replacing fan, be sure fan label is to outside of instrument to assure fan cable is directed toward center of rear panel for connection to System Assembly Board.

6-35. Removal and Replacement of Keyboard Assembly

1. Disconnect power cable.
2. Remove power supply by following the steps previously detailed in paragraph 6-8.
3. Detach keyboard cable from System Board Assembly.
4. Remove the four screws securing Keyboard Assembly to front of instrument cabinet.
5. The keyboard assembly, keypad, housing, label overlay, RPG and knob will come off front panel as one unit.
6. Disconnect RPG cable from keyboard assembly.
7. Leave keyboard spacer in place between key board and front panel.
8. Replace keyboard assembly by reversing this procedure.