élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

# *EL2020C*
## *50 MHz Current Feedback Amplifier*

## Features

- Slew rate 500 V/μs
- ±33 mA output current
- Drives ±2.4V into 75Ω
- Differential phase <0.1°
- Differential gain <0.1%
- V supply ±5V to ±18V
- Output short circuit protected
- Uses current mode feedback
- 1% settling time of 50 ns for 10V step
- Low cost
- 9 mA supply current
- 8-pin mini-dip

## Applications

- Video gain block
- Residue amplifier
- Radar systems
- Current to voltage converter
- Coax cable driver with gain of 2

## Ordering Information

| Part No. | Temp. Range | Pkg. | Outline# |
|---|---|---|---|
| EL2020CN | −40°C to +85°C | P-DIP | MDP0031 |
| EL2020CM | −40°C to +85°C | 20-Lead SOL | MDP0027 |

## General Description

The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain then a conventional voltage feedback operational amplifier.

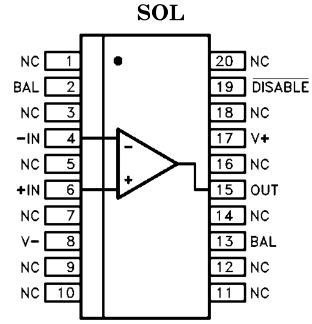
The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

Elantec products and facilities comply with Elantec document, QRA-1: *Processing-Monolithic Products.*

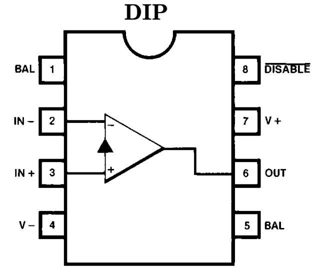
## Connection Diagrams

**SOL**




2020–2

**DIP**

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Manufactured under U.S. Patent No. 4,893,091.

## Absolute Maximum Ratings (25°C)

| | | |
|---|---|---|
| $V_S$ | Supply Voltage | ±18V or 36V |
| $V_{IN}$ | Input Voltage | ±15V or $V_S$ |
| $\Delta V_{IN}$ | Differential Input Voltage | ±10V |
| $I_{IN}$ | Input Current (Pins 2 or 3) | ±10 mA |
| $I_{INS}$ | Input Current (Pins 1, 5, or 8) | ±5 mA |
| $P_D$ | Maximum Power Dissipation (See Curves) | 1.25W |
| $I_{OP}$ | Peak Output Current | Short Circuit Protected |
| | Output Short Circuit Duration (Note 2) | Continuous |
| $T_A$ | Operating Temperature Range | −40°C to +85°C |
| $T_J$ | Operating Junction Temperature Plastic Package, SOL | 150°C |
| $T_{ST}$ | Storage Temperature | −65°C to +150°C |

**Important Note:**
**All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.**

| Test Level | Test Procedure |
|---|---|
| I | 100% production tested and QA sample tested per QA test plan QCX0002. |
| II | 100% production tested at $T_A$ = 25°C and QA sample tested at $T_A$ = 25°C, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002. |
| III | QA sample tested per QA test plan QCX0002. |
| IV | Parameter is guaranteed (but not tested) by Design and Characterization Data. |
| V | Parameter is typical value at $T_A$ = 25°C for information purposes only. |

## Open Loop Characteristics $V_S$ = ±15V

| Parameter | Description | Temp | Limits Min | Typ | Max | Test Level | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ (Note 1) | Input Offset Voltage | 25°C | −10 | 3 | +10 | I | mV |
| | | $T_{MIN}$, $T_{MAX}$ | −15 | | +15 | III | mV |
| $\Delta V_{OS}/\Delta T$ | Offset Voltage Drift | | | −30 | | V | µV/°C |
| CMRR (Note 3) | Common Mode Rejection Ratio | ALL | 50 | 60 | | II | dB |
| PSRR (Note 4) | Power Supply Rejection Ratio | 25°C | 65 | 75 | | I | dB |
| | | $T_{MIN}$, $T_{MAX}$ | 60 | | | III | dB |
| $+I_{IN}$ | Non-inverting Input Current | 25°C, $T_{MAX}$ | −15 | 5 | +15 | II | µA |
| | | $T_{MIN}$ | −25 | | +25 | III | µA |
| $+R_{IN}$ | Non-Inverting Input Resistance | ALL | 1 | 5 | | II | MΩ |
| +IPSR (Note 4) | Non-Inverting Input Current Power Supply Rejection | 25°C, $T_{MAX}$ | | 0.05 | 0.5 | II | µA/V |
| | | $T_{MIN}$ | | | 1.0 | III | µA/V |
| $-I_{IN}$ (Note 1) | −Input Current | 25°C, $T_{MAX}$ | −40 | 10 | +40 | II | µA |
| | | $T_{MIN}$ | −50 | | +50 | III | µA |

TD is 2.8in

## Open Loop Characteristics $V_S = \pm 15V$ — Contd.

| Parameter | Description | Temp | Limits | | | Test Level | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| −ICMR (Note 3) | −Input Current Common Mode Rejection | 25°C, $T_{MAX}$ | | 0.5 | 2.0 | II | μA/V |
| | | $T_{MIN}$ | | | 4.0 | III | μA/V |
| −IPSR (Note 4) | −Input Current Power Supply Rejection | 25°C, $T_{MAX}$ | | 0.05 | 0.5 | II | μA/V |
| | | $T_{MIN}$ | | | 1.0 | III | μA/V |
| $R_{ol}$ | Transimpedence ($\Delta V_{OUT}/\Delta(-I_{IN})$) $R_L = 400\Omega$, $V_{OUT} = \pm 10V$ | 25°C, $T_{MAX}$ | 300 | 1000 | | II | V/mA |
| | | $T_{MIN}$ | 50 | | | III | V/mA |
| $A_{VOL1}$ | Open Loop DC Voltage Gain $R_L = 400\Omega$, $V_{OUT} = \pm 10V$ | 25°C, $T_{MAX}$ | 70 | 80 | | II | dB |
| | | $T_{MIN}$ | 60 | | | III | dB |
| $A_{VOL2}$ | Open Loop DC Voltage Gain $R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$ | 25°C, $T_{MAX}$ | 60 | 70 | | II | dB |
| | | $T_{MIN}$ | 55 | | | III | dB |
| $V_O$ | Output Voltage Swing $R_L = 400\Omega$ | 25°C, $T_{MAX}$ | ±12 | ±13 | | II | V |
| | | $T_{MIN}$ | ±11 | | | III | V |
| $I_{OUT}$ | Output Current $R_L = 400\Omega$ | 25°C, $T_{MAX}$ | ±30 | ±32.5 | | II | mA |
| | | $T_{MIN}$ | ±27.5 | | | III | mA |
| $I_s$ | Quiescent Supply Current | 25°C | | 9 | 12 | I | mA |
| | | $T_{MIN}$, $T_{MAX}$ | | | 15 | III | mA |
| $I_{s\ off}$ | Supply Current, Disabled, $V_8 = 0V$ | ALL | | 5.5 | 7.5 | II | mA |
| $I_{logic}$ | Pin 8 Current, Pin 8 = 0V | ALL | | 1.1 | 1.5 | II | mA |
| $I_D$ | Min Pin 8 Current to Disable | ALL | | 120 | 250 | II | μA |
| $I_e$ | Max Pin 8 Current to Enable | ALL | | | 30 | II | μA |

TD is 4.1in

## AC Closed Loop Characteristics EL2020C $V_S = \pm 15V$, $T_A = 25°C$

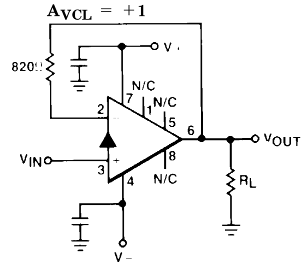
| Parameter | Description | Min | Typ | Max | Test Level | Units |
|---|---|---|---|---|---|---|
| | Closed Loop Gain of 1 V/V (0 dB), $R_F = 1\ k\Omega$ | | | | | |
| SR1 | Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$ | 300 | 500 | | I | V/µs |
| FPBW1 | Full Power Bandwidth (Note 5) | 4.77 | 7.95 | | I | MHz |
| $t_r1$ | Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90% | | 6 | | V | ns |
| $t_f1$ | Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90% | | 6 | | V | ns |
| $t_p1$ | Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% Points | | 8 | | V | ns |
| | Closed Loop Gain of 1 V/V (0 dB), $R_F = 820\Omega$ | | | | | |
| BW | −3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100\ mV$ | | 50 | | V | MHz |
| $t_s$ | 1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$ | | 50 | | V | ns |
| $t_s$ | 0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$ | | 90 | | V | ns |
| | Closed Loop Gain of 10 V/V (20 dB), $R_F = 1\ k\Omega$, $R_G = 111\Omega$ | | | | | |
| SR10 | Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, Test at $V_O = \pm 5V$ | 300 | 500 | | I | V/µs |
| FPBW10 | Full Power Bandwidth (Note 5) | 4.77 | 7.95 | | I | MHz |
| $t_r10$ | Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90% | | 25 | | V | ns |
| $t_f10$ | Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90% | | 25 | | V | ns |
| $t_p10$ | Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% points | | 12 | | V | ns |
| | Closed Loop Gain of 10 V/V (20 dB), $R_F = 680\Omega$, $R_G = 76\Omega$ | | | | | |
| BW | −3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100\ mV$ | | 30 | | V | MHz |
| $t_s$ | 1% Settling Time, $R_l = 400\ \Omega$, $V_O = 10V$ | | 55 | | V | ns |
| $t_s$ | 0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$ | | 280 | | V | ns |

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between pins 1 and 5 with the wiper connected to $V_{CC}$ (Pin 7) to make the output offset voltage zero.
Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.
Note 3: $V_{CM} = \pm 10V$.
Note 4: $\pm 4.5V \leq V_S \leq \pm 18V$.
Note 5: Full Power Bandwidth is guaranteed based on Slew Rate measurement. FPBW $= SR/2\pi V_{peak}$.

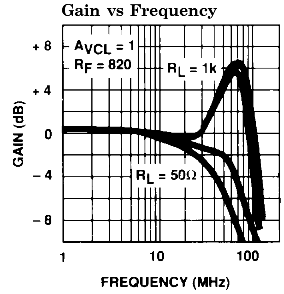
TD is 3.2in

## Typical Performance Curves Non-Inverting Gain of One

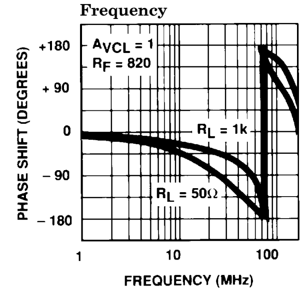
$A_{VCL} = +1$



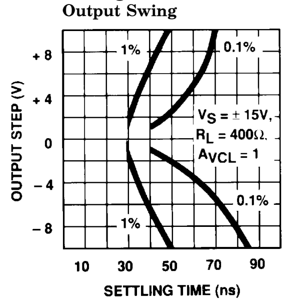

Gain vs Frequency



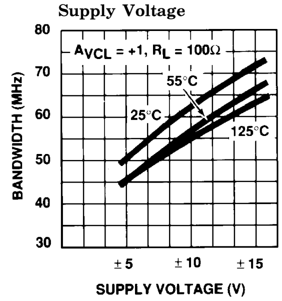

Phase Shift vs Frequency



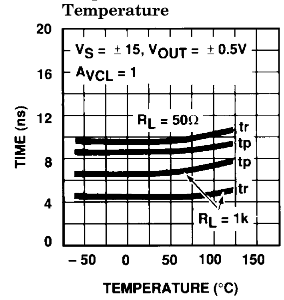

Settling Time vs Output Swing



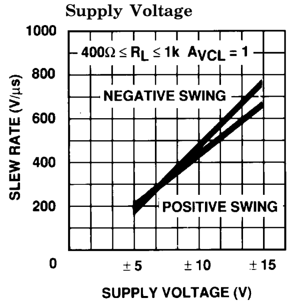

−3 dB Bandwidth vs Supply Voltage



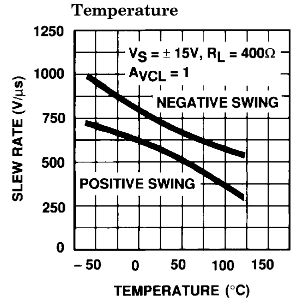

Rise Time and Prop Delay vs Temperature




Slew Rate vs Supply Voltage



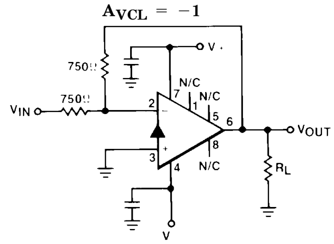

Slew Rate vs Temperature



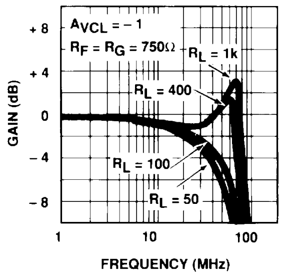

2020–4

## Typical Performance Curves — Contd. Inverting Gain of One

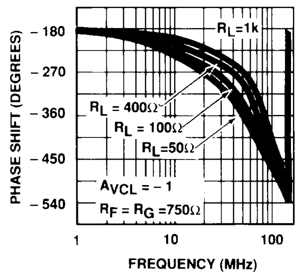
$A_{VCL} = -1$



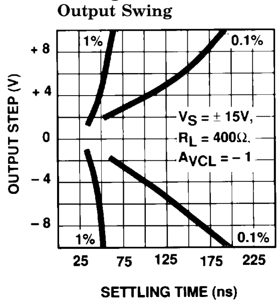

**Gain vs Frequency**



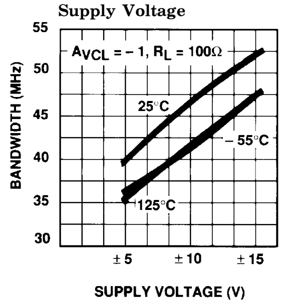

**Phase Shift vs Frequency**



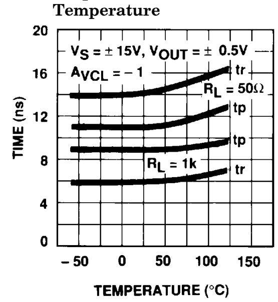

**Settling Time vs Output Swing**



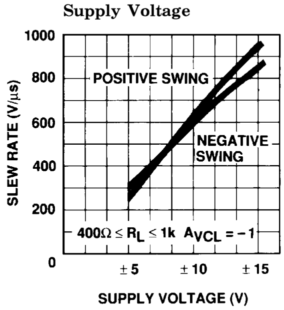

**−3 dB Bandwidth vs Supply Voltage**



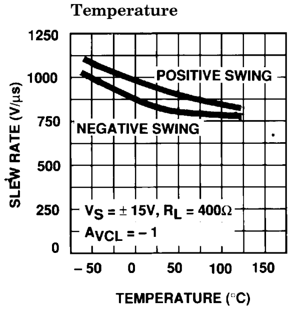

**Rise Time and Prop Delay vs Temperature**




**Slew Rate vs Supply Voltage**




**Slew Rate vs Temperature**

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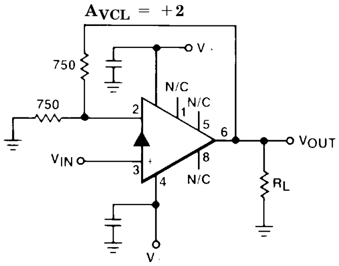
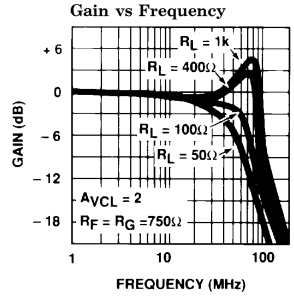
## Typical Performance Curves — Contd. Non-Inverting Gain of Two

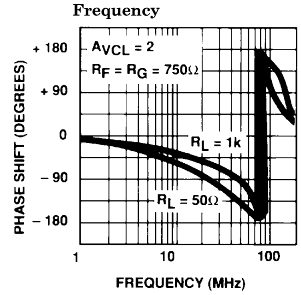
$A_{VCL} = +2$



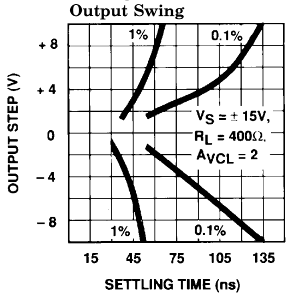

Gain vs Frequency



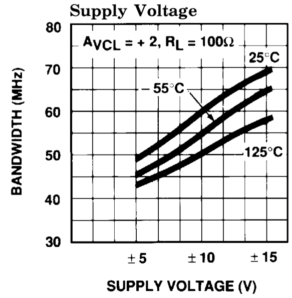

Phase Shift vs Frequency



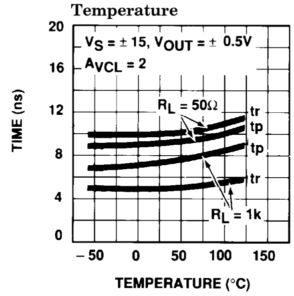

Settling Time vs Output Swing



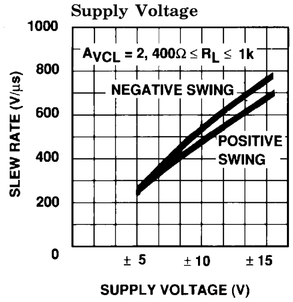

−3 dB Bandwidth vs Supply Voltage



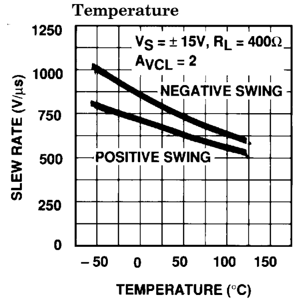

Rise Time and Prop Delay vs Temperature




Slew Rate vs Supply Voltage



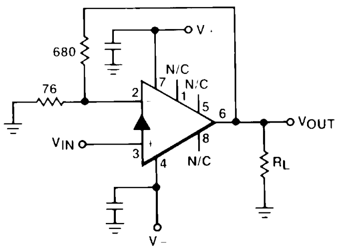

Slew Rate vs Temperature



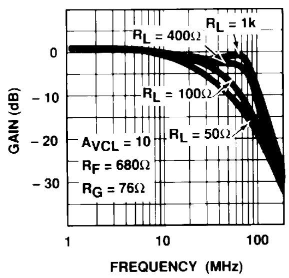

2020-6

## Typical Performance Curves — Contd. Non-Inverting Gain of Ten

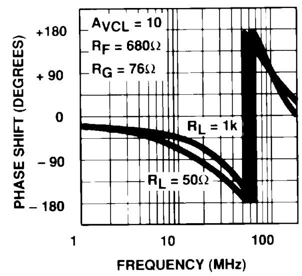
$A_{VCL}$ = +10



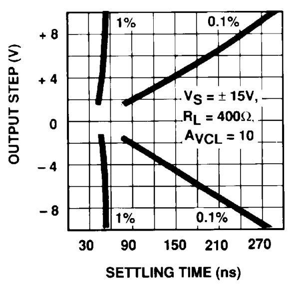

**Gain vs Frequency**



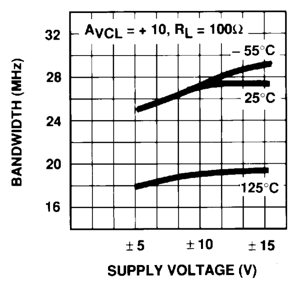

**Phase Shift vs Frequency**



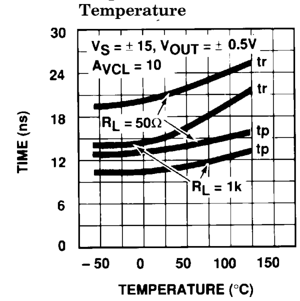

**Settling Time vs Output Swing**



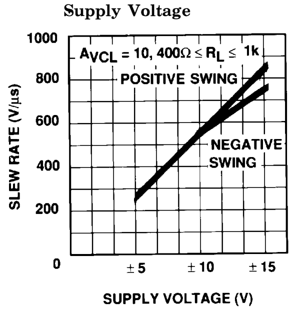

**−3 dB Bandwidth vs Supply Voltage**



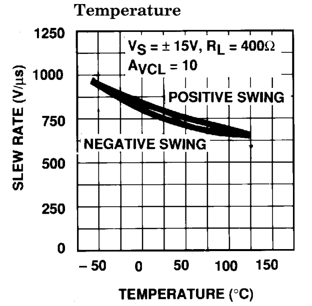

**Rise Time and Prop Delay vs Temperature**




**Slew Rate vs Supply Voltage**



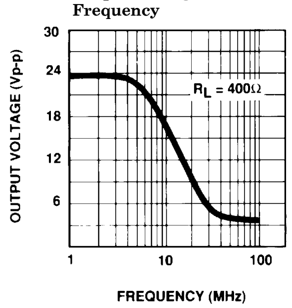

**Slew Rate vs Temperature**



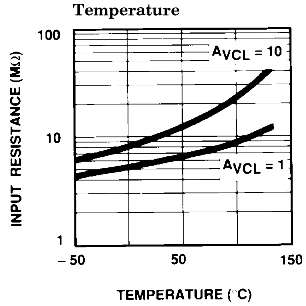

2020–7

## Typical Performance Curves — Contd.

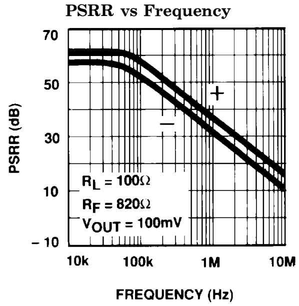
**Maximum Undistorted Output Voltage vs Frequency**



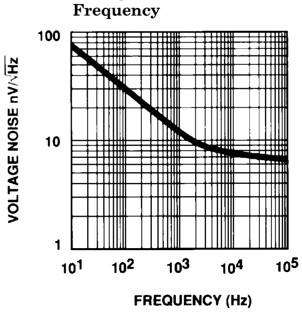

**Input Resistance vs Temperature**



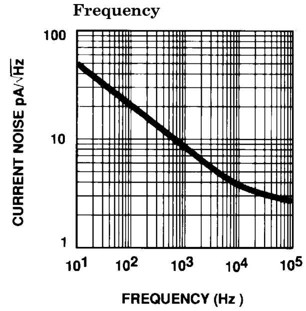

**PSRR vs Frequency**



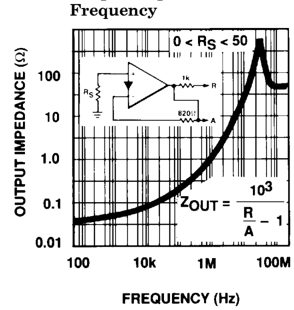

**Voltage Noise vs Frequency**



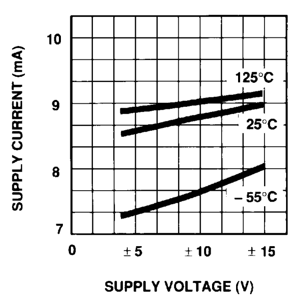

**Current Noise vs Frequency**



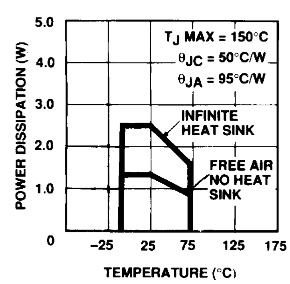

**Output Impedance vs Frequency**



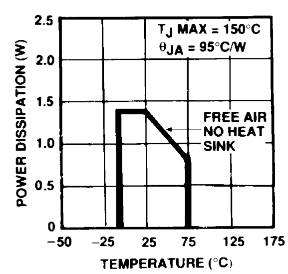

**Supply Current vs Supply Voltage**




**8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature**




**20-Lead SOL Maximum Power Dissipation vs Ambient Temperature**

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## Application Information

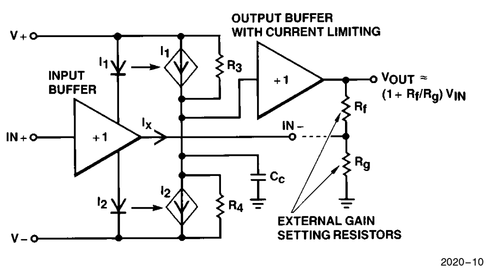
### Theory of Operation

The EL2020 has a unity gain buffer similar to the EL2003 from the non-inverting input to the inverting input. The error signal of the EL2020 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is the transresistance ($R_{OL}$) of the EL2020 [$V_{OUT} = R_{OL} * I_{INV}$]. Since $R_{OL}$ is very large ($\approx 10^6$), the current flowing into the inverting input in the steady state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first order approximation for circuit analysis, namely that. . .

1. The voltage across the inputs $\approx$ 0 and
2. The current into the inputs is $\approx$ 0

**Simplified Block Diagram of EL2020**




### Resistor Value Selection and Optimization

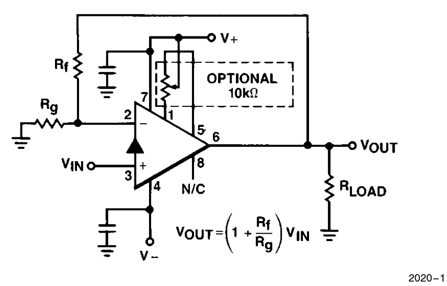
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2020. A nominal value for the feedback resistor is 1 kΩ, which is the value used for production testing. This value guarantees stability. For a given gain, the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth will be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed loop transfer function which results from stray capacitance between the inverting input and ground.

### Power Supplies

The EL2020 may be operated with single or split power supplies as low as ±3V (6V total) to as high as ±18V (36V total). The slew rate degrades significantly for supply voltages less than ±5V (10V total), but the bandwidth only changes 25% for supplies from ±3V to ±18V. It is not necessary to use equal value split power supplies, i.e., −5V and +12V would be excellent for 0V to 1V video signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2020 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.

**Non-Inverting Amplifier**

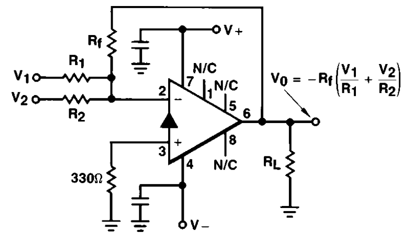



**EL2020 Typical Non-Inverting Amplifier Characteristics**

| $A_V$ | $R_F$ | $R_G$ | Bandwidth | 10V Settling Time | |
|---|---|---|---|---|---|
| | | | | 1% | 0.1% |
| +1 | 820Ω | None | 50 MHz | 50 ns | 90 ns |
| +2 | 750Ω | 750Ω | 50 MHz | 50 ns | 100 ns |
| +5 | 680Ω | 170Ω | 50 MHz | 50 ns | 200 ns |
| +10 | 680Ω | 76Ω | 30 MHz | 55 ns | 280 ns |

## Application Information — Contd.

**Summing Amplifier**

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**EL2020 Typical Inverting Amplifier Characteristics**

| $A_V$ | $R_F$ | $R_1, R_2$ | Bandwidth | 10V Settling Time | |
|---|---|---|---|---|---|
| | | | | 1% | 0.1% |
| −1 | 750Ω | 750Ω | 40 MHz | 50 ns | 130 ns |
| −2 | 750Ω | 375Ω | 40 MHz | 55 ns | 160 ns |
| −5 | 680Ω | 130Ω | 40 MHz | 55 ns | 160 ns |
| −10 | 680Ω | 68Ω | 30 MHz | 70 ns | 170 ns |

### Input Range

The non-inverting input to the EL2020 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input charactersitics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

### Source Impedance

The EL2020 is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources may cause oscillations; a 1 kΩ resistor in series with the input lead will usually eliminate problems without sacrificing too much speed.

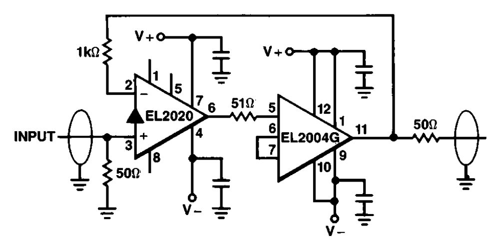
### Current Limit

The EL2020 has internal current limits that protect the output transistors. The current limit goes down with junction temperature rise. At a junction temperature of +175°C the current limits are at about 50 mA. If the EL2020 output is shorted to ground when operating on ±15V supplies, the power dissipation could be as great as 1.1W. A heat sink is required in order for the EL2020 to survive an indefinite short. Recovery time to come out of current limit is about 50 ns.

### Using the 2020 with Output Buffers

When more output current is required, a wideband buffer amplifier can be included in the feedback loop of the EL2020. With the EL2003 the subsystem overshoots about 10% due to the phase lag of the EL2003. With the EL2004 in the loop, the overshoot is less than 2%. For even more output current, several buffers can be paralleled.

**EL2020 Buffered with an EL2004**

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### Capacitive Loads

The EL2020 is like most high speed feedback amplifiers in that it does not like capacitive loads between 50 pF and 1000 pF. The output resistance works with the capacitive load to form a second non-dominate pole in the loop. This results in excessive peaking and overshoot and can lead to oscillations. Standard resistive isolation techniques used with other op amps work well to isolate capacitive loads from the EL2020.

## Application Information — Contd.

### Offset Adjust

To calculate the amplifier system offset voltage from input to output we use the equation:

Output Offset Voltage $= V_{OS} (R_F/R_G + 1) \pm I_{BIAS} (R_F)$

The EL2020 output offset can be nulled by using a 10 kΩ potentiometer from pins 1 to 5 with the slider tied to pin 7 ($+V_{CC}$). This adjusts both the offset voltage and the inverting input bias current. The typical adjustment range is ±80 mV at the output.

### Compensation

The EL2020 is internally compensated to work with external feedback resistors for optimum bandwidth over a wide range of closed loop gain. The part is designed for a nominal 1 kΩ of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

The EL2020 becomes *less* stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2020 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small, with ground plane kept away from this node.

### Active Filters

The EL2020's low phase lag at high frequencies makes it an excellent choice for high performance active filters. The filter response more closely approaches the theoritical response than with conventional op amps due to the EL2020's smaller propagation delay. Because the internal compensation of the EL2020 depends on resistive feedback, the EL2020 should be set up as a gain block.

### Driving Cables

The EL2020 was designed with driving coaxial cables in mind. With 30 mA of output drive and low output impedance, driving one to three 75Ω double terminated coax cables with one EL2020 is practical. Since it is easy to set up a gain of +2, the double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 data sheet.

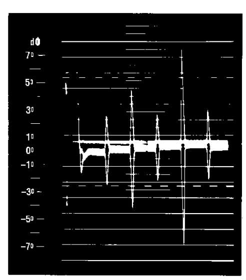
### Video Performance Characteristics

The EL2020 makes an excellent gain block for video systems, both RS-170 (NTSC) and faster. It is capable of driving 3 double terminated 75Ω cables with distortion levels acceptable to broadcasters. A common video application is to drive a 75Ω double terminated coax with a gain of 2.

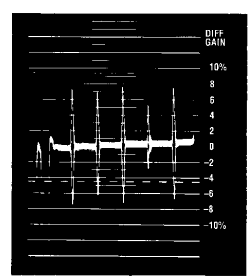
To measure the video performance of the EL2020 in the non-inverting gain of 2 configuration, 5 identical gain-of-two circuits were cascaded (with a divide by two 75Ω attenuator between each stage) to increase the errors.

The results, shown in the photos, indicate the entire system of 5 gain-of-two stages has a differential gain of 0.5% and a differential phase of 0.5°. This implies each device has a differential gain/phase of 0.1% and 0.1°, but these are too small to measure on single devices.

**Differential Phase of 5 Cascaded Gain-Of-Two Stages**



**Differential Gain of 5 Cascaded Gain-Of-Two Stages**

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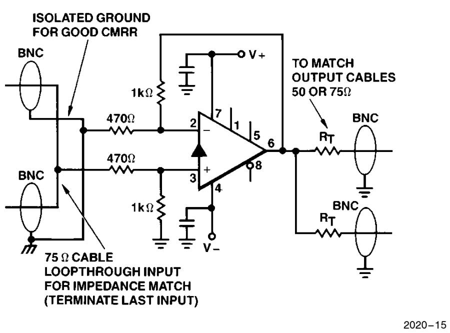
## Application Information — Contd.

### Video Distribution Amplifier

The distribution amplifier shown below features a difference input to reject common mode signals on the 75Ω coax cable input. Common mode rejection is often necessary to help to eliminate 60 Hz noise found in production environments.

**Video Distribution Amplifier with Difference Input**




### EL2020 Disable/Enable Operation

The EL2020 has an enable/disable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to pin 7, $V_{CC}$. When more than 250 μA is pulled from pin 8, the EL2020 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is halved. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (~1.1 mA) if pin 8 is grounded.

To draw current out of pin 8 an "open collector output" logic gate or a discrete NPN transistor can be used. This logic interface method has the advantage of level shifting the logic signal from 5V supplies to whatever supply the EL2020 is operating on without any additional components.

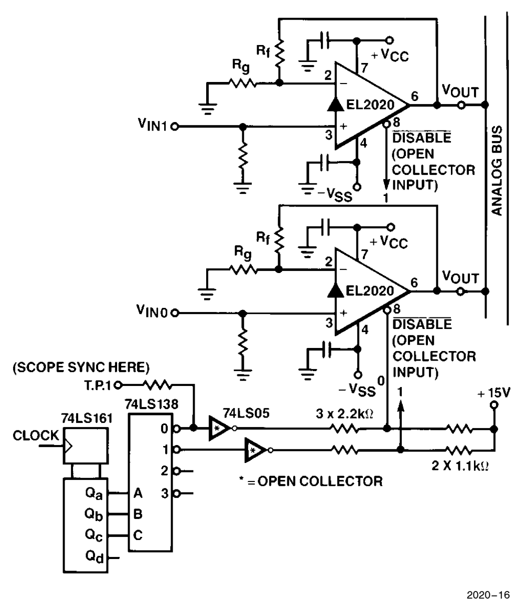
### Using the EL2020 as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown.

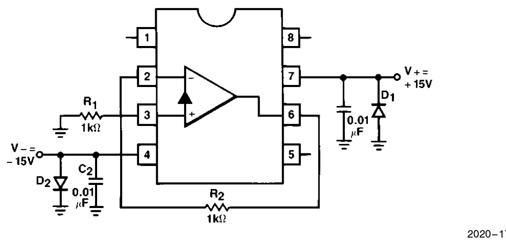
When the EL2020 is disabled, the DC output impedance is very high, over 10 kΩ. However there is also an output capacitance that is non-linear. For signals of less than 5V peak to peak, the output capacitance looks like a simple 15 pF capacitor. However, for larger signals the output capacitance becomes much larger and non-linear.

The example multiplexer will switch between amplifiers in 5 μs for signals of less than ±2V on the outputs. For full output signals of 20V peak to peak, the selection time becomes 25 μs. The disabled outputs also present a capacitive load and therefore only three amplifiers can have their outputs shorted together. However an unlimited number can sum together if a small resistor (25Ω) is inserted in series with each output to isolate it from the "bus". There will be a small gain loss due to the resistors of course.

**Using the EL2020 as a Multiplexer**

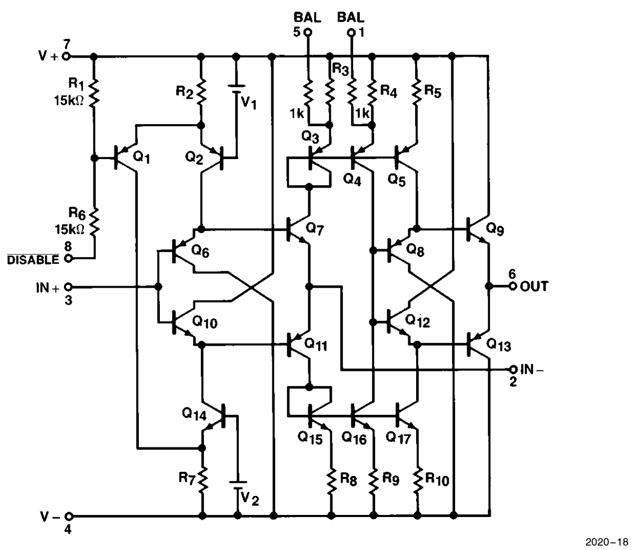


## Burn-In Circuit




Pin numbers are for DIP Packages.
All Packages Use the Same Schematic.

## Equivalent Circuit



## EL2020 Macromodel

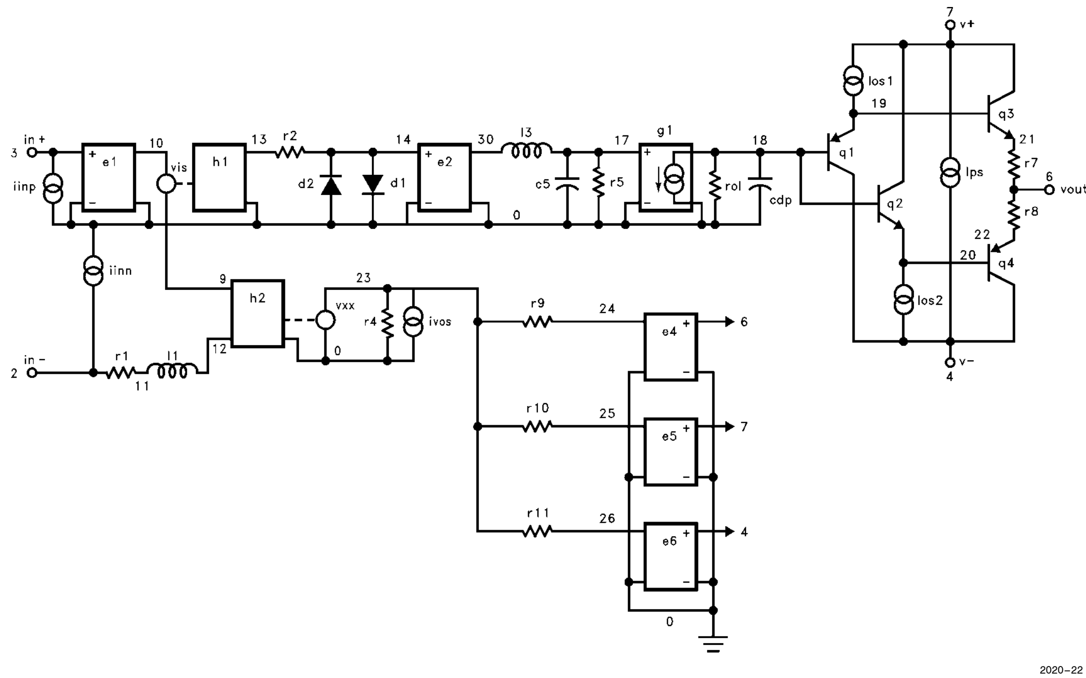
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:   +input
*                  |   -input
*                  |     |   +Vsupply
*                  |     |     |   -Vsupply
*                  |     |     |     |   output
*                  |     |     |     |     |
.subckt M2020      3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 29nH
iinp 3 0 10µA
iinm 2 0 5µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
15 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 5pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
```

## EL2020 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 3mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.2nS)
.model qp pnp (is=5e-15 bf=100 tf=0.2nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=1.67 n=4)
.ends
```

TD is 3.1in

## EL2020 Macromodel



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# *EL2020C*

## *50 MHz Current Feedback Amplifier*

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