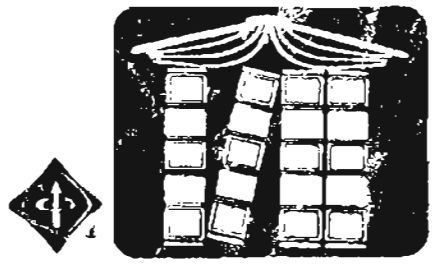
Bonebrake

IEEE SHORT COURSES PROGRAM NOTES

PHASE LOCKED LOOPS

Dr. Jacob Klapper



Continuing Education Service

PHASE-LOCKED LOOPS

Dr. Jacob Klapper
Department of Electrical Engineering
New Jersey Institute of Technology

Contents

Primary References For This Course

1. J. Klapper and J. T. Frankle, Phase-Locked and Frequency-Feedback Systems: Principles and Techniques, Academic Press, 1972.

2. W. F. Egan, Frequency Synthesis by Phase Lock, J. Wiley and Sons, 1981.

Glossary of Terms

α	Input CNR referred to PLL noise bandwidth, B_n
α_b	Entire baseband threshold CNR
α_{CH}	Channel threshold CNR in FDM
δ_2, δ_3	Distortion coefficient
Δ	Deviation percentage error
Δf_p	Peak signal frequency deviation (hertz)
$\Delta\omega$	VCO frequency deviation (radians per second) about quiescent center frequency
$\Delta\omega_p$	Peak signal frequency deviation (radians)
θ_n	Noise angle
$(\Delta\omega_{rms})^2$	Mean-square signal frequency deviation (radians per second)^2
$(\dot{\Delta}\omega)_{max}$	Maximum sweep frequency (radians per second squared)
η	Spectral density level (watts per hertz)
η_m	Modulation density in terms of phase modulation (radians squared per hertz)
λ	Limiter-discriminator sensitivity (also K_1)
Λ	Normalized phase margin

μ	VCO sensitivity (radians per volt-second (also K_3)
μs	Microsecond
ξ	Damping factor (also z)
ρ	Carrier-to-noise ratio (CNR)
σ	Root-mean-square (rms) modulation index; also standard deviation
τ	Delay (seconds)
Φ	Phase angle, frequency domain
ϕ	Phase angle, time domain (radians)
ϕ_b	Excess phase shift per base bandwidth (radians)
ϕ_d	Distortion generator in terms of phase modulation (radians)
ϕ_e	Loop phase error (radians)
ϕ_{es}	Modulation-induced phase error component (radians)
ϕ_{en}	Noise-induced phase error component (radians)
ϕ_i	Input signal phase modulation (radians)
ϕ_{ir}	Received signal phase modulation (radians)
ϕ_{np}	Equivalent peak phase error, noise component (radians)
ϕ_r	VCO phase modulation (radians)
ϕ_{rd}	Loop response distortion component in terms of phase modulation (radians)
ψ	Phase angle (radians)
ω	Radian frequency (radians per second)
ω_a	Bottom frequency of speech spectrum model or of FDM baseband (radians per second)
ω_b	Top baseband frequency of transmission (radians per second)
ω_c	Signal center frequency (radians per second)
ω_{CH}	Channel center frequency (radians per second)
ω_e	IF center frequency (FMFB) (radians per second)
ω_i	Input signal center frequency (radians per second)
ω_n	Loop natural frequency (radians per second)
ω_r	VCO center frequency (radians per second)
ω_T	Test-tone frequency (radians per second)
a, b	Loop zero constants
b'	Ratio of predetection semibandwidth to base bandwidth
dB	Decibels

e_n	Equivalent noise input generator that accounts for voltage-controlled oscillator internal noise
e_s	Demodulated signal or loop output signal (volts)
f	Frequency (hertz)
f_b	Base-bandwidth or top baseband transmission frequency (hertz)
h	Impulse response of closed loop
h_I	Impulse response of IF filter
h_{bI}	Equivalent baseband impulse response of internal IF filter
kHz	Kilohertz (kilocycles per second)
mH	Millihenry
m_p	Peak modulation index (also $\Delta\omega_p/\omega_b$)
$n(t)$	Noise
nsec	Nanosecond
r	Radius of gyration
rad	Radian
rms	Root-mean-square
sec	Second
$\circledcirc$	Convolution
A	Signal amplitude or constant carrier amplitude (volts)
AFC	Automatic frequency control
AGC	Automatic gain control
AM	Amplitude modulation
B	Channel noise bandwidth in frequency-division multiplex (hertz); also, a bandwidth-related parameter in ERPLD
B_p	Predetection bandwidth (hertz)
B_{CR}	Carson's rule bandwidth (hertz)
BER	Bit error rate
B_{IF}	IF filter 3-dB bandwidth (hertz)
BINR	Baseband intrinsic noise ratio
B_n	Equivalent noise bandwidth (hertz)
B_R	Bit rate
BWR	Base-bandwidth to channel-bandwidth ratio
CNR	Carrier-to-noise ratio (ρ)
$(CNR)_{AM}$	Input CNR referred to twice base bandwidth ($2f_b$)
$(CNR_{AM})_{TH}$	Threshold CNR referred to twice base bandwidth ($2f_b$)

D	Deviation index
DC	Direct current
D_e	rms frequency deviation (hertz)
DPSK	Differentially coherent phase-shift keying
E/η	Energy ratio
ERPLD	Extended-range phase-locked demodulator
F	Frequency modulation feedback factor
FDM	Frequency-division multiplex
FM	Frequency modulation
FMFB	FM feedback loop
FMFB-ERPLD	Compound-loop FMFB demodulator, ERPLD as internal demodulator
FMFB-FMFB	Compound-loop FMFB demodulator, FMFB as internal demodulator
FMFB-PLL	Compound-loop FMFB demodulator, phase-locked loop as internal demodulator
FSK	Frequency shift keying
GHz	Gigahertz (gigacycles per second)
$G(s)$	Open-loop transfer function
$H_2(s)$	Transfer function of loop baseband filter
$H_D(s)$	Transfer function of internal demodulator
$H(j\omega)$	Closed-loop response
$H(s)$	Closed-loop transfer function
$H_1(s)$	Transfer function of IF filter (FMFB)
$H_{L1}(s)$	Lowpass equivalent of $H_1(s)$
$H_{b1}(s)$	Baseband equivalent of $H_1(s)$
Hz	hertz (cycles per second)
IF	Intermediate frequency
K	Loop gain constant (product of phase detector sensitivity, amplifier gain, and voltage-controlled oscillator sensitivity in the phase-locked loop)
K_0	Closed-loop gain in FMFB
K_1	Phase-locked loop phase detector sensitivity (volts per radian); also LD sensitivity in FMFB
K_2	Amplifier gain (PLL and FMFB)
K_3	VCO sensitivity (radians per volt-second) (PLL and FMFB)

L	Multiplex noise loading ratio
LD	Limiter-discriminator
LLI	Loss-of-lock impulses
MHz	Megahertz (megacycles per second)
$\lvert M(j\omega)\rvert$	Magnitude of predetection filter response (PLL)
$\lvert M_p(j\omega)\rvert$	Magnitude of predetection filter response (FMFB)
MLR	Maximum likelihood receiver
MTBF	Mean time between failure
N	Spike rate, cycle skipping rate
$N(t)$	Additive noise
NCR	Noise-to-carrier ratio
NIF	Noise improvement factor
N_{po}	Output noise power from postdetection filter following the PLL (watts)
NPR	Noise power ratio
NT	Average number of encirclements per bit
PCM	Pulse code modulation
P	Noise penalty factor
P_e	Probability of error
P_s	Signal power
P_n	Noise power
PLD	Phase-locked demodulator
PLL	Phase-locked loop
PM	Phase modulation
rf	Radio frequency
$\lvert R(j\omega)\rvert$	Magnitude of postdetection filter response
RLC	Resistance-inductance-capacitance (network)
SNR	Signal-to-noise ratio
SNR_{TT}	Test-tone signal-to-noise ratio
S_p	Speech power
S_{po}	Postdetection filter output signal power (watts)
$S(\omega)$	Power spectral density of transmitted baseband (watts per hertz)
ThI	Threshold impulses
TT	Test-tone
V	Voltage
VCO	Voltage-controlled oscillator
VCXO	Voltage-controlled crystal oscillator
VSWR	Voltage standing wave ratio
$W(f)$	Power spectral density function
$\cong$	Approximately equal

INTRODUCTION

Introduction to Phase-Locked Loops

The Phase-Locked Loop or PLL is a negative-feedback circuit in which the controlled variable is the phase of a carrier. A block diagram of the basic PLL is shown in Fig. 1. It consists of a Phase-Detector, a Lowpass Filter/Amplifier, and a Controlled Oscillator. The input to the PLL is a carrier fed to one of the two inputs of the Phase Detector while the output is taken either from the output of the Controlled Oscillator or from its input, depending upon application. In the usual operation of the PLL, the frequency of the Controlled Oscillator is identical to that of the input carrier (on a cycle to cycle count basis) and the phases are nearly the same.

If the frequency of the input carrier differs from the free-running frequency of the Controlled Oscillator then a control signal develops in the loop which forces the two frequencies to be the same. This control signal is generated in the Phase Detector and is amplified by the Lowpass Filter/Amplifier before being applied to the Controlled Oscillator. In other words, if the free-running frequencies differ, then in the locked loop it is reflected as a phase difference. Typically, the gain of the loop is made high so that this phase difference is small.

There are two basic areas of application for the PLL: Synchronization and FM detection. In synchronization applications, a replica of the desired input carrier is obtained from the output of the Controlled Oscillator; in FM detection applications the output is the control signal fed to the Controlled Oscillator. In both of these application areas the PLL often outperforms other available techniques. One of the earliest widespread use of the PLL was as a synchronizer in television receivers. In a more sophisticated operation as a synchronizer, the PLL generates

an almost unlimited number of ultra-stable frequencies in very fine steps, using only a single crystal oscillator as a reference. This is known as Frequency Synthesis. On the other hand, as an FM detector, the PLL can reduce the noise threshold effect -- something that is not possible with conventional discriminators. In these applications the PLL was used before the advent of integrated circuits. With the appearance of the single chip PLL (except for the components of the Lowpass Filter), it became advantageous to use the PLL in a myriad of other applications because of its low cost and size.

A basic design parameter of the loop is its bandwidth. The PLL designed for synchronization applications is typically of very narrow bandwidth so that it locks only to a particular frequency at the input and ignores all other carriers, including sidebands. On the other hand, a PLL designed for FM detection must at least be wide enough to follow the frequency deviations of the desired carrier. However, for all PLL designs there is an optimum bandwidth. It cannot be too narrow for it will not follow the frequency variations of the desired carrier. Then, it should not be wider than necessary because a wider bandwidth means that more noise and interference appearing at the input will affect the operation of the loop and its output.

The dynamics and the bandwidth of the PLL are a function of the open loop gain and the frequency response of the Lowpass Filter. Mostly, the PLL response is designed to be of second order (two poles in its complex frequency response), but first and third order loops are also used in special applications. The order of the loop is determined by the Lowpass Filter but the open loop gain also enters when the bandwidth and damping are considered. While the PLL is a nonlinear device due to the presence of a phase detector, most calculations are made using a Linear Equivalent Model.

To understand the linear model, we first introduce the exact model

shown in Fig. 2. The input to the model, $\phi_i(t)$, is the phase of the desired carrier appearing at the input to the PLL. The loop responds with $\phi_r(t)$, the phase of the Controlled Oscillator. The Phase Detector output is generally a nonlinear function of the phase error $\phi_e(t) = \phi_i(t) - \phi_r(t)$. This is why the Phase Detector is represented by a subtractor and a nonlinear block $\mathcal{V}[\ ]$. Ignoring the noise n(t) for the present, we proceed to the Lowpass Filter/Amplifier which is represented by itself since the input/output quantities are voltage analogs of phase. The Controlled Oscillator is modeled as an integrator because its output is phase while its input is proportional to frequency deviation. It can be shown [Ref.1] that the bandpass noise present at the input to the PLL can be represented by a lowpass noise n(t) introduced as indicated. The noise n(t) is the lowpass equivalent of the bandpass noise, appropriately scaled. In particular, if the bandpass noise is of bandwidth B and power density η, then n(t) is lowpass with bandwidth B/2 and power density $2\eta/A^2$, where A is the amplitude of the desired carrier at the circuit point where η is measured.
K_1 is the sensitivity of the phase detector at the operating point.

The basic nonlinearity of the PLL is in the Phase Detector. Typical Phase Detector characteristics are shown in Fig. 3. Now suppose the phase error $\phi_e(t)$ is small; then over that small region of operation any of the Phase Detector characteristics can be considered linear. This is what leads to the linear equivalent model shown in Fig. 4. Observe that the nonlinearity $\mathcal{V}[\ ]$ has been replaced by the constant K_1. Using the linear model, we can apply all the techniques of linear analysis to the PLL -- certainly not a minor consideration. It turns out that in many design cases a linear analysis will suffice to provide performance and optimization guidelines. There are, however, a class of problems where nonlinear analysis must be made and phase-plane or Fokker-Planck techniques (Ref. 1) are then resorted to.

The typical Lowpass Filter for the popular second-order PLL is the

lead-lag network shown in Fig. 5, while the first-order loop has no filter at all. The design parameters for the second-order loop are the overall loop gain and the pole and zero of the lowpass filter. The first-order loop has only the gain as a design parameter; therefore, it does not provide sufficient flexibility. Higher-order loops improve performance only in very limited applications (e.g. frequency ramp tracking) and tend to be unstable; hence, they are shunned. There are also second-order loops with filters having zeros in the right-half of the complex frequency plane that provide improved performance in some applications (Ref. 2 Ch. 8). Using linear analysis we may obtain the closed-loop transfer function $H(s)$ and noise bandwidth B_n. These are listed in Table I and apply to both outputs of the PLL.

It has been assumed so far that the PLL is always in synchronism, i.e., the input carrier and the Controlled Oscillator are of identical frequency but possibly of different phase. There are no known useful applications of the PLL where synchronism is not required. However, as the carrier is applied to the PLL, synchronism may only have to be achieved (acquisition problems). Furthermore, once acquired, synchronism may be lost if the input carrier frequency varies unduly (holding problems). Calculations for <u>acquisition</u> and <u>holding</u> must be made on the nonlinear model of the PLL. The following definitions are of interest in reference to synchronism:

<u>Hold-in Range</u>: Consider a PLL synchronized with $\omega_i = \omega_{ro}$, where ω_i is the input frequency and ω_{ro} is the free-running frequency of the Controlled Oscillator. Now slowly vary ω_i and ω_r will follow, but only up to a limit. The hold-in range is defined as the value of $|\omega_i - \omega_{ro}|$ for which ω_r just fails to follow ω_i, resulting in a loss of synchronization.

The hold-in range can be calculated for any PLL by finding the maximum control we have available for the Controlled Oscillator. It

is the product of the maximum DC output from the Phase Detector multiplied by the gain of the Lowpass Filter/Amplifier and the sensitivity of the Controlled Oscillator. There is usually no problem in obtaining a sufficient hold-in range in a second-order PLL. However, we often do have problems in obtaining sufficient lock-in and pull-in ranges. These are defined next.

Lock-in Range: Consider the case where the PLL is not locked when the input is applied. The lock-in range is the maximum frequency difference $|\omega_i - \omega_{ro}|$ for which the loop will lock without slipping cycles; only a phase transient will appear. Approximately, the lock-in range equals the frequency at which the open-loop response has unity gain.

Pull-in Range: This is the maximum initial frequency difference $|\omega_i - \omega_{ro}|$ for which the loop will eventually lock. Some approximate formulas for the pull-in range are given in the references. However, one cannot utilize the full theoretical pull-in range since it is affected by noise and DC offsets, and the time it takes to pull in is often too long. A number of schemes have been developed to extend the pull-in range and decrease the pull-in time. (See, for example, Ref. 3).

The examples which follow highlight some advantages in the use of the PLL. The list of actual applications of the PLL in current electronics equipment is indeed extensive.

Example: FM Detector (Ref.2 , Ch. 6)

Consider the detection of an FM carrier modulated by voice (300-3300 H_z) with a peak frequency deviation of 10KH_z. Optimizing the second-order PLL for a minimum phase error due to both signal and noise, one obtains the following parameters: K (open-loop gain) = 6.6×10^5 radians/sec., b (pole of Lowpass Filter) = 1.9 kiloradians/sec., and a (zero of lowpass filter) = 35.4 kiloradians/sec.

Figure 6 shows a plot of output signal-to-noise ratio versus input carrier-to-noise ratio (experimentally measured) with the predetection filter having a Carson's rule bandwidth (a widely-accepted rule). The improved performance of the PLL over the conventional limiter-discriminator in the region of low received carrier power is readily apparent. One should note, however, that even if the improved performance is not of interest one would frequently prefer the PLL over the discriminator for reasons of economy and size. The PLL in addition to acting as an amplitude-insensitive discriminator, may also perform (to a degree) simultaneously as an IF filter.

JK/dm

Example: Frequency Synthesizer (Ref. 4)

A simple frequency synthesis PLL is shown in Fig. 7. In addition to the conventional components of Fig. 1, there is a Programmable Frequency Divider between the Controlled Oscillator and the Phase Detector. The input reference frequency f_{ref} is usually derived from a crystal oscillator and is very stable. With the PLL in synchronism, $f_o/N = f_{ref}$ and, therefore, the output frequency $f_o = Nf_{ref}$. Since N is programmable, the output frequency can be varied in steps of f_{ref}. Furthermore, it has the same fractional stability as f_{ref}. Frequency synthesizers are now used extensively for tuning receivers and transmitters as well as test generators.

Related loops: There are a host of loops related to the PLL such as Costas, Early-late Gate, etc., and a variety of multiple loops. Also, the PLL can be implemented using equivalent digital operations.

References

For a thorough treatment of the PLL in FM detection as well as the use of multiple loops the reader is referred to reference 2. Reference 4 is the equivalent for frequency synthesis. For nonlinear analyses the reader is referred to reference 1 (classical topics) and reference 5 (most general). Reference 3 is a second edition of a popular general text (very lucid) and reference 7 is helpful in linear analysis. For a discussion of related loops the reader is referred to reference 6.

1. A.J. Viterbi, Principles of Coherent Communication, McGraw-Hill Book Co., 1966.
2. J. Klapper and J.T. Frankle, Phase-Locked and Frequency-Feedback Systems: Principles and Techniques, Academic Press, 1972.
3. F.M. Gardner, Phaselock Techniques, John Wiley and Sons, 1979 (2nd Ed.).
4. V. Manassewitsch, Frequency Synthesizers: Theory and Design, John Wiley and Sons, 1980.

W. F. Egan, Frequency Synthesis by Phase Lock, John Wiley and Sons, 1981.

5. W.C. Lindsey, Synchronization Systems in Communication and Control, Prentice-Hall, 1972.

6. W.C. Lindsey and M.K. Simon, Telecommunication Systems Engineering, Prentice-Hall, 1973.

7. A. Blanchard, Phase-Locked Loops: Application to Coherent Receiver Design, John Wiley and Sons, 1976.

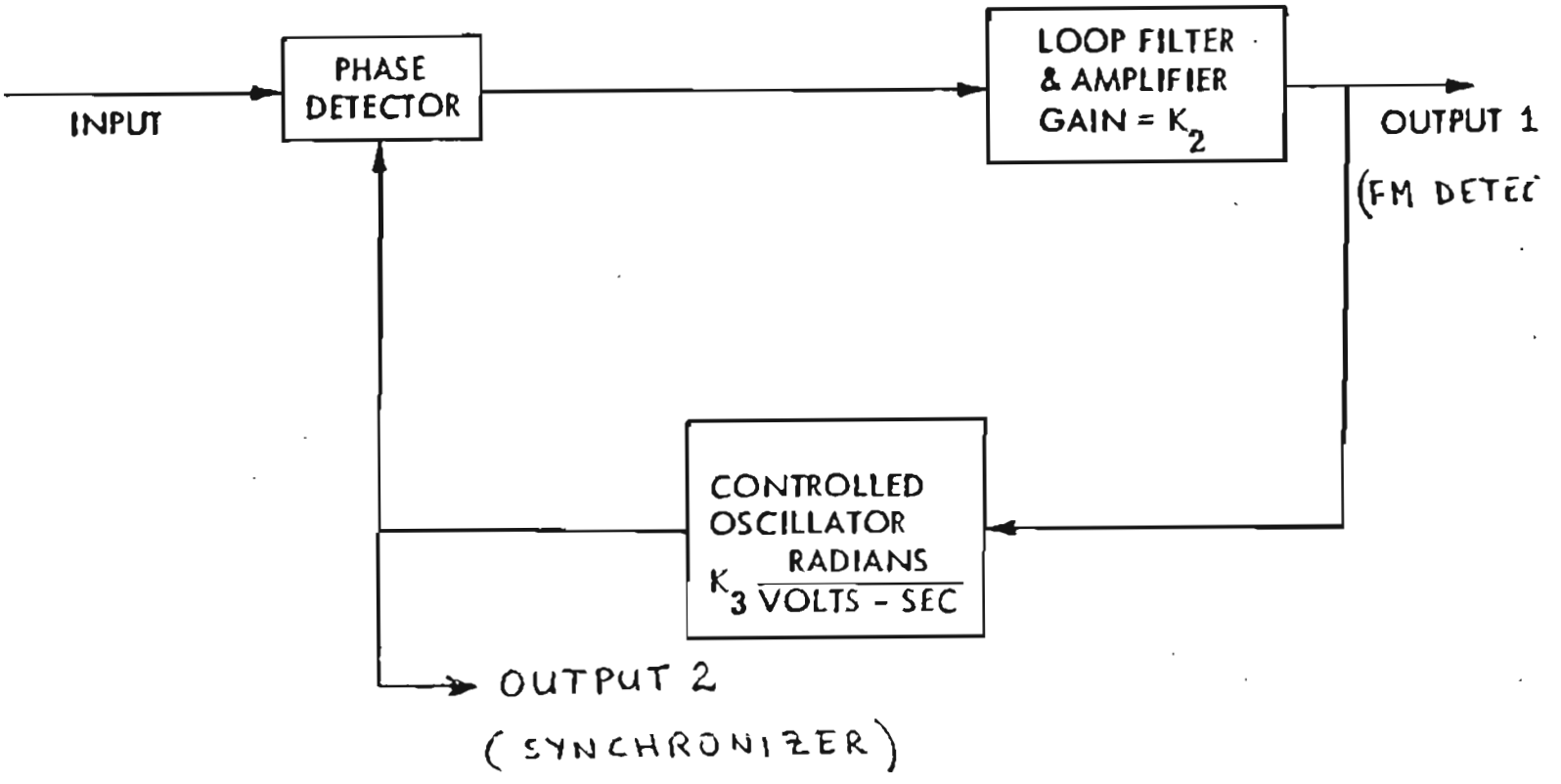
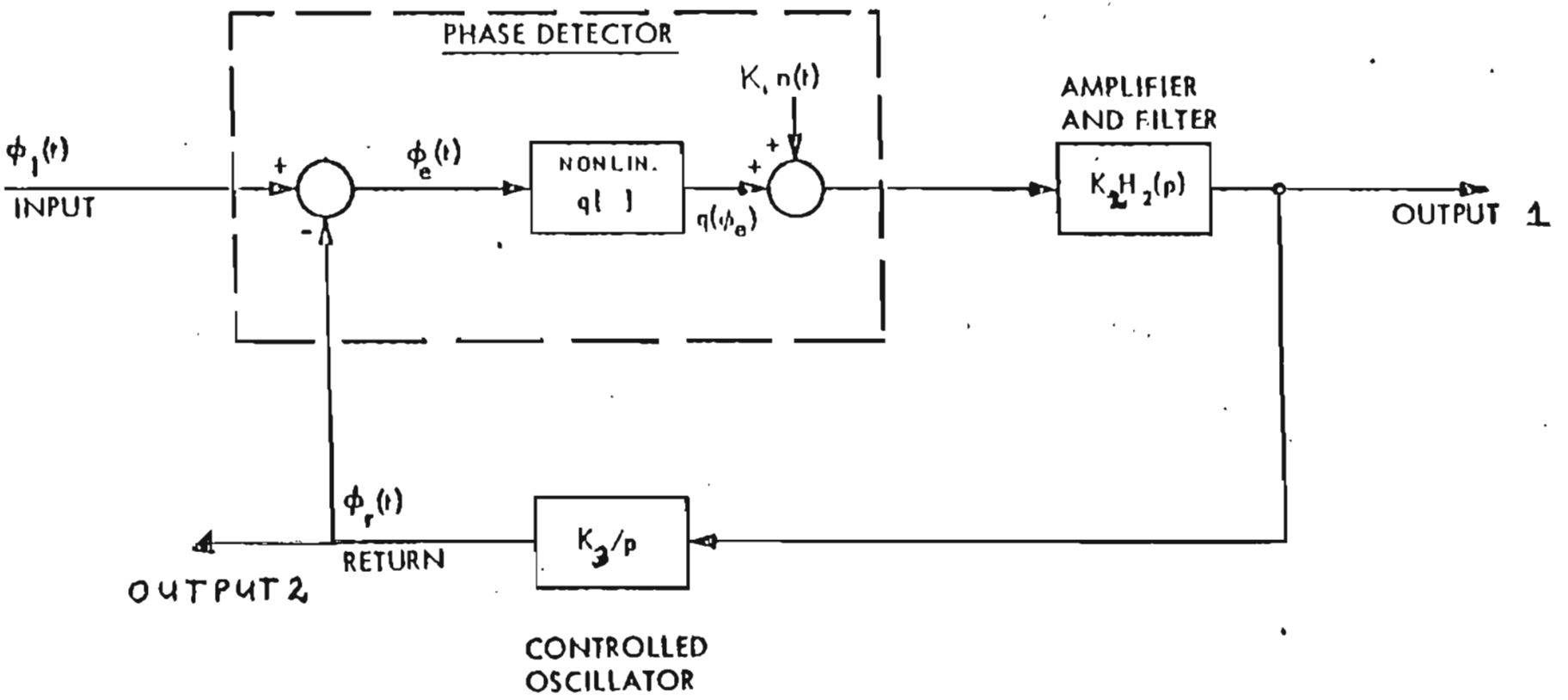


FIG. 1 Basic Phase-Lock Loop

FIG. 2 EXACT PLL MODEL



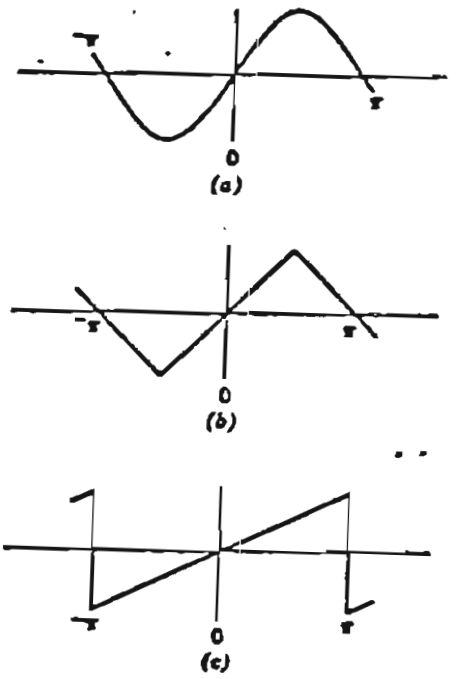


FIGURE 3 Phase-detector characteristics.
(a)Sinusoidal (b)Triangular(c)Sawtooth.

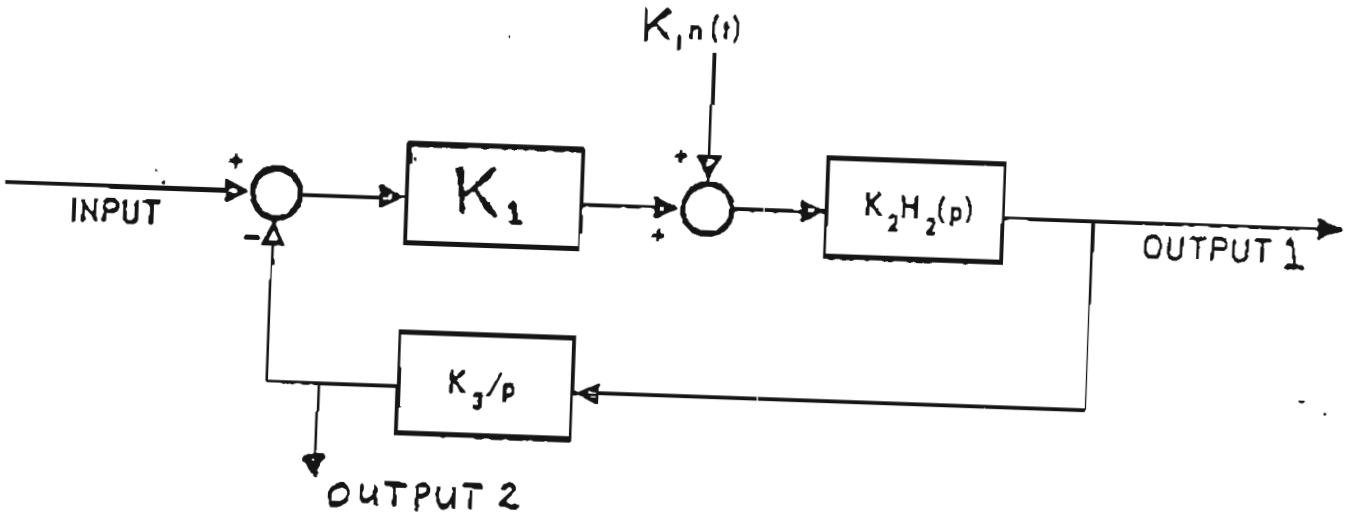


FIGURE 4 LINEAR PLL MODEL

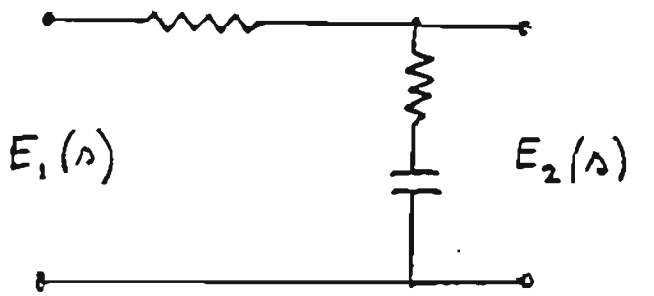


FIG. 5 LEAD - LAG NETWORK

LOOP ORDER = NUMBER OF POLES IN G(S)

G(S) = OPEN LOOP RESPONSE

H(S) = CLOSED LOOP RESPONSE

$K = K_1 K_2 K_3$

LOOP ORDER	FILTER $H_2(S)$	OPEN-LOOP RESP. $G(S)$	CLOSED LOOP RESP. $H(S)$	LOOP NOISE BANDWIDTH B_n (Hz)
1	1	$\frac{K}{S}$	$\frac{1}{\frac{S}{K}+1}$	$\frac{K}{4}$
2	$\frac{\frac{S}{a}+1}{\frac{S}{b}+1}$	$\frac{K}{S}\ \frac{(\frac{S}{a}+1)}{(\frac{S}{b}+1)}$	$\frac{(\frac{S}{a}+1)}{\frac{S^2}{Kb}+(\frac{1}{K}+\frac{1}{a})S+1}$	$\frac{Kb\left(\frac{K}{a}+a\right)}{4a\left(\frac{K}{a}+b\right)}$

TABLE 1

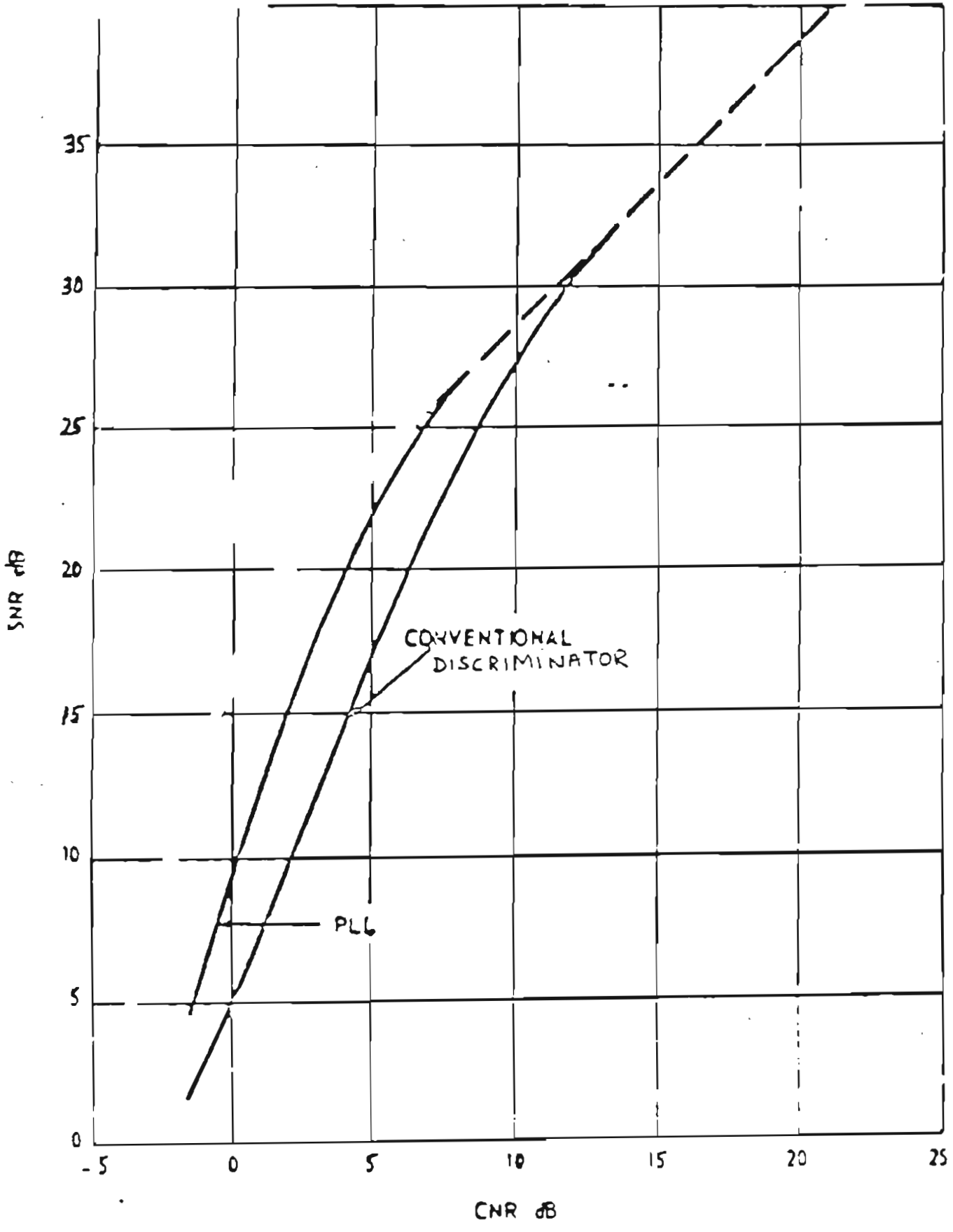


FIG. 6 PLL PERFORMANCE AS AN FM DETECTOR

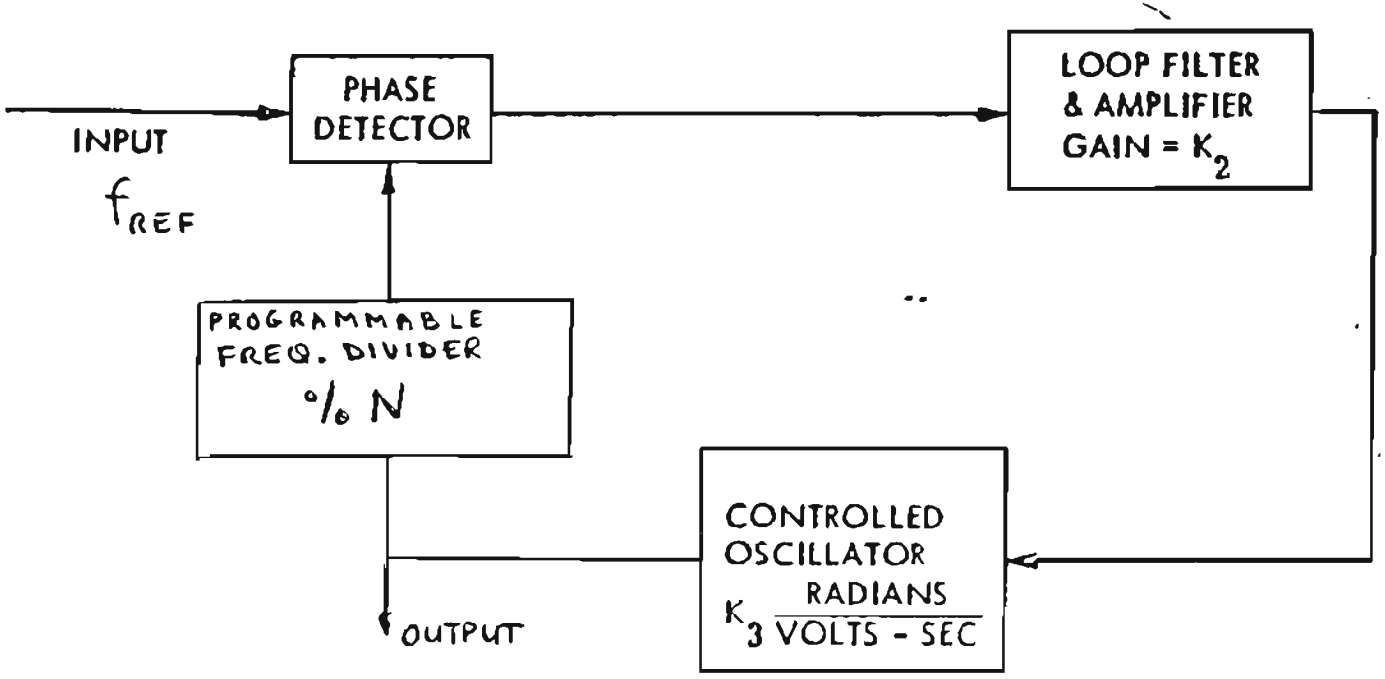
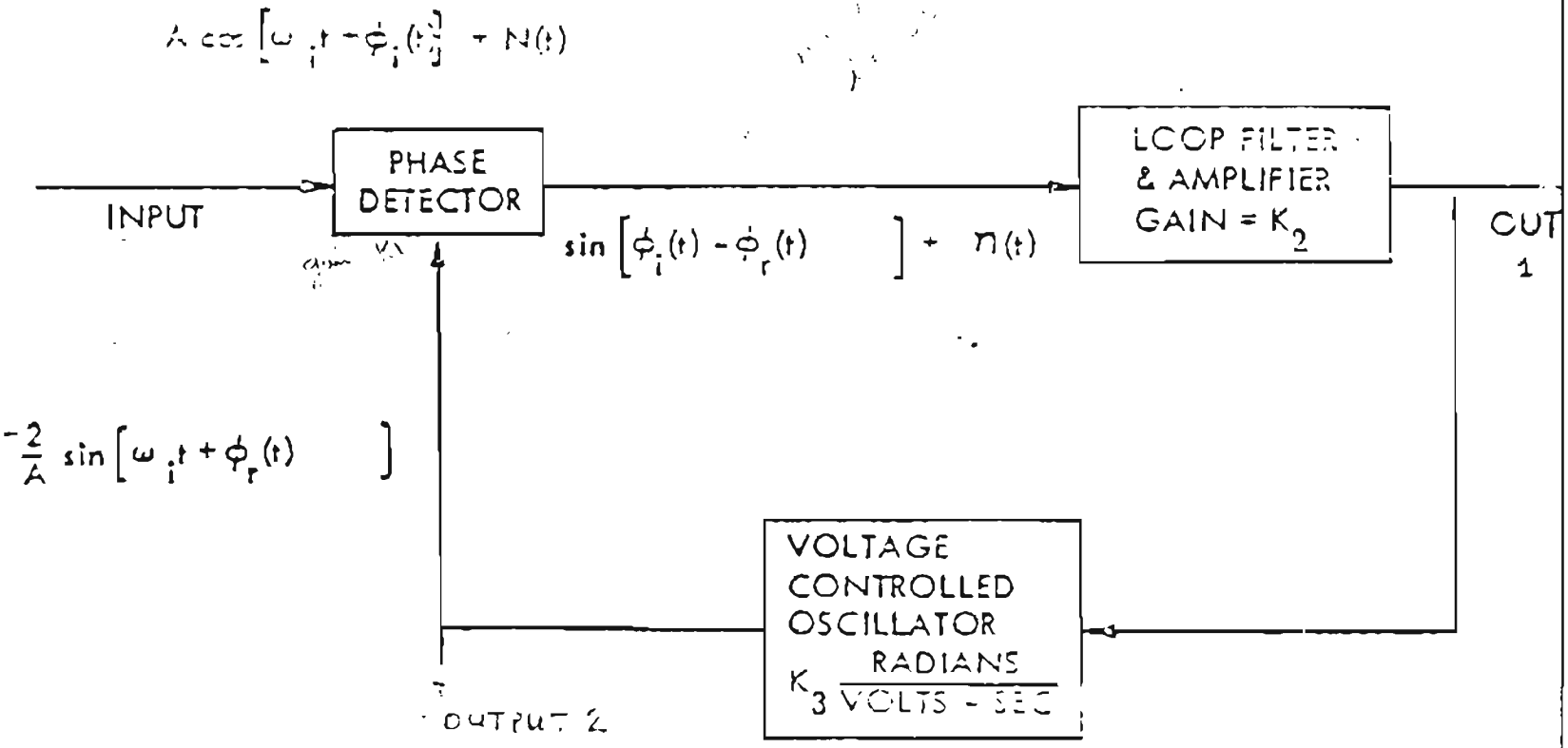


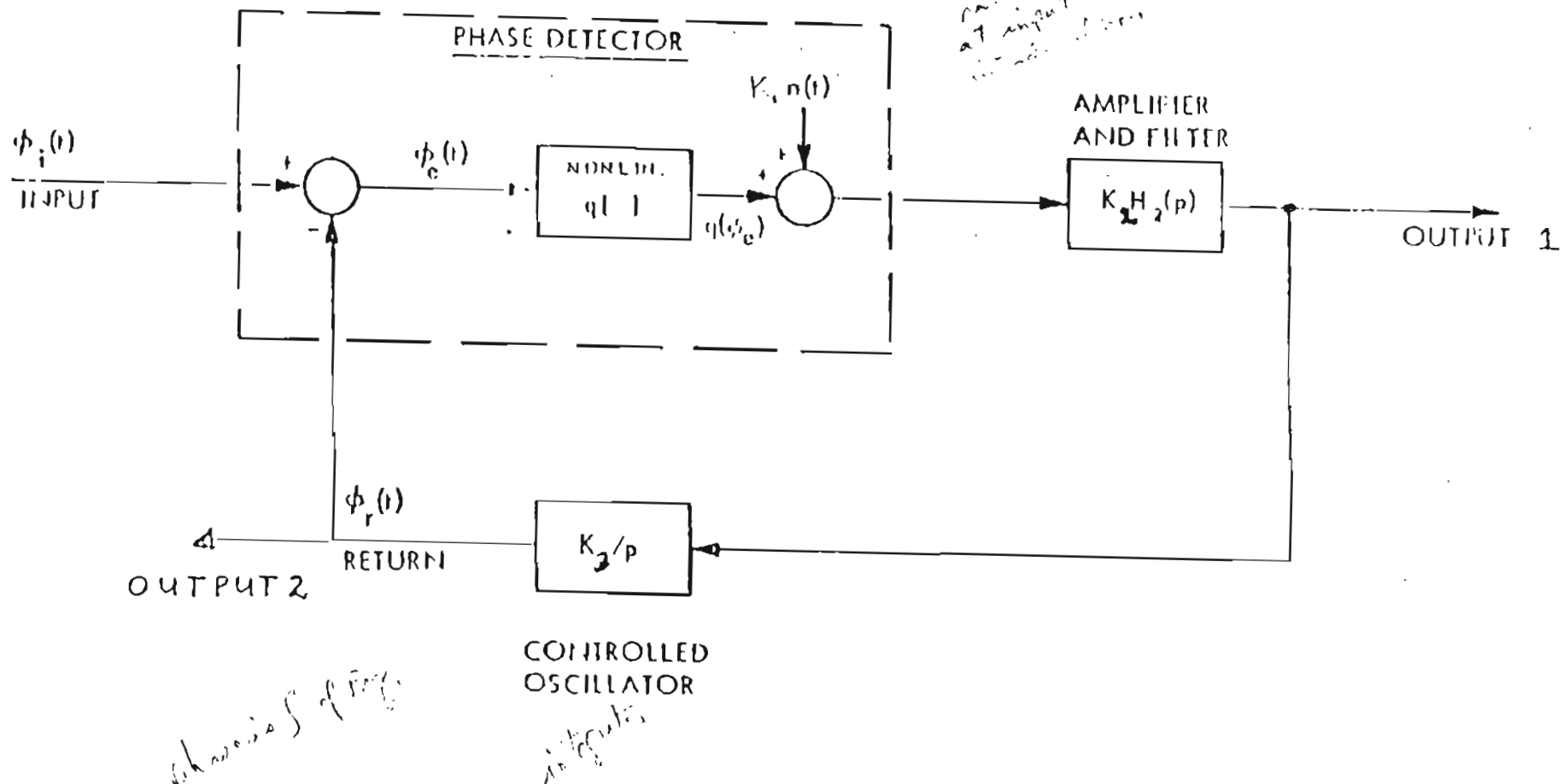
FIG. 7 FREQUENCY SYNTHESIZER

LINEAR ANALYSIS.



Basic Phase-Lock Loop in Synchronized Mode

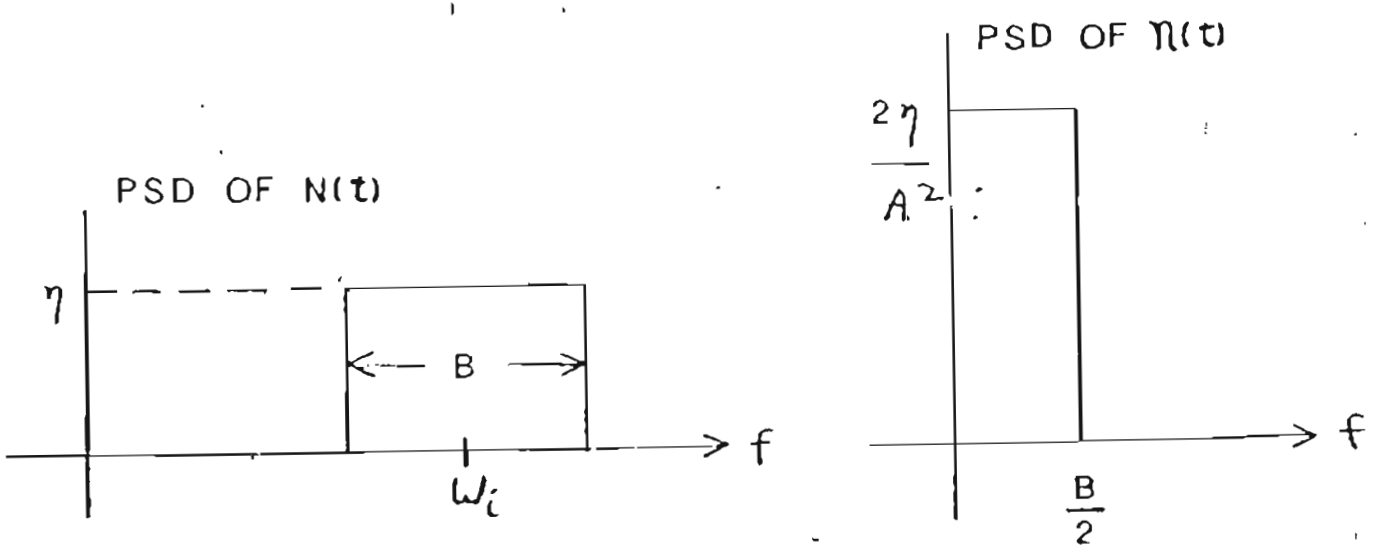
FIG. 2 EXACT PLL MODEL



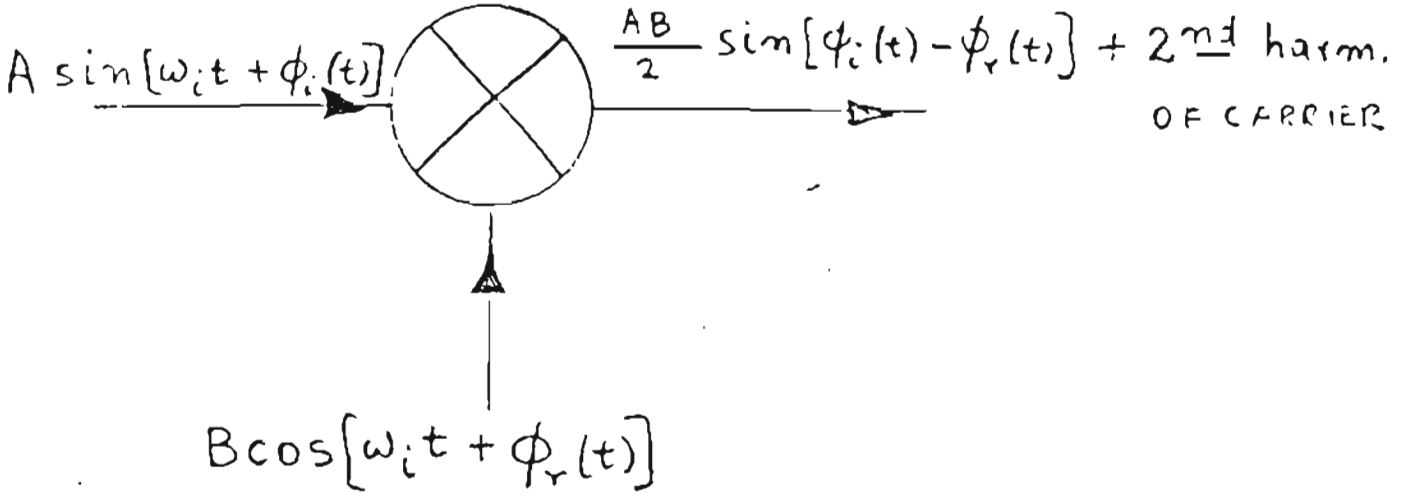
CHARACTERIZATION OF $n(t)$ vs $N(t)$

$N(t)$ = INPUT NOISE

$n(t)$ = EQUIV. GEN. IN PLL MODEL



MULTIPLIER-TYPE PHASE DETECTOR



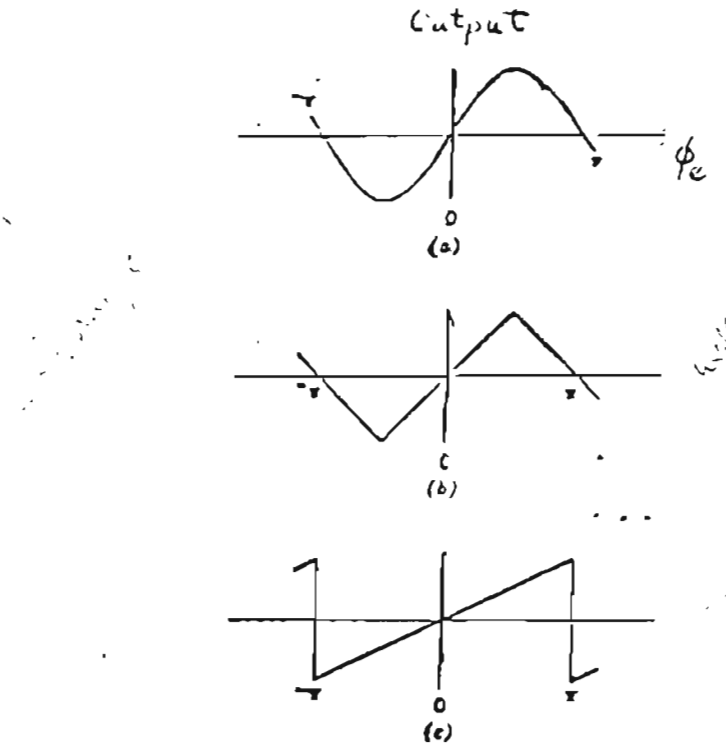


FIGURE 3 Phase-detector characteristics
(a)Sinusoidal (b)Triangular (c)Sawtooth

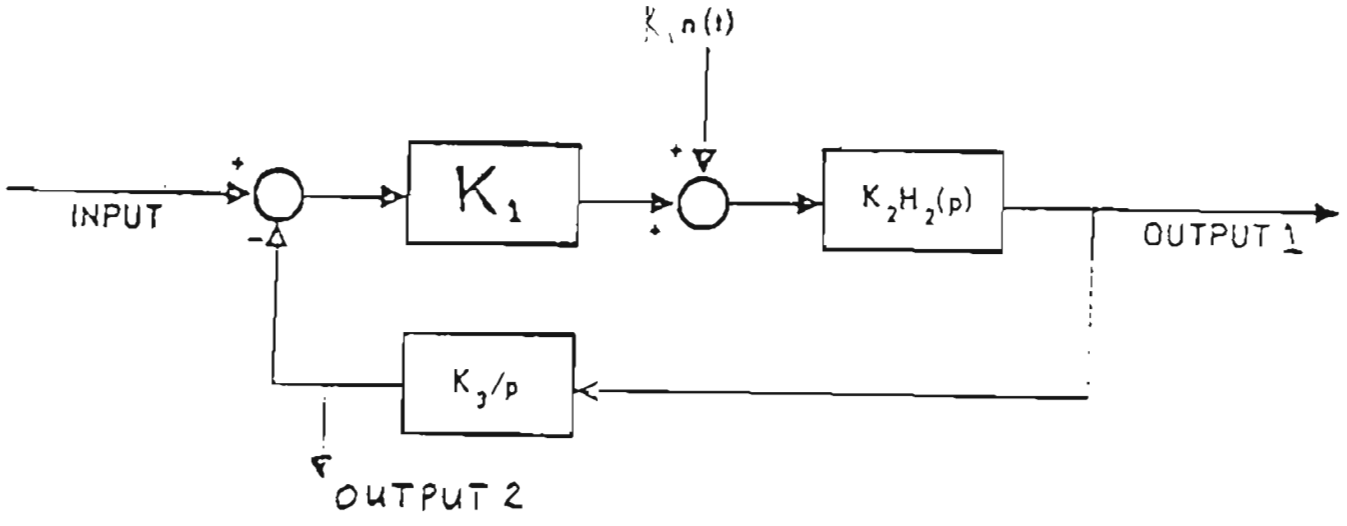


FIGURE 4 LINEAR PLL MODEL
[Applies for a limited range of ϕ e]

NOW THAT WE HAVE AN EQUIVALENT LINEAR MODEL, WE CAN APPLY ALL THE THEORY OF LINEAR SYSTEMS.

PLL TRANSFER FUNCTIONS

LOOP ORDER = NUMBER OF POLES IN G(S)

G(S) = OPEN LOOP RESPONSE

H(S) = CLOSED LOOP RESPONSE

$K = K_1K_2K_3$

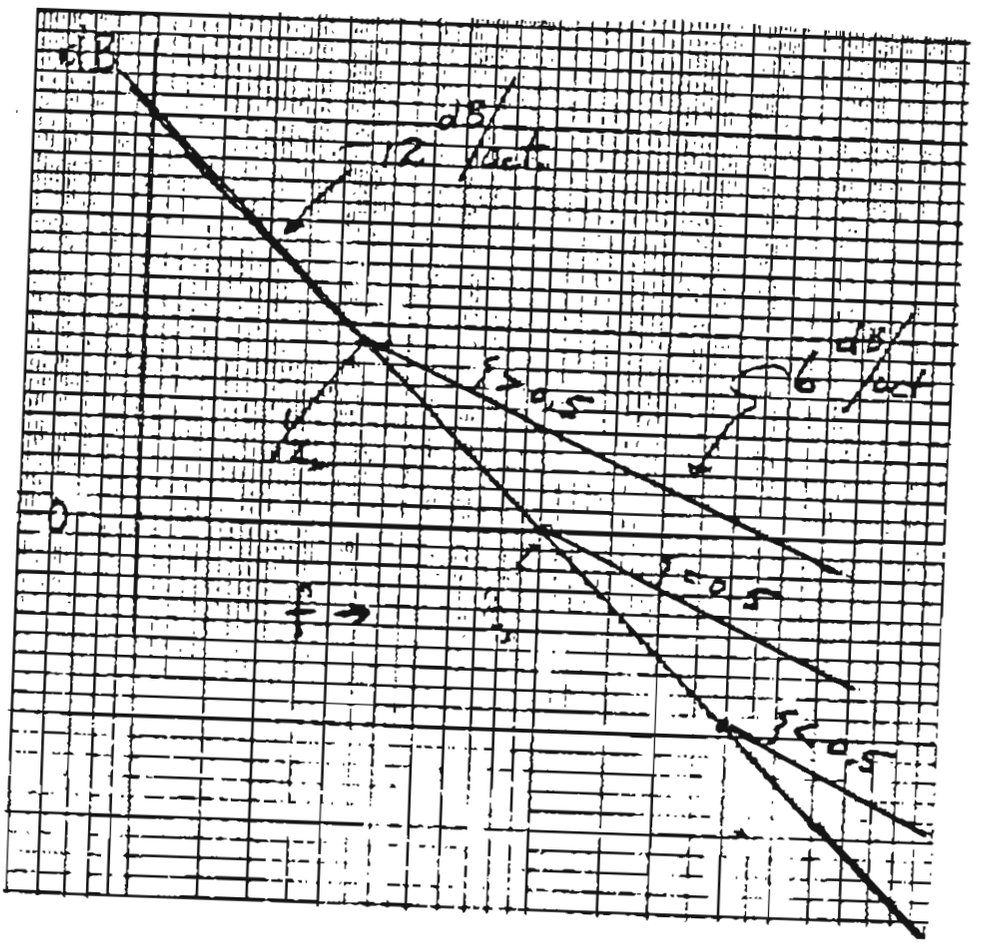
LOOP ORDER	FILTER $H_2(S)$	OPEN-LOOP RESP. G(S)	CLOSED LOOP RESP. H(S)	LOOP NOISE BANDWIDTH Bn (H_2)
1	1	$\frac{K}{S}$	$\frac{1}{\frac{S}{K}+1}$	$\frac{K}{4}$
2	$\frac{\frac{S}{a}+1}{\frac{S}{b}+1}$	$\frac{K}{S}\frac{(\frac{S}{a}+1)}{(\frac{S}{b}+1)}$	$\frac{(\frac{S}{a}+1)}{\frac{S^2}{Kb}+(\frac{1}{k}+\frac{1}{a})S+1}$	$\frac{Kb(\frac{Kb}{a}+a)}{4a(\frac{Kb}{a}+b)}$

TABLE 1

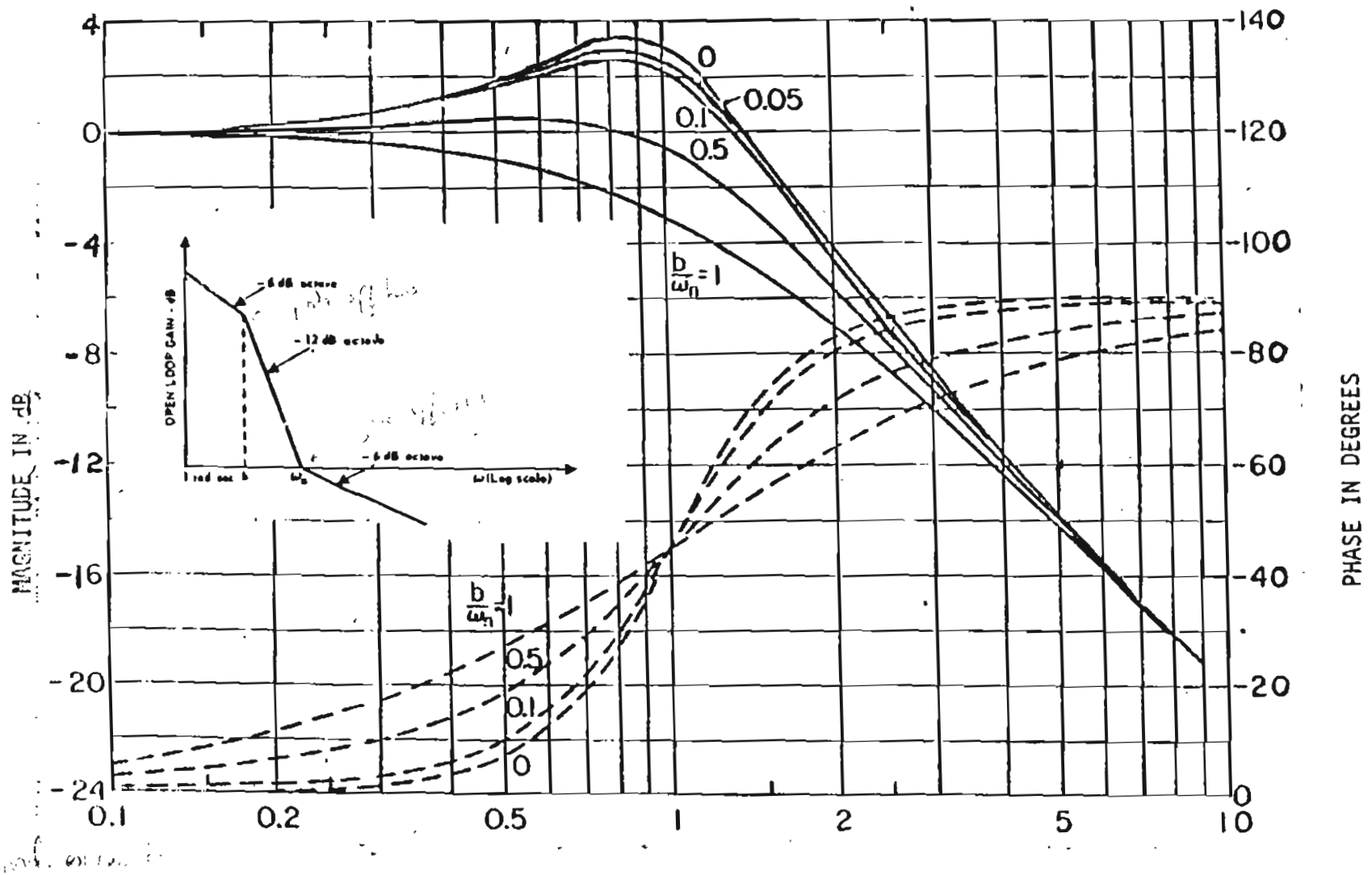
OPEN-LOOP RESPONSE

$$G(s) = \frac{K_o}{s} H_2(s) = \frac{K_o}{s} \frac{s^2 t_2 + 1}{s^2 t_1}$$

	G(s)
$s \to 0$	$\frac{K_o}{s^2 t_1} \to \infty$
$s \to \infty$	$K_o \frac{t_2}{t_1} \to 0$



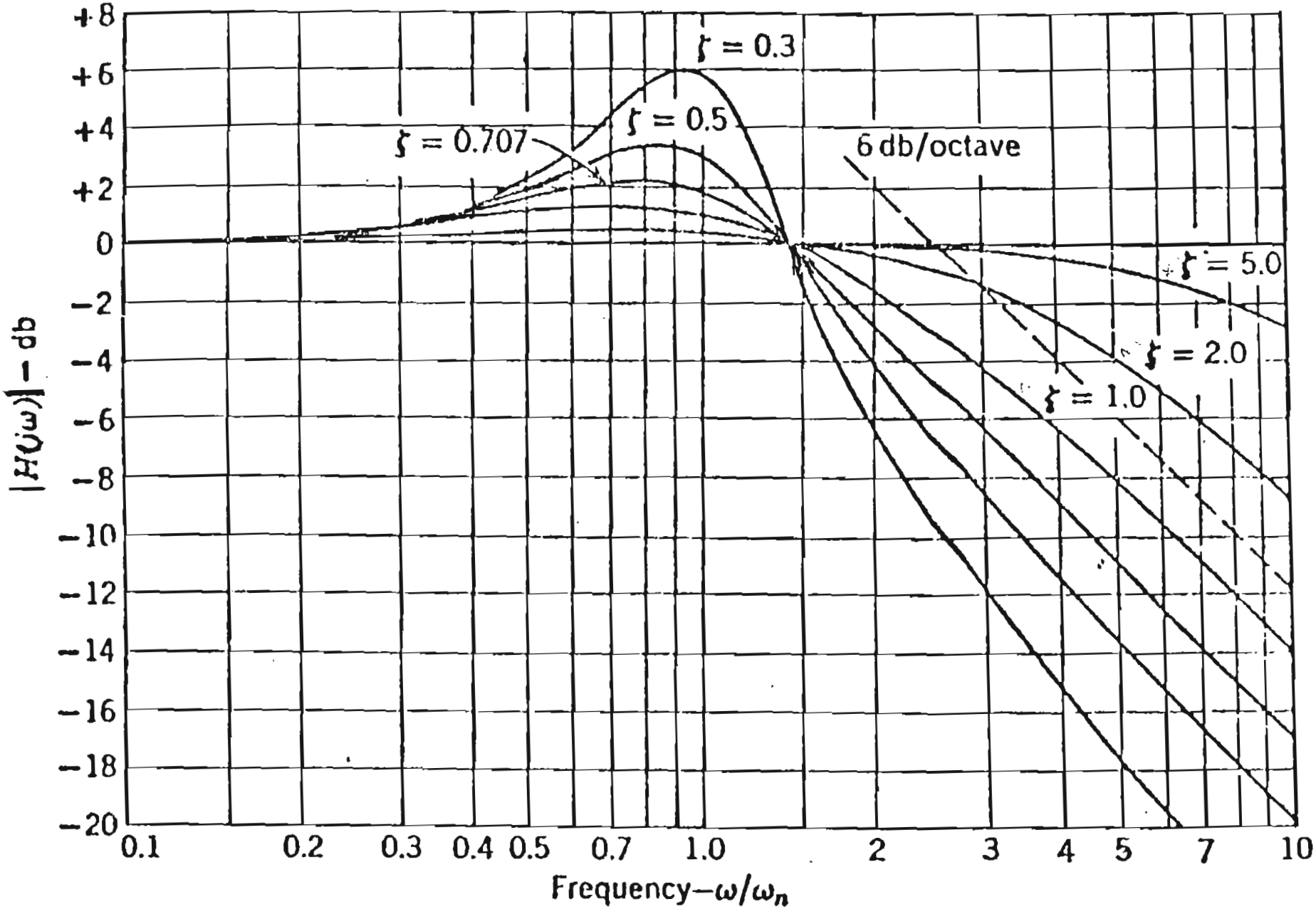
F 3

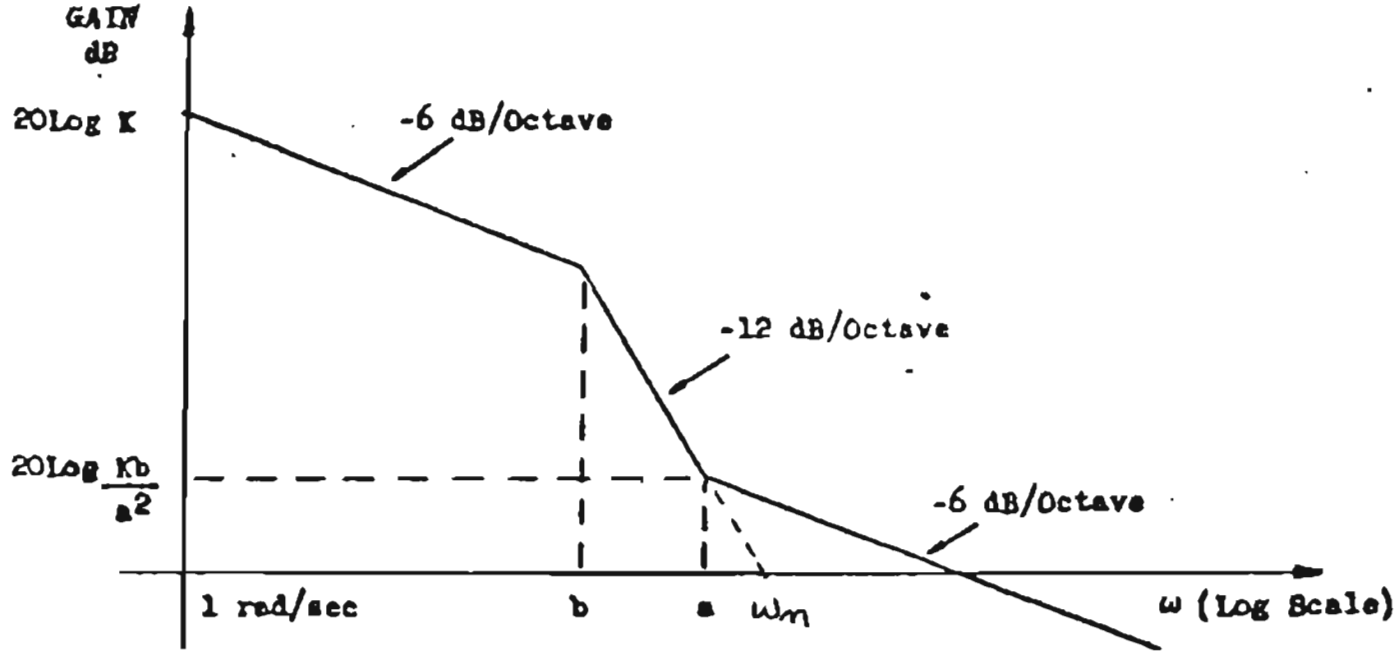


(a)

Responses of first and second-order, type-one PLL (a)Closed-loop response with the pole frequency as a parameter. (Example: $w_n = a = (Kb)^{1/2}$; Nominal design: b=0; b/w_n=1 is first-order loop, b/w_n is less than unity for second-order loops-: magnitude;---:phase.) (b)Open-loop amplitude response (asymptotic).

PLL CLOSED-LOOP RESPONSES





GRAPHICAL DETERMINATION OF K AND W_n

STEP RESPONSE

The ϕ_e for a step in frequency at the input, is (by lin. analysis)

$$\phi_e(t) \approx \frac{\Delta w_i}{K} \left[1 + \frac{a}{b} e^{-at} - \frac{a}{b} e^{-\frac{Kb}{a} t} \right]$$

1. Transient component much larger than steady-state, by factor $\frac{a}{b}$.

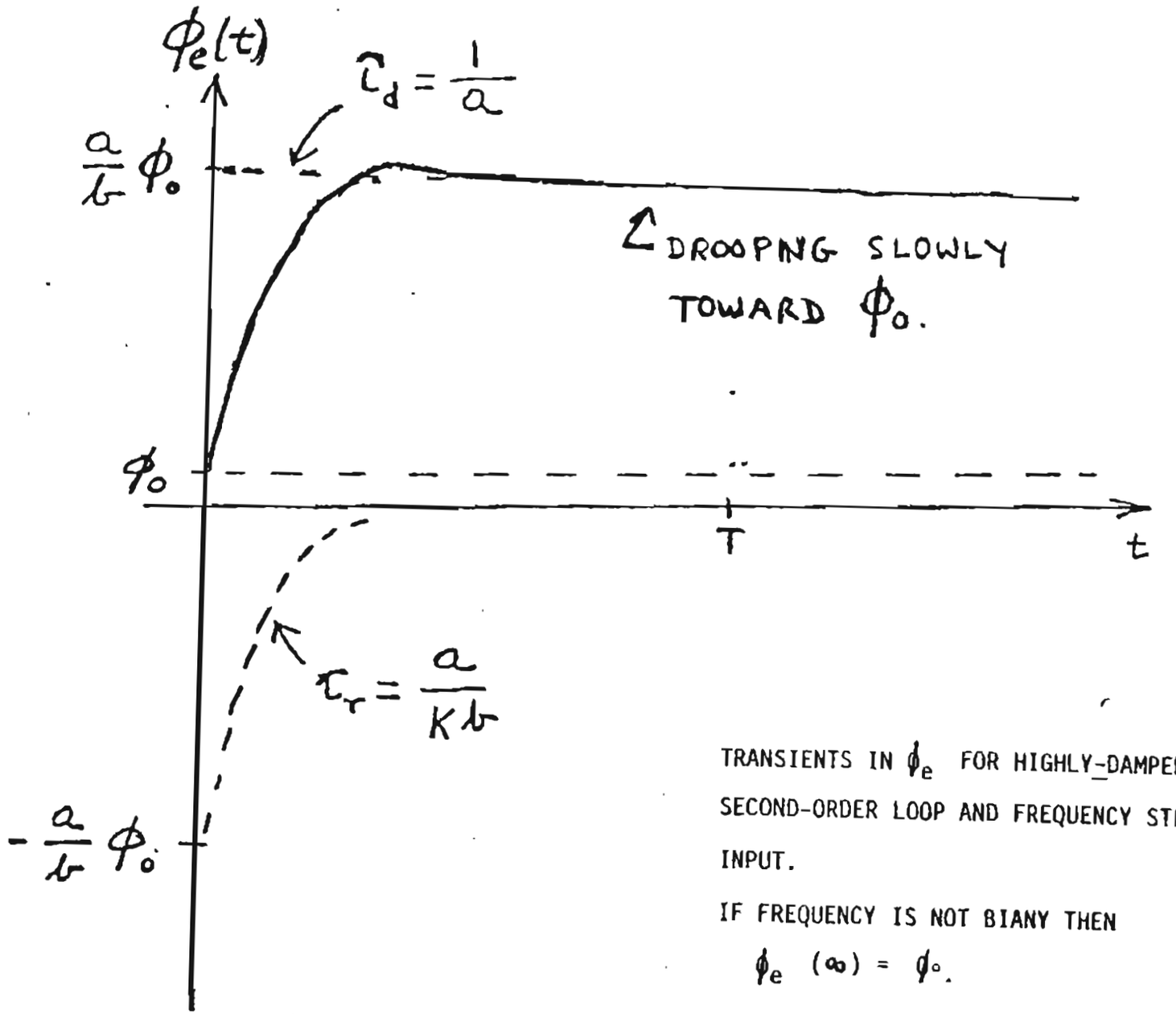
2. There are 2 parts to transient:

   one rises radidly with

   $$\tau_r = \frac{a}{Kb}$$

   The other droops slowly with

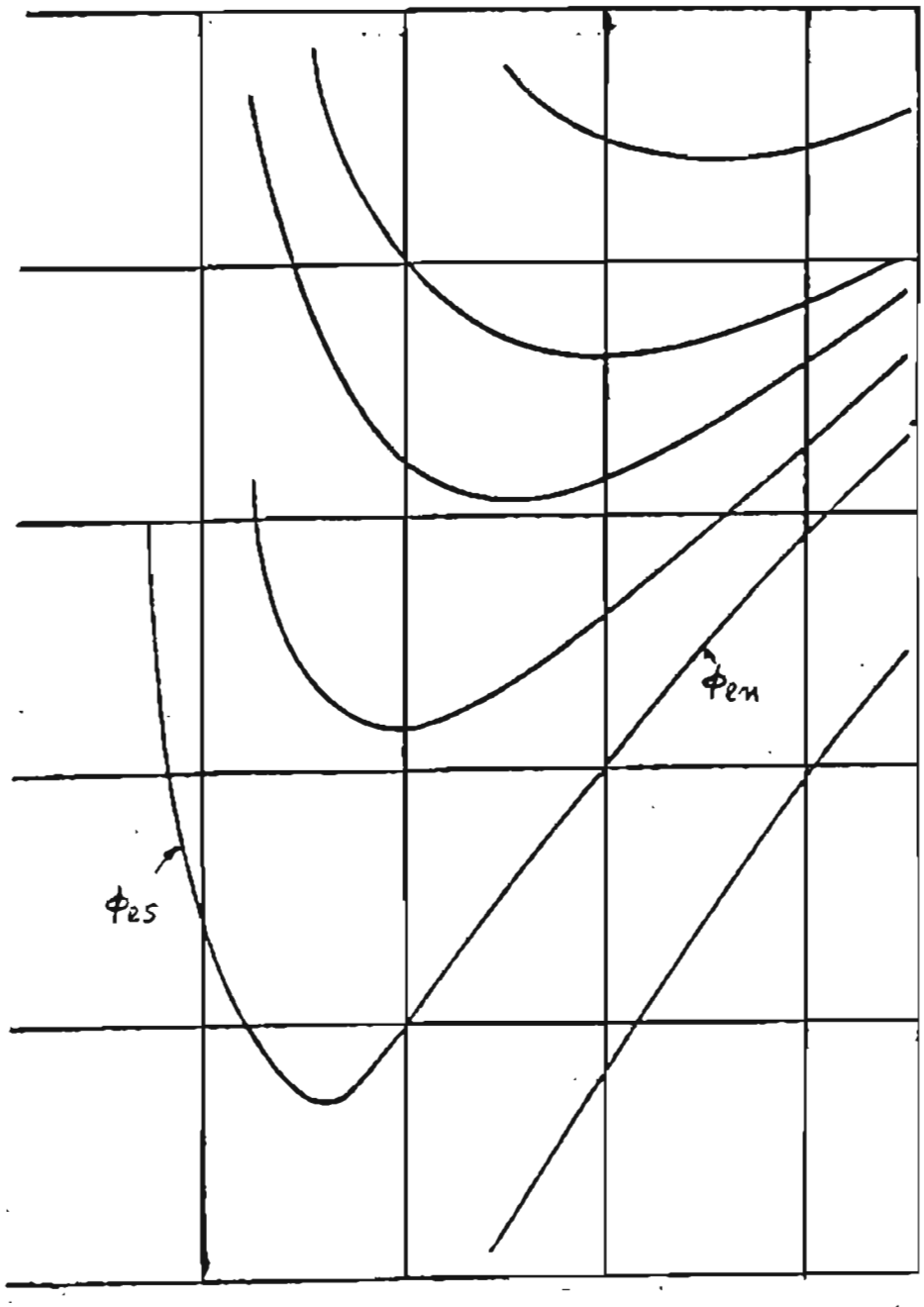
   $$\tau_d = \frac{1}{a}$$



TRANSIENTS IN ϕ_e FOR HIGHLY-DAMPED SECOND-ORDER LOOP AND FREQUENCY STEP INPUT.

IF FREQUENCY IS NOT BIANY THEN

$\phi_e(\infty) = \phi_0$.



ϕ_{en} = phase error due to noise
(increases with Bn)

ϕ_{es} = phase error due to signal
(decreases with Bn)

Illustration of phase error vs. PLL bandwidth
(Parameter: modulation)

In a certain class of design problems the PLL bandwidth is optimized for a minimum total phase error, given the signal deviation and interference.

PROBLEMS FOR LINEAR ANALYSIS

A PLL has the following parameters:

K_1 = 250 mV/rad K_2 = 4 K_3 = 10,000 RPS/V

The phase detector is a multiplier.

$$H_2(s) = \frac{\frac{s}{1000} + 1}{\frac{s}{100} + 1}$$

The free-running VCO output is $4\cos(10^6 t + 45^*)$

1. The input to the PLL is $2\sin(10^6 t + 10^3 t)$.

   Find (a) Output 1, (b) Output 2, and (c) phase error. All at steady state.

2. Repeat problem 1 with a PLL input of

   $2\sin(10^6 t + 30^* + 0.5\sin 1000t)$

3. The input to the PLL is $2\sin 10^6 t$ plus noise of power spectral density 10^{-6} W/Hz which is flat over the band of interest. Find the mean-square value of the phase jitter of the VCO output due to this noise.

SOLUTIONS TO PROBLEMS FOR LINEAR ANALYSIS

GENERAL

$K = K_1 K_2 K_3 = (0.25)\ (4)\ (10{,}000) = 10^4$

$a = 1000, \quad b = 100$

$w_n = \sqrt{Kb} = 1000 = a$ A response plot for this case is on p.

Problem 1

(a) Output 1 $= \dfrac{\Delta w}{K_3} = \dfrac{10^3}{10^4} = 0.1$ volts

(c) Phase error $= \dfrac{0.1}{4 \times 0.25} = 0.1$ radians $= 5.7°$

(b) Output 2 $= 4 \cos (10^6 t + 10^3 t + 5.7°)$

Problem 2

(b) The modulation is at 1000RPS and the peak phase deviation is 0.5 rad.

The response curve for $\dfrac{w}{w_n} = 1$ (our case) shows an output phase 3dB higher than the input phase and a phase shift of -45°.

Otherwise the output should follow the input.

Result:

Output 2 $= 4 \cos [\ 10^6 t + 30° + 0.5 \sqrt{2} \sin (1000t - 45°)]$

SOLUTIONS (lin. anal. -- cont'd)

(a) Output 1 is the input to the V C O.

$$\frac{1}{K_3} \frac{d\phi_r}{dt} = 10^{-4} (0.5) \sqrt{2} \; 10^3 \cos (1000t - 45°)$$

(c) $\phi_e(t) = \phi_i(t) - \phi_r(t)$

$= 0.5 \sin 1000t - 0.5 \sqrt{2} \sin (1000t - 45°)$

3. Input to equiv. model:

PSD of noise $= \frac{2\eta}{A^2} = \frac{2 \times 10^6}{4} = 0.5 \times 10^{-6}$ W/Hz

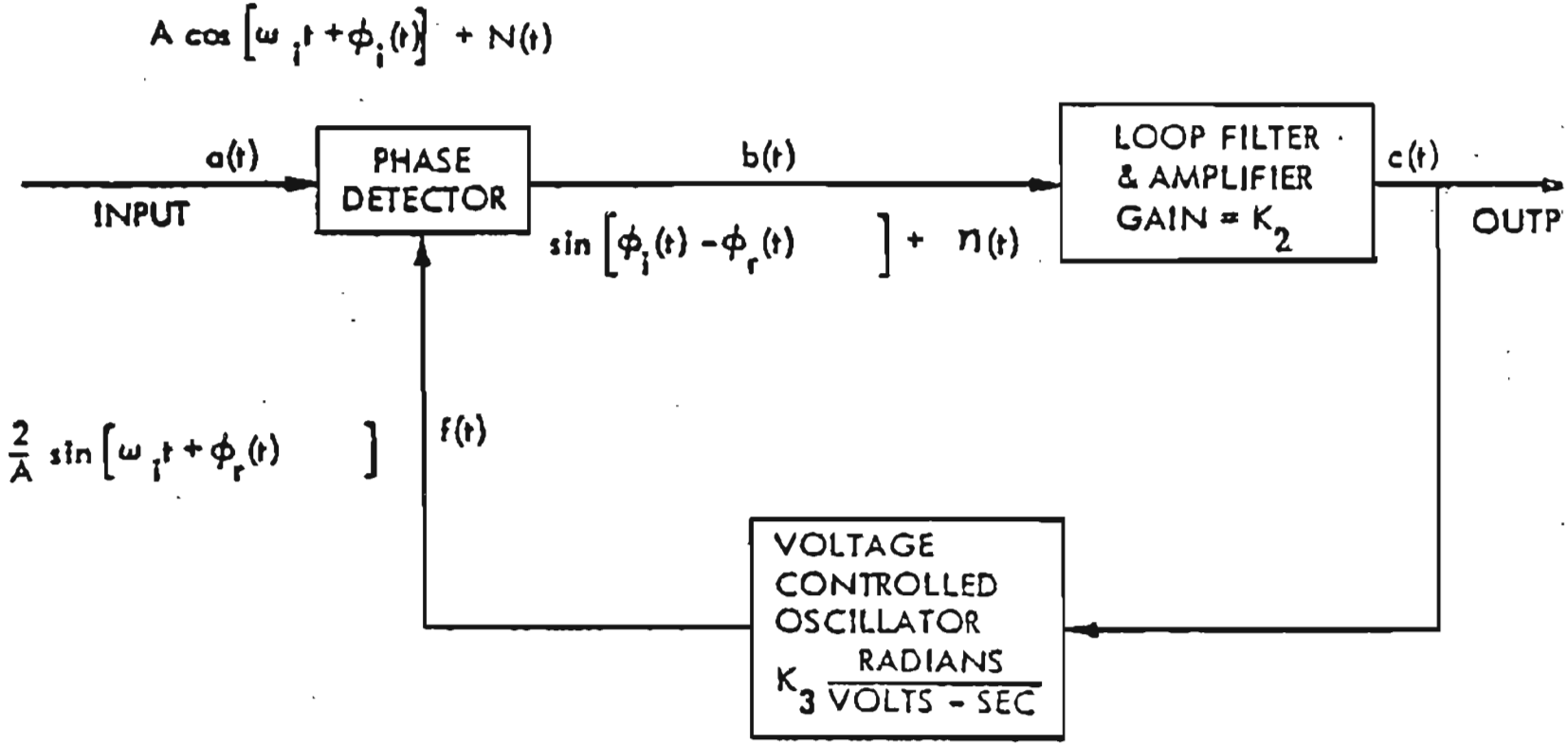
$$B_n \text{ (see Table)} = \frac{K_b \left(\frac{K_b}{a} + a\right)}{4a \left(\frac{K_b}{a} + b\right)}$$

In our case $K_b = a^2$ and $\frac{K}{a} >> 1$ $\therefore B_n \approx \frac{a}{2}$ Hz $= 500.$ Hz

Result:

$$\overline{\phi^2} = 0.5 \times 10\text{-}6 \times 500 = 0.25 \times 10^{-3} \text{ rad}^2$$

NONLINEAR ANALYSIS



Basic Phase-Lock Loop in Synchronized Mode

INHERENT NONLINEARITY:

phase detector

a) NONLINEAR

b) MULTIVALUED

c) $\overset{+}{-}$ SLOPE

NONLINEARITY OF OTHER BLOCKS CAN BE REMOVED VIA $

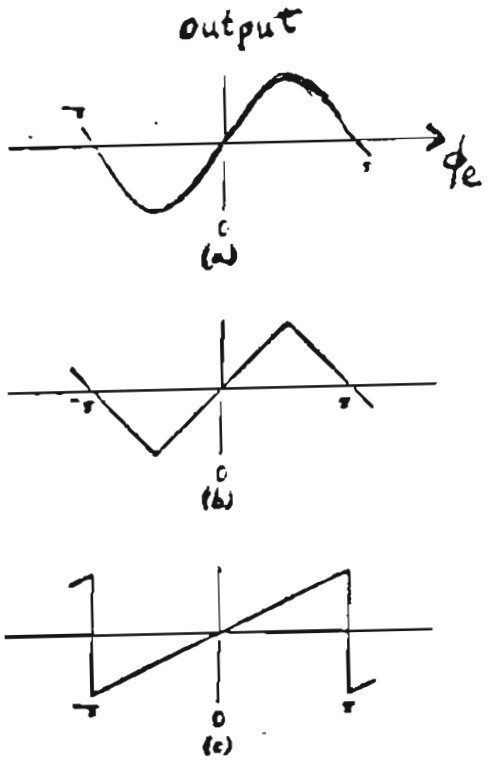


FIGURE 3 Phase-detector charecteristics

(a)Sinusoidal (b)Triangular (c)Sawtooth

METHODS FOR NONLINEAR ANALYSIS:

1. PHASE PLANE TRAJECTORIES

2. FOKKER-PLANCK TECHNIQUES
   (Random Walk)

3. CYCLE SLIPPING RATE

4. APPROXIMATIONS

5. ESTIMATED NONLINEAR PERFORMANCE FROM LINEAR ANALYSIS

PHASE PLANE METHOD:

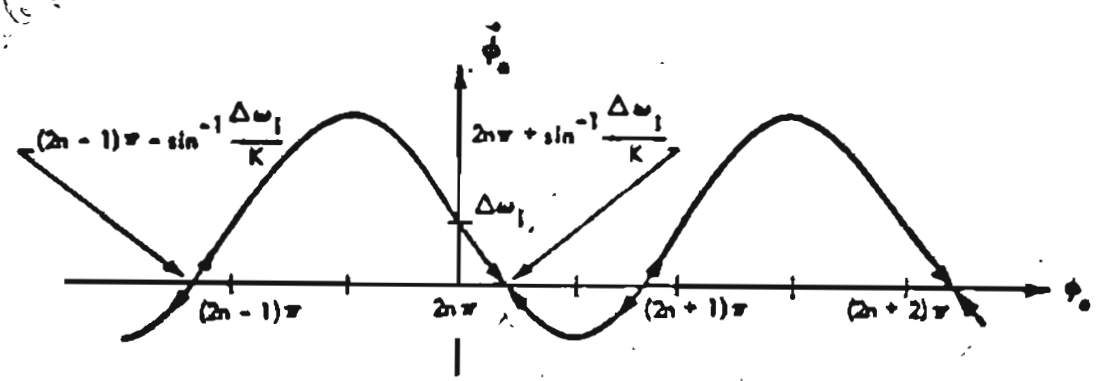
PLOT OF $\dot{\phi}_e$ vs ϕ_e

NOW ASSUME SINUSOIDAL PHASE DET. CHARACTERISTIC

FIRST-ORDER LOOP:

$$\dot{\phi}_e(t) = -K\sin\phi_e(t) + \Delta w_i$$

$$(\Delta w_i = w_i - w_{\text{free-running vco}})$$



PHASE PLANE TRAJECTORY NEED: Δw_i, K

NOTE: PATH OF TRANSIENT

ϕ_e (∞)

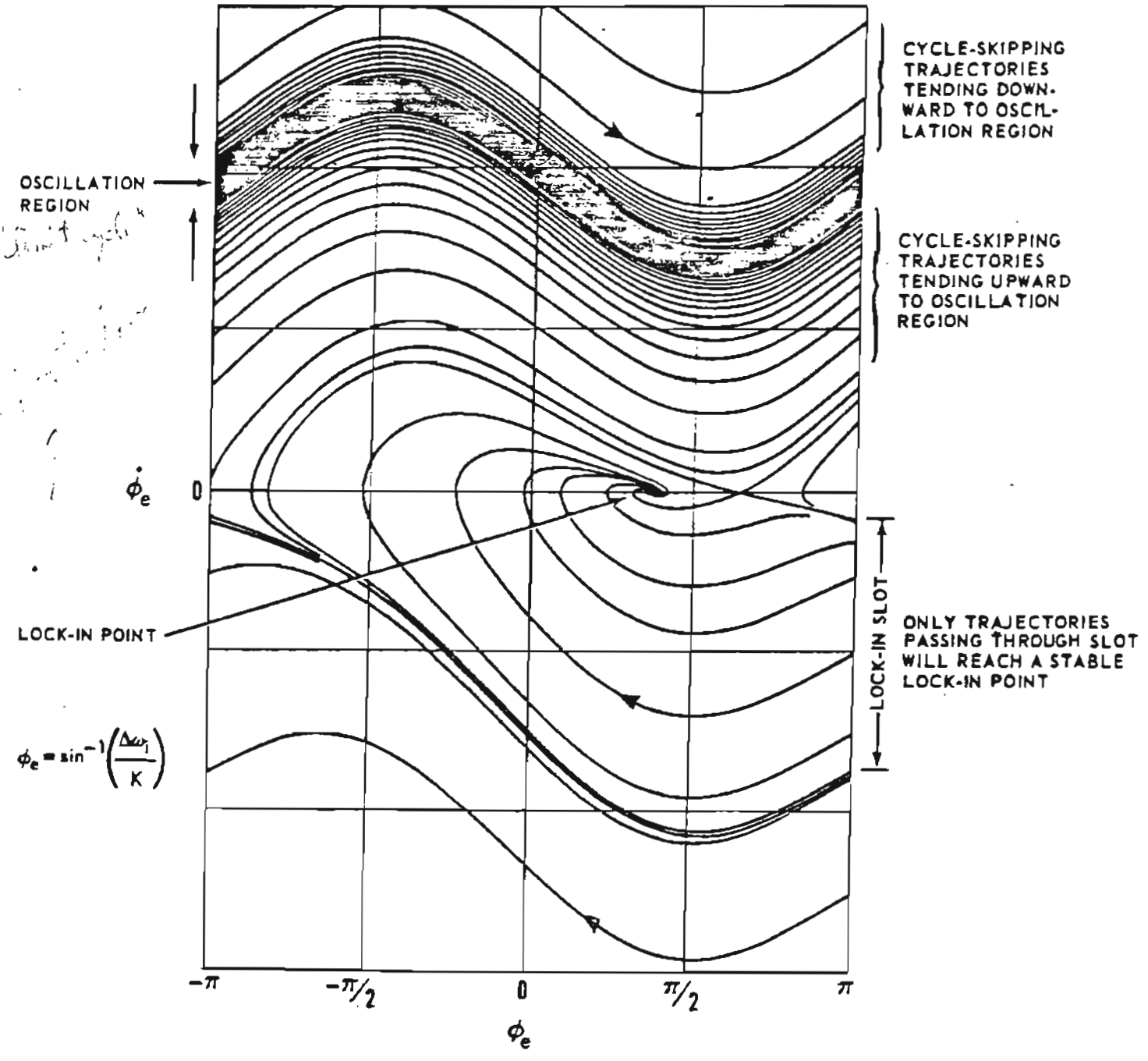
STABLE AND UNSTABLE POINTS

WILL IT LOCK?

SECOND-ORDER PLL:

$$\ddot{\phi}_e + \dot{\phi}_e\left[\flat + \frac{K\flat}{2}\cos\phi_e\right] + \flat K \sin\phi_e = \flat\,\Delta\omega_i$$

Note: Large $\frac{\Delta\omega_i}{K}$



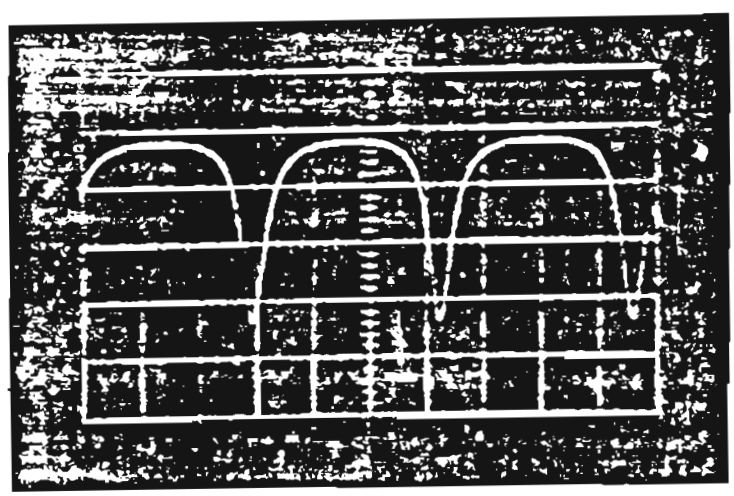
WHAT DOES PHASE PLANE TELL?

A. GIVEN INITIAL CONDITIONS AND $\Delta\omega$;
WILL LOOP ACHIEVE SYNCHRONISM?

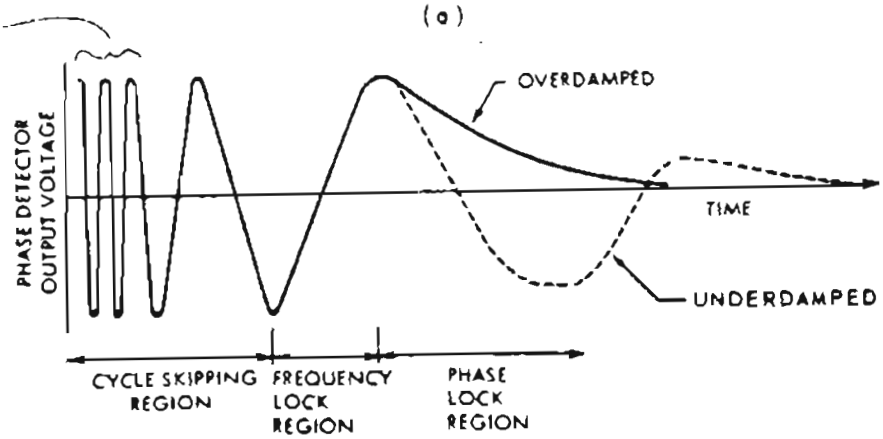
B. HOW LONG WILL IT TAKE TO SYNCHRONIZE?

C. HOW MANY CYCLES WILL BE SKIPPED BEFORE SYNCHRONISM?

D. WHAT IS THE PHASE ERROR AT SYNCHRONISM?



(a)



(b)

Phase detector outputs in nonsynchronous mode. (a) First-order PLL outside pull-in range. $\Delta\omega_i/A = 1.1$. (b) Second-order type-two PLL during pull-in.

FOKKER-PLANCK:

EXACT ANALYSIS FOR VARIANCE OF PHASE ERROR,

LOSS OF LOCK RATE, WITH AWGN (ADDITIVE WHITE GAUSSIAN NOISE)

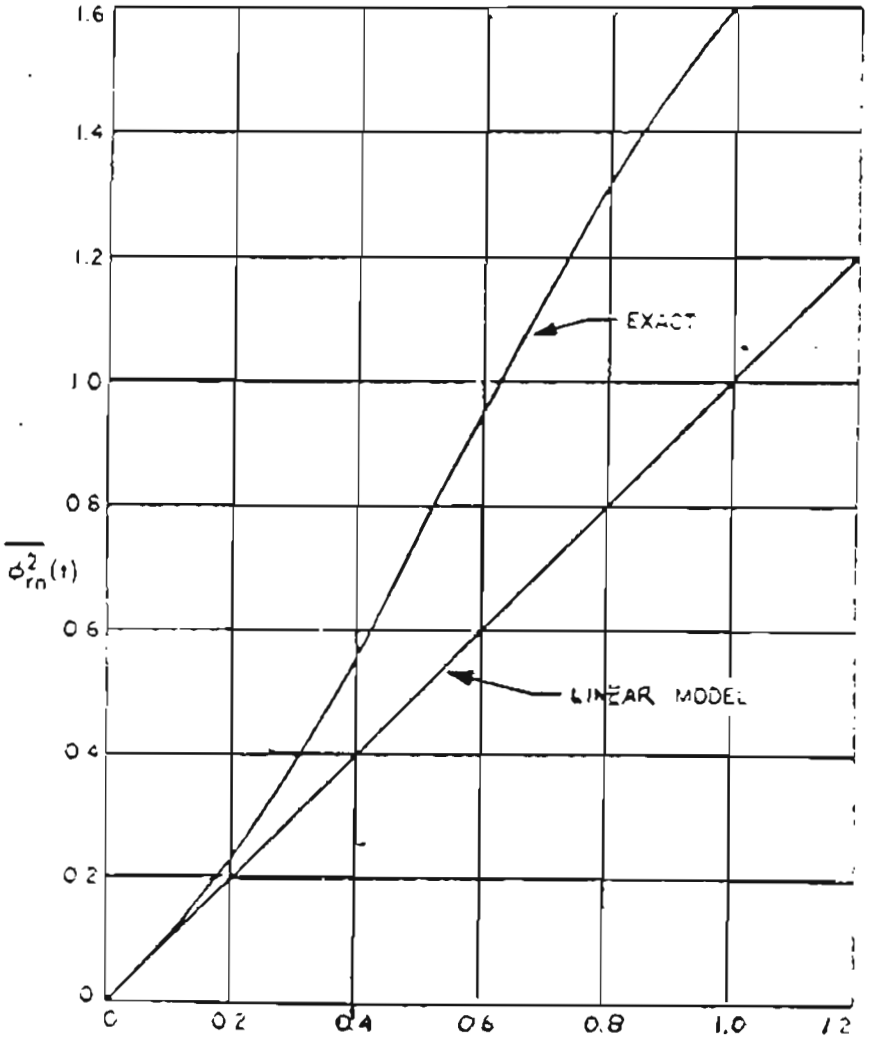
EXISTS FOR

FIRST ORDER PLL

NO FREQUENCY OFFSET

NO MODULATION

(USING FOKKER-PLANCK TECHNIQUES)



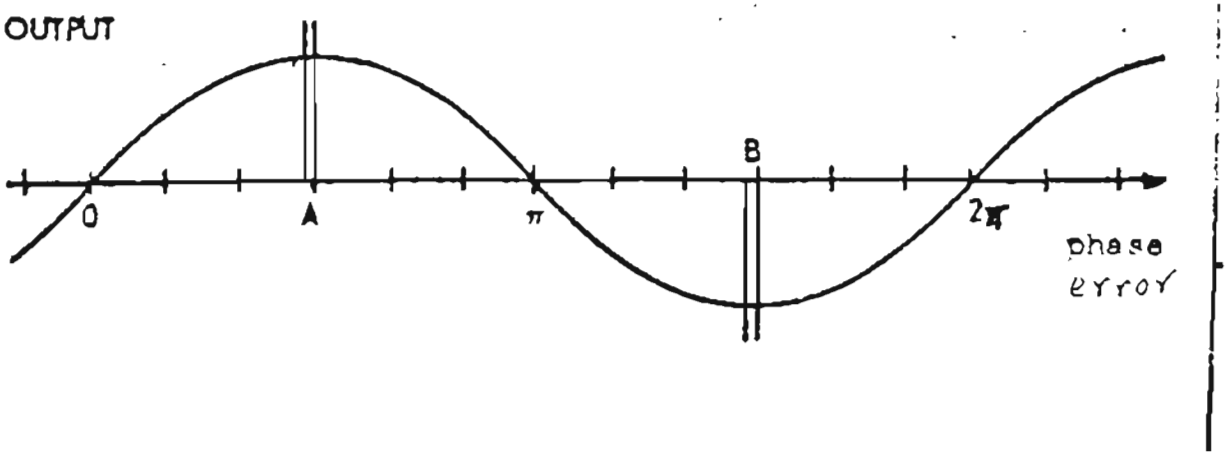
CYCLE SLIPPINGS:

BRIEF LOSS OF SYNCHRONISM

WHEN PHASE ERROR CAUSES PHASE DETECTOR OUTPUT TO GO OVER THE PEAK

REGENERATIVE ACTION BRINGS LOOP TO NEXT STABLE OPERATING POINT

PHASE DETECTOR CHARACT. (Multiplier type)



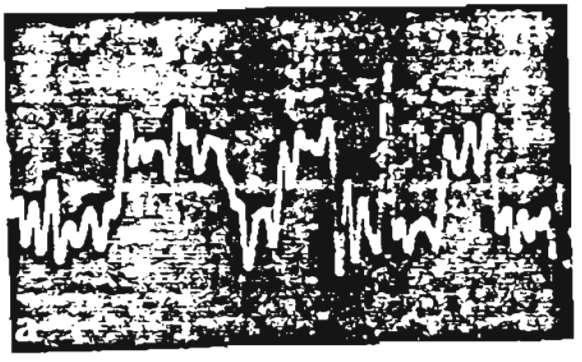
The following are equivalent:

CYCLE SKIPPED OR SLIPPED

PHASE STEP OF 2π ADDED TO VCO OUTPUT

SPIKE OF AREA 2π APPEARS AT INPUT TO VCO

We call these Loss of Lock Impulses or LLI



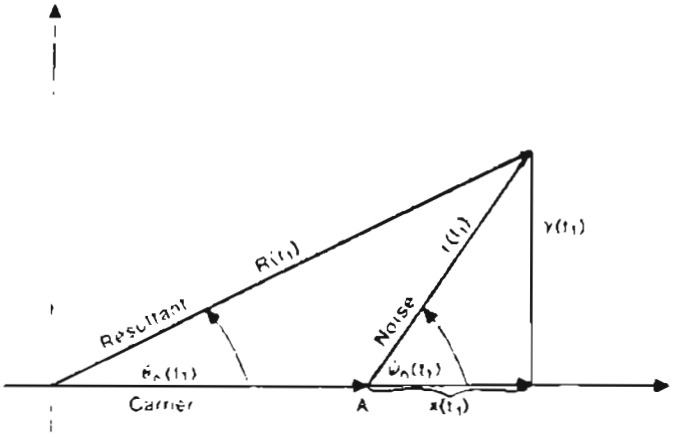
↑
LLI

Consider, in general, a sinewave carrier plus noise:

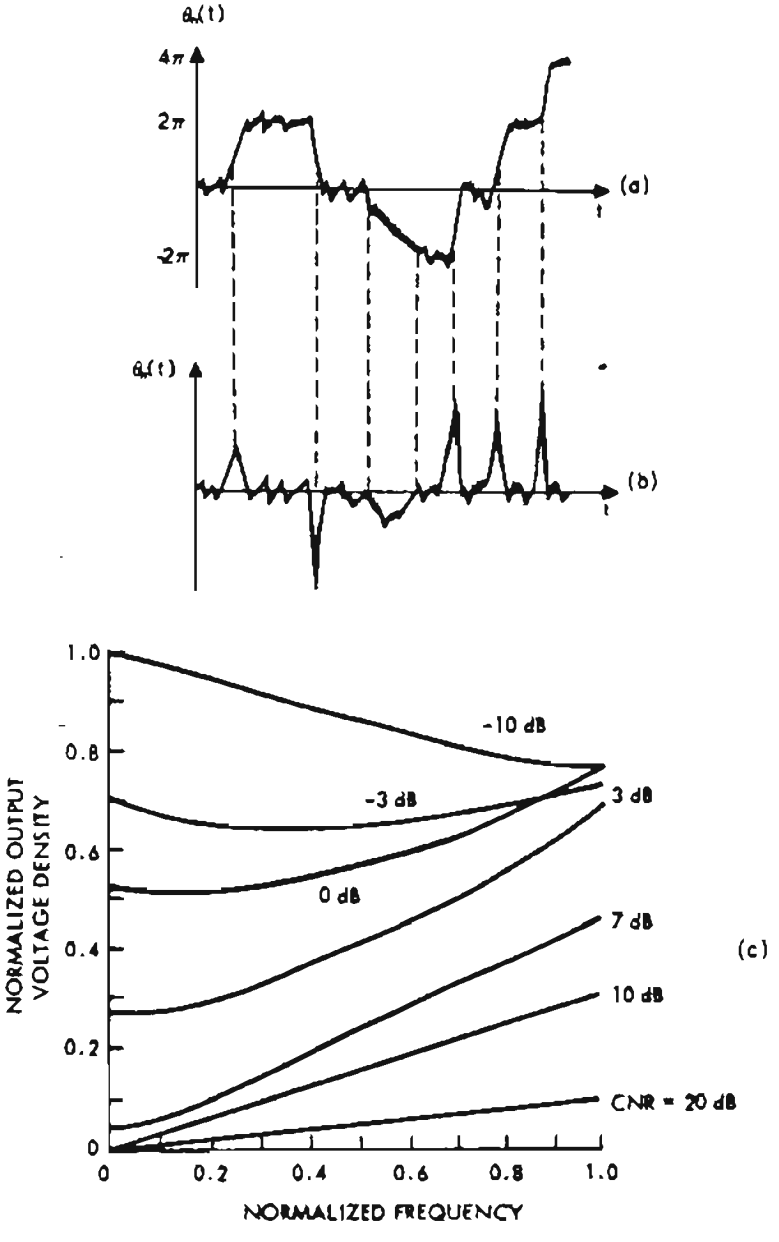
Noise causes cycle slippings in carrier when resultant encircles the origin.

First, let the carrier be unmodulated and be considered the reference in phase. The phasor addition of carrier and noise produces a resultant having a time-varying amplitude $R(t)$ and angle $\theta_n(t)$, per Eq. (3-5). It is assumed that the limiter removes completely the AM from $R(t)$; therefore, only the angle $\theta_n(t)$ and its time derivative $\dot{\theta}_n(t)$ are of interest. It is observed from Fig. 3-3a that the angle $\theta_n(t)$ is given by

$$\theta_n(t) = \tan^{-1} \frac{y(t)}{[A + x(t)]} \qquad [\phi_i(t) = 0]$$



(a)



Threshold effects. (a) Phase steps. (b) Noise spikes. (c) Detected noise voltage spectra. (The rms voltage of the noise in a small band of B Hz is $(B/B_p)^{1/2}$ times the value given by the curve; from Stumpers.[8])

We call these Threshold Impulses or ThI.

By the mechanism of cycle slippings, the PLL does not transfer all of the ThI (that appear at its input) to its outputs.

The sharper phase steps don't make it.

The smaller the PLL bandwidth, the fewer ThI are transferred to the output.

This is desirable..

However, if there is a frequency deviation on the desired carrier then a smaller bandwidth will cause a larger phase error and thereby a larger rate of LLI.

There is an optimum bandwidth of the PLL which minimizes the sum of LLI and ThI, which we call the spike (or cycle slipping) rate N.

This is usually a desired design goal for a high noise environment.

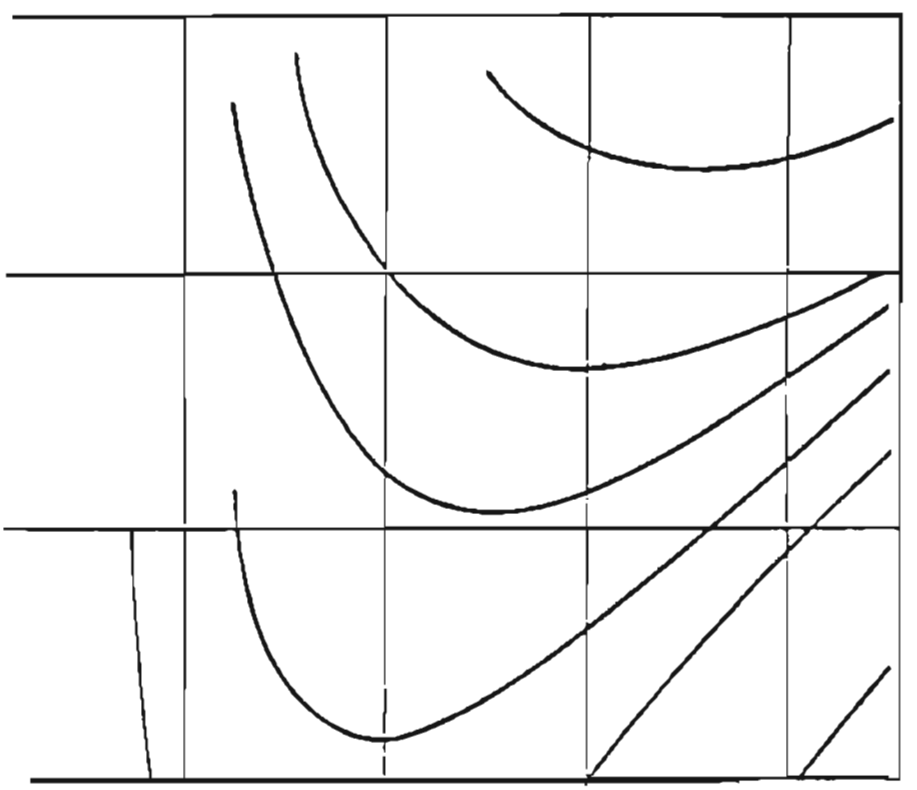


ILLUSTRATION: Δw_i is a parameter

THE SPIKE RATE IS TYPICALLY OF FORM

$$N = c\, w_n\, e^{-D\alpha}$$

c and D are constants

α = input carrier to noise ratio referred to the PLL noise bandwidth

For Example,

for a first-order PLL without deviation

$$N \approx \frac{K}{\pi} e^{-2\alpha}$$

NONLINEAR PERFORMANCE FROM LINEAR ANALYSIS:

Minimizing phase error in linear model also minimizes the phase error and LLI + ThI in actual nonlinear PLL.

In some cases there is a known relation between nonlinear and linear performance.

PROBLEMS (Nonlinear Analysis)

1. Draw a phase plane trajectory for a first-order PLL under the following conditions:

$\Delta\omega_i$ = 10,000 RPS K=20,000 RPS

A multiplier is used as a phase detector

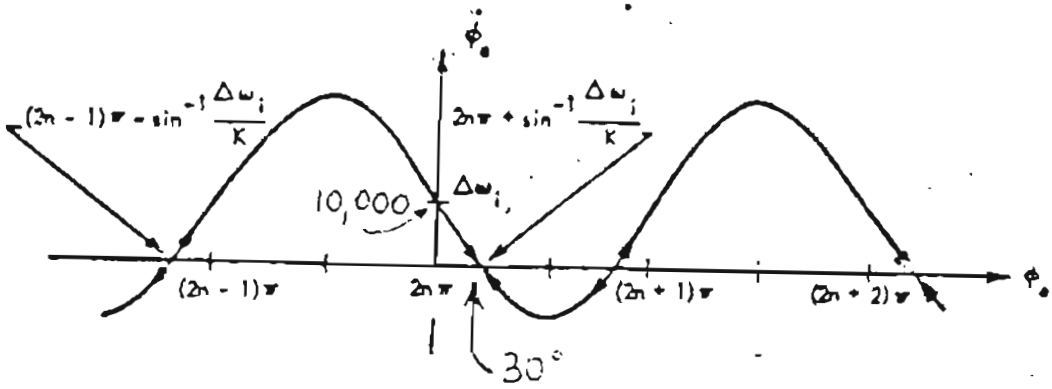
2. The carrier to noise ratio (CNR) at the input to a first-order PLL with the noise measured in the PLL bandwidth, is 10dB. Suppose now the CNR has increased by 3dB. How much has the cycle slipping rate decreased?

(Assume signal is unmodulated)

3. What is the mean square value of the phase error in the linear model when the actual noise (due to the nonlinearity of the sinusoidal phase detector) is 1dB higher?

SOLUTIONS (NONLINEAR ANALYSIS)

1.



Phase plane trajectory

2. $N_1 = \frac{K}{\Pi} e^{-2\alpha}$, $N_2 = \frac{K}{\Pi} e^{-4\alpha}$

$$\frac{N_2}{N_1} = e^{-2\alpha} = e^{-20} = 2 \times 10^{-9}$$

3. See Curve: $\frac{2\mathcal{Y}\, Bn}{A^2} \approx 0.25 \text{ rad}^2$

ACQUISITION

A. SYNCHRONIZATION PARAMETERS

DEFINITION: HIR

HOLD-IN RANGE (ALSO KNOWN AS "LOCK RANGE"):

CONSIDER A PLL SYNCHRONIZED WITH $w_i = w_{ro}$,

WHERE w_{ro} = FREE-RUNNING VCO FREQUENCY AND w_i IS THE INPUT FREQUENCY.

NOW SLOWLY VARY w_i AND w_r WILL FOLLOW.

HIR $\triangleq$ $| w_i - w_{ro} |$ FOR WHICH w_r JUST FAILS TO FOLLOW w_i, RESULTING IN LOSS OF SYNCHR.

HIR = (MAX Ø DET. OUTPUT) $(K_2 K_3)$

FOR A MULTIPLIER-TYPE Ø DET., HIR = K

WHERE K = OPEN LOOP DC GAIN; FOR ALL ORDERS OF THE PLL.

EXAMPLE:

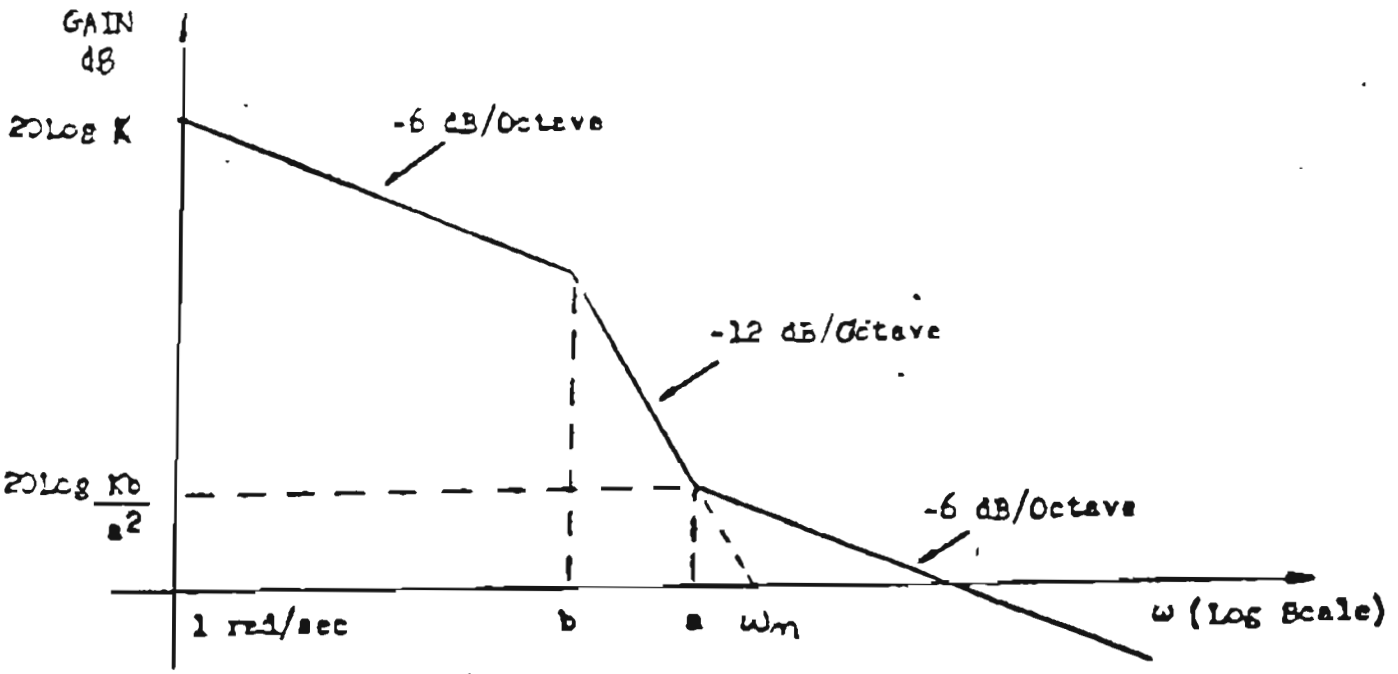
VCO SENS. = 100 MHz/V, Ø DET SENS = 0.1 V/RAD

BASEBAND GAIN = 78. (MULTIPLIER AS Ø DET.)

THEN HIR = 780.MHz.

USING A LEAD-LAG NETWORK THERE IS USUALLY NO PROBLEM IN GETTING A LARGE ENOUGH HIR.

OPEN-LOOP RESPONSE



GRAPHICAL DETERMINATION OF K and ω_n

This figure illustrates that in a second-order loop, Hold-in range and bandwidth can be independently specified.

This is not so in a first-order loop.

DEFINITIONS

PULL-IN RANGE (PIR): Max. initial $|w_i - w_{yo}|$ for which loop eventually locks into synchronism.

(also known as capture range)

LOCK-IN RANGE (LIR): Max. initial $|w_i - w_{yo}|$ for which loop locks into synch. without losing or adding a cycle.

$$\text{HIR} \geq \text{PIR} \geq \text{LIR}$$

FIRST-ORDER LOOP

$$\text{LIR} = \text{PIR} = \text{HIR} = K$$

$$\text{LOCK-IN TIME CONSTANT} \approx \frac{1}{K}$$

$$\text{s.s. } \phi_e \approx \frac{\Delta w_i}{K} \left(\text{ARCSIN} \quad \frac{\Delta w_i}{K} \right)$$

Offset.

SECOND-ORDER LOOP

LIR = 0-dB FREQ. of OPEN LOOP = $\frac{Kb}{a}$ RPS

PIR $\approx$ $2\left[(Kb)\left(1+\frac{K}{2a}\right)\right]^{\frac{1}{2}}$ RPS

PULL-IN TIME = $T_p \approx a\left(\frac{\Delta w_i}{Kb}\right)^2$ sec

s.s. $\phi_e \approx \frac{\Delta w_i}{K}$ RAD

EXAMPLE

$K = 6.6 \times 10^5$ RPS, $a = 35.4$ KRPS,

$b = 1880$ RPS, AND LET $\Delta w_i = 100$ KRPS

THEN LIR = 35,400 RPS (LIR = a in this design)

PIR $\approx$ 226 KRPS, $T_p \approx$ 0.23 msec

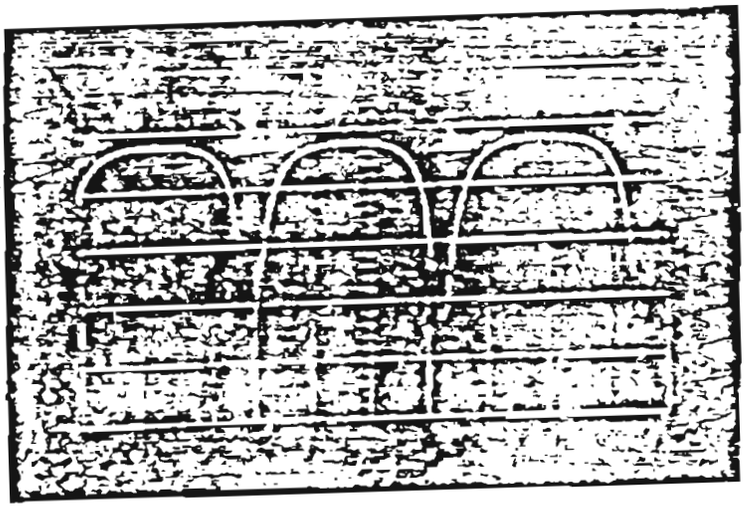
s.s. $\phi_e \approx$ 0.15 RAD = 8.7°

s.s. $\triangleq$ steady-state

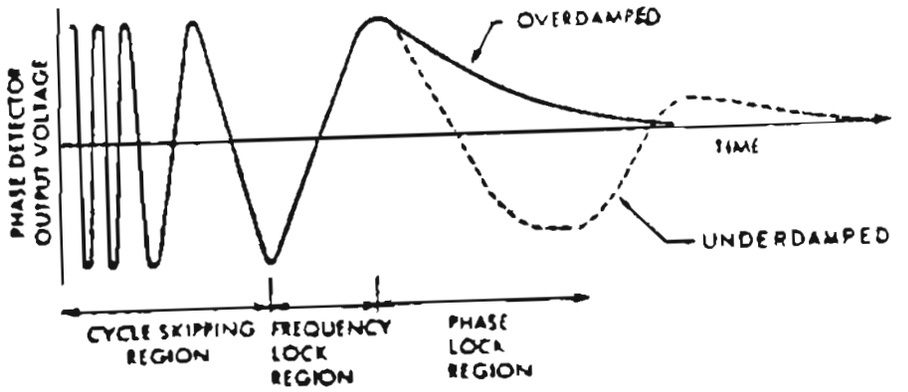
In the picture below:

The first-order loop does not have sufficient gain to pull in in spite of the DC in the output.

The second-order loop responds to a very small imbalance in the phase-detector output, building up the DC in the capacitor (interration).



(a)



(b)

Phase detector outputs in nonsynchronous mode (a) First-order PLL outside pull-in range, $\Delta\omega_i/K < 1.1$. (b) Second-order type-two PLL during pull-in

WHAT CAN GO WRONG?

1. "HANG UP". IF $\Delta w_i = 0$ BUT ORIGINAL ϕ_e IS 180°,

   IT MAY TAKE A LONG TIME TO GET THE PLL INTO SYNCHRONISM.

   REASON? THERE IS NO Ø DET OUTPUT!

2. EXTRANEOUS PHASE SHIFTS CAN CAUSE PUSH-OUTS OR EVEN

   FALSE LOCKS.

3. NOISE

4. DC OFFSETS

"Pull-in" is accomplished by small DC voltages produced during each cycle of phase detector output (in the closed loop) while attempting synchronization. These become extremely small and unreliable (because of extraneous DC offsets) far away from the lock-in range.

CONSIDER THE CASE WHERE THE Ø DET IS NOT OF THE MULTIPLIER TYPE.

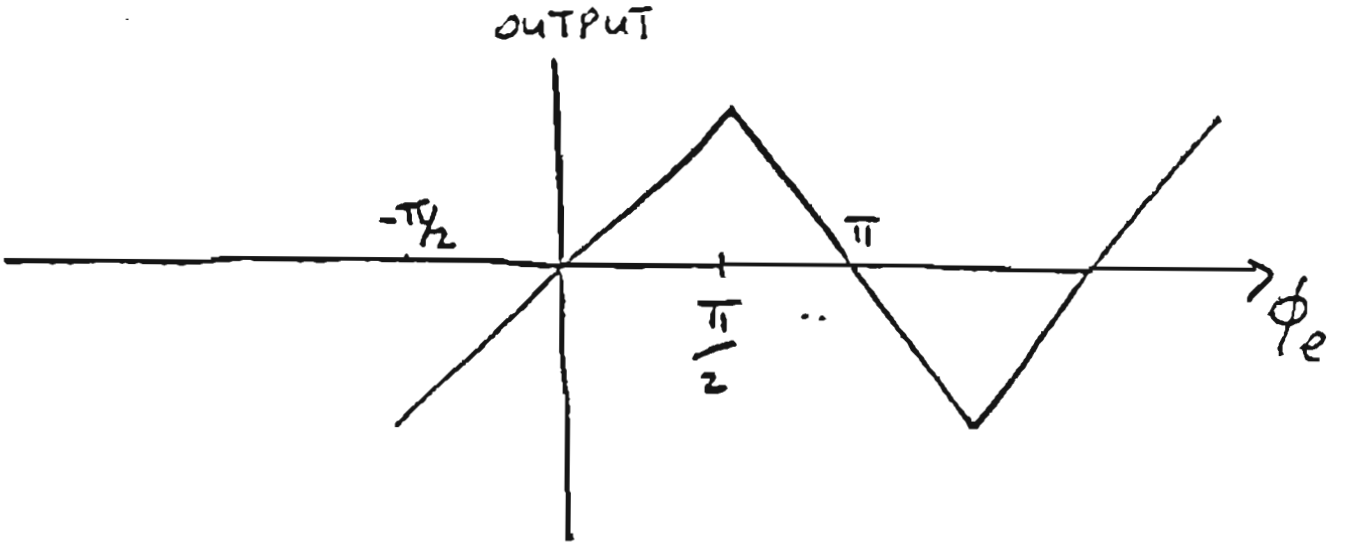
RECALL THAT THE Ø DET SLOPE (=SENSITIVITY) ENTERS AS A GAIN FACTOR IN THE LOOP, AND THEREFORE ALSO IN THE LOOP BANDWIDTH. WE NORMALLY OPERATE WITH SMALL $\emptyset_e$.

THEREFORE, THE SLOPE AT $\emptyset_e \approx 0$ DETERMINES THE LOOP BANDWIDTH. KEEPING THIS SLOPE CONSTANT, THE MAX. OUTPUT OF THE Ø DET DEPENDS ON THE SHAPE OF THE CHARACTERISTIC.

ASSUME A SLOPE OF 1 AT $\emptyset_e \approx 0$.

FOR A MULTIPLIER-TYPE Ø DET, THE MAX OUTPUT = 1.

FOR A TRIANGULAR ϕ DET CHAR,
THE MAX OUTPUT = $\frac{\pi}{2}$



THIS ϕ DET IS OBTAINED USING A MULTIPLIER BUT SQUARE WAVES INSTEAD OF SINE WAVES AS CARRIERS.

FOR A SAWTOOTH ϕ DET CHARACTERISTIC WITH MONOTONIC RANGE $\pm N\pi$, THE MAX OUTPUT IS $N\pi$.

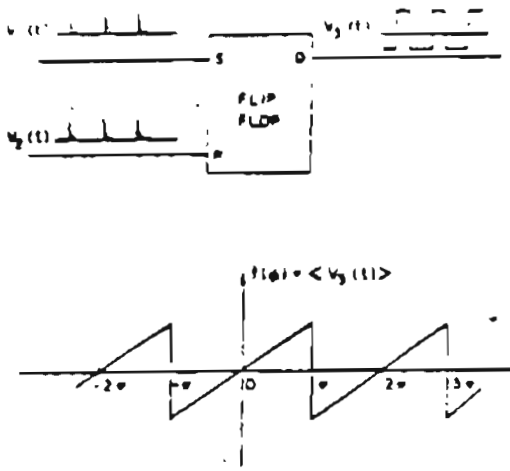
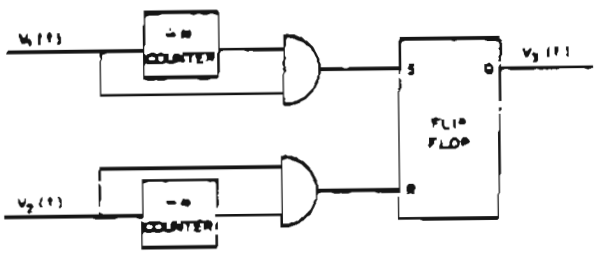


Fig. 2 Sawtooth phase comparator



Sawtooth PC with counters

THE HOLD-IN, LOCK-IN, AND PULL-IN RANGES ARE ESSENTIALLY INCREASED PROPORTIONATELY TO THE MAX Ø DET OUTPUT.

REFERENCES

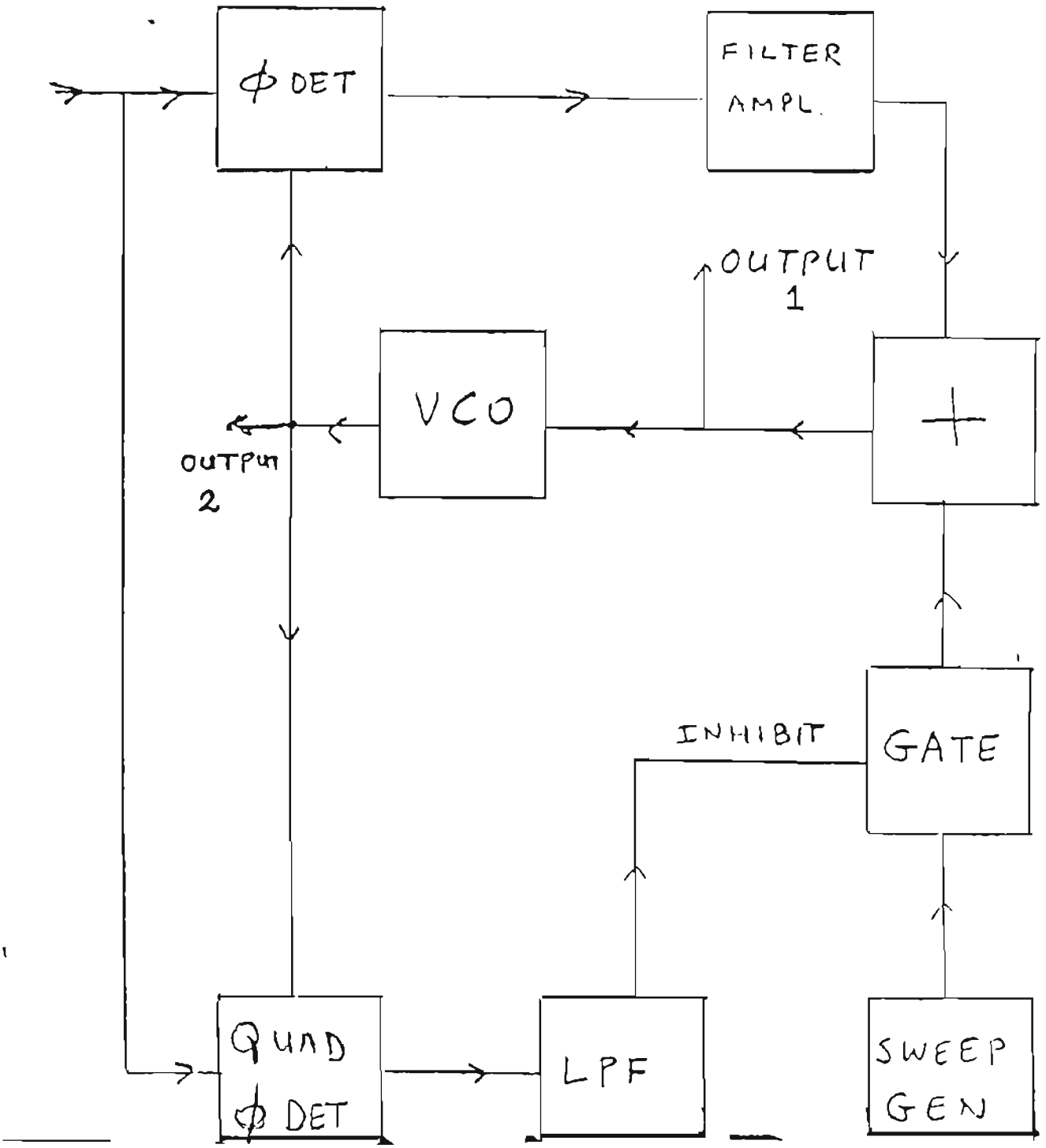
1. KLAPPER & FRANKLE

2. F. GARDNER, "RAPID SYNCHRONIZATION", MICROWAVE SYSTEMS NEWS, FEB/MARCH 1976, pp. 57-64.

3. J. OBERST, "GENERALIZED PHASE COMPARATORS FOR IMPROVED PHASE-LOCKED LOOP ACQUISITION", IEEE TRANS. ON COM. TECH., DEC, 1971, pp. 1142-1148.

B. ACQUISITION AIDS

AUXILIARY SWEEP



AUXILIARY SWEEP

1. MOST POPULAR ACQUISITION AID

2. QUADR: Ø DET. IS USUALLY ON THE SAME CHIP

3. SWEEP RATE $\frac{dw}{dt} \leq w_n^2 = Kb$, THEORETICAL IN SECOND-ORDER LOOP.

   TO INCLUDE ALL POSSIBLE INITIAL CONDITIONS, LIMIT IS

   $$\frac{dw}{dt} < \frac{1}{2} w_n^2$$

4. IN THE PRESENCE OF NOISE, USE

   $$\frac{dw}{dt} < \left(1-\frac{1}{G^2}\right) \frac{Kb}{2}$$

   WHERE G = CNR IN LOOP BANDWIDTH.

THIS HAS EXPERIMENTALLY GIVEN A 90% PROBABILITY OF ACQUISITION

5. NEEDS $G > 6dB$

EXAMPLE

VCO SENSITIVITY = $2\pi \times 25{,}000$ RPS/V

$K = 6.6 \times 10^5$ RPS, $\quad b = 1880$ RPS

LET $G = 9$dB and $\Delta w_i = \pm 5 \times 10^5$ RPS

THEN $\frac{dw}{dt} < (1 - \frac{1}{\sqrt{8}}) \frac{6.6 \times 10^5 \times 1880}{2} = 4 \times 10^8$ RPS/SEC

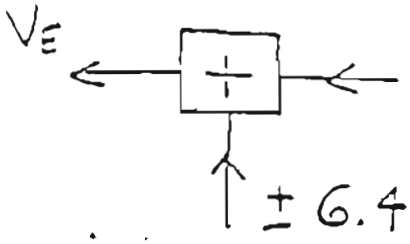
LET US SWEEP OVER TWICE THE UNCERTAINTY

P - P VOLT. SWING = $\frac{2 \times 10^6}{2\pi \times 25{,}000} = 12.8$ VOLTS

MAX. VOLT. SLOPE = $\frac{4 \times 10^8}{2\pi \times 25{,}000} = 2.5 \times 10^3$ VOLT/SEC

REPETITION RATE OF SWEEP $\leq 100 H_z$

WHAT IF THE SWEEP IS LEFT ON AFTER LOCK?



$\sim$ = TRIANG. WAVE

$$V_E = \frac{\sim}{1 + \frac{K H_2(S)}{S}} \approx \frac{\sim}{1 + \frac{K}{S}} \approx \frac{\sim}{K/S}$$

$$= \frac{S \sim}{K} = \frac{\pm 2.5 \times 10^{3} \text{ SQUARE WAVE}}{6.6 \times 10^{5}} = \pm 3.8 \times 10^{-3} \text{ V}$$

THIS RESULTS IN A SQ. WAVE FM

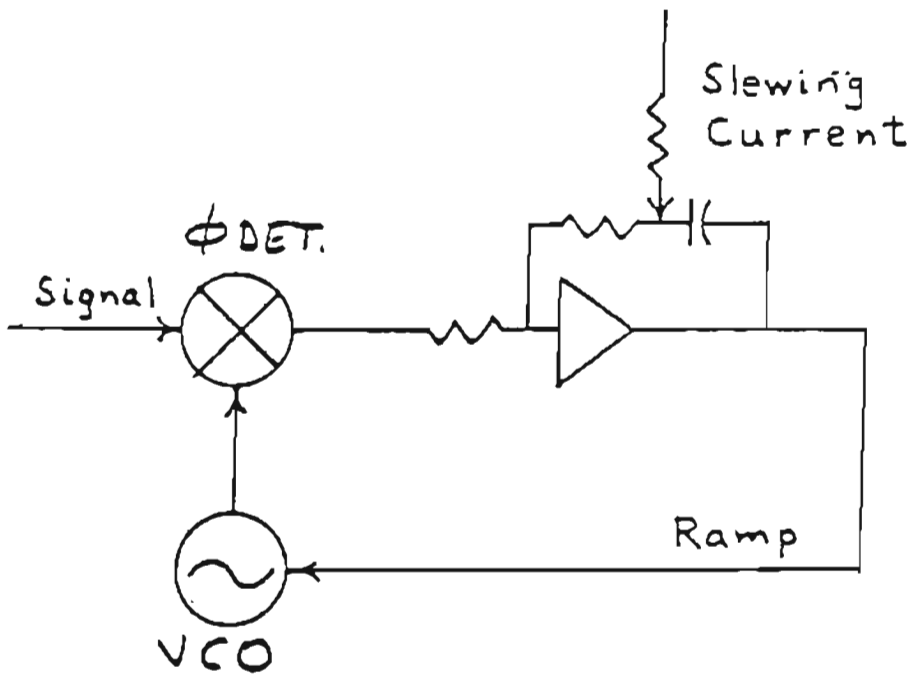
OF FREQ. DEV. $\pm$ 3.8 x 10^{-3} x 25,000 = $\pm$ 95 H_z

AT THE RATE OF $\sim$ 100H_z.

COMPARE THIS AGAINST FREQ. DEV. DUE TO SIGNAL AND THE SIGNAL FREQ. BAND TO SEE IF IT CAN BE LEFT ON WITHOUT DISTURBING THE OUTPUT.

Sweep Implementation

(Second-order PLL)

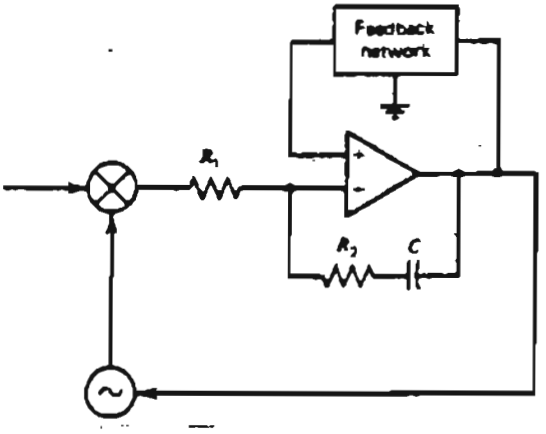


A fixed current injected into the integrator of a 2nd-order PLL causes a voltage ramp to appear at the integrator output.

Ramp causes the VCO to sweep, thereby searching for signal.

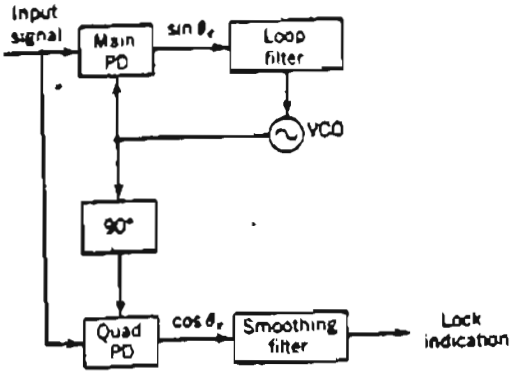
SIMPLIFIED SWEEP CIRCUIT:

LOOP FILTER IS PART OF LOW-FREQ. OSC..
WHEN LOOP LOCKS, NEG. FEEDBACK
AROUND LOOP EXTINGUISHES THE OSC..



Positive-feedback sweep.

LOCK INDICATOR:



QUAD. PHASE DET. IS USUALLY ON SAME CHIP.

Discriminator-Aided Frequency Acquisition

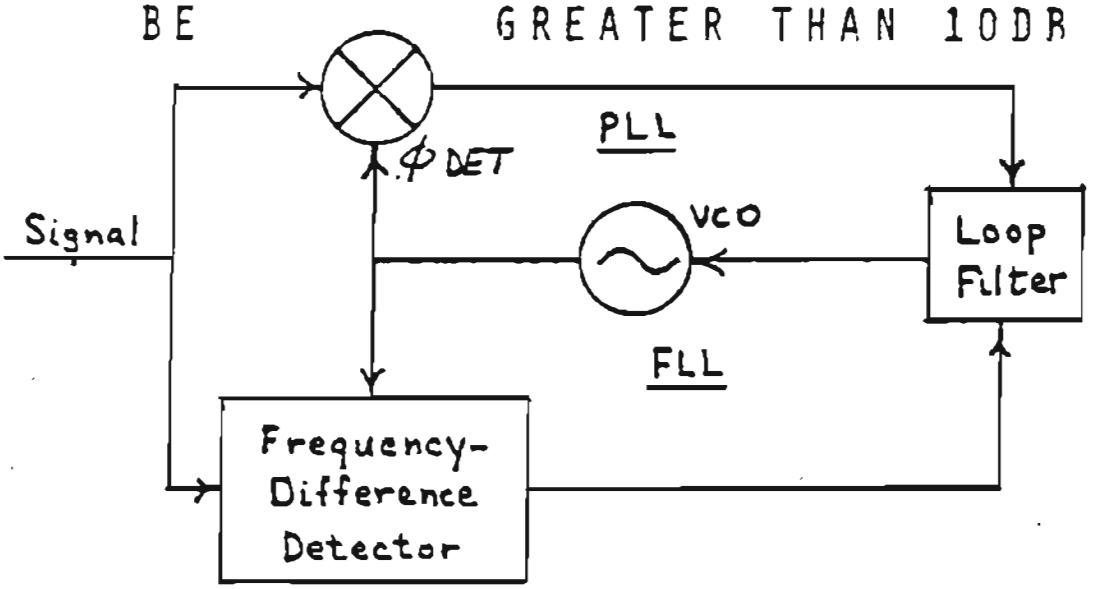
If input SNR is large enough to permit use of a frequency discriminator, then frequency acquisition can be performed by the discriminator.

Prior to lock, phase loop is inoperative and discriminator forms conventional AFC loop.

When frequency error is reduced within lock-in range, the phase loop takes over and goes into phase lock; the frequency can either be disabled or can be permitted to furnish the loop damping.

Very fast frequency acquisition is possible.

CNR IN DISCRIMINATOR BANDWIDTH MUST BE GREATER THAN 10DB (TO BE

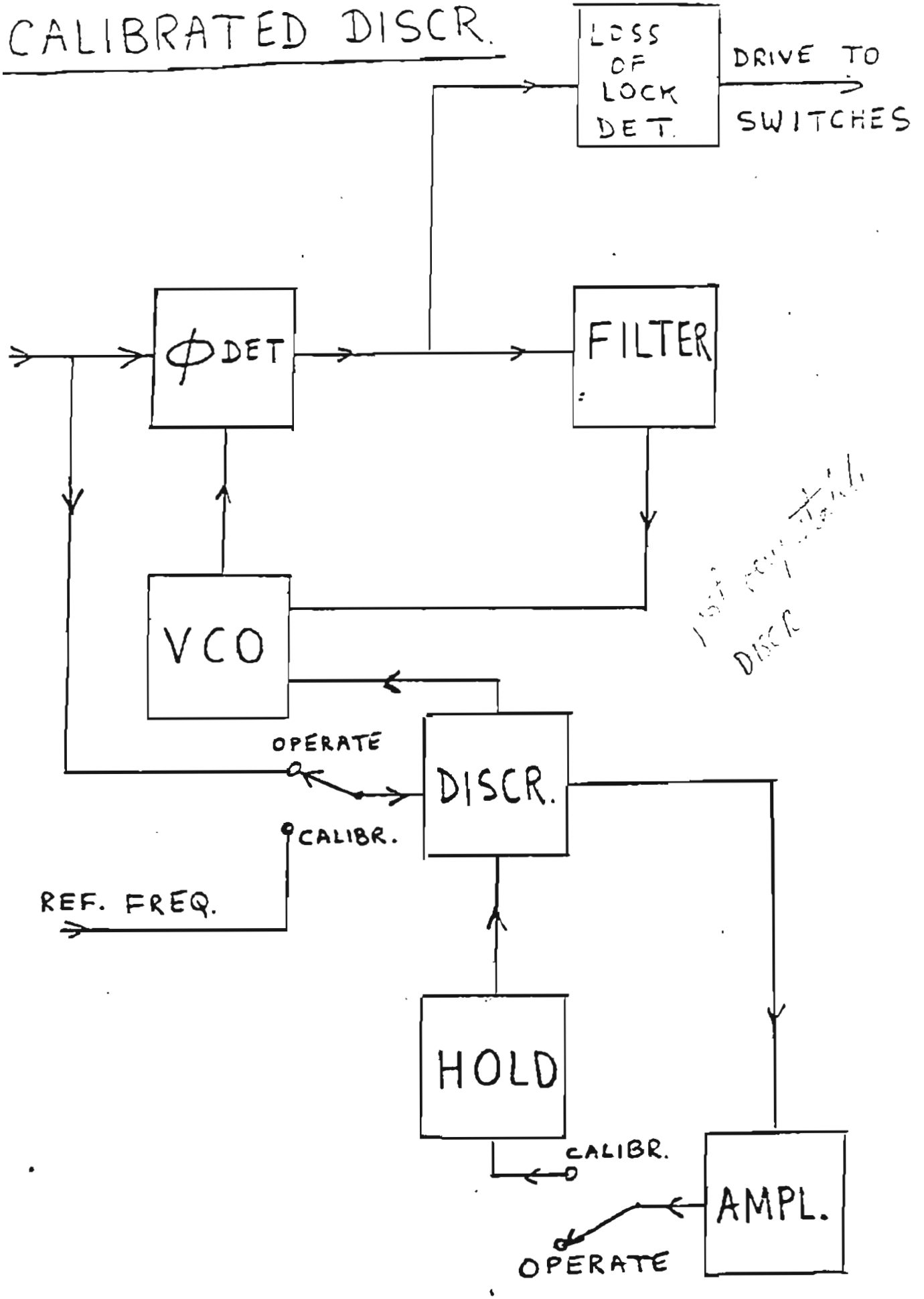


ABOVE THRESHOLD).

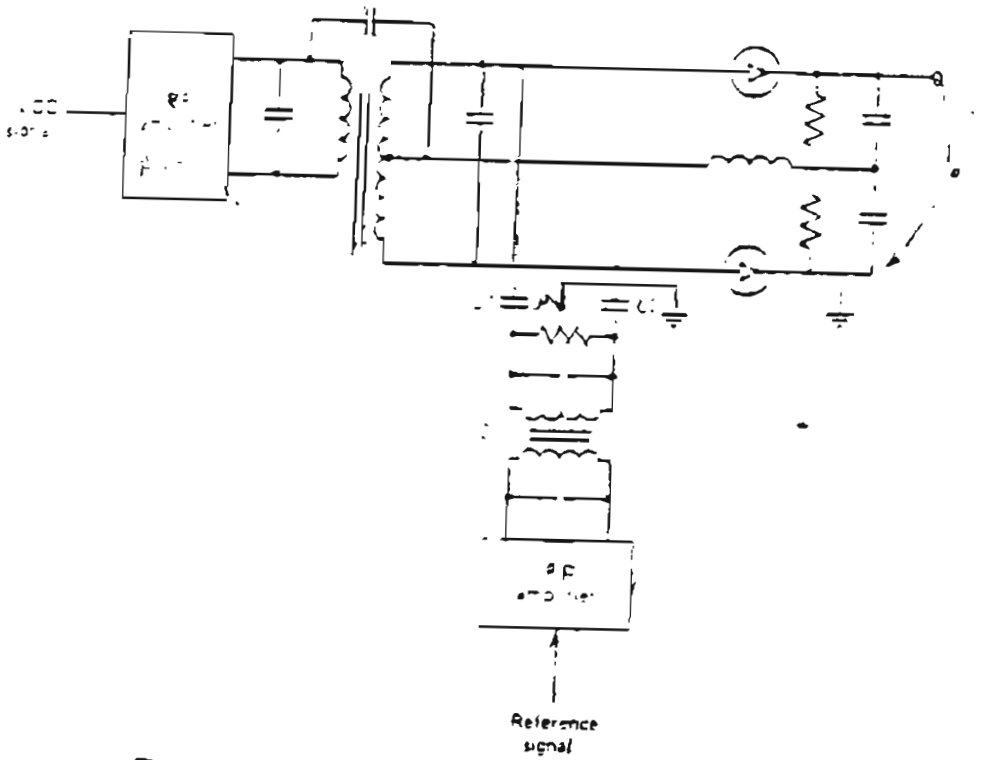
LIMITED BY DISCR. CENTER FREQ. STABILITY WHICH MAY BE GREATER THAN PLL PIR.

Reference: D. Richman, "Color-Carrier Reference Phase Synchronization Accuracy in NTSC Color Television", Proc. IRE, 42, pp. 106-133, Jan. 1954

CALIBRATED DISCR.



Reference: J. Harp, " Have Phase-Lock Accuracy and Top Lock-Up Time, Too", Microwaves, December, 1972, pp. 48-53.



The balanced discriminator

ACTS AS FREQ. DET. WHEN OUT OF LOCK AND THEN AS PHASE DETECTOR.

Sequential Phase Detectors

Operate on transition edges of rectangular waveforms (or pulses).

Contain memory of past sequences.

Can be constructed from "digital" IC's.

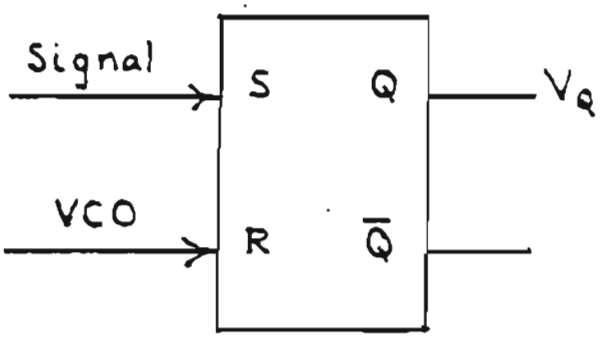
Outputs are rectangular, two-level waveforms.

But useful output is DC average of output pulses: an analog quantity.

A PLL with a sequential PD is an analog loop, even though the PD circuit may be constructed with digital components.

Flip-Flop Phase Detectors

The simplest sequential PD is an RS Flip Flop.



Typical operation:

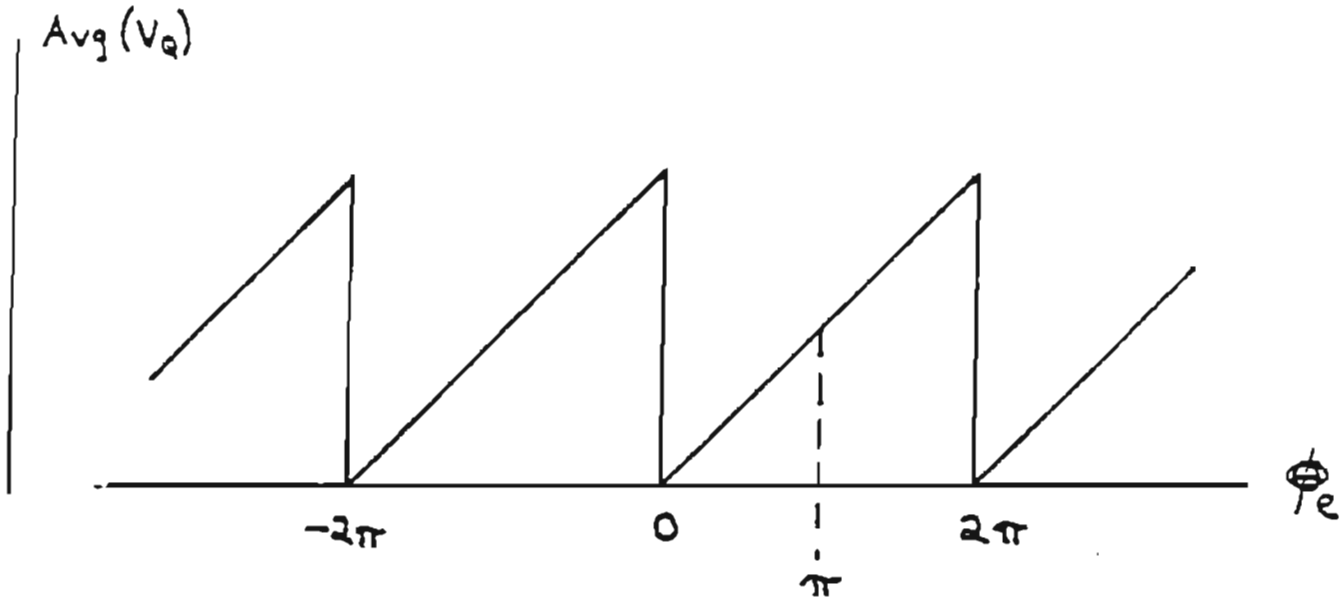
Q is set true by negative edges of signal.

Q is reset by negative edges of VCO.

Widely used in laboratory phase meters.

DC Output of FF PD

Average DC output of Q terminal is linear function of phase difference ϕ_e between signal and VCO.



Phase detector has sawtooth characteristic repeating every 360^0.

Linear over full 360^0. (Compare to sinusoidal PD.)

Normal tracking would be in center of linear region at $\phi_e = 180^0$.

Modified FF PD

Problem: If any signal transitions are missing, VCO resets RS FF, which then remains reset, indicating 180^{0} phase error from normal. Loop tries to compensate apparent error by slewing away from correct tracking phase towards an extreme.

Conclusion: RS FF is suitable only if all transitions are certain to exist.

Modification: Let VCO toggle FF rather than reset it.

Tracking operation is identical to RS FF.

Loss of signal causes FF to toggle on each VCO transition, giving 50% duty cycle on Q (equivalent to zero-error analog output).

References:

C.J. Byrne, "Properties and Design of the Phase-Controlled Oscillator with a Sawtooth Comparator", BSTJ, 41, pp. 559-602, March 1962.

A.J. Goldstein, "Analysis of the Phase-Controlled Loop with a Sawtooth Comparator", BSTJ, 41, pp. 603-633, March 1962.

Sequential PD Response to Noise

Additive noise causes excess transitions on signal input.

Sequential PD responds to first "signal" transition following a VCO transition, irrespective of whether transition is real signal or caused by noise.

Noise crossings will bias the DC output of the sequential PD, as well as cause jitter,because the PD ignores the true signal crossing if a noise crossing occurs first.

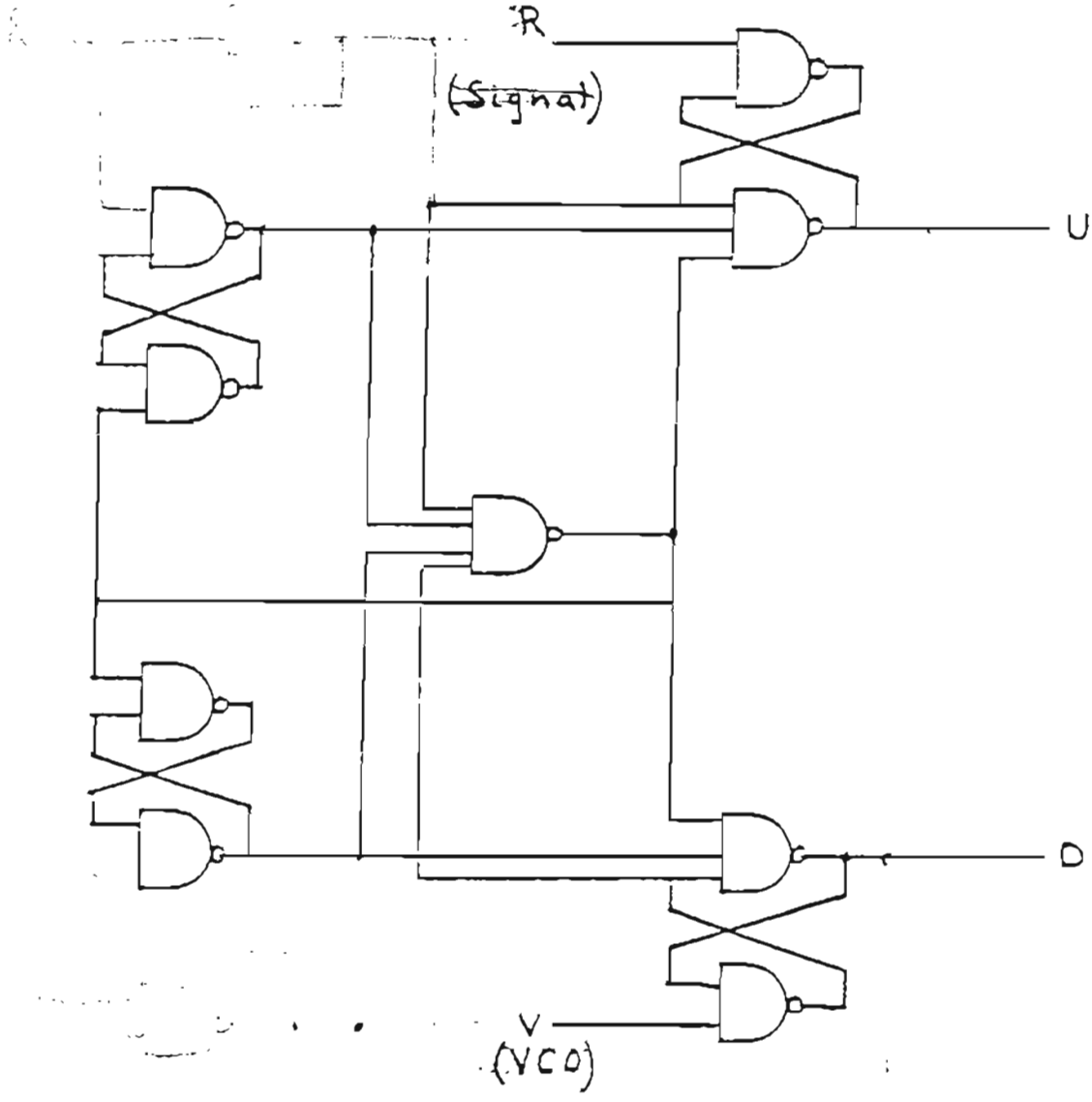
Consequences: A sequential PD breaks up when subjected to significant noise; its threshold is much higher than that of a multiplier PD. A sequential PD is usable only if signal exceeds noise by a substantial margin.

Noise intolerance is inherent to all sequential PD's and not just FF's.

Phase-Frequency (P-F) Detector

A popular sequential PD available as an inexpensive integrated circuit.

Consists of 4 interconnected flip flops.



Reference: Phase-Locked Loop Data Book, 2nd ed., Motorola, Inc.; August 1973.

J. F. Oberst, "Generalized Phase Comparators for Improved Phase-Locked Acquisition," IEEE Trans., Com. Tech., Dec. 1971, PP. 1142-1148.

M. A. Rich, "Designing Phase-locked Oscillators for Synchronization," IEEE Trans., Communications, July 1974, pp. 890-896.

Features of P-F Detector

1. Active phase range is $\pm 360^{\circ}$: double that of other PD's. Linear over entire active range.

2. Output characteristic is aperiodic, in distinction to all other PD's discussed. If PLL is unlocked, the P-F detector provides a steady Low condition on U or D, as appropriate, to indicate direction of frequency error. This slews VCO towards correct frequency for lock. Action is faster, more powerful and more reliable than pull-in. Phase-frequency detector provides aided frequency acquisition at no extra cost.

3. Both outputs quiescent at $\theta = 0$. Small θ causes short pulses at U or D. Much easier to filter than 50% duty-cycle pulses of FF or Exclusive-OR phase detectors. (Less trouble with ripple.)

4. Severely disrupted by missing transitions. Has same noise intolerance as all sequential PD's.

5. PULL-IN RANGE = HOLD-IN RANGE = $2\pi K$.

6. PULL-IN TIME, Tp,

$$Tp \approx \frac{1}{b} \ln \left[1 - \frac{\dot{\phi}_e (0)}{\Delta w - K \operatorname{sgn} \dot{\phi}_e (0)} \right]$$

WHERE sgn = "THE SIGN OF". PULL-IN IS RAPID

Operation of Ø-F Detector

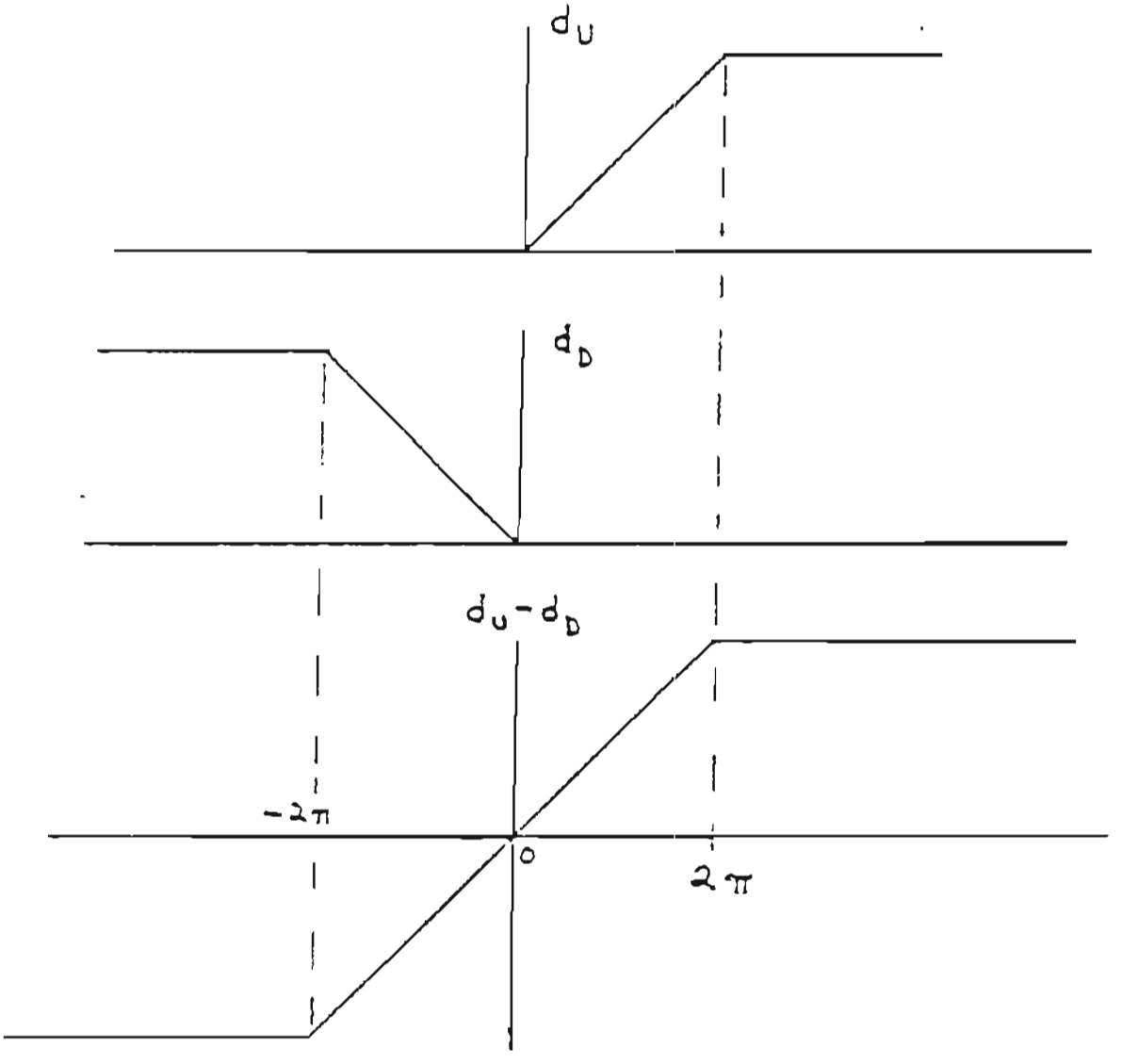
Device has two output terminals, U and D. Low (pulled-down) condition is active; High is inactive. Both U and D can be High simultaneously, but not Low.

Low U indicates positive θ between R and V.

Low D indicates negative θ between R and V.

Duty cycle, d_U or d_D, of low condition indicates magnitude of θ.

Useful output (DC analog average) is $d_U - d_D$.



DOUBLE-LOOP PLL

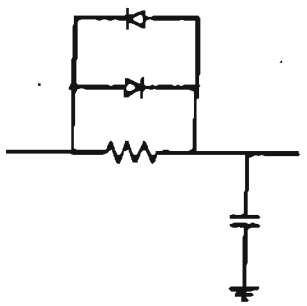
IT IS POSSIBLE TO HAVE A WIDER LOOP DURING PULL-IN AND THEN NARROW THE LOOP AFTER LOCK-IN.

THE OUTPUT OF THE QUADRATURE DET. (WHICH INDICATES LOCK) CAN BE USED AS THE SWITCHING SIGNAL.

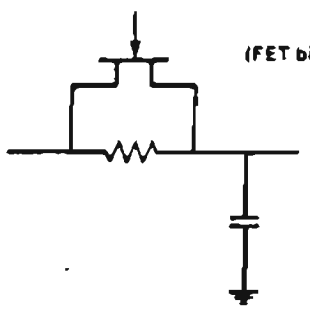
WE CAN SWITCH EITHER THE GAIN OR AN ELEMENT OF THE LOOP FILTER.

CHANGING PLL BANDWIDTH:

WIDER DURING ACQUISITION



(a)



(FET bias circuits not shown)

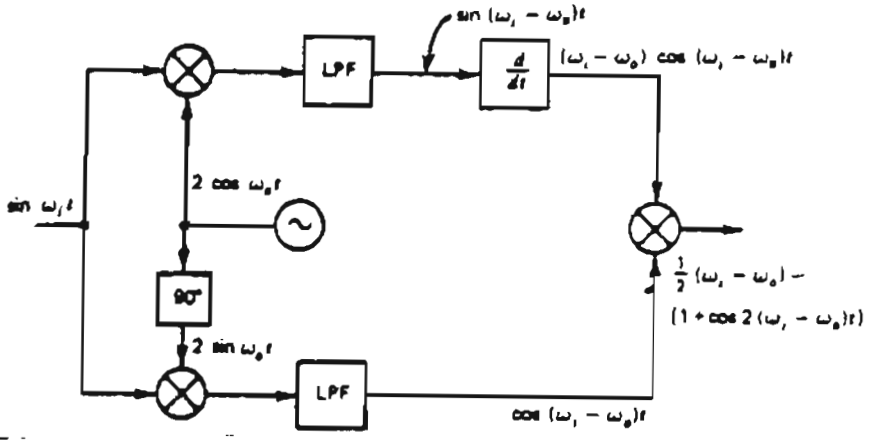
(b)

Modifying loop-filter parameters to aid acquisition. In (*a*) the filter-corner frequency is higher for larger input changes. In (*b*) the bandwidth is switched by an external signal.

INCREASED NOISE BANDWIDTH MAY BE A PROBLEM.

QUADRICORRELATOR:

QUASI-COHERENT FREQ. DIFFERENCE DETECTOR.



Quadricorrelator (frequency-difference detector).

OPERATION:

FORM BEAT FREQUENCY

DIFFERENTIATE (DISCRIMINATOR ACTION)

DETECT COHERENTLY

Problem

An order-2 type-1 PLL has a closed-loop response given by

$$H(s) = \frac{\frac{s}{1000} + 1}{\frac{s^2}{10^6} + \frac{s}{1000} + 1}$$

The open-loop response has one of its poles at 10 RPS.

Find: (a) Hold-in range, (b) Pull-in range, (c) Pull-in time for a frequency offset of 10,000 RPS, (d) max. slope permitted for sweep in search and lock configuration, and (e) PLL closed-loop noise bandwidth.

The phase detector is a multiplier.

Answers: 10^5 RPS, 14,000 RPS, 0.1 sec, 10^6 RPS/sec, 500Hz.

SOLUTION (ACQUISITION)

FROM GIVEN H(s) AND THE TABLE IN LINEAR ANALYSIS:

$$a = 1000 \text{ RPS}, \quad Kb = 10^6, \quad Bn = \frac{Kb\,(\frac{Kb}{a} + a)}{4a\,(\frac{Kb}{a} + b)} \quad \text{Hz}$$

b = 10 RPS (Given); THEREFORE, $K = 10^5$ RPS.

(a) $HIR = K = 10^5$ RPS

(b) $PIR = 2\,[10^6(1 + \frac{10^5}{2000})]^{\frac{1}{2}} \approx 14{,}000$ RPS

(c) $PIT \approx \frac{10^3(10^4)^2}{(10^6)^2} = 0.1$ SEC.

(d) $w_n^2 = Kb = 10^6$ RPS/SEC

(e) $Bn = \frac{10^6(10^3 + 10^3)}{4 \times 10^3\,(10^3 + 10)} = 500$ Hz

DISTORTION AND NOISE CALCULATIONS

Jacob Klapper

WE SHALL CONSIDER:

(1) LINEAR DISTORTION AND

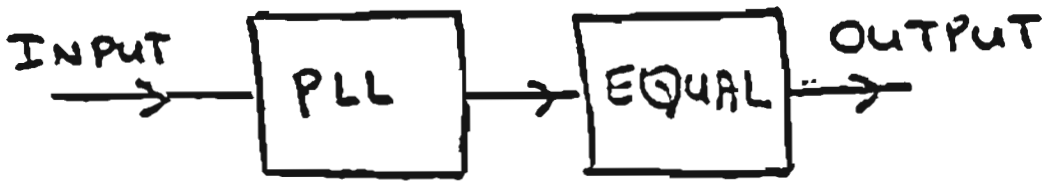
(2) NONLINEAR DISTORTION

LINEAR DISTORTION $\triangleq$ DISTORTION OF OUTPUT WAVESHAPE CAUSED BY LINEAR TIME-INVARIANT COMPONENTS THAT CHANGE AMPLITUDE AND PHASE RELATIONSHIPS AT THE DIFFERENT FREQUENCIES AT WHICH THE WAVE HAS ENERGY.

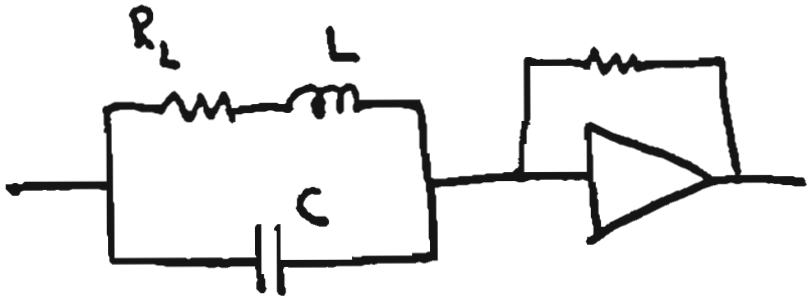
EXAMPLE: SQUARE WAVE FED INTO INTEGRATOR BECOMES A TRIANGULAR WAVE AT ITS OUTPUT.

PLL FREQ. RESPONSE CAN CAUSE LINEAR DISTORTION.

ANTIDOTE: USE EQUALIZER $R_1(s)$

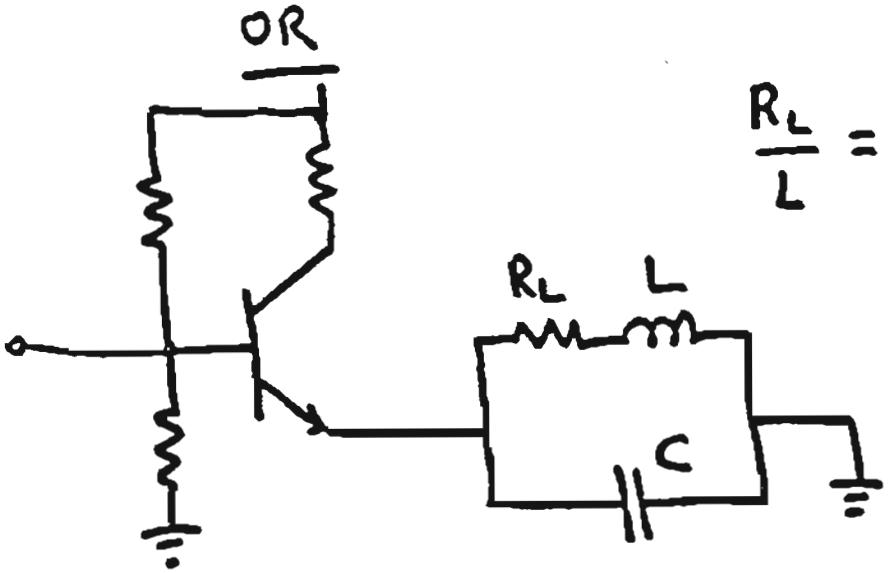


$$R_1(s) = \frac{1}{H(s)} = \frac{\left(\frac{s}{\omega_m}\right)^2 + \left(\frac{s}{\omega_m}\right) + 1}{\frac{s}{\omega_m} + 1}$$



DESIGN EQUATIONS:

$$\frac{R_L}{L} = \frac{1}{\sqrt{LC}} = \omega_m$$



EXAMPLE: FOR THE 600 CHANNEL FDM/FM DESIGN DISCUSSED EARLIER, $\omega_m = 43 \times 10^6$ RPS.

$R_L = 430\,\Omega$, $L = 10\,\mu H$, $C = 54\,pF$

NOTE: THERE IS NO UNIQUE SET OF R_L, L, AND C.

CHOOSE ONE PARAMETER WITH CONVENIENT VALUE AND THEN CALCULATE THE OTHER TWO.

NONLINEAR DISTORTION

SOURCES:

(1) Φ DET. (MULTIPL. TYPE)

(2) VCO NONLINEARITY

(3) BASEBAND AMPL. OVERLOAD

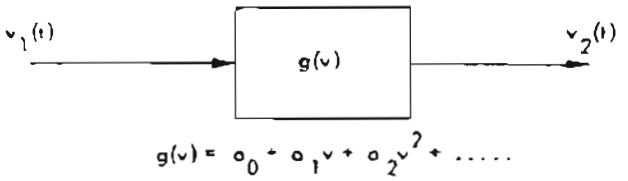
DISTORTION (NONLINEAR)

FOR SMALL VALUES OF DISTORTION :

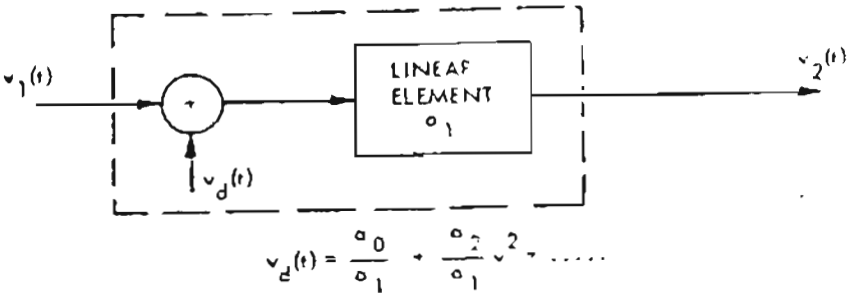
1. WRITE NONLINEAR CHARACTERISTICS IN TERMS OF TRUNCATED POWER SERIES.

2. REPLACE NONLINEAR ELEMENT BY LINEAR ELEMENT PLUS DISTORTION GENERATOR.

3. USE LINEAR ANALYSIS TO OBTAIN AMOUNT OF DISTORTION.



(a)

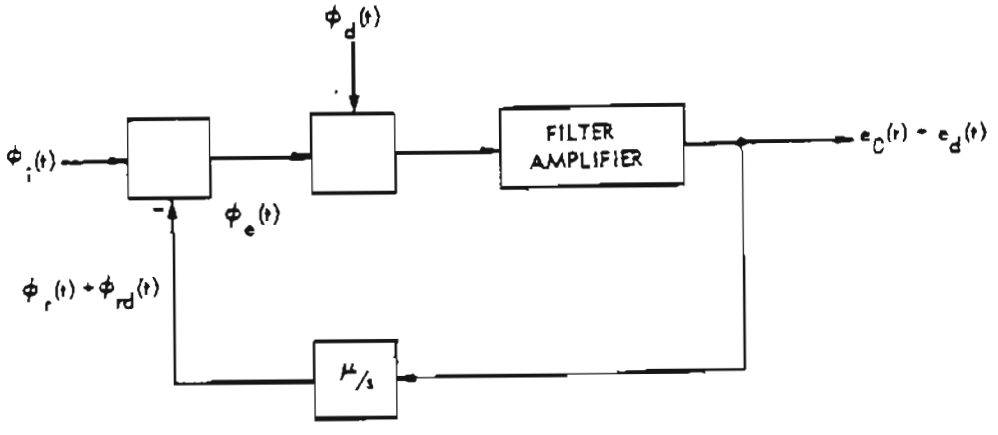


(b)

EXAMPLE : PHASE DETECTOR DISTORTION

$$\text{SIN}\ \phi_e(t) = \phi_e(t) - \frac{\phi_e^3(t)}{3!} + \cdots$$

$$\therefore\ \phi_d(t) = -\frac{\phi_e^3(t)}{6} = \frac{-1}{G}\left[(1-H(s))\,\Phi_i(s)\right]^3$$



EXAMPLE: TWO-TONE TEST OF VOICE CHANNEL, SECOND-ORDER PLL.

$$\Phi_i(t) = \frac{\Delta\omega_1}{\omega_1}\cos\omega_1 t + \frac{\Delta\omega_2}{\omega_2}\cos\omega_2 t$$

LET $\omega_1 = 2\pi \times 10^3$ RPS AND $\omega_2 = 2\pi \times 9 \times 10^3$ RPS

THEN

$$\Phi_d(t) = -\frac{1}{6}\left[\frac{\omega_1 \Delta\omega_1}{\omega_n^2}\cos(\omega_1 t + \psi) + \frac{\omega_2 \Delta\omega_2}{\omega_n^2}\cos(\omega_2 t + \theta)\right]$$

OBTAINED USING APPROXIMATION

$$|1 - H(s)| \approx \left|\left(\frac{s}{\omega_n}\right)^2\right| ,$$

ψ AND θ ARE THE ANGLES OF

$1 - H(s)$ AT ω_1 AND ω_2, RESPECTIVELY.

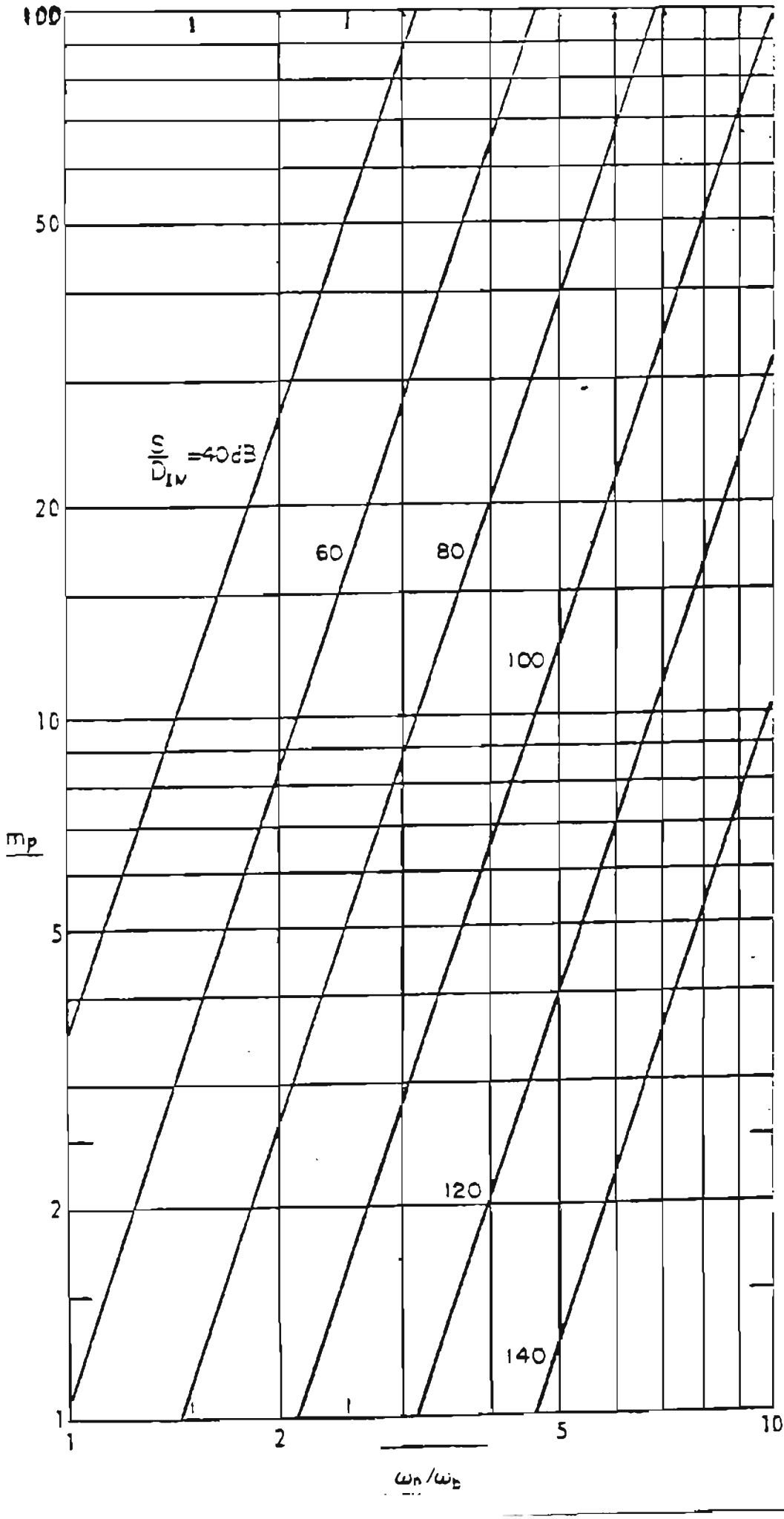
SEPARATING INTO INTERMODULATION (IM) AND HARMONIC (H) TYPES, AND EXCLUDING FREQUENCIES OUTSIDE OF 4-KH_z VOICE BAND, WE GET

$$\left(\frac{S}{D}\right)_{IM} = \frac{8\omega_m^6}{\Delta\omega_1\,\Delta\omega_2\,\omega_1^2\,\omega_2\,(\omega_2 - 2\omega_1)}$$

AND

$$\left(\frac{S}{D}\right)_{H} = \frac{8\omega_m^6}{(\Delta\omega_1)^2\,\omega_1^4}$$

Phase detector distortion contours



EXAMPLE: VCO DISTORTION

$\Delta\omega(t)$ = DEVIATION AWAY FROM CENTER FREQ.

$v(t)$ = INPUT CONTROL VOLTAGE

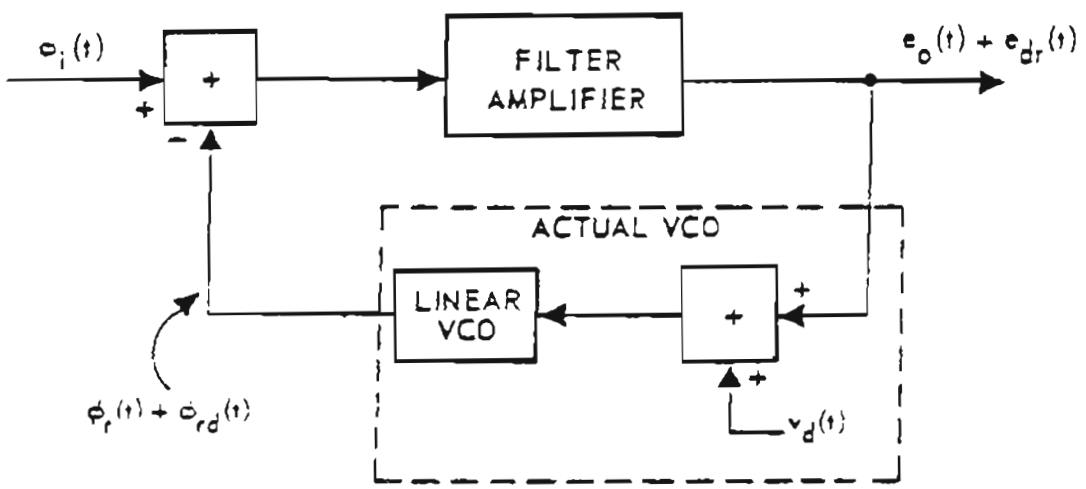
$$\Delta\omega(t) = a_1 v(t) + a_2[v(t)]^2 + a_3[v(t)]^3 + \cdots$$

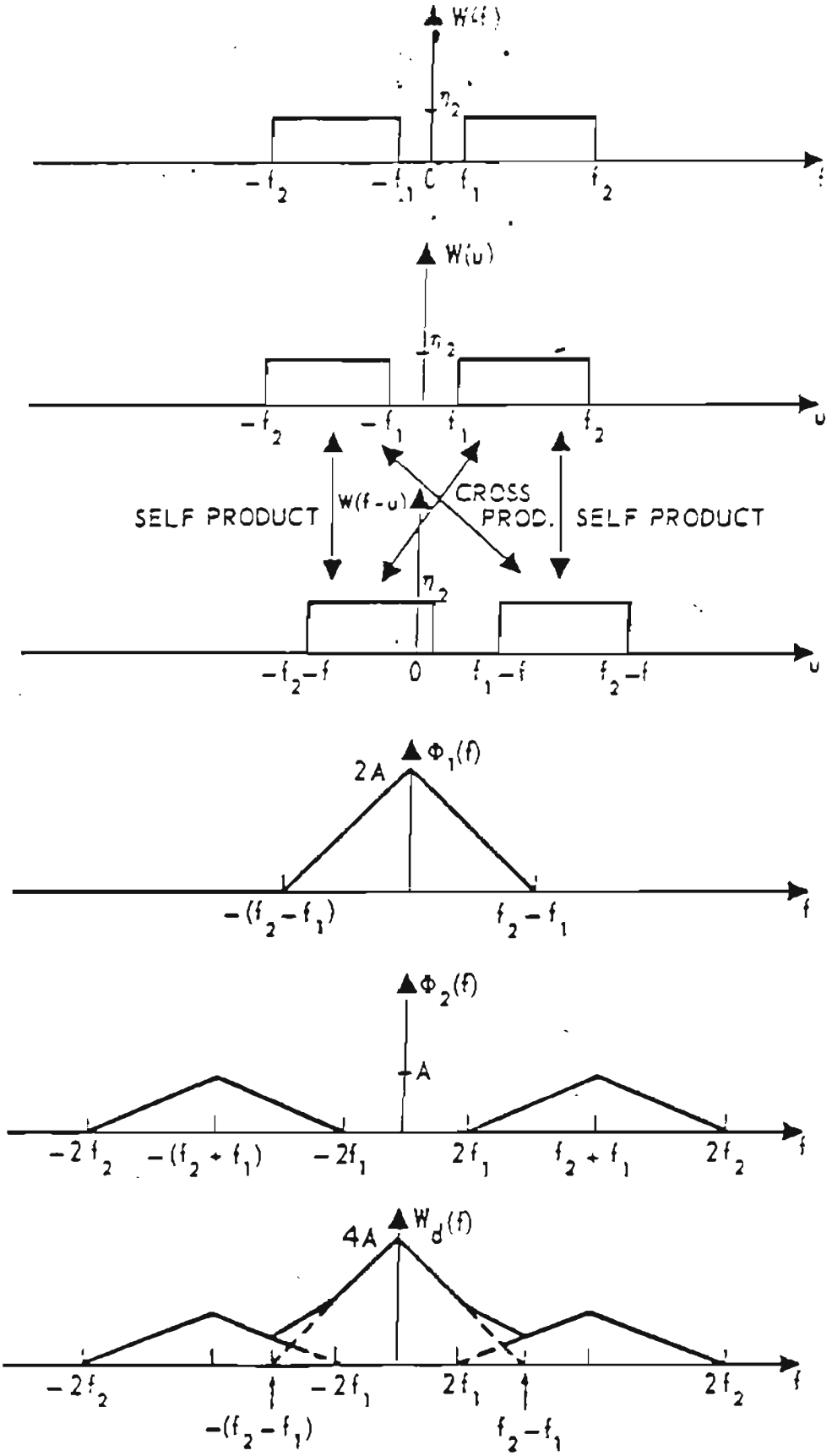
TYPICALLY SQUARE-LAW DOMINATES UNLESS PUSH-PULL ARRANGEMENTS ARE MADE.

THEN $$v_d(t) \approx \frac{a_2}{a_1}[v(t)]^2$$

CONSIDER FDM OF (TWO-SIDED) POWER SPECTRAL DENSITY $W(f)$, THEN

$$W_d(f) = \left(\frac{a_2}{a_1}\right)^2 2 \int_{-\infty}^{\infty} W(u) W(f-u)\, du + \overline{v^2(t)}\,\delta(f)$$


$\theta_i(t)$
+
+
−
FILTER
AMPLIFIER
$e_o(t) + e_{dr}(t)$
ACTUAL VCO
LINEAR
VCO
+
+
+
$\phi_r(t) + \theta_{rd}(t)$
$v_d(t)$


W(f)
η_2
$-f_2$
$-f_1$
C
f_1
f_2
W(u)
η_2
$-f_2$
$-f_1$
f_1
f_2
u
SELF PRODUCT
W(f-u)
CROSS PROD.
SELF PRODUCT
η_2
$-f_2-f$
0
f_1-f
f_2-f
u
$\Phi_1(f)$
2A
$-(f_2-f_1)$
f_2-f_1
f
$\Phi_2(f)$
A
$-2f_2$
$-(f_2+f_1)$
$-2f_1$
$2f_1$
f_2+f_1
$2f_2$
f
$W_d(f)$
4A
$-2f_2$
$-2f_1$
$2f_1$
$2f_2$
f
$-(f_2-f_1)$
f_2-f_1

TO LOWER DISTORTION

1. USE TRIANGULAR OR OTHER LINEAR Ø DET.
   (APPLICABLE ONLY FOR HIGH CNR)

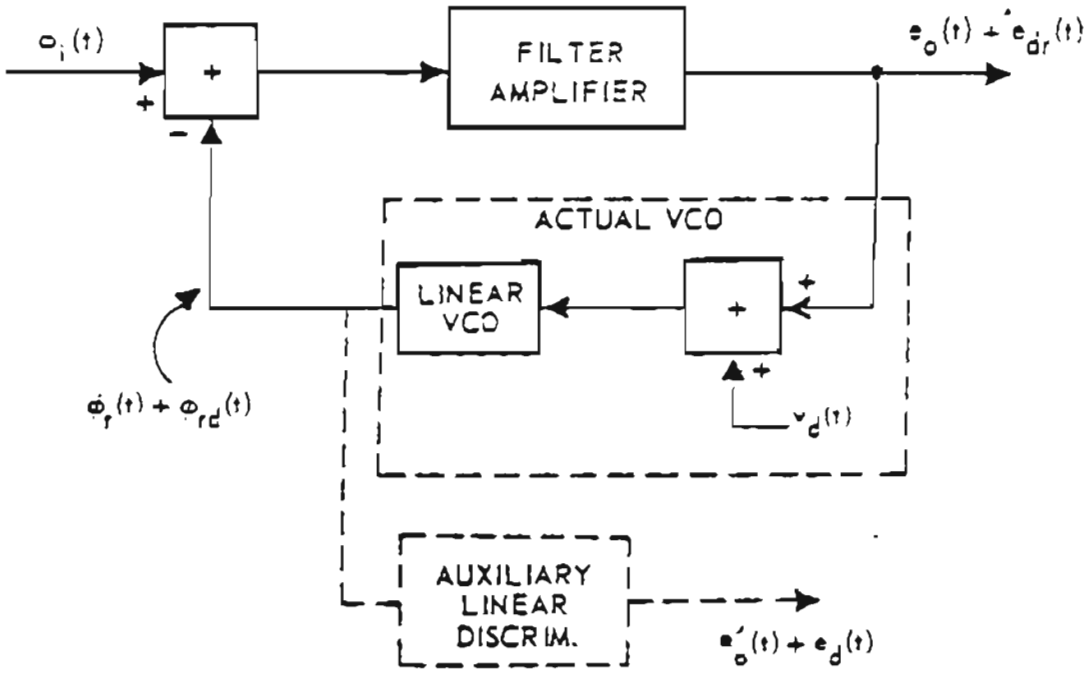
2. USE ERPLD

3. VCO: USE PUSH-PULL TECHNIQUES, MULTVIBRATOR TYPE

4. AS CARRIER AMPLITUDE RISES ABOVE THRESHOLD AND DISTORTION BECOMES DOMINATING, LET INCREASING AMPLITUDE INCREASE LOOP K.

5. CHOOSE APPROPRIATELY OUTPUT OF LOOP. DISTORTION REDUCED BY LOOP GAIN IF OUTPUT IS TAKEN AT OUTPUT OF DISTORTING ELEMENT.

THIS SCHEME LOWERS DISTORTION DUE TO VCO



VCO NOISE DUE TO NOISY LOOP ELEMENTS:

AS FOR DISTORTION, REPLACE NOISY ELEMENT BY NOISELESS ELEMENT PLUS AN EQUIVALENT NOISE GENERATOR AT VCO OR LOOP INPUT.

EQUIVALENT NOISE GEN. IS OBTAINED BY MEASURING VCO NOISE IN OPEN LOOP.

AT LOOP INPUT

$$\phi_i(t) = \phi_{is}(t) + \phi_n(t)$$

WHERE

$\phi_{is}(t)$ = MODULATION DUE TO SIGNAL

$\phi_n(t)$ = MODUL. DUE TO VCO PHASE NOISE.

EXAMPLE

SUPPOSE MEASUREMENTS SHOW EQUIV. NOISE GEN. AT VCO INPUT TO HAVE A POWER SPECTRAL DENSITY En (f)

$$En\ (f) = \frac{\eta_4}{\left(\frac{w}{w_b}\right)^2 + 1}$$

THEN THE EQUIV. PHASE NOISE GEN. AT THE PLL INPUT HAS THE PSD

$$W_n(f) = \frac{K_3^2\ \eta_4}{w^2\left[\left(\frac{w}{w_b}\right)^2 + 1\right]} \quad , \quad K_3 = \text{VCO SENS.}$$

THE PHASE ERROR DUE TO THIS NOISE IS

$$\overline{\phi_{en}^2\ (t)} = \int_0^\infty W_n(f)\ \left|1 - H\ (jw)\right|^2\ d\ f$$

FOR SECOND-ORDER LOOP $\left(\zeta = \frac{1}{2}\right)$

$$\overline{\phi_{em}^2(t)} = \frac{K_3^2 \eta_m}{2\pi\omega_n} \int_0^\infty \frac{\left(\frac{\omega}{\omega_n}\right)^2 d\left(\frac{\omega}{\omega_n}\right)}{\left[\left(\frac{\omega}{\omega_L}\right)^2 + 1\right]\left[\left(\frac{\omega}{\omega_n}\right)^4 - \left(\frac{\omega}{\omega_n}\right)^2 + 1\right]}$$

CONSIDER LOOP FOR REFERENCE EXTRACTION (NARROW BAND), THEN

$$\omega_n \ll \omega_L$$

AND $$\overline{\phi_{em}^2(t)} = \frac{K_3^2 \eta_m}{4\omega_n}$$

REFERENCE: KLAPPER & FRANKLE, CH. 6.

EXCESS DELAY

Open-loop excess phase shift or delay are due to:

Physical electrical length of signal path

Stray high-frequency poles

Finite response time of elements

We can model it as pure delay, based on the phase shift in the critical region, i. e., where $|G(jw)| \simeq 1$.

$G_d(s)$ = open-loop response including delay = $G(s)e^{-sT}$

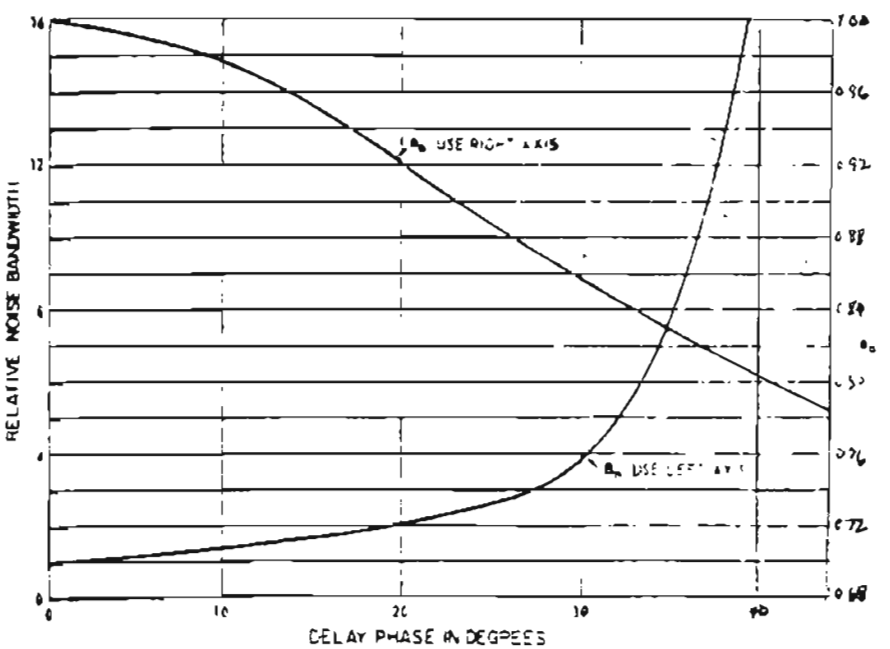
T = delay due to excess phase shift

Delay increases noise bandwidth of closed loop.

We can minimize B_n by moving zero a.

Graph below illustrates increase in minimum B_n caused by excess phase shift and the ratio of the new value of a to the optimum value of a for a loop without excess phase shift.

For example, for an excess phase shift of 20*, the noise bandwidth is doubled and the optimum zero frequency is 8% lower.



Minimum relative noise bandwidth of second-order type-two PLL, i.e., $B_n(\phi)/B_n(0)$, as a function of delay phase $\phi = \tau\omega_n$.

PROBLEM (Distortion)

Consider a VCO with a nonlinearity dominated by the square-law term. Find the equivalent distortion generator if the control voltage is $2\sin 1000t$ and the second harmonic distortion component is 40dB below the desired fundamental.

SOLUTION (DISTORTION)

$$\Delta w(t) = a_1 v(t) + a_2 [v(t)]^2$$

$$v_{d(t)} = \frac{a_2}{a_1} [v(t)]^2$$

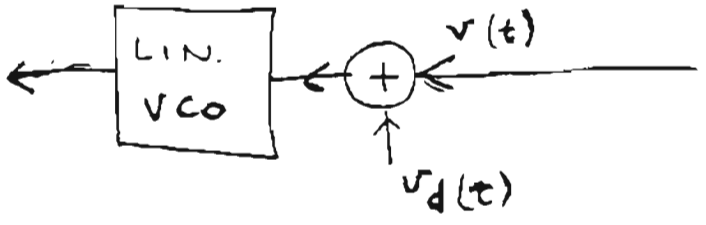
$$a_2[2 \sin 1000t]^2 = 4 a_2 \sin^2 1000t$$

$$= -2a_2 \cos 2000t + 2a_2$$

$$\frac{2a_2}{2a_1} = 10^{-2} \qquad \therefore \quad \frac{a_2}{a_1} = 10^{-2}$$

$$v_{d(t)} = 10^{-2} [2 \sin 1000t]^2 = 4 \times 10^{-2} \sin^2 100t$$

ACTUAL VCO



FREQUENCY SYNTHESIS

FREQUENCY SYNTHESIZER:

A VERY STABLE SOURCE WHOSE FREQUENCY CAN BE CHANGED INCREMENTALLY.

EARLY VERSIONS USED SWITCHING FROM XTAL TO XTAL.

MODERN VERSION USES A SINGLE XTAL OSC AND A PLL.

EXAMPLE:

HP3325A SYNTHESIZES 1 μHz to 21 MHz with 11 DIGIT RESOLUTION.

REFERENCES:

1. W. EGAN, FREQ. SYNTHESIS BY PHASE LOCK, 1981.
2. V. MANASSEWITSCH, FREQ. SYNTHESIZERS, 2nd. ED., 1980.
3. D. DANIELSON AND S. FROSETH, "A SYNTHESIZED SOURCE WITH FUNCTION GENERATOR CAPABILITIES", HP Journal Jan. 1979, pp. 18-26.
4. MOTOROLA LITERATURE

PARAMETERS OF INTEREST:

RANGE OF OUTPUT FREQUENCIES

RESOLUTION

SPEED OF RESPONSE TO AN INSTRUCTION

PHASE NOISE ABOUT THE CARRIER

PURITY OF OUTPUT (SPURIOUS)

EXAMPLE OF SPECS:

Partial Performance Specification for the First Local Oscillator of Model DCR-30 Computer-Controlled Receiver, Manufactured by GI Electronic Systems Division

Frequency range:	92.67 to 122.17 MHz
Frequency increments:	100 Hz
Nonharmonically related spurious outputs:	(*a*) Spurious outputs falling in the passband of the front end or first IF frequencies, −110 dB (*b*) Elsewhere, −80 dB
Phase noise:	See Fig. 7-19
Switching time:	5 msec

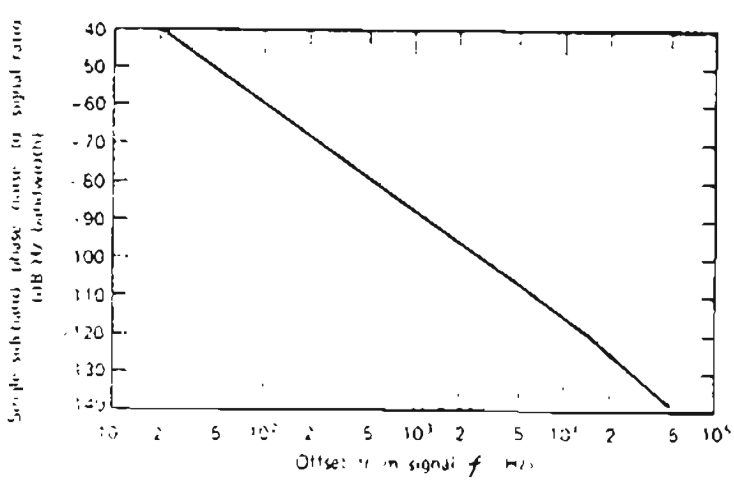


Figure 7-24 Phase-noise requirement for the first local oscillator of model DCR-30B computer-controlled receiver, manufactured by GI Electronic Systems Division.

TYPE OF SYNTHESIZERS:

1. ALL DIGITAL

2. DIRECT

3. INDIRECT (PHASE-LOCKED)

OF THESE, THE INDIRECT IS THE LEAST EXPENSIVE BUT REQUIRES THE GREATEST SOPHISTICATION IN DESIGN BECAUSE OF CONFLICTING REQUIREMENTS ON THE PARAMETERS.

FOR EXAMPLE:

LOWER SPURIA REQUIRE SMALLER PLL BANDWIDTH, BUT THIS MAY DECREASE UNDULY SPEED OF RESPONSE.

THIS IS ONLY ONE OF A NUMBER OF SUCH CONFLICTING REQUIREMENTS.

INDIRECT TYPES:

- ANALOG
- $\frac{0}{8}$ N
- DUAL-MODULUS
- FRACTIONAL N

The Digital (Look-Up-Table) Synthesizer

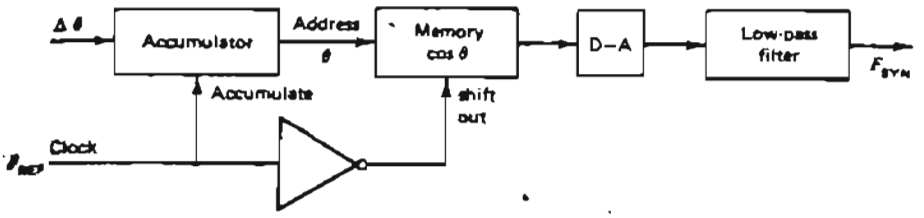
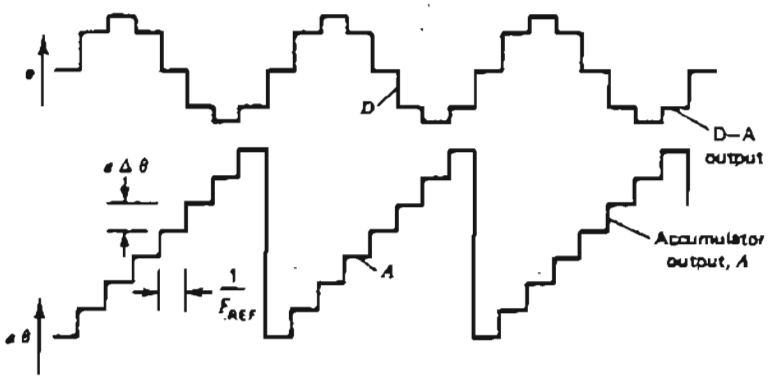


Figure 2.1 Basic diagram of a digital synthesizer.



Some signals from the digital synthesizer.

OPERATION:

1. WAVEFORM SYNTHESIZED PIECE BY PIECE.
2. A NUMBER, $\Delta\phi$, IS SHIFTED INTO ACCUMULATOR AT CLOCK FREQUENCY.

   ACCUMULATOR OUTPUT IS AS SHOWN.

   FOR A HIGHER FSYN, USE LARGER $\Delta\theta$.

   CAPACITOR OF ACCUMULATOR CORRESPONDS TO ONE COMPLETE CYCLE.

   WHEN ACCUMULATOR REACHES CAPACITY, IT RESETS.

3. MEMORY CHANGES ϕ TO COS ϕ (via table look-up).

PROPERTIES OF ALL-DIGITAL:

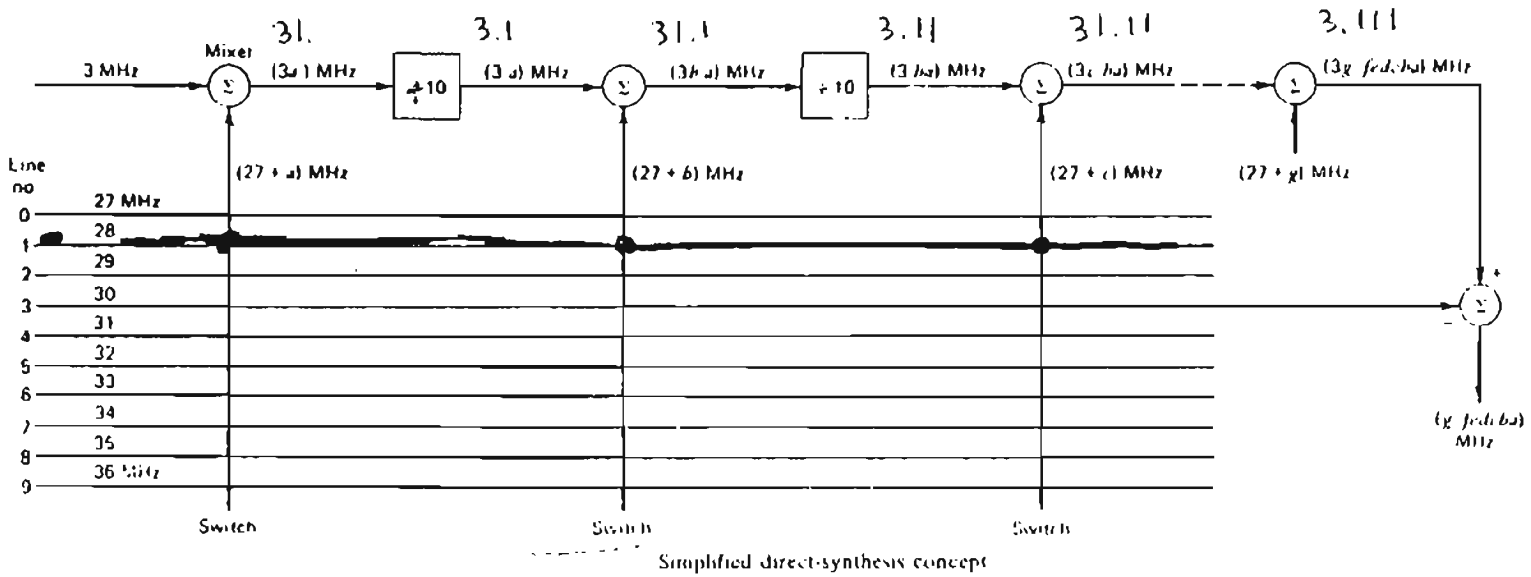
1. FAST RESPONSE (+)

2. FINE RESOLUTION (+)

3. UPPER FREQ. LIMITED BY CURRENT MEMORIES (-)

4. BEST REPORTED SPURIOUS SUPPRESSION: 50-60dB (-)

DIRECT SYNTHESIS



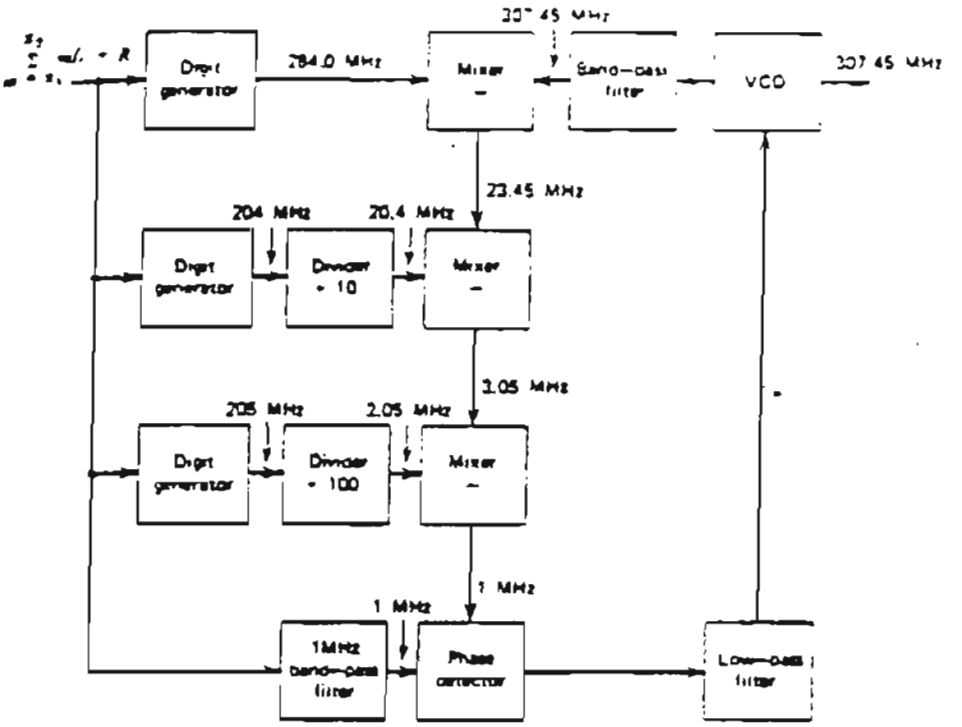
Simplified direct-synthesis concept

EXAMPLE USES 28.MHz LINE

PROPERTIES:

1. FAST RESPONSE
2. FINE RESOLUTION
3. LOW SPURIA
4. COSTLY & BULKY

INDIRECT (PLL) SYNTHESIZER TYPE



Analog phase-locked loop synthesizer, parallel injection: an example.

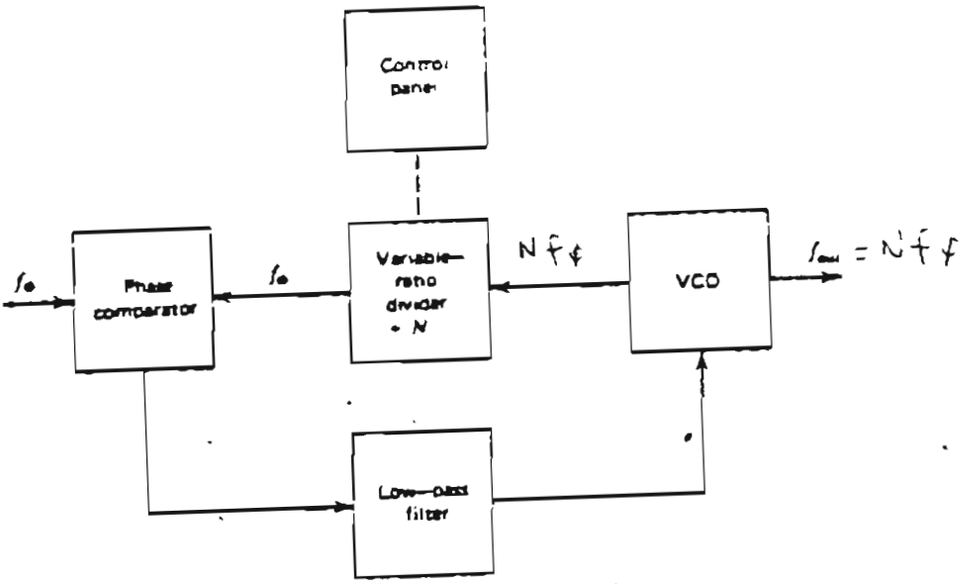
RANGE:

300 MHz – 309.99 MHz IN 10 KHz STEPS.

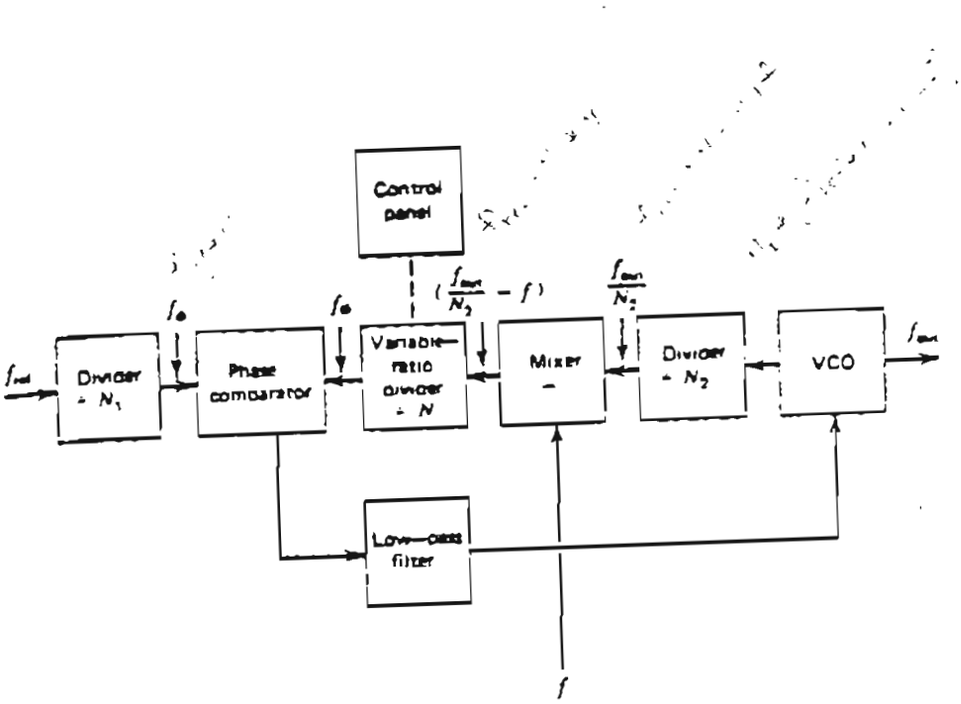
1000 FREQUENCIES, 3 DECIMAL DIGITS.

OPERATION:

EACH MIXER REMOVES A DIGIT

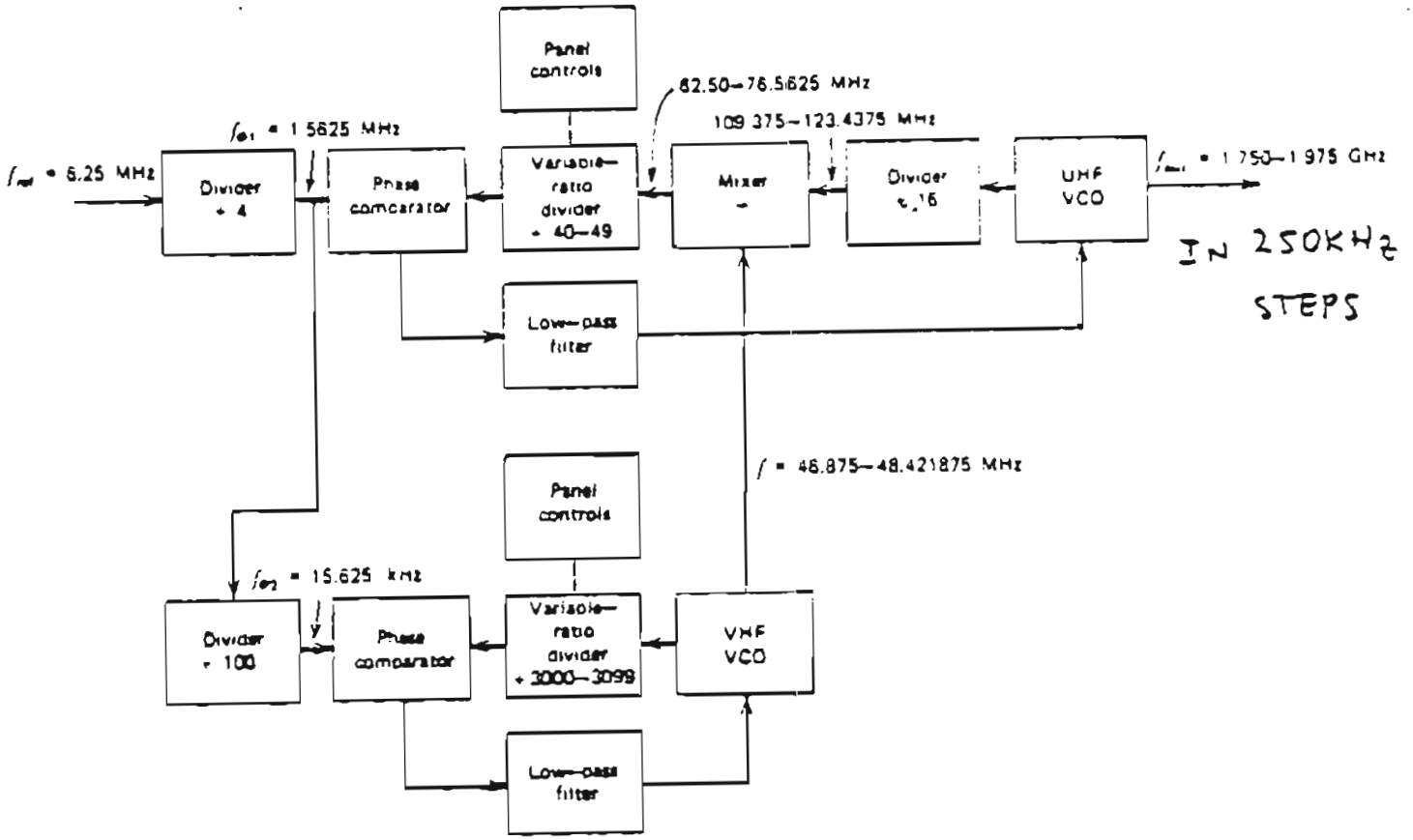


Digital phase-locked loop synthesis: basic configuration.



Digital phase-locked loop synthesis, main phase-locked loop.

ADDITIONAL FLEXIBILITY VIA FIXED DIVIDER N_2 AND THE MIXER.



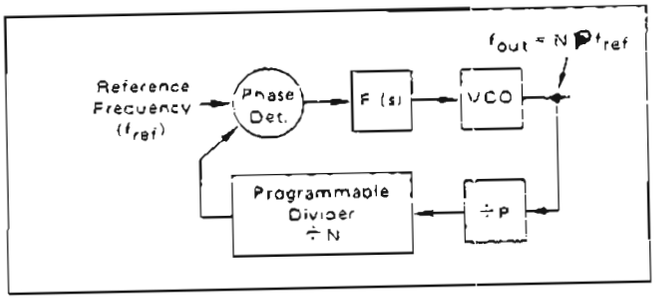
Double digital phase-locked loop synthesis: an example.

IN 250KHz STEPS

SECOND LOOP PERMITS FINER RESOLUTION

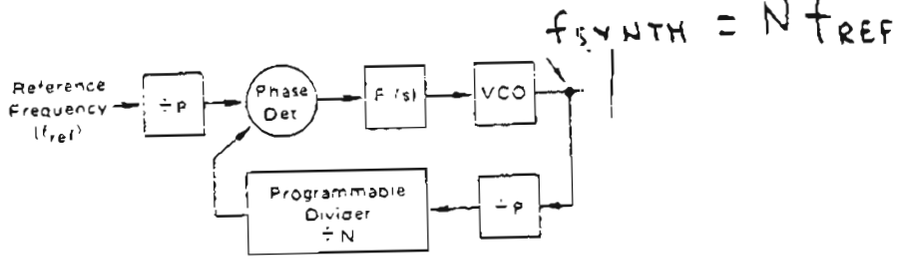
IF VCO FREQ. IS TOO HIGH FOR PROGRAMMABLE DIVIDER, USE FIXED DIVIDER FIRST.

– FREQUENCY SYNTHESIS BY PRESCALING



PROBLEM: $\Delta f = P f_{REF}$

ALTERNATE POSSIBILITY:

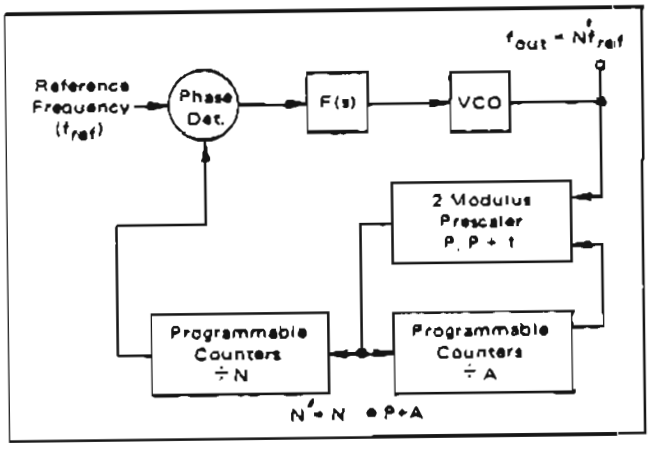


HERE $\Delta f = f_{REF}$ BUT PLL BANDWIDTH IS REDUCED BY FACTOR P.

WE CAN HAVE A HIGH-FREQUENCY PRESCALAR AND RETAIN $\Delta f = f_{REF}$ AND THE PLL BANDWIDTH BY USE OF

DUAL-MODULUS DIVIDERS.

– FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



LOOP INCLUDES:

PROGRAMMABLE COUNTER %N

" " %A

TWO-MODULUS PRESCALAR (DIVIDE BY P OR P+1)

EQUATION FOR DESIGN:

$$f_{SYNTH} = [N \cdot P + A] f_{REF}$$

(PROOF IS IN MC12012) last in steps of Af_{ref}

FOR A RANGE OF N_{TOTAL} VALUES IN SEQUENCE:

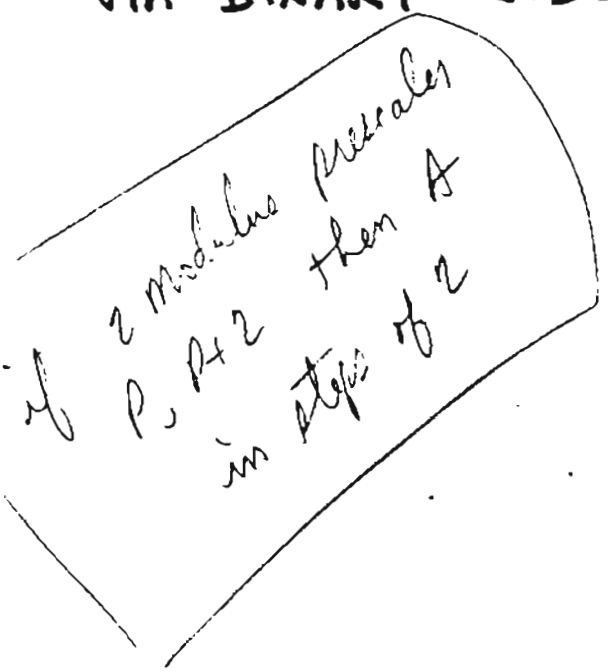
A. SEQUENCE $\frac{\bullet}{o}$ A FROM 0 TO P-1

B. INCREMENT N BY 1

C. SEQUENCE $\frac{\bullet}{o}$ A FROM 0 TO P-1

ETC..

IF $P = 2^K$ (K = INTEGER), THEN PROGRAMMING CAN USUALLY BE DONE VIA BINARY CODE, FOR THE N_{TOTAL}.



Next page 1st

AS WE INCREMENT "A", WE CHANGE FSYNTH BY FREF. HOWEVER, PROGRAMMABLE COUNTERS HAVE INPUT FREQ = $\frac{fsyn}{P}$

NOTE:

NUMBER IN N COUNTER MUST BE GREATER OR EQUAL TO NUMBER IN "A" COUNTER. OTHERWISE ERRORS WILL OCCUR.

Ntotal(MIN) $>$ (P-1)P.; Ntotal (MAX) = Nmax P + AMAX

EXAMPLE:

fsynth = 90 MHz to 110 MHz in 100KHz steps use P=10

SOLUTION:

fref = 100 KHZ, A = 0 to 9, N = 10 to 110

lowest fsyn for N = 90 and A = 0

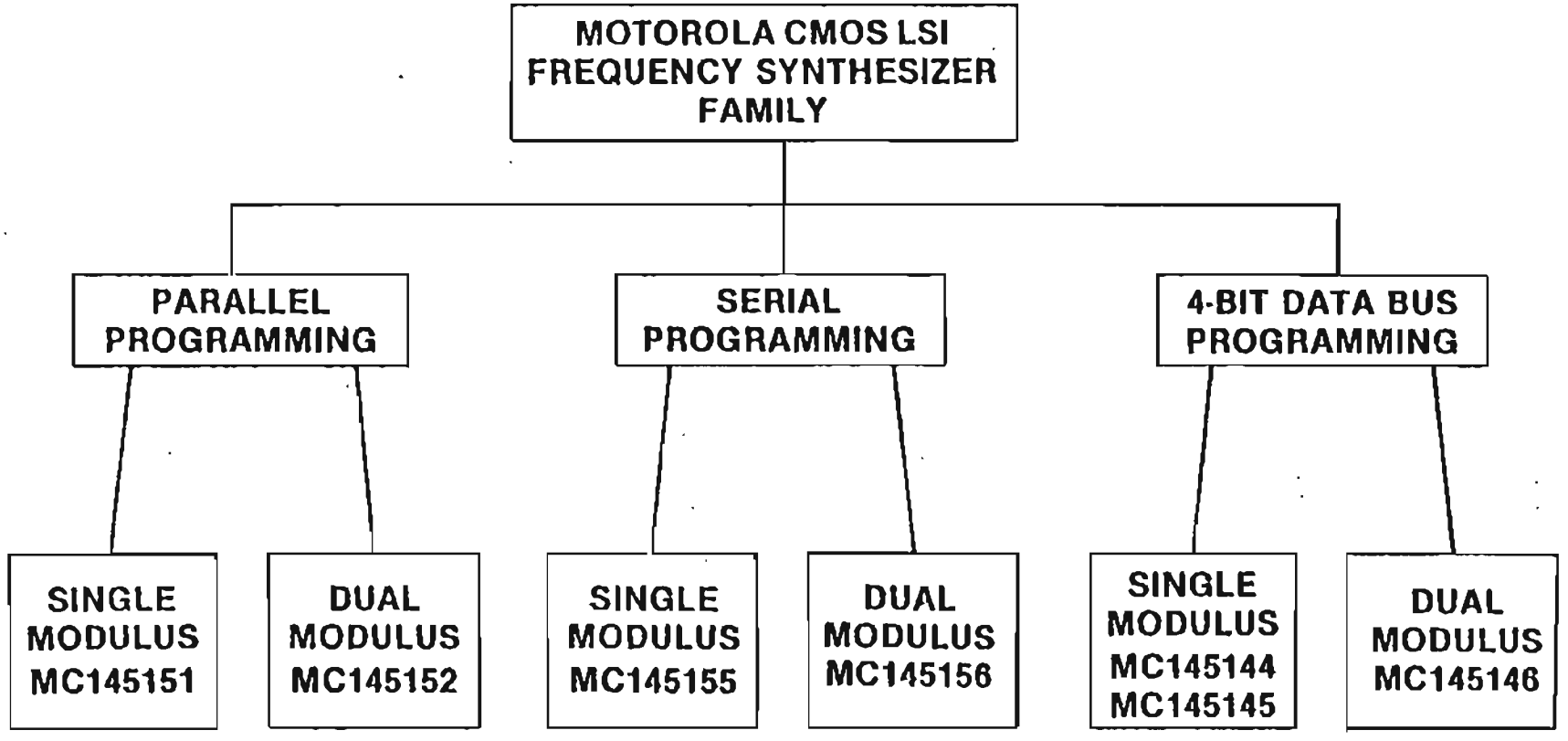
highest fsyn for N = 110 and A = 0

For N = 90, A = 1, we have (901) fref = 90.1 MHZ

NOTE: N $\geq$ A; (P-1) P = 90;

MOTOROLA SEMICONDUCTOR GROUP
MOS INTEGRATED CIRCUITS DIVISION
LOGIC AND SPECIAL FUNCTIONS

FREQUENCY SYNTHESIZER FAMILY

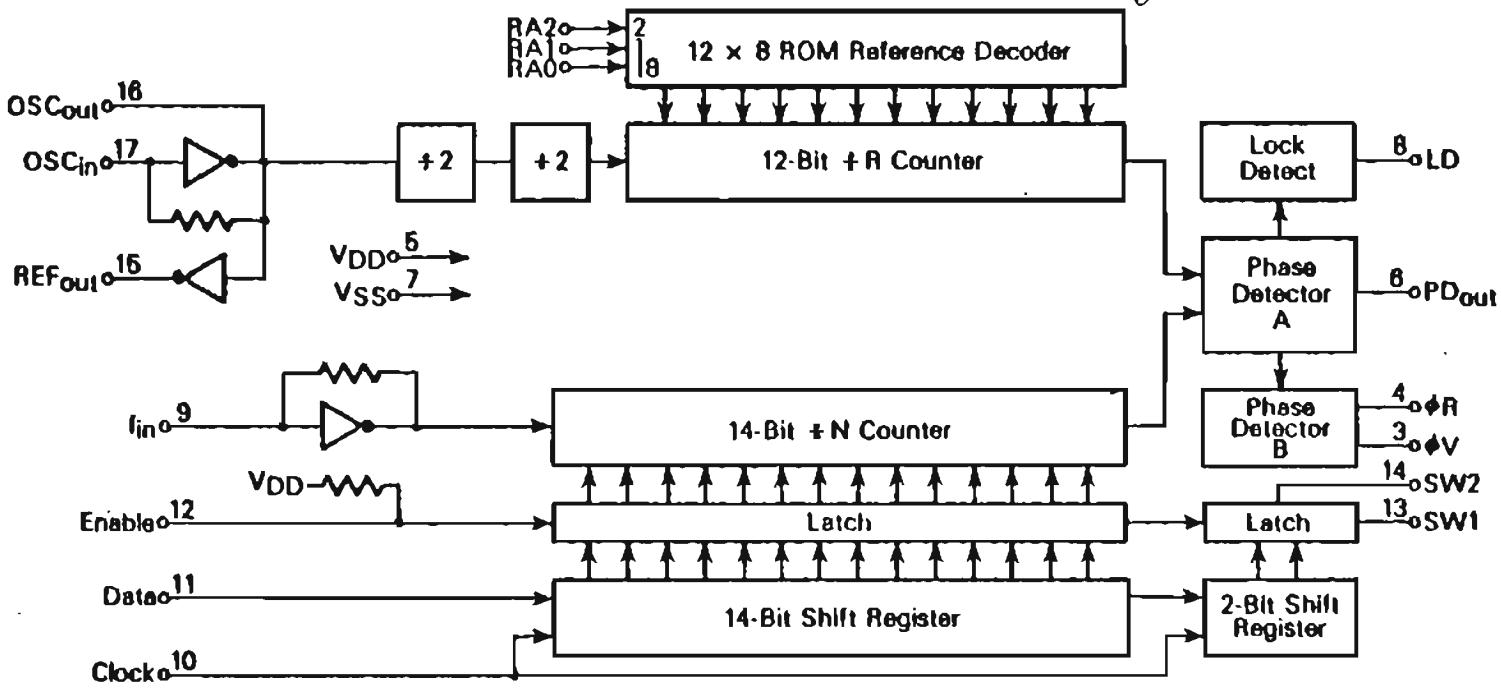


MOTOROLA SEMICONDUCTOR GROUP
MOS INTEGRATED CIRCUITS DIVISION
LOGIC AND SPECIAL FUNCTIONS

PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

PRODUCT	SCHEDULED INTRODUCTION DATE
• MC145144: 4-BIT DATA BUS PROGRAMMABLE, SINGLE MODULUS FOR TV TUNING (2nd SOURCE MATSUSHITA MN6044)	MAR '80
• MC145145: 4-BIT DATA BUS PROGRAMMABLE, SINGLE MODULUS	MAR '80
• MC145146: 4-BIT DATA BUS PROGRAMMABLE, DUAL MODULUS	MAR '80
• MC145151: PARALLEL PROGRAMMABLE, SINGLE MODULUS	MAR '80
• MC145152: PARALLEL PROGRAMMABLE, DUAL MODULUS	MAR '80
• MC145155: SERIAL PROGRAMMABLE, SINGLE MODULUS	OCT '79
• MC145156: SERIAL PROGRAMMABLE, DUAL MODULUS	OCT '79

MC145155



AA00678

MC145155 SINGLE MODULUS PRESCALE SERIAL PROGRAMMING

- 18 PIN PACKAGE
- 25 MHz TYPICAL INPUT FREQUENCY
- IMPROVED 3 STATE PHASE DETECTOR
- TWO PHASE DETECTOR OUTPUT METHODS
- PROGRAMMABLE 14-BIT + N COUNTER
- 8 ROM PROGRAMMED REFERENCE DIVIDER VALUES
- ON CHIP OSCILLATOR (EXTERNAL XTAL)
- IDEAL FOR MICROPROCESSOR CONTROL

AA00577

MOTOROLA

SEMICONDUCTORS

MC145156

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

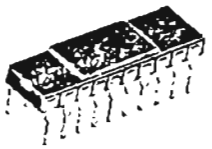
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications –
  - CATV
  - TV Tuning
  - AM/FM Radios
  - Scanning Receivers
  - Two-Way Radios
  - Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- > 30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values – 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options –
  - Single Ended (Three-State)
  - Double Ended

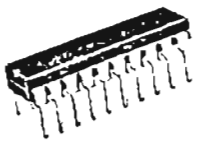
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

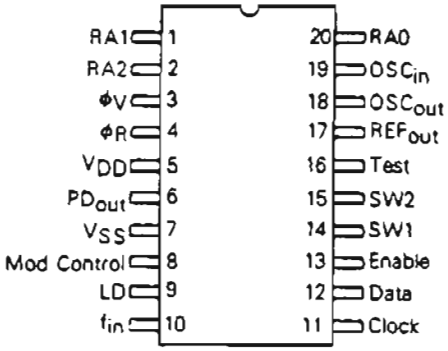


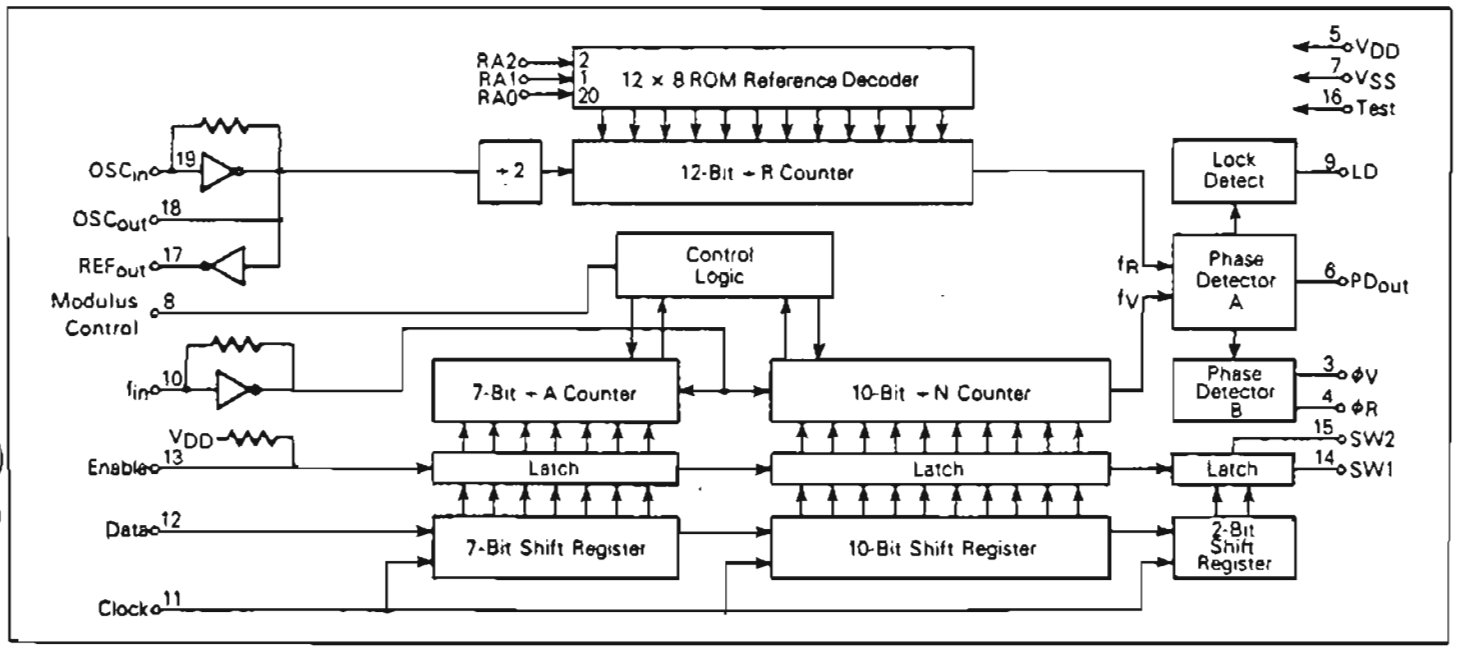
L SUFFIX
CERAMIC PACKAGE
CASE 729-01



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT





DS9809

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mA
DC Current Drain V_{DD} or V_{SS} Pins	I	30	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

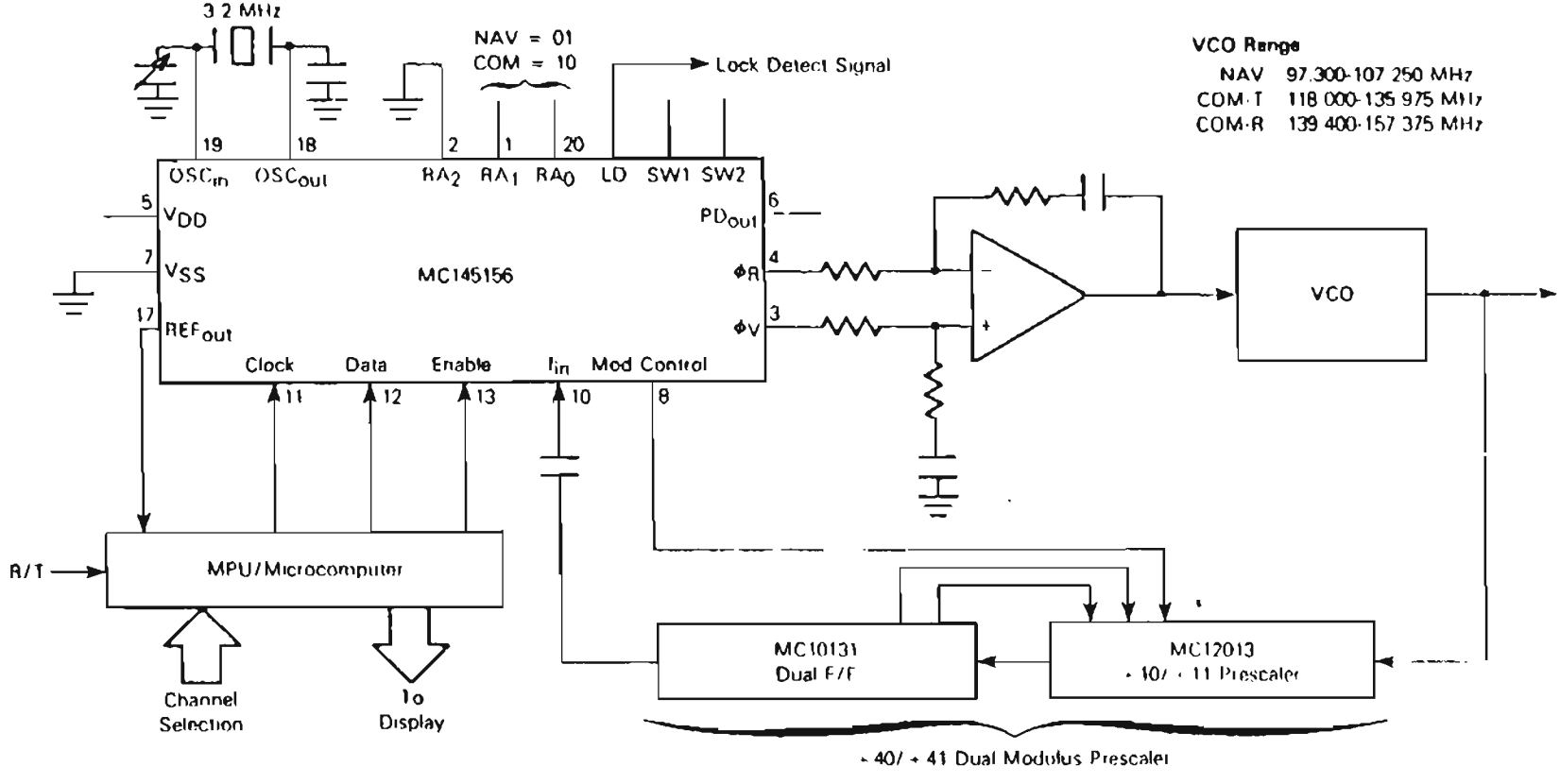
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	T_{Low} Min	T_{Low} Max	25°C Min	25°C Typ	25°C Max	T_{High} Min	T_{High} Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	Vdc
Output Voltage 0 Level V_{in} = V_{DD} or 0	V_{OL}	3	–	0.05	–	0	0.05	–	0.05	Vdc
		5		0.05	–	0	0.05	–	0.05	
		9	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD} 1 Level	V_{OH}	3	2.95	–	2.95	3	–	2.95	–	
		5	4.95	–	4.95	5	–	4.95	–	
		9	8.95	–	8.95	9	–	8.95	–	
Input Voltage 0 Level V_O = 2.5 or 0.5	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	Vdc
V_O = 4.5 or 0.5		5	–	1.5	–	2.75	1.5	–	1.5	
V_O = 8.5 or 1.5		9	–	2.7	–	4.05	2.7	–	2.7	
V_O = 0.5 or 2.5 1 Level	V_{IH}	3	2.10	–	2.10	1.65	–	2.10	–	
V_O = 0.5 or 4.5		5	3.5	–	3.5	2.75	–	3.5	–	
V_O = 1.5 or 8.5		9	6.3	–	6.3	4.95	–	6.3	–	
Reverse Breakdown Voltage SW1, SW2	V_{BDSO}	3-9	15	–	15	24	–	15	–	V
Output Current Source V_{OH} = 2.7	I_{OH}	3	−0.44	–	−0.35	−0.66	–	−0.22	–	mAdc
V_{OH} = 4.6		5	−0.64	–	−0.51	−0.88	–	−0.36	–	
V_{OH} = 8.5		9	−1.3	–	−1.0	−1.3	–	−0.7	–	
V_{OL} = 0.3 Sink	I_{OL}	3	0.44	–	0.35	0.66	–	0.22	–	
V_{OL} = 0.4		5	0.64	–	0.51	0.88	–	0.36	–	
V_{OL} = 0.5		9	1.3	–	1.0	1.3	–	0.7	–	
Output Current Modulus Control Source V_{OH} = 2.7	I_{OH}	3	0.15	–	0.25	0.5	–	0.08	–	mAdc
V_{OH} = 4.6		5	0.45	–	0.75	1.5	–	0.23	–	
V_{OH} = 8.5		9	0.75	–	1.25	2.5	–	0.38	–	
Output Current SW1, SW2, Modulus Control V_{OL} = 0.3 Sink	I_{OL}	3	0.48	–	0.8	1.6	–	0.24	–	mA
V_{OL} = 0.4		5	0.90	–	1.5	3	–	0.45	–	
V_{OL} = 0.5		9	2.10	–	3.5	7	–	1.05	–	
Input Current Other Inputs	I_{IL}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	µAdc
Enable		9	–	−60	–	−25	−50	–	−35	
f_{in}, OSC_{in}		9	–	±15	–	±5	±10	–	±8	
f_{in}, OSC_{in}	I_{IH}	9	–	±15	–	±5	±10	–	±8	
Other Inputs		9	–	±0.3	–	±0.00001	±0.1	–	±1.0	
Input Capacitance	C_{in}	3-9	–	10	–	6	10	–	10	pF
Output Capacitance	C_{out}	3-9	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	µAdc
		5	–	1200	–	300	1200	–	2400	
		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current PD_{out}	I_L	9	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc

NOTE: T_{low} = −40°C
T_{high} = 85°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 8 — AVIONICS NAV AND COM SYNTHESIZER



NOTES:

1) for NAV F_R = 50 kHz, ÷ R = 64 using 10.7 MHz lowside injection, N_{total} = 1946.2145
for COM-T F_R = 25 kHz, ÷ R = 128 using 21.4 MHz highside injection, N_{total} = 4720.5430
for COM-R F_R = 25 kHz, ÷ R = 128 using 21.4 MHz highside injection, N_{total} = 5576.6280
2) A ÷ 32/ ÷ 33 dual modulus approach is provided by substituting an MC12011 (÷ 8/ ÷ 9) for the MC12013. The devices are pin equivalent.
3) A 6.4 MHz oscillator crystal can be used by selecting ÷ R = 128 (code 010) for NAV and ÷ R = 256 (code 011) for COM.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145156 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by the MC145156.

Several dual modulus prescaler approaches suitable for use with the MC145156 are given in Figure 7. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145156 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145156

The system total divide value (N_{total}) will be dictated by the application, i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P − 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. The constraint N > A always applies. If $A_{max} = P - 1$ then $N_{min} > P - 1$. Then $N_{total-min} = (P - 1)\,P + A$ or $(P - 1)\,P$ since A is free to assume the value of zero.

$$N_{total-max} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{vco} max), the value used for P must be large enough such that:

A. F_{vco} max divided by P may not exceed the frequency capability of Pin 10 of the MC145156.

B. The period of F_{vco}, divided by P, must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the MC145156.

A sometimes useful simplification in the MC145156 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

A. Assume the ÷A counter contains "b" bits where $2^b = P$.

B. Always program all higher order ÷A counter bits above "b" to zero.

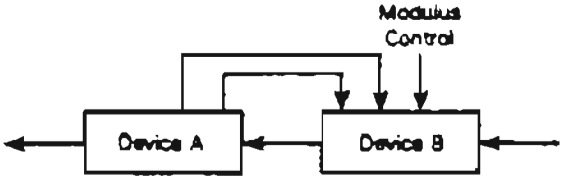
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145156

MC12009	÷5/÷6	440 MHz
MC12011	÷8/÷9	500 MHz
MC12013	÷10/÷11	500 MHz
*MC3393	÷15/÷16	140 MHz

*Proposed introduction in 1980

By using two devices several dual modulus values are achievable:



Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10136	÷50/÷51	÷80/÷81	÷100/÷101
MC10178	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷129/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent

DELAY LIMITATIONS OF DUAL-MOD SYNTH:

PERIOD OF FVCO/P MUST BE GREATER THAN THE SUM OF THE

A. PROPAGATION DELAY THROUGH DUAL-MOD PRESCALER.

B. PRESCALER SETUP OR RELEASE TIME RELATIVE TO ITS MODULUS CONTROL SIG.

C. PROPAGATION TIME FROM FIN (DUAL-MOD PRESCALER OUTPUT) TO THE MODULUS CONTROL OUTPUT OF THE SYNTHESIZER.

A AND B ARE OBTAINED FROM DUAL-MOD PRESCALER SPECS, WHILE C IS PROPERTY OF SYNTHESIZER.

PROBLEM (SYNTHESIZER):

DESIGN A FREQ. SYNTHESIZER

fsyn = 18. MHz to 180. MHZ

in 50 KHz STEPS

USE A DUAL-MODULUS CHIP.

SOLUTION:

USE MC 145156 SYNTH

USE MC 12013 ÷10 / ÷11 PRESCALAR

HIGHEST NP + A = $\frac{180}{.05}$ = 3600

LOWEST NP + A = $\frac{18}{.05}$ = 360

USE 1 MHZ XTAL, R = 1020

LET N = 36 to 360

A = 0 to 9

P = 10/11

PROBLEMS WITH $\frac{1}{N}$ SYNTHESIS:

fsynth = Nfref

fref = ΔF (Freq. increments).

small Δf results in small PLL $\frac{N}{B}$ADWIDTH.

MULTIPLE LOOPS ARE COSTLY AND HAVE MORE SPURIA.

USE FRACTIONAL N SYNTHESIS:

LET N HAVE DECIMAL FRACTIONAL DIGITS

e.g. N = A.abc

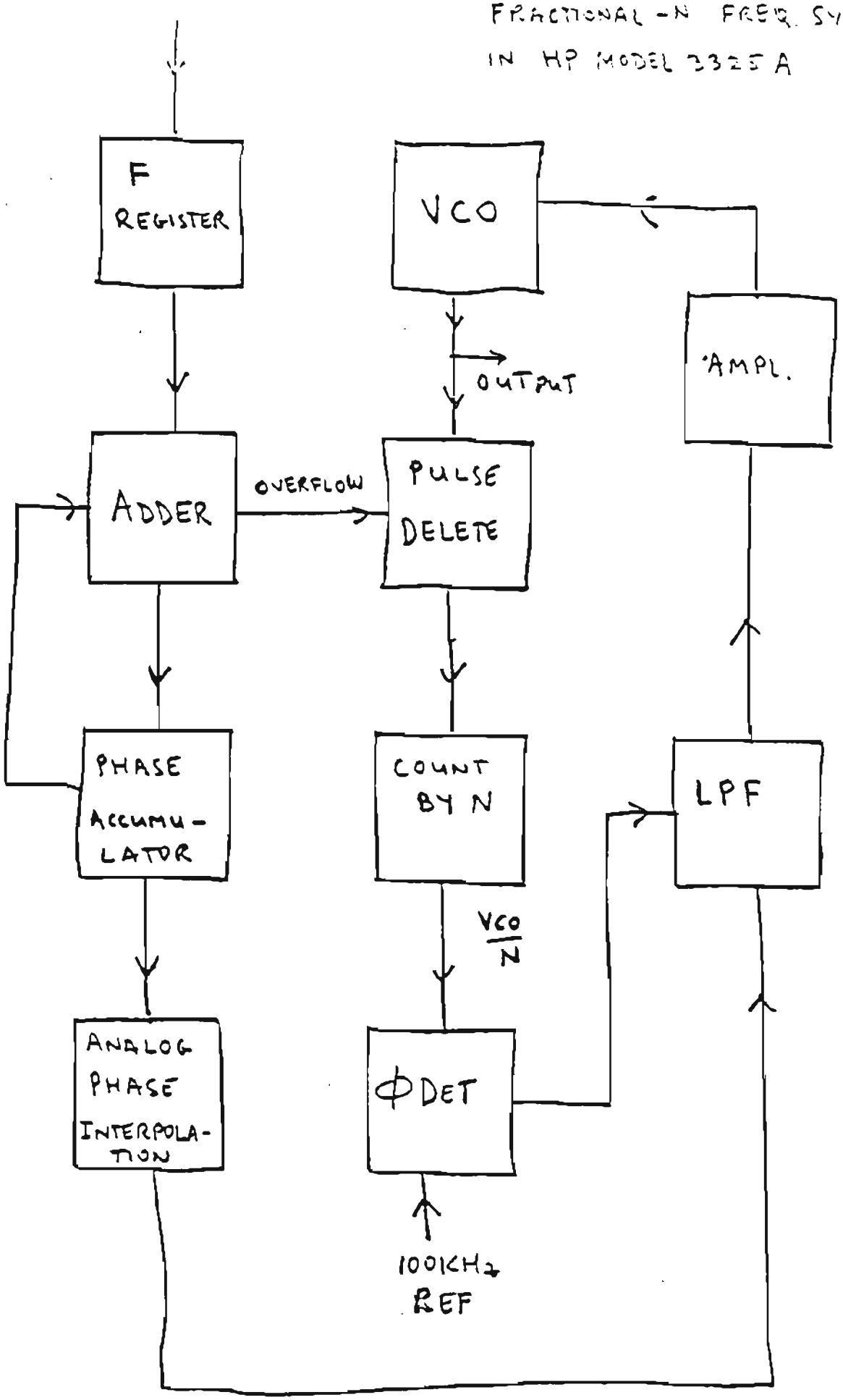
fsynth = A.abc*fref

Δ f = .00Cfref

EXAMPLE: LET N = 450.123, fref = 1KHZ.

THEN $\Delta f = 10^{3} \times .003 = \underline{3HZ}$

FRACTIONAL-N FREQ. SYNTH
IN HP MODEL 3325A



FRACTIONAL-N SYNTHESIS:

INCLUDES COMPONENTS OF DIVIDE-BY-N SYNTHESIS.

OUTPUT FREQ. = N.F X fref

HP's N IS BETWEEN 300 AND 600 AND fref = 100 KHZ

F IS ANY INTEGER 12 DIGITS LONG.

THE FRACTIONAL PART F IS ENTERED INTO F REGISTER IN BCD FORM AND STORED THERE. ONCE DURING EACH CYCLE OF THE 100KHZ REF, THE CONTENTS OF F REGISTER ARE ADDED TO CONTENTS OF PHASE ACCUMULATOR.

WHENEVER THIS ADDITION CAUSES ADDER TO OVERFLOW, ONE CYCLE OF THE VCO OUTPUT IS DELETED FROM COUNT-BY-N INPUT.

EXAMPLE

SUPPOSE WE WANT FREQ. N.1 X 100KHZ.

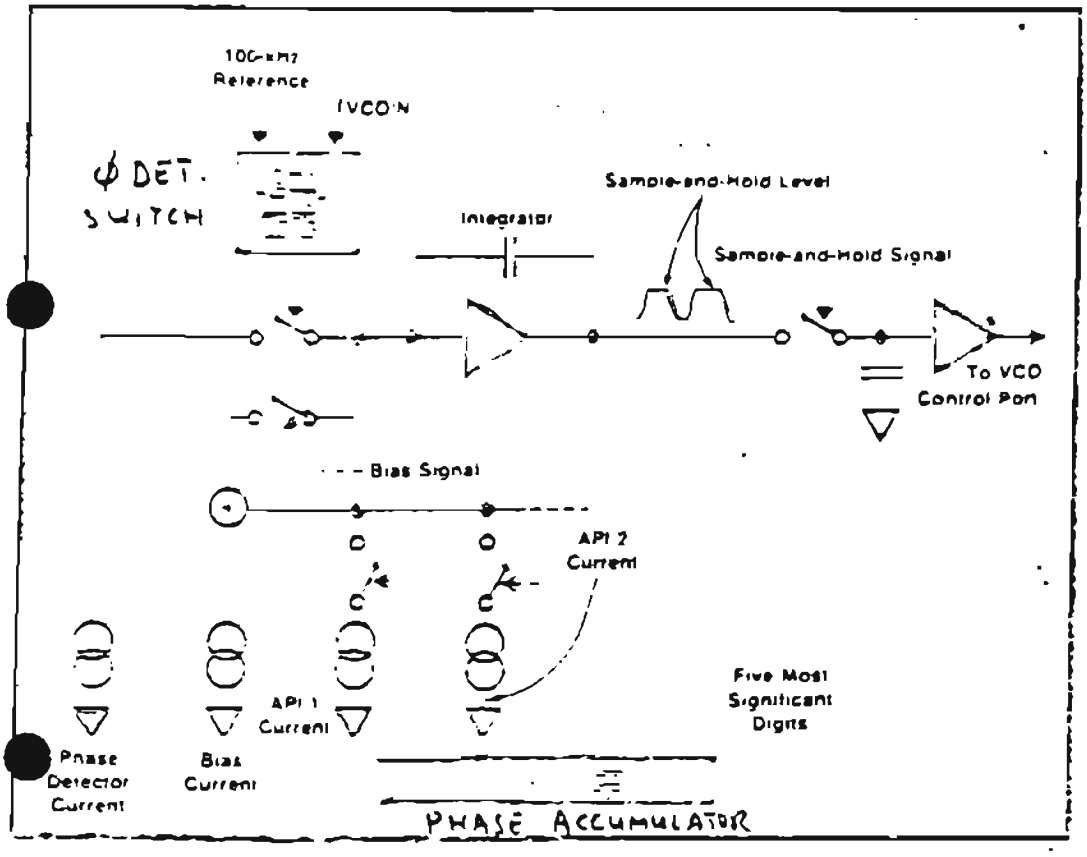
ENTER 0.1 IN F REGISTER.

0.1 IS ADDED TO ACCUMULATOR EVERY REFERENCE CYCLE.

ADDER OVERFLOWS EVERY 10 REF CYCLES.

VCO HAS 10N + 1 REF CYCLES $\Rightarrow$ N.1

ANALOG PHASE INTERPOLATOR (API)



Details of analog phase interpolator.

AFTER SAMPLING INTEGRATOR IS BROUGHT BACK TO A REFERENCE LEVEL.

WHEN THE DESIRED OUTPUT IS NOT AN INTEGRAL MULTIPLE OF f_{REF}, THE VCO/N PULSE GAINS A FRACTIONAL PART OF A CYCLE WITH RESPECT TO THE REF EACH TIME IT OCCURS.

THUS THE ϕDET PULSE BECOMES WIDER DURING EACH SUCCESSIVE REF CYCLE.

THIS RESULTS IN UNDESIRABLE MODULATION SIDEBANDS.

COUNTER - ACTION: USE API

API ANTICIPATES THIS SPURIOUS PHASE FROM THE SETTINGS OF THE F REGISTER AND COMPENSATES FOR IT.

IT MAKES THE INTEGRATOR START FROM A LOWER LEVEL SO THAT ITS OUTPUT WILL NOT BE EFFECTED BY THIS EXTRA PHASE.

HOWEVER SIDEBAND SUPPRESSION IS LIMITED.

CURRENTLY ~ 50-60 dBC. (dBC = dB with respect to carrier)

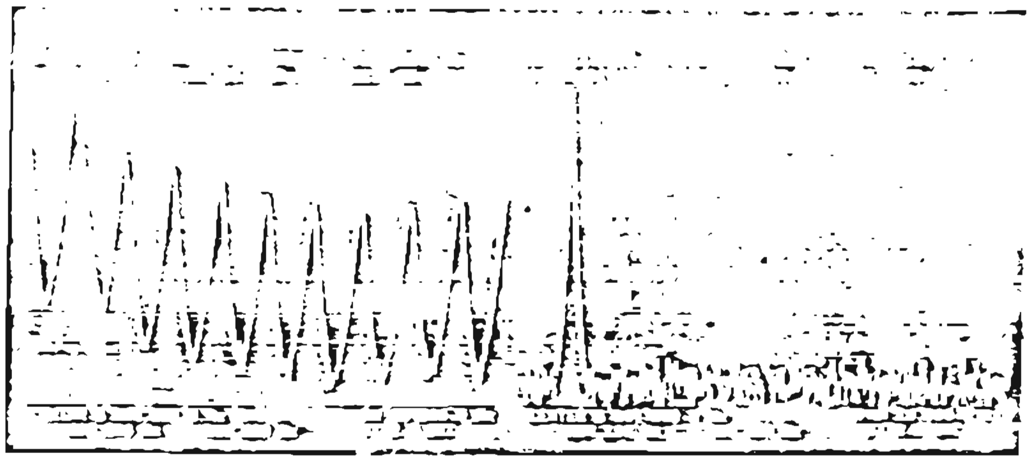


Fig. 4. Spectrum [illegible] the effect of analog phase interpolation (API). [illegible] at left, which shows the spectrum of a 5.001-MHz sine-wave output without the use of API. Photo at right shows the spectrum of the same output with API.

100-kHz reference pulse turns it off. Thus, the level of the integrator output after the ramp up is proportional to the phase difference between VCO/N and the 100-kHz reference. This level is retained by the sample-and-hold circuit and passed to the VCO. Following the sampling, the bias signal turns on the bias current which ramps the integrator down to the starting level.

When the desired output frequency is not an integral multiple of the reference frequency, the VCO/N pulse gains a fractional part of a cycle with respect to the reference each time it occurs. Thus, until a pulse deletion occurs, the phase detector pulse becomes wider and the integrator ramps up further during each succeeding reference cycle. It is therefore necessary to ramp down further each time so the integrator ramp up will always end at the same level.

The necessary change in ramp-down current is controlled by the API switches which are in turn controlled by the phase accumulator. At the end of each reference cycle, the number stored in the accumulator corresponds to the difference in phase between the VCO/N pulse and the reference. Each of the top five decimal digits of this number controls one of the five API bias switches, and turns on the switch for a period inversely proportional to the numerical value of the digit. The bias current is thus adjusted according to the phase difference.

Since the number in the phase accumulator controls the phase of the VCO through the action of the API currents, the VCO phase can be changed arbitrarily by changing this number. Hence, by adding an increment to the F register for one reference cycle and

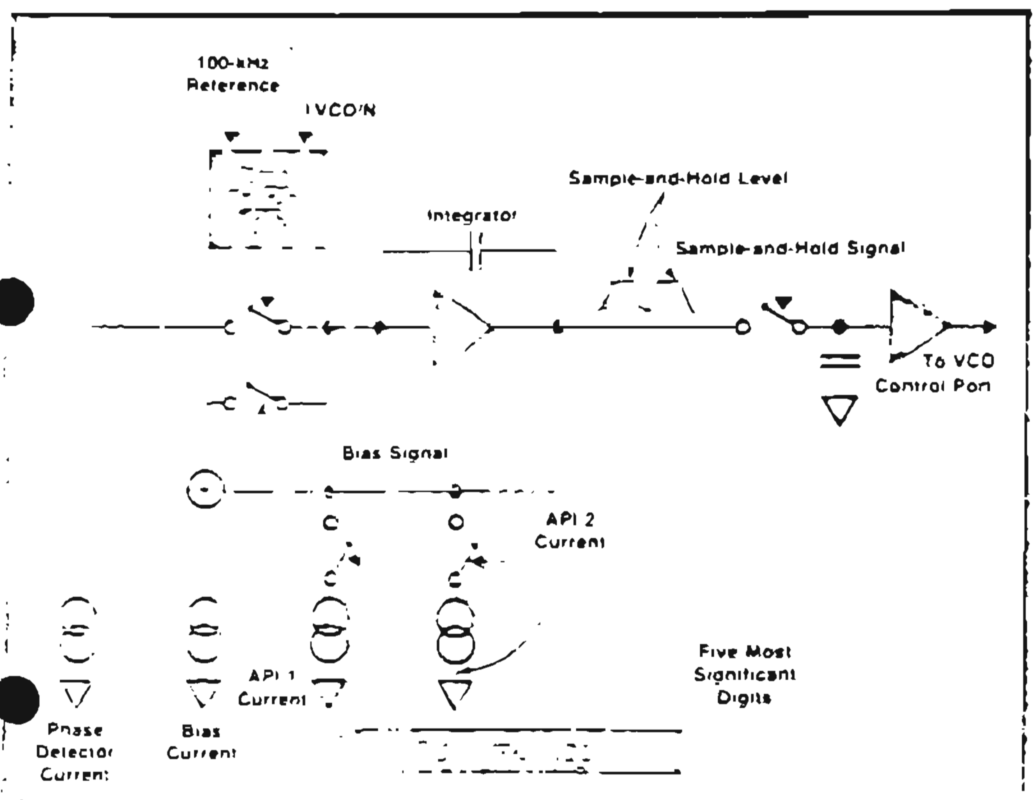


Fig. 5. Details of analog phase interpolator.

SPECIFICATIONS

HP Model 3325A Synthesizer/Function Generator

Waveform Characteristics

DC Offset

Phase Offset

Sweepwise Amplitude Modulation

Phase Modulation

Frequency Sweep

Auxiliary Outputs

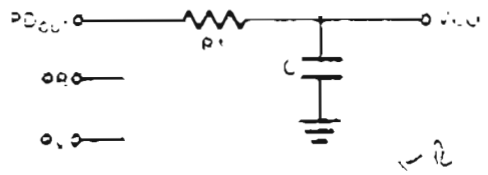
HP-IB Control

Option 001 High Stability Frequency Reference

Option 002 High Voltage Output

Options

A)

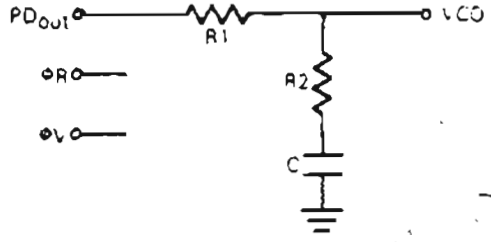


$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NR1C}}$$

$$\zeta = 1/2\,\omega_N\,(N/K_\phi K_{VCO})$$

$$F(s) = \frac{1}{R1CS + 1}$$

B)

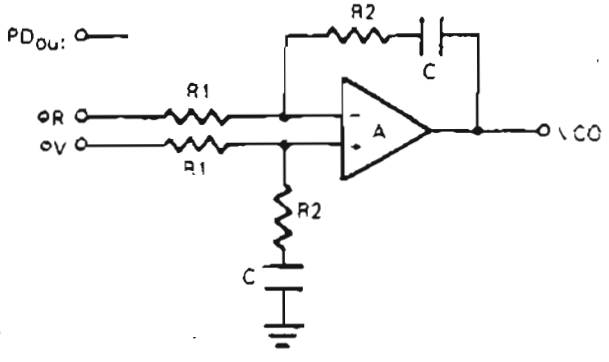


$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NC(R1 + R2)}}$$

$$\zeta = 1/2\,\omega_N\,(R2C + N/K_\phi K_{VCO})$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

C)



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large then

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE Sometimes R1 is split into two series resistors each R1 – 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N.

DEFINITIONS. N = Total Division Ratio in feedback loop

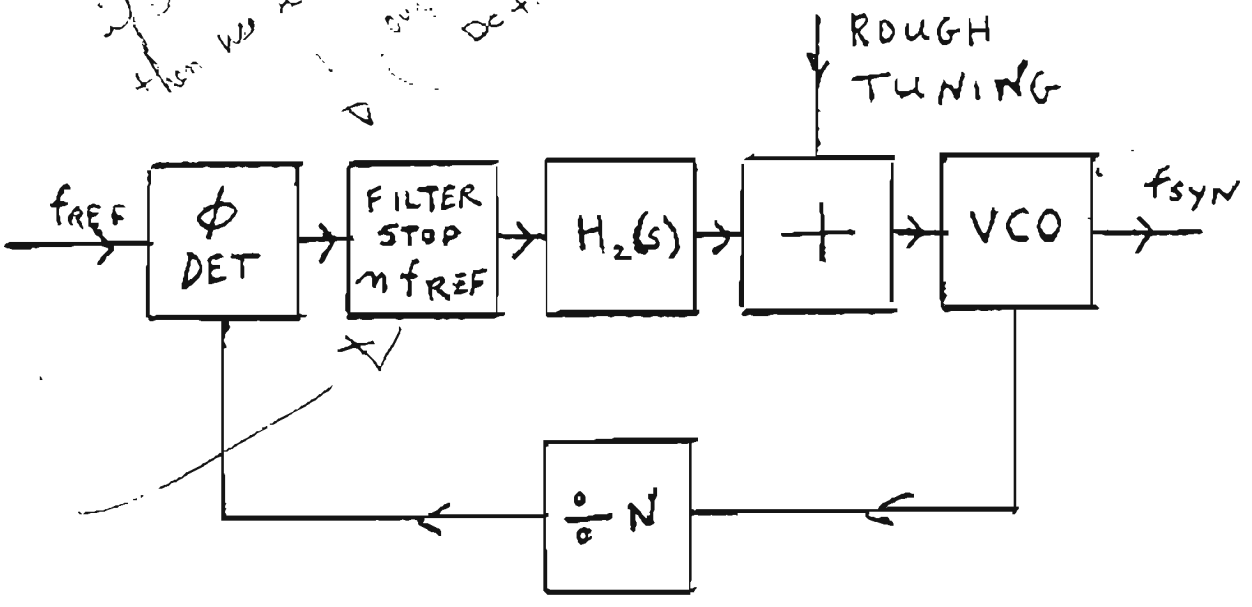
$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N = (2\pi/10)\,f_r$ (at phase detector input)

$\zeta = 1$



NEW IN THIS DIAGRAM:

1. SHARP LOWPASS FILTER OR TRAP TO REJECT FREF AND/OR ITS HARMONICS.

2. DC FOR ROUGH TUNING OF VCO.

NOTE:

AS N VARIES, SO DOES THE LOOP GAIN K.

THIS VARIES w_n, ETC.

SOME REAL WORLD PROBLEMS:

. NOISE FROM REFERENCE SOURCE

. NOISE FROM VCO

. NOISE FROM AMPLIFIER

. SPURIA FROM PHASE DET.

. EXTRA DELAYS AND PHASE SHIFTS

. NONLIN. VCO CHARACTERISTIC

PROBLEM (Synthesizer):

Design a frequency synthesizer covering the range of 10.89 to 12.5 MHz in 0.5 KHz steps. Programming is by a microprocessor. In particular, do the following:

1. Choose an appropriate synthesizer chip.
2. Is a dual-modulus prescalar desirable? If so, which chips?

   P = ?

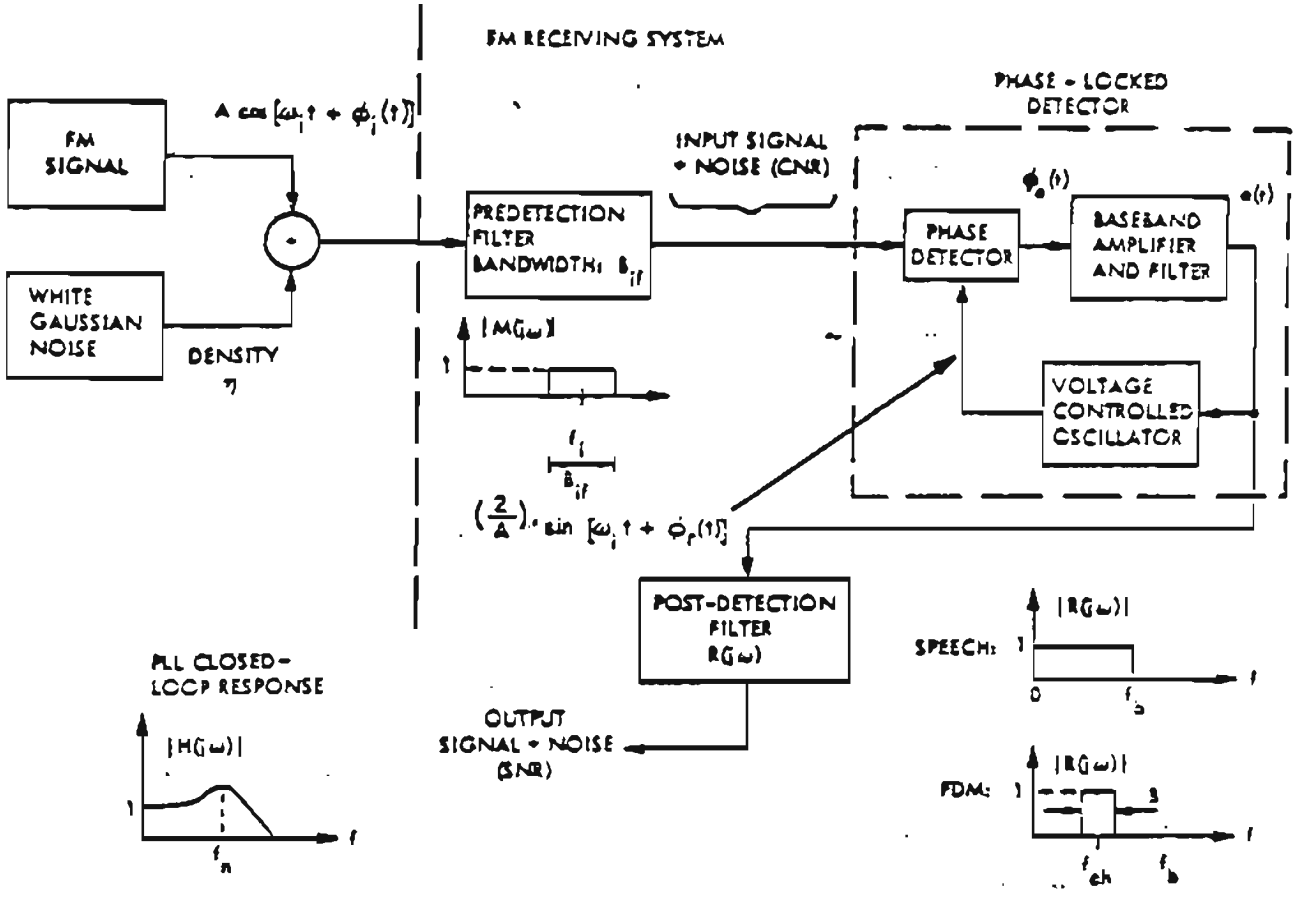
3. Do you meet the conditions of $N > A$, $A < P$?
4. What is the range of N_{total} in your design?
5. Do you meet the delay requirement for the dual-modulus mode?
6. Choose the frequency of the reference oscillator and the $\div$ R
7. What are the values of K_1, K_3?
8. What would you choose K_2 as?
9. What ζ did you choose? (range)
10. What is w_n, w_x (0dB crossover frequency), a, b?
11. Design the loop filter
12. How much time does it take for a change of one increment for the freauency to be at 90% of increment?
13. What is your Hold-in Range?
14. What is your lock-in range?
15. Are acquisition aids needed? If yes, design one.
16. What is the highest spurious level at the output of the phase detector? The input to the VCO? The output of the VCO?
17. What is the power consumption of the synthesizer?

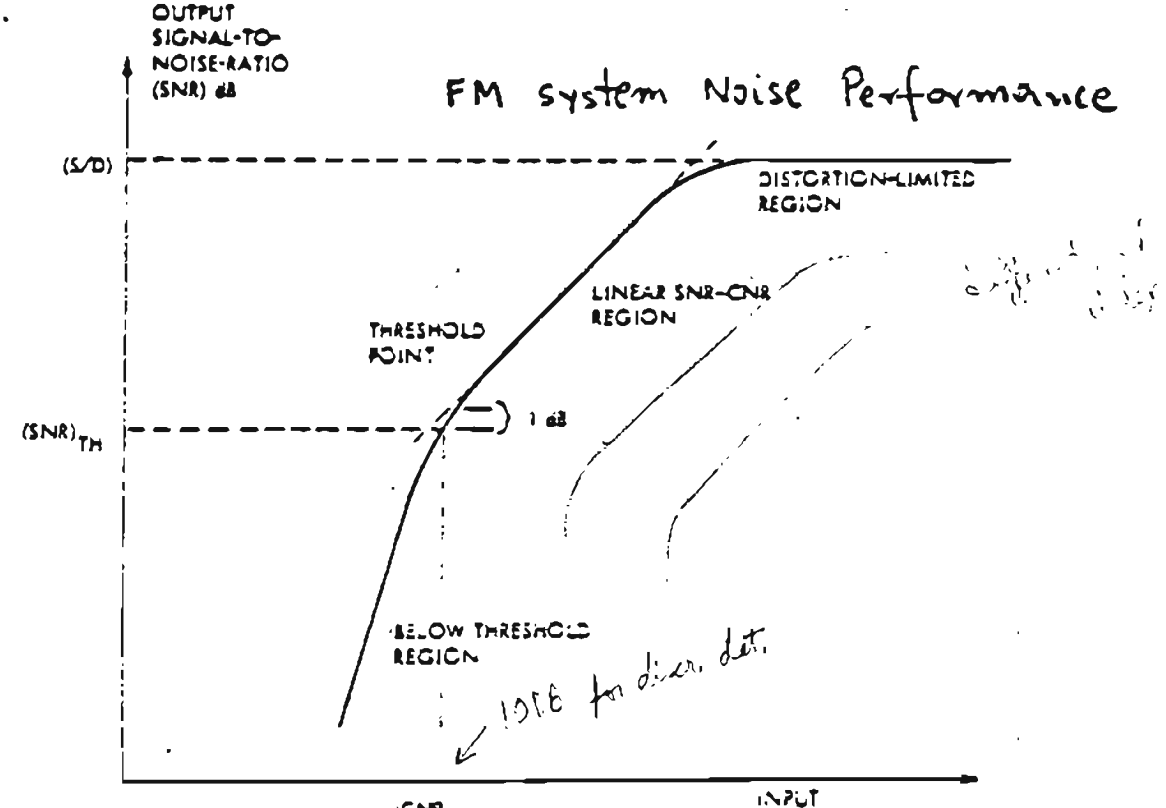
FM DETECTION

Reference: J. Klapper and J. Frankle
PHASE-LOCKED AND FREQUENCY-FEEDBACK SYSTEMS
Chapter 6, Academic Press, 1972.

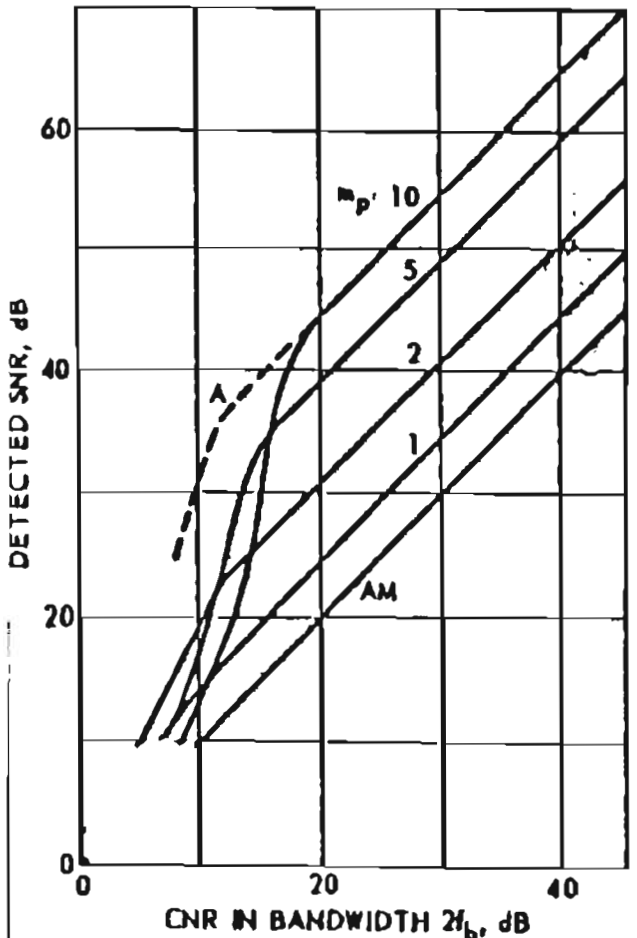
Dr. Jacob Klapper

FM DEMODULATION





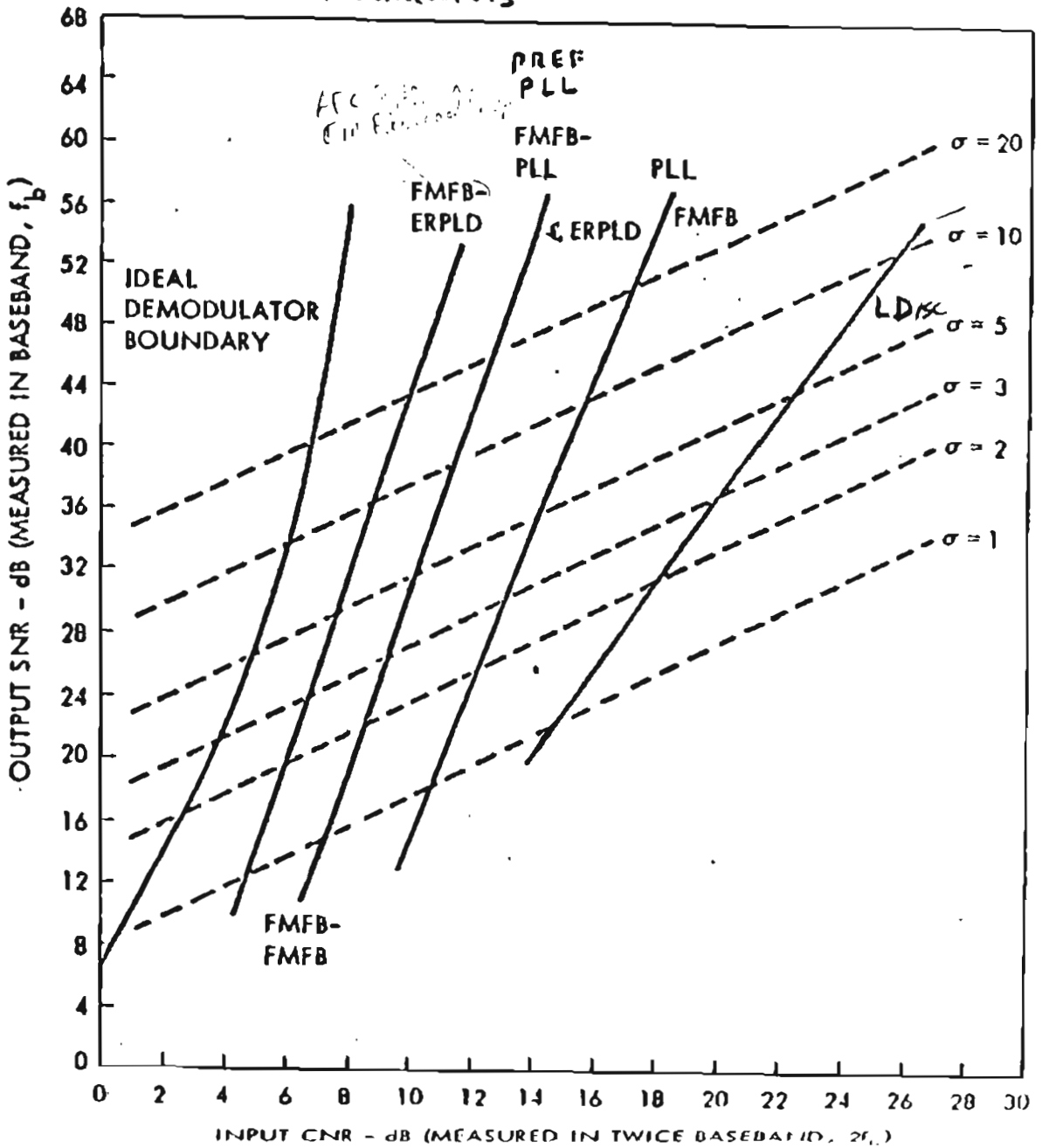
Family of FM Noise Performance Characteristics

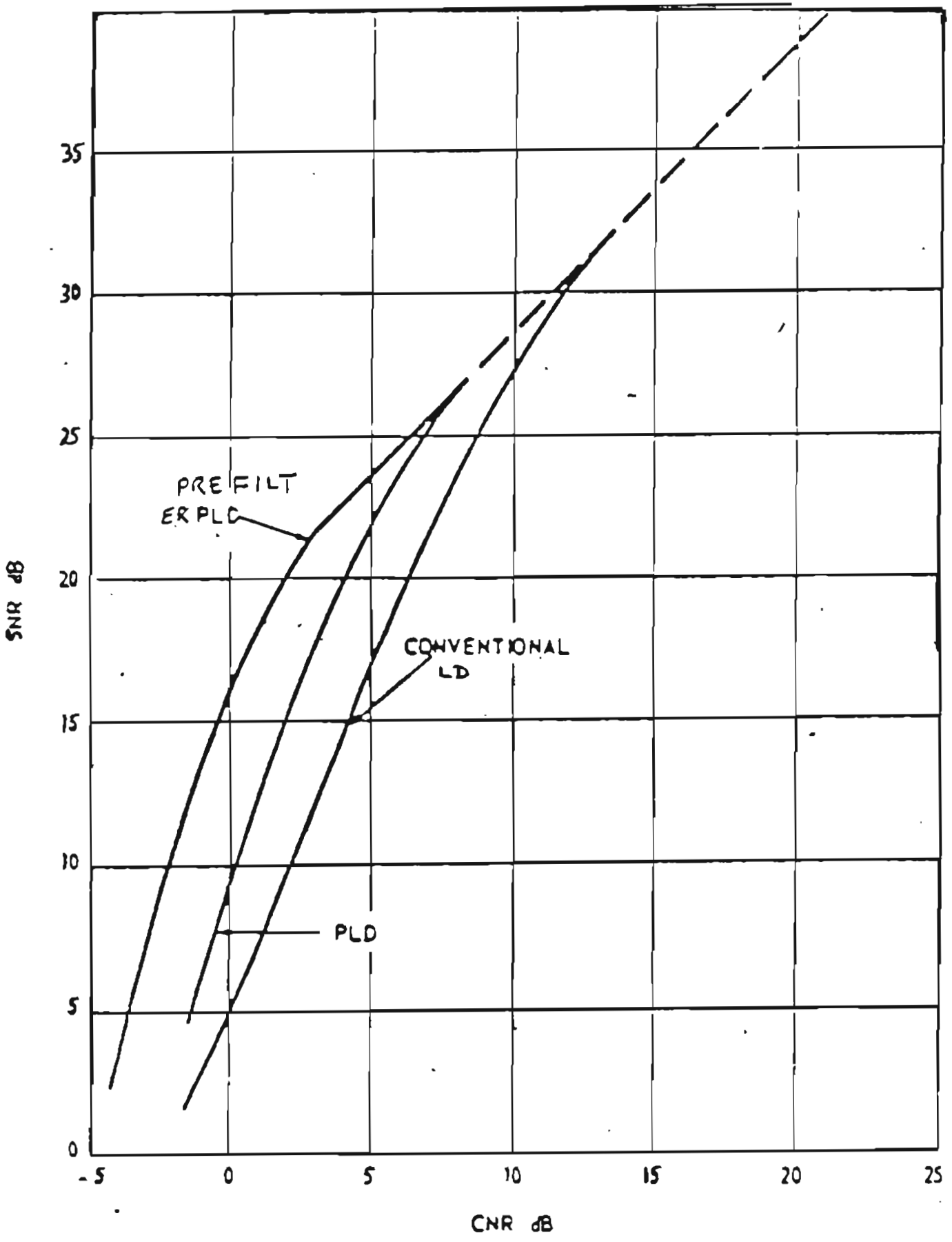


m_p = Peak Modulation Index

f_b = Top baseband frequency

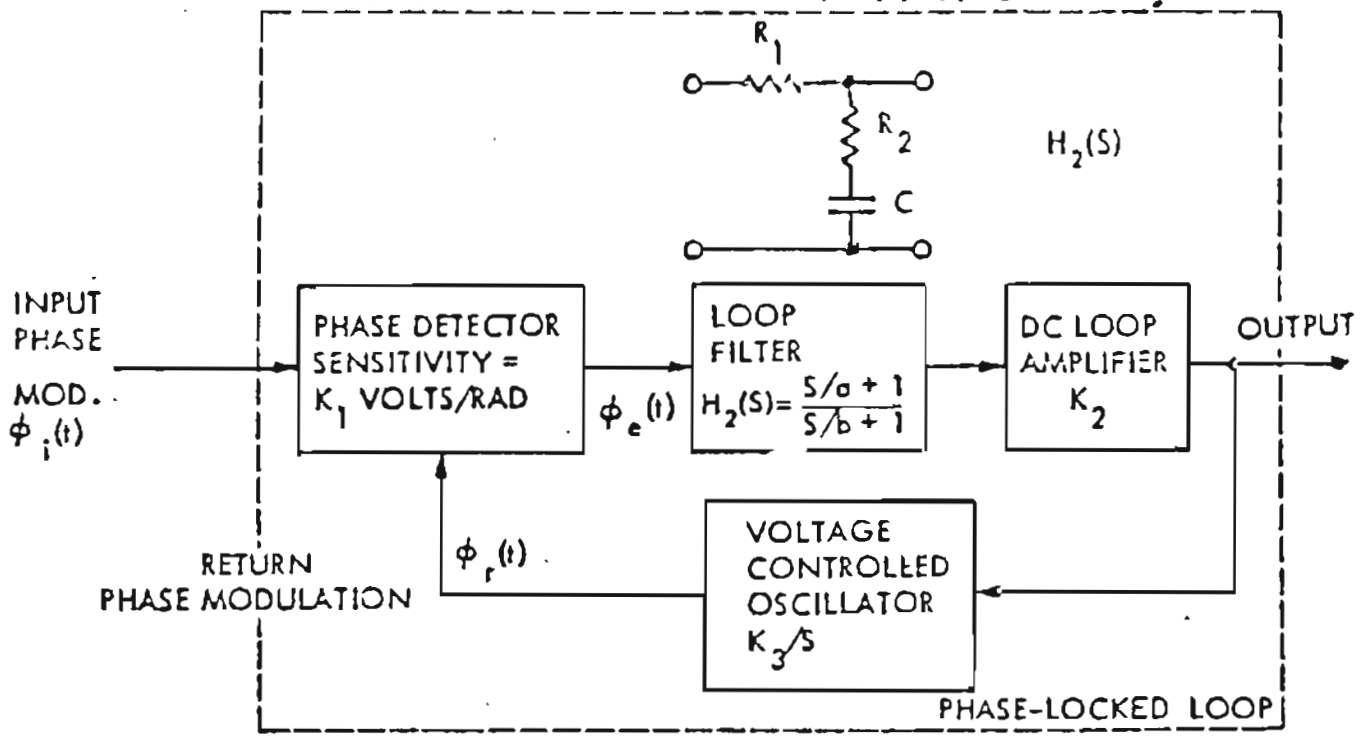
Threshold Performance of Various FM Demodulators





PLL AND ERPLL PERFORMANCE FOR ANALOG SIGNALS

PLL BLOCK DIAGRAM INCLUDING LOOP FILTER



LOW - THRESHOLD DESIGN

CONDITIONS : WIDE PREDETECTION FILTER

NOISE-LIKE SIGNAL (FDM, VOICE, ETC.

NOISE AND SIGNAL STATIST. INDEPENDENT

$\overline{\phi_e^2(t)} = \overline{\phi_{es}^2(t)} + \overline{\phi_{en}^2(t)} = 0.25$ AT THRESHOLD

TO BE OBTAINED AT LOWEST CNR INPUT

USE 2nd-ORDER LOOP.

$$H(S) = \frac{\frac{S}{a}+1}{\frac{S^2}{Kb}+\left(\frac{1}{K}+\frac{1}{a}\right)S+1} = \text{CLOSED-LOOP RESPONSE}$$

WE HAVE a, b, K FOR OPTIMIZATION

FOR $a \ll K$ (O.K. IN PRACTICE)

WE HAVE ONLY a, bK FOR OPTIMIZATION

PROCEDURE

STEP 1 : MINIMIZE B_n FOR FIXED Kb

(MINIMIZES $\overline{\phi_{en}^2(t)}$ WITH $\overline{\phi_{es}^2(t)} \approx$ CONSTANT)

$\frac{\partial B_n}{\partial a}$ GIVES $a = \omega_n = \sqrt{Kb}$

$B_n = \frac{\omega_n}{2}$ AND $\xi \approx \frac{1}{2}$

$$\therefore \quad H(S)_{OPT} = \frac{\frac{S}{\omega_n} + 1}{\left(\frac{S}{\omega_n}\right)^2 + \frac{S}{\omega_n} + 1}$$

GIVES SHAPE OF RESPONSE

STEP 2 : MINIMIZE $\overline{\phi_e^2(t)}$

$\frac{d}{d\omega_n}\overline{\phi_e^2(t)} = 0$ GIVES $\overline{\phi_e^2(t)} = \frac{5}{4}\overline{\phi_{rn}^2(t)}$

$a = \omega_n = (20y)^{1/4}$ WHERE $y = \int_0^{f_b} \omega^4 W_{\phi_i}(f)\,df$

and $B_n = \left(\frac{5}{16\,\overline{\phi_e^2(t)}}\,y\right)^{1/4}$

$W_{\phi_i}(f)$ = POWER SPECTRAL DENSITY OF $\phi_i(t)$

WE NOW KNOW ω_n , a, $\sqrt{Kb}$

STEP 3 :

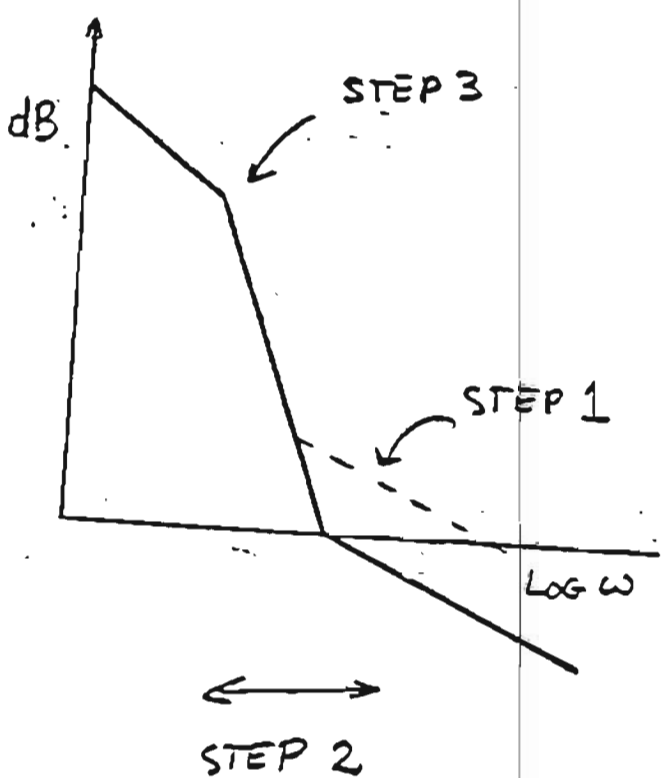
CHOOSE $b <$ LOWEST BASEBAND FREQUENCY

AND CONSISTENT WITH "HOLD-IN" RANGE.

$\therefore$ K ALSO SPECIFIED

OPEN LOOP RESPONSE

OPTIMIZATION STEPS



EXAMPLE

GIVEN :

600 CHANNEL FDM/FM

BASEBAND 60 KHZ – 2.54 MHZ (FLAT)

RMS FREQ. DEVIATION 7.1 MHZ

PEAK TO RMS 10 dB

FOR THIS CASE :

$W_{\dot{\phi}_i}$ = PSD OF BASEBAND = η_m

$$\therefore W_{\phi_i} = \frac{\eta_m}{\omega^2}$$

$$y = \frac{1}{3}(2\pi)^2 \eta_m f_b^3$$

BUT $$\eta_m = \frac{(\Delta\omega_{RMS})^2}{f_b}$$

$$\therefore y = \frac{1}{3}\omega_b^2 (\Delta\omega_{RMS})^2 = 167 \times 10^{27}$$

THEN

$$a = 43 \times 10^6 \text{ RAD/SEC}$$

$$b = 376 \times 10^3 \text{ RAD/SEC} \quad (2\pi \times 60 \text{ KHz})$$

$$K = 4.9 \times 10^9 \text{ SEC}^{-1}$$

$$(CNR_{IF})_{TH} = 3.3 \text{ dB} \quad (\text{SEE KLAPPER \& FRANKLE})$$

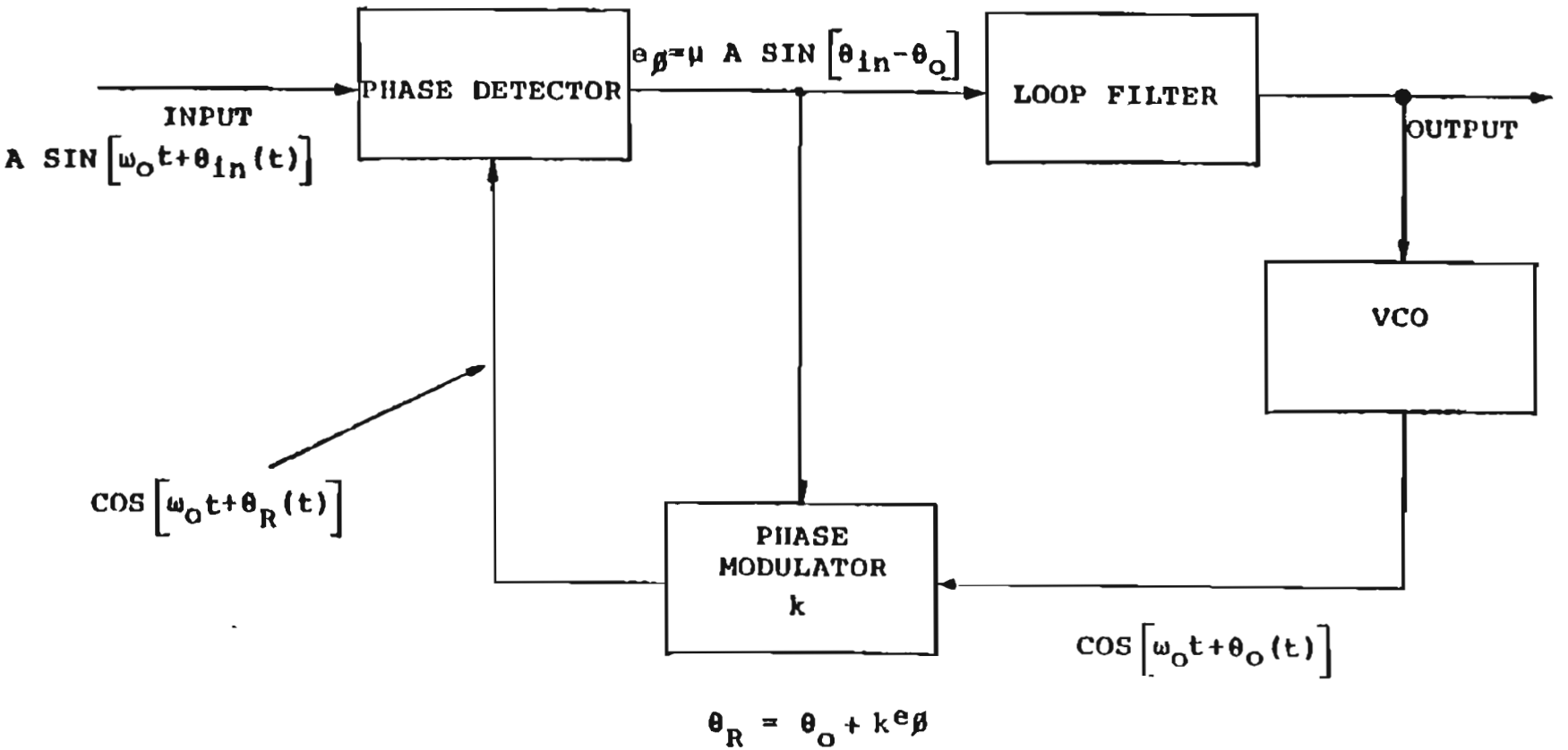


Figure 3. The ERPLD using phase feedback

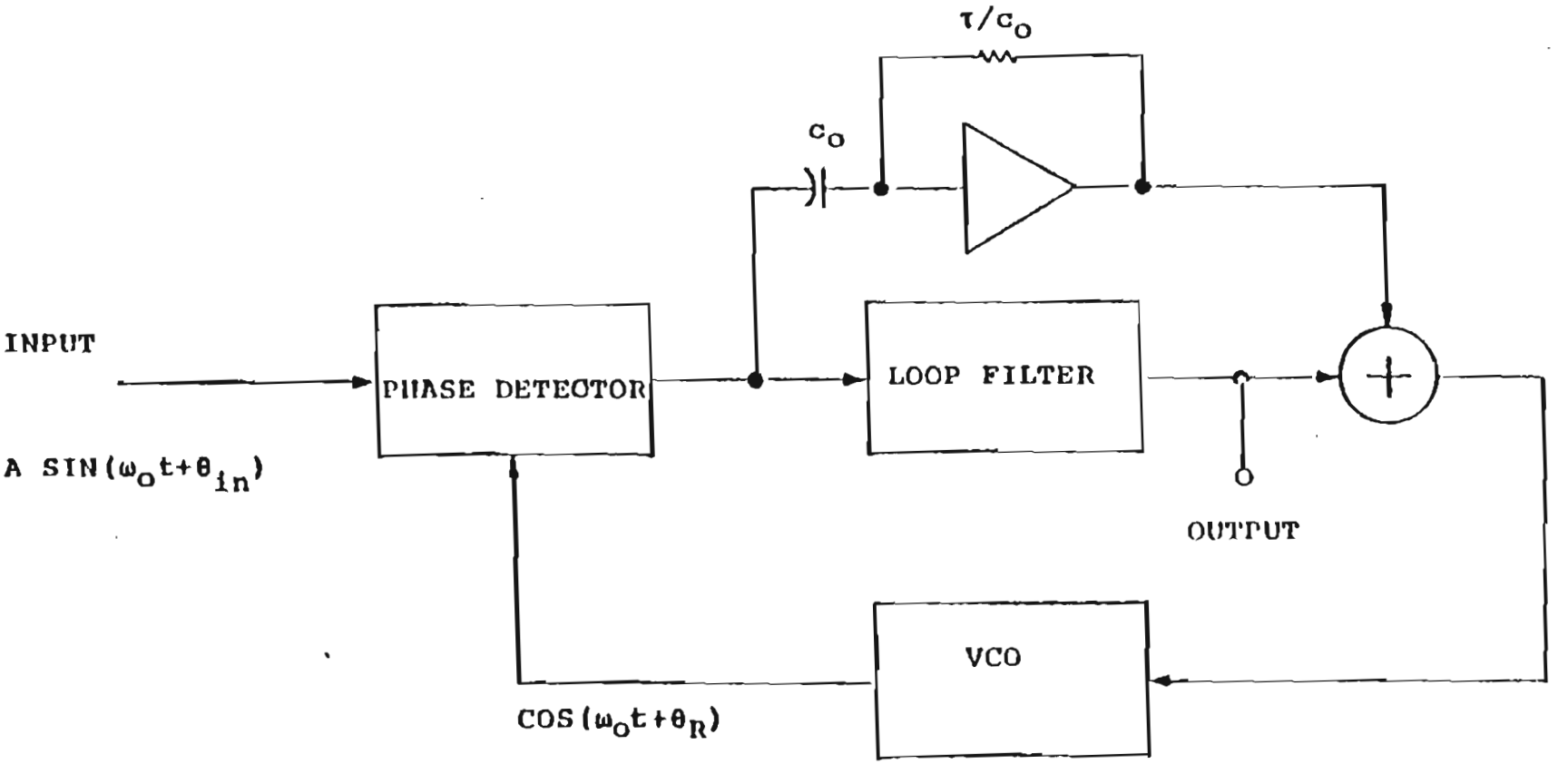


FIGURE 2. PLL WITH THE AUGEMENTED LOOP FILTER

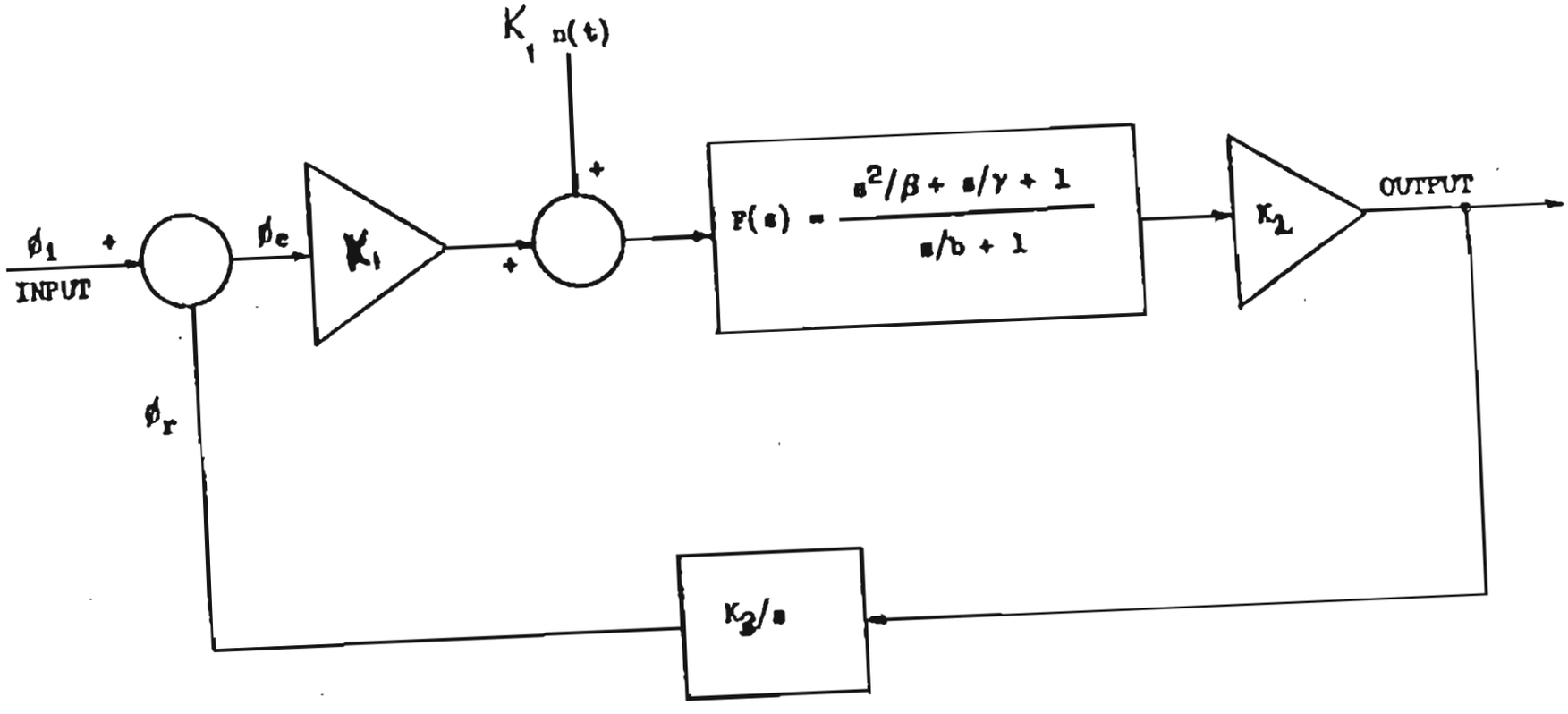
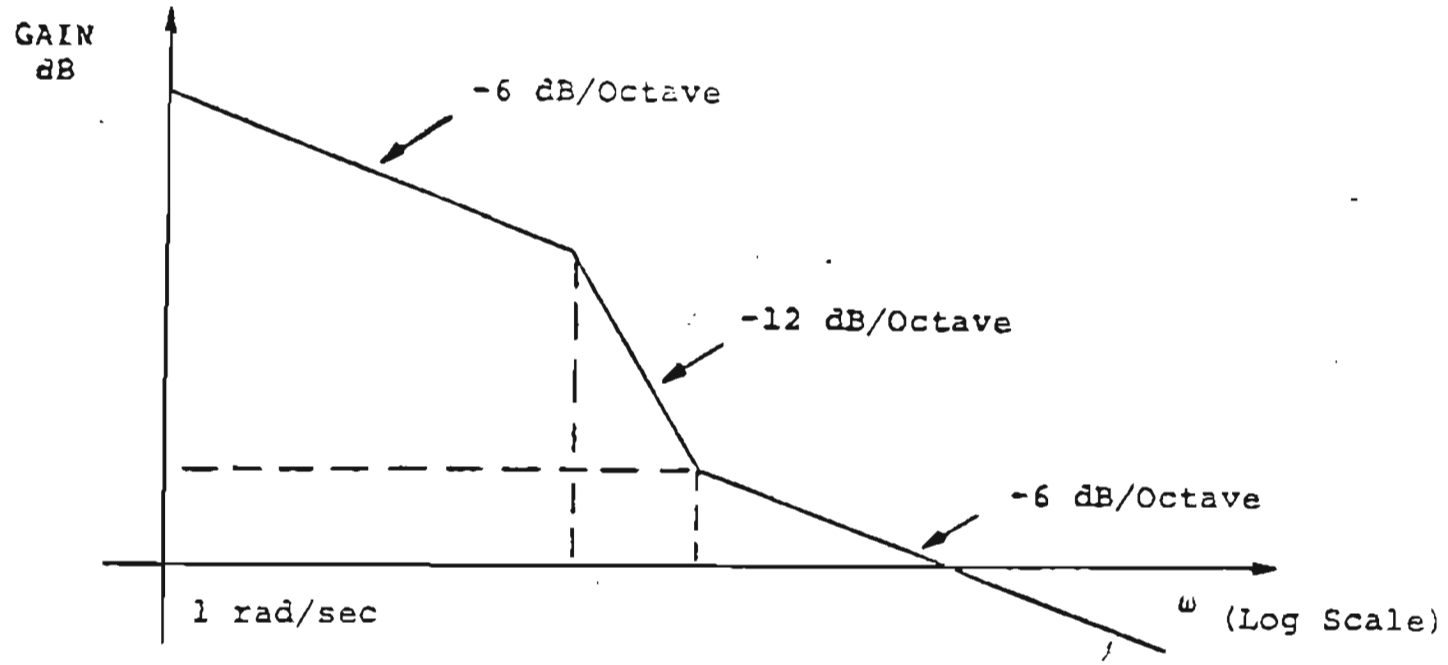
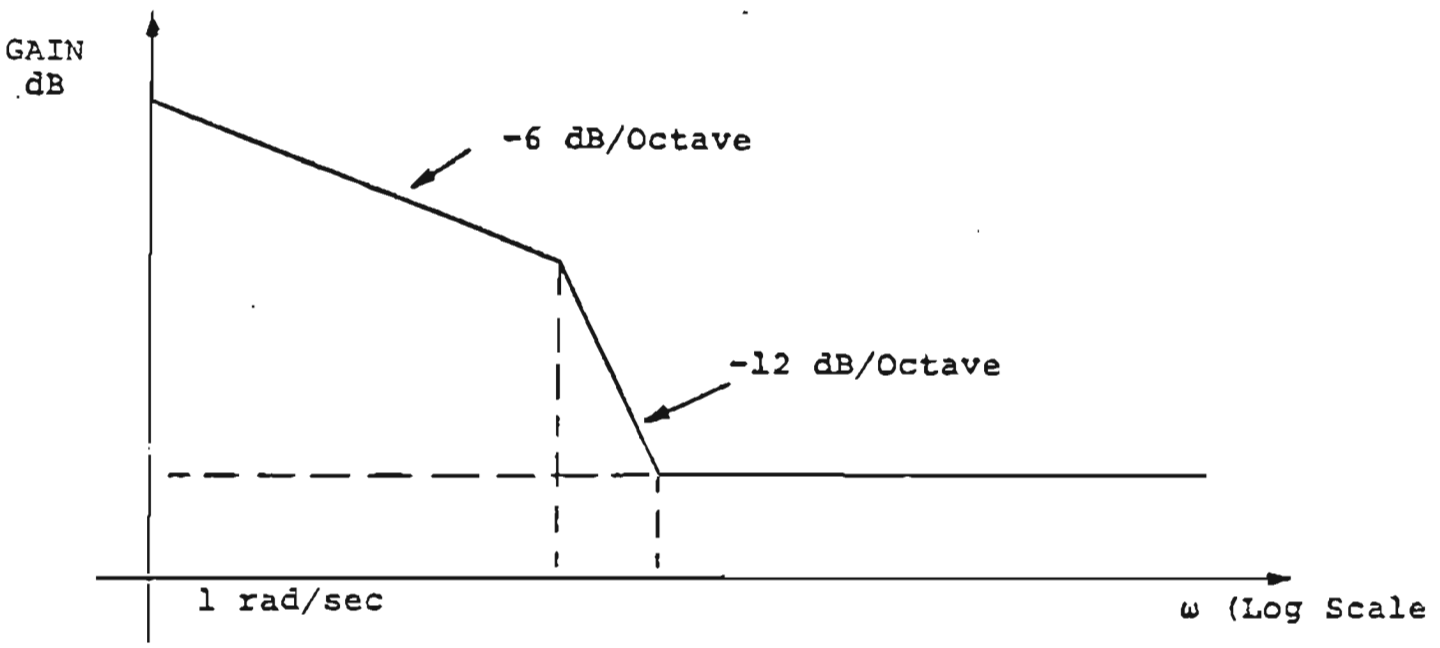


FIGURE 3. LINEAR EQUIVALENT MODEL OF THE GENERALIZED SECOND-ORDER PLL. (or ERPLD)



(a)



(b)

Typical Open-loop Amplitude Response (asymptotic).
(a) Conventional second-order, (b) ERPLD

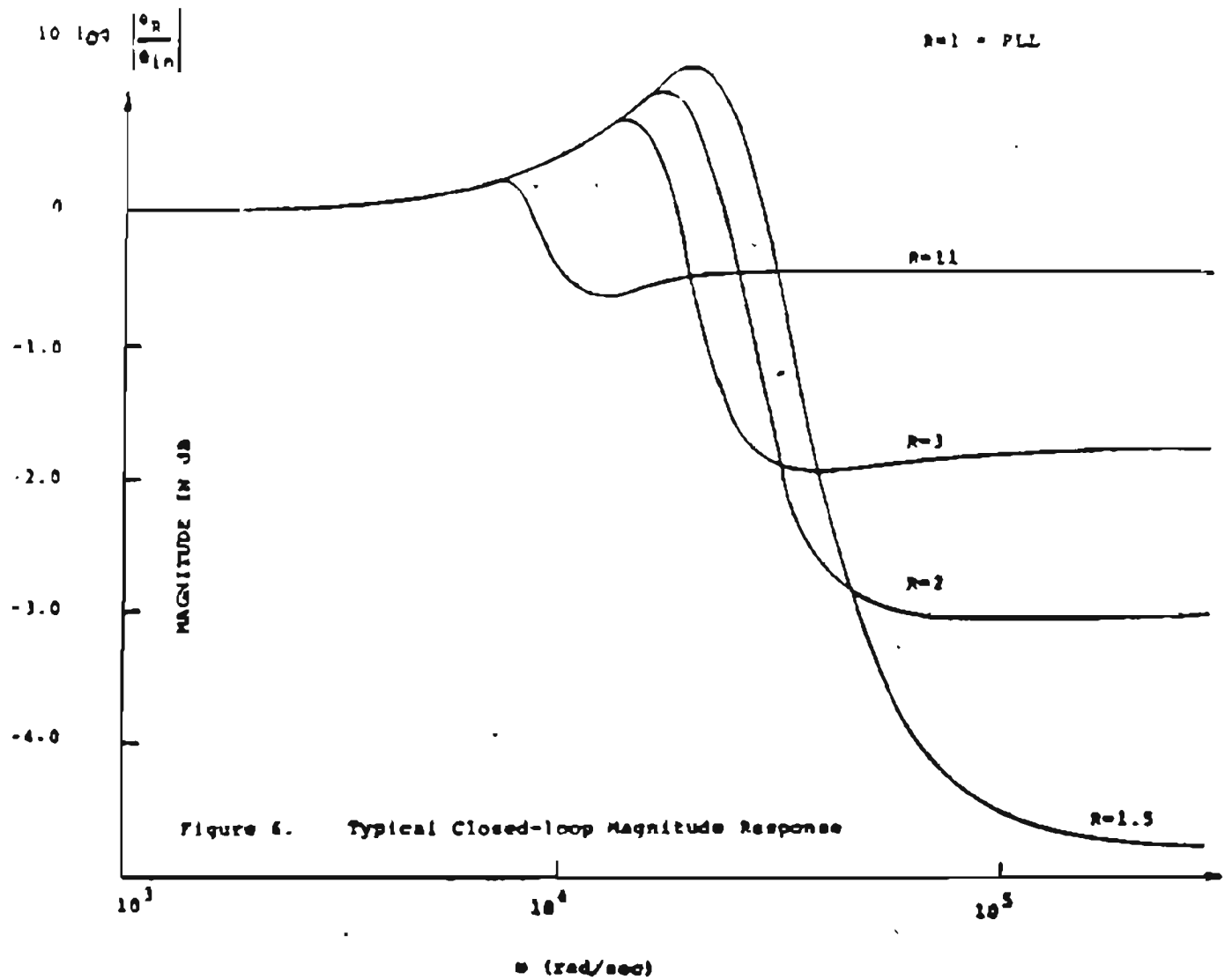


Figure 6. Typical Closed-loop Magnitude Response

R = 1+AMX. LOOP GAIN

Typical Closed-loop Magnitude Response

DESIGN INCLUDING PREDETECTION FILTER

ASSUME

PREDETECTION FILTER SHARP

BANDWIDTH PER CARSON'S RULE : $B_{IF} = 2(\Delta f + f_b$

RULE OF THUMB

ADVANTAGE EXISTS IF $\frac{B_{IF}}{y^{1/4}} < 5.8$

USE LOOP FILTER OF FORM

$$H_2(S) = \frac{\frac{S^2}{\beta} + \frac{S}{\gamma} + 1}{\frac{S}{b} + 1}$$

TO GET β, γ, b, K USE COMPUTER PROGRAMS (INCLUD

FEED IN AS FOLLOWS :

OMEGA

SEE APPENDIX A

OMEGB

DELSQ

NU = 0.25

BP

EXAMPLE

GIVEN :

600 CHANNEL FDM/FM

BASEBAND : 60 KHZ — 2.54 MHZ

RMS FREQ. DEVIATION : 7.1 MHZ

PEAK TO RMS = 10 dB

IF BANDWIDTH = 50 MHZ

THEN

$\beta = 2.83 \times 10^{15}$ $(\text{RAD/SEC})^2$

$\gamma = 6.75 \times 10^{7}$ RAD/SEC

$b = 6.38 \times 10^{6}$ RAD/SEC

$K = 4.75 \times 10^{8}$ SEC^{-1}

$(\text{CNR}_{IF})_{TH} \approx 1 dB$

(COMPARE AGAINST 3.3 dB OF EARLIER DESIGN)

DETECTION OF TONE MODULATION

ϕ_e is also sinusoidal.

LOSS OF LOCK OCCURS PRIMARILY AT PEAK OF PHASE ERROR.

$$\left|\phi_{es}\right|_{peak} \approx \frac{\Delta w_p \; w_t}{Kb}$$

Δw_p = PEAK FREQ. DEVIATION: w_t = FREQ. OF TONE.

WE TREAT $\left|\phi_{es}\right|_{peak}$ as a "bias". Noise peaks exceeding $\frac{\pi}{2} - \left|\phi_{es}\right|_{peak}$ will cause loss of lock.

WHEN EXCEEDED WITH PROBABILITY 0.0015 THEN WE HAVE "THRESHOLD".

Setting $\frac{\partial (CNR)_2 f_L}{\partial B_n} = 0$ we get

$$\left(\frac{B_n}{f_L}\right)_{opt} = \left(\frac{10\pi \Delta\omega_p \omega_T}{\omega_L^2}\right)^{1/2} \quad \text{where } B_n = \frac{\sqrt{K_L}}{2}$$

= Loop noise bandwidth, and f_L = Top baseband freq.

AS BEFORE, $a = \sqrt{Kb}$ AND

b = LOWEST BASEBAND FREQ. (OR TO SATISFY HIR AND P IR

NOTE: ϕ_e DUE TO OFFSETS ARE ALSO TREATED AS A "BIAS", REDUCING FROM THE AVAILABLE $\frac{\pi}{2}$ RADIANS.

EXAMPLE:

BASEBAND = 300 - 4,000Hz, VOICE

PEAK SIGNAL DEVIATION = 10KHz

HOWEVER, DESIGN PLL AS IF IT WERE TO DETECT A 1KHz TEST TONE.

SOLUTION

B_n = 17.7 KHz $\qquad\qquad$ $a = 2B_n$ = 35,400 RPS

b = 1880 RPS (LOWEST BASEBAND FREQ.)

$K = \frac{4Bn^2}{b} = 6.6 \times 10^5$

ERPLD FOR TONE DETECTION

CONSIDER TONE CAN BE ANYWHERE OVER SPECIFIED BASEBAND.

$$\theta_{in}(t) = \frac{\Delta f}{fm} \sin w_m t$$

$$\theta_{es} \Big|_{peak} \quad \text{occurs at } w_n$$

$$\theta_{es} \Big|_{peak} = \frac{\pi}{2} \frac{\Delta f}{Bn} \left(1 + \frac{1}{4\zeta^2}\right) \quad \text{RAD. FOR PLL}$$

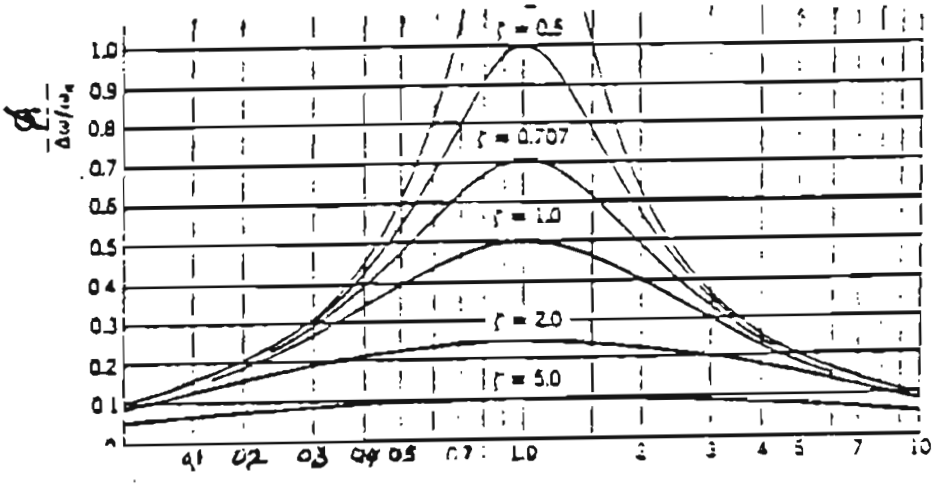
and

$$\theta_{es} \Big|_{peak} = \frac{1}{R} \frac{\pi}{2} \frac{\Delta f}{Bn} \left(1 + \frac{1}{4\zeta^2}\right) \quad \text{RAD. FOR ERPLD}$$

WHERE R = 1 + GAIN AROUND DIFFERENTIATOR LOOP

HOWEVER R CAN INCREASE B_n.

θ_e FOR TONE MODUL →



ANALYTICAL OPTIMIZATION FOR LEAST NOISE FINDS

$$R_{opt.} = \frac{1}{2}\left(1 + \frac{\Delta w}{\emptyset_p BIF}\right) + \frac{1}{2}\left[\left(1 + \frac{\Delta w}{\emptyset_p BIF}\right)^2 - \frac{3\,\Delta w}{\emptyset_p BIF}\left(1 - \frac{1}{4\zeta^2}\right)\right]^{\frac{1}{2}}$$

TYPICALLY R == 2.

EXAMPLE:

SEE BRUNO, MOSER, AND KLAPPER, "IMPROVED FM DETECTION USING AN EXTENDED RANGE PHASE LOCK DETECTOR", 1978 NAT. TELECOMM. CONF.

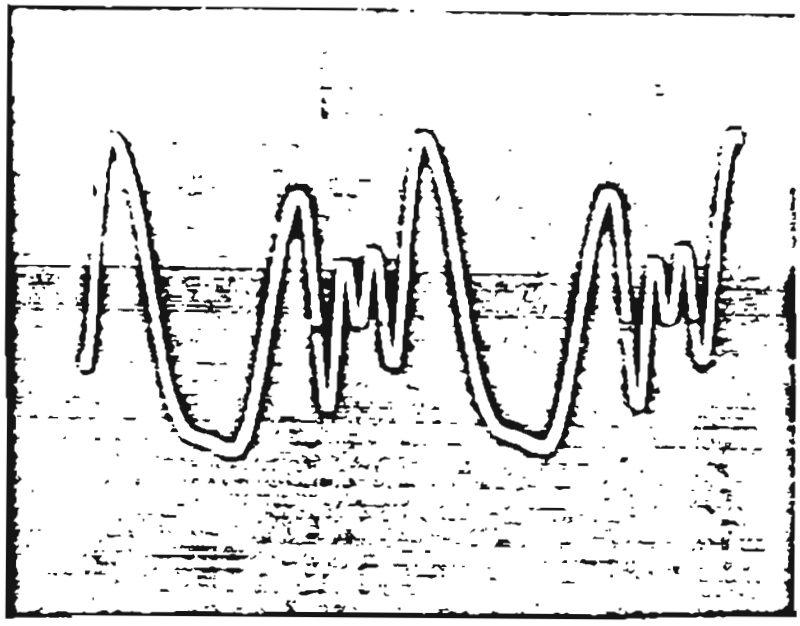


Figure 14. PLL Output, f_m=10KHz, Δf=75KHz

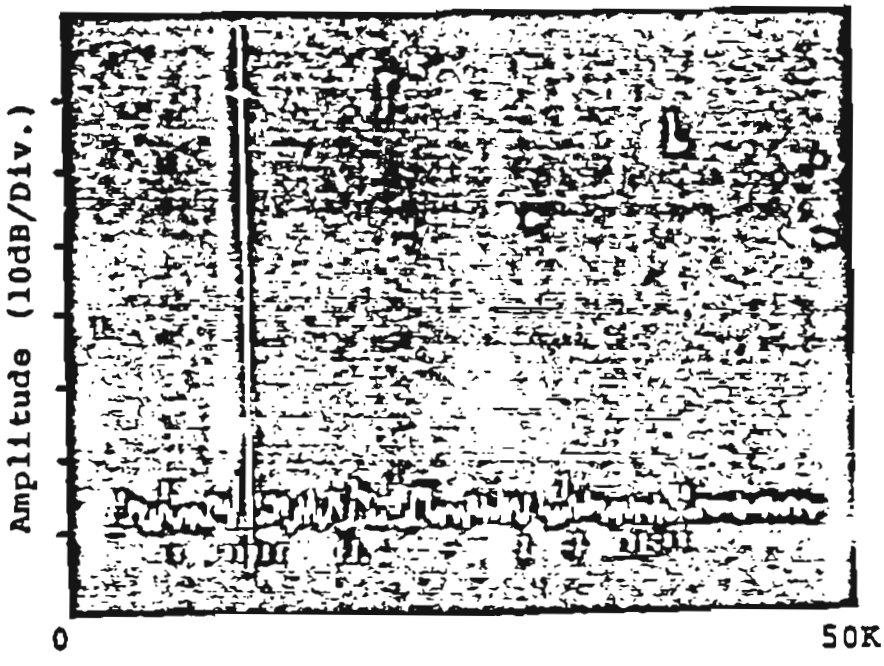


Figure 15. PLL Output Spectrum

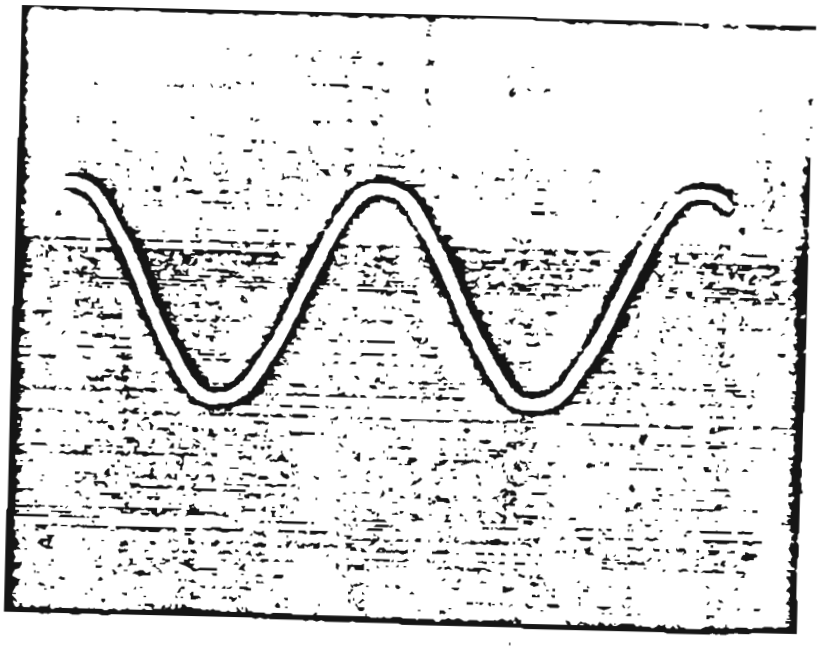


Figure 16. ERPLD Output, f_m=10KHz, Δf=75KHz

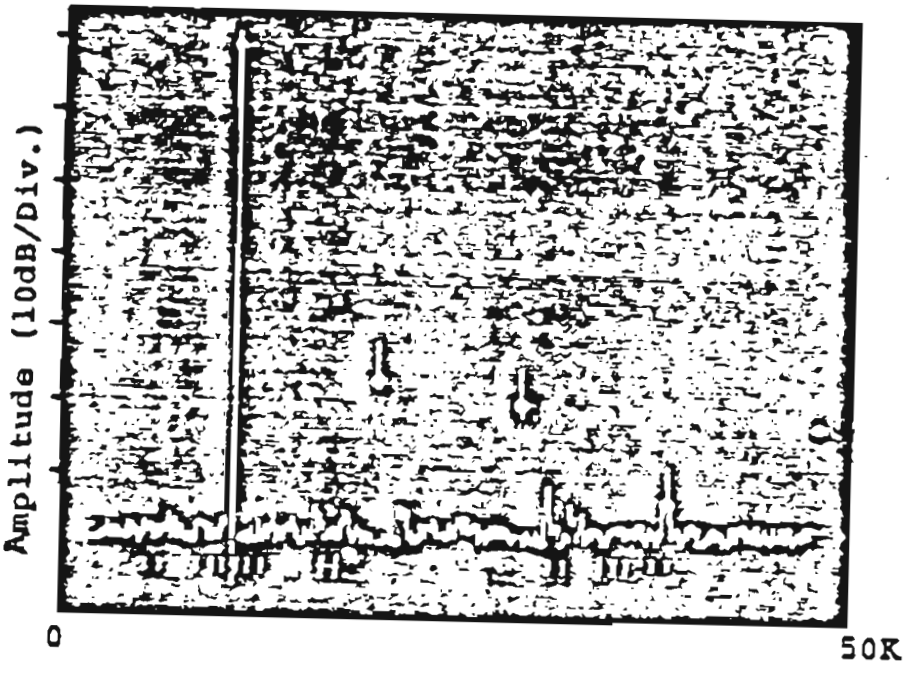


Figure 17. ERPLD Output Spectrum

WHAT CAN GO WRONG?

PHASE SHIFTS AROUND LOOP DUE TO EXTRANEOUS POLES AND TRANSPORT DELAY (INCREASE Bn)

INSUFFICIENT POST-PLL FILTERING (REDUCES SNR)

DISTORTION (REDUCES SNR)

VCO WITH LARGE FREQ. UNCERTAINTY OR NOISY
(LARGE $\emptyset_o$ INCREASES THRESHOLD, REDUCES GAIN, AND INCREASES DISTORTION)

PHASE DETECTOR SATURATES

PHASE DETECTOR OTHER THAN MULTIPLIER TYPE

EFFECT OF LIMITER

LIMITER INCREASES THRESHOLD ~ 1 dB.

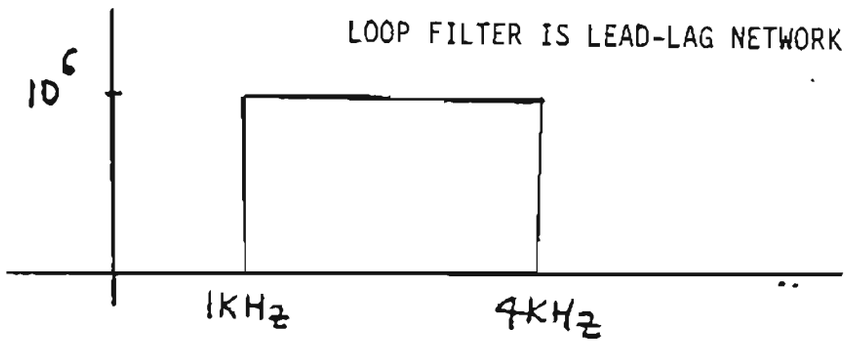
AMPLITUDE VARIATIONS (OF INPUT) EFFECT Ø DET. SENSITIVITY AND (THEREBY) K.

AGC IS PREFERRED WHERE THRESHOLD IS CRITICAL.

Ø DET. SATURATING FROM INPUT SIGNAL IS EQUIVALENT TO LIMITER.

PROBLEMS: FM Detection

I. Design a PLL for minimum threshold for an FM signal having a noise-like baseband of power spectral density shown:



Give the following

1. The shape of the desirable asymptotic open loop response.

2. The values for all corner frequencies.

3. The sensitivities of the blocks in the loop

4. The closed-loop natural frequency.

The closed-loop damping factor

Answers: a=64 KRPS, b=6.3 KRPS, f_n=10 KHz, K=6.5x10^5, ζ=0.5

II. Repeat for a test tone, as follows:

Baseband 300-4000 Hz

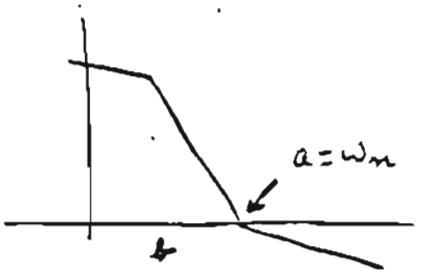
Test tone frequency 1 KHz

$$\frac{\Delta\omega_p}{\omega_f} = 1$$

Answers: B_n=11.4 KHz, K=275,000 b=1880 a=22,800

SOLUTIONS (FM DETECTION)

PROBLEM I:



$\xi = \underline{0.5}$ $\quad \omega_n = a$ $\quad b = \underline{2\pi \times 10^3 \text{ RPS}}$ $\quad Kb = a^2$

$a = ?$ $\quad K = ?$

$a = (204)^{1/4}$, $\quad Y = \frac{1}{3}(2\pi)^2 \eta_m f_b^3$

$= \frac{1}{2} \times 40 \times 10^6 \times 10^9 = 2 \times 10^{16}$

$a = (40 \times 10^{16})^{1/4} = \underline{2.5 \times 10^4 \text{ RPS}} = \omega_n$

$K = \frac{a^2}{b} = \frac{(2.5 \times 10^4)^2}{10^3 \times 2\pi} = \underline{10^5}$

PROBLEM II:

b = LOWEST BASEBAND FREQ. = 1880. RPS

$a = \omega_n$ (as BEFORE)

$$B_m = \left[\frac{10\pi \Delta\omega_p \omega_t}{\omega_t}\right]^{1/2} f_b = \left[\frac{10\pi(1)2\pi\times10^3}{2\pi\times10^3\times4}\right]^{1/2}\times 4{,}000 = 11.2\,KH_z$$

$$K = \frac{4B_m^2}{b} = \frac{4(11.2)^2 10^6}{1{,}880} = \underline{267\times10^3}\ RPS$$

$$a = \omega_n = \sqrt{Kb} = \sqrt{267\times10^3\times1880} = \underline{22{,}400}$$

APPENDIX A

COMPUTER DESIGN PROCEDURE INCLUDING PREDETECTION FILTER

The optimization program utilizes an algorithm based upon the Powell Search Technique in conjugate directions. The algorithm is set up to search in four variable directions; one for each of the design parameters β, γ, κ and b. The main optimization program is used in conjunction with a subprogram for the particular modulation case being considered. The subprogram is basically an expression for $(CNR_{IF})TH$ in terms of the closed-form solution described elsewhere. It should be noted that the subprogram is written to include all three possible cases of the closed-form solution.

In order to run the program, it is first necessary to enter the system parameters. As an example in the FDM-FM case, statements are included to fix the predetection bandwidth B_p (BP), the upper and lower baseband frequencies ω_a (OMEGA) and ω_b (OMEGB), the mean-square frequency deviation $(\Delta\omega_{rms})^2$ (DELSQ) and the mean-square phase error at threshold ν (NU). In addition to these parameters it is necessary to include an initial set of parameters for β (BETA), γ (GAMMA), κ and b (B). This initial "first guess" at the parameters provides a starting point from which the search procedure begins. As with most optimization algorithms it may be necessary to take more than one initial starting point before the optimum can be determined. This requirement comes about because the search may enter a forbidden region (such as negative parameters) or may reach a local minimum and terminate, whereas another minimum corresponding to a better design may exist.

APPENDIX A

COMPUTER PROGRAM USED TO IMPLEMENT POWELL'S METHOD AND RELATED SUBPROGRAMS

Basic Optimization Prooram

```
1       PROGRAM POWELL
2 C THIS ALGORITHM USES THE POWELL SEARCH TECHNIQUE IN CONJUGATE DIRECTIC
3       DIMENSION X(50,4),ESV(4,4),Y(50),B(5),XO(4),X1(4),XC(4),DL(4),O(4
4       DIMENSION X3(4)
5       READ 5,N,KMAX,C,STEP,TCLX,FLN
6     5 FORMAT (2I3,2F5.1,2F7.4)
7       READ 10, (X(1,J),J = 1,N)
8    10 FORMAT (F10.1)
9       DO 11 IK=1,N
10      DO 11 JK=1,N
11   11 ESV(JK,IK)=0.0
12      DO 15 IK=1,N
13   15 ESV(IK,IK)=1.0
14      I=1
15   20 DELTM=0.0
16      MTEST=0
17      J=1
18      DO 22 IK=1,N
19   22 X3(IK)=X(1,IK)
20      Y(I)=FIT(X3)
21      B(J)=Y(I)
22      BJT=B(J)
23   25 DO 30 JK=1,N
24   30 XO(JK)=X(I,JK)
25 C  THE UNRESTRICTED SEARCH BEGINS.
26 C  IN THE RARE CASE WHERE TWO SUCCESSIVE FUNCT ARE EXACTLY EQUAL
27 C  SEARCH IS STOPPED AND THE PROGRAM TERMINATED.
28      KR=1
29   35 DO 100 K=1,KMAX
30   40 S=2.0**(K-1)*STEP
31      DO 50 IK=1,N
32   50 XO(IK)=XO(IK)+S*ESV(IK,J)
33      YT=FIT(XO)
34      IF(C*YT-C*BJT) 60,350,100
35   60 IF(K-1) 70,90,70
36   70 IF(KR-1) 73,73,110
37   73 DO 80 IK=1,N
38      X1(IK)=XO(IK)
39   80XO(IK)=XO(IK)-(S+((2.0**(K-2))*STEP))*ESV(IK,J)
40      GO TO 110
```

```
41      90    DO 95 IK=1,N
42      95    X1(IK)=X0(IK)
43            STEP=-STEP
44            KR=KR+1
45     100    BJT=YT
46            GO TO 340
47     110    R=3.0*((2.0**(K-2))*ABS(STEP))
48            NM=1.0-4.75*ALOG10(FLN/R)
49            DO 120 IK=1,N
50            DL(IK)=0.618*(X1(IK)-X0(IK))
51            X0(IK)=X1(IK)-DL(IK)
52     120    X1(IK)=X1(IK-0.618*DL(IK)
53            W=FIT(X0)
54            V=FIT(X1)
55            DO 180 KNM=1,NM
56            DO 130 IK=1,N
57     130    DL(IK)=0.618*DL(IK)
58            IF(ABS(W-V)-0.01*TOLX) 185,135,135
59     135    IF(C*W-C*V) 160,350,140
60     140    DO 150 IK=1,N
61            XC(IK)=X1(IK)
62            X1(IK)=X0(IK)
63     150    X0(IK)=XC(IK)-DL(IK)
64            V=W
65            W=FIT(X0)
66            GO TO 180
67     160    DO 170 IK=1,N
68            XC(IK)=X0(IK)
69            X0(IK)=XL(IK)
70     170    X1(IK)=XC(IK)+DL(IK)
71            W=V
72            V=FIT(X1)
73     180    CONTINUE
74     185    J=J+1
75            DO 190 IK=1,N
76     190    X0(IK)=0.5*(X0(IK)+X1(IK))
77  C    THE FOLLOWING STATEMENTS TO 280 DETERM THE NEW SEARCH DIRECT
78            B(J)=FIT(X0)
79            BJT=B(J)
80            DELT=ABS(B(J)-B(J-1))
81            IF(DELTM-DELT) 200,210,210
82     200    DELTM=DELT
83            MAX=J-1
84     210    KR=1
85            IF(J-N) 35,35,220
86     220    AMPU=0.000001
87            DO 230 IK=1,N
88            U(IK)=X0(IK)-X(I,IK)
89            AMPU=AMPU+U(IK)**2
90     230    X1(IK)=2.0*X0(IK)-X(I,IK)
```

```
91          DO 232 IK=1,N
92    232   U(IK)=U(IK)/SQRT(AMPU)
93          YT=FIT(X1)
94          IF(C*YT-C*B(1)) 290,290,240
95    240   A=(B(1)-2.0*B(N+1)+YT)*(B(1)-B(N+1)-DELTM)**2
96          BT=0.5*DELTM*(B(1)-YT)**2
97          IF(C*A-C*BT) 290,290,250
98    250   IF(MTEST-1) 260,20,20
99    260   M1=N-1
100         IF(MAX-M1) 265,265,275
101   265   DO 270 JK=MAX,M1
102         DO 270 IK=1,N
103   270   ESV(IK,JK)=ESV(IK,JK+1)
104   275   DO 280 IK=1,N
105   280   ESV(IK,N)=U(IK)
106         DELTM=0.0
107         J=N
108         MTEST=1
109         GO TO 35
110   290   DO 300 IK=1,N
111         IF(ABS(XO(IK)-X(I,IK))-TOLX) 300,310,310
112   300   CONTINUE
113         GO TO 330
114   310   I=I+1
115         DO 320 IK=1,N
116   320   X(I,IK)=XO(IK)
117         IF(I-40) 20,20,500
118   330   YOPT=FIT(XO)
119         PRINT 331
120   331   FORMAT ('0THIS IS THE VALUE OF YOPT')
121         PRINT 332,YOPT
122   332   FORMAT (F22.6)
123         PRINT 333
124   333   FORMAT ('0THESE ARE THE VALUES OF X(1),X(2)')
125         PRINT 334,(XO(IK),IK=1,N)
126   334   FORMAT (2F22.6)
127   500   PRINT 335
128   335   FORMAT ('0THESE ARE THE BASE POINTS')
129         PRINT 336,((X(IJ,IK),IK=1,N),IK=1,I)
130   336   FORMAT (2F22.6)
131         PRINT 337
132   337   FORMAT ('0THESE ARE THE FUNCTION VALUES AT THE BASE POINTS')
133         PRINT 338,(Y(IK),IK=1,I)
134   338   FORMAT (F22.6)
135         IF(I-40) 400,400,390
136   390   PRINT 395
137   395   FORMAT ('0THE SOLUTION DID NOT CONVERGE')
138         GO TO 400
139   340   PRINT 345
140   345   FORMAT ('0THERE IS NO MAX,MIN')
141         GO TO 400
142   350   PRINT 360
143   360   FORMAT ('0TWO FUNCTION VALUES ARE EQUAL')
144   400   CONTINUE
145         STOP
```

Subprogram for Generalized Second-Order PLL - FDM-FM Case

```
      FUNCTION FIT(X3)
      DIMENSION X3(4)
      REAL K,MAGNT,INTVL,NU
      COMPLEX G,J,CPLX1,CPLX2,CPLX3,CPLX4,CPLX5,CPLX6,CPLX7,CPLX8
      COMPLEX CPLX9,CPLX10,CPLX11,CPLX12
       SBETA=X3(1)
      SGAMMA=X3(2)
      SB=X3(3)
      SK=X3(4)
      BETA=SBETA*1.0E15
      GAMMA=SGAMMA*1.0E7
      B=SB*1.0E5
      K=SK*1.0E9
      BPRIM=3.142E8
      BP=5.0E7
      NU=0.25
      OMEGA=3.770E5
      OMEGB=1.596E7
      DELSQ=1.990E15
      APRIM=1.0/(K*B)**2
      BPRIM=1.0/K**2
      XNEWA=1.0/(BETA**2)
      XNEWB=1.0/(GAMMA**2)-2.0/BETA
      XNEWC=(1.0/(K*B)+1.0/BETA)**2
      XNEWD=(1.0/K+1.0/GAMMA)**2-2.0*(1.0/(K*B)+1.0/BETA)
      XNEW1=XNEWD/(2.0*XNEWC)
      XNEWM=XNEW1**2
      XNEWN=1.0/XNEWC
      IF(XNEWM.GT.XNEWN.AND.XNEWD.GT.0.0) GO TO 150
      XNEW2=(-1.0)*SQRT(1.0/XNEWC-(XNEWD/(2.0*XNEWC))**2)
      G=CMPLX(XNEW1,XNEW2)
      IF(XNEWD.GE.0.0)GO TO 75
      XNEW3=ATAN(XNEW2/XNEW1)
      WRITE(6,50)
50    FORMAT(1H , 13HCASE 1 REGION)
      GO TO 80
75    XNEW3=ATAN(XNEW2/XNEW1)+3.1415927
      WRITE(6,60)
60    FORMAT(1H , 13HCASE 2 REGION)
80    XNEW4=XNEW3/2.0
      THETA=XNEW4+3.1415927
      MAGNT=SQRT(SQRT(1.0/XNEWC))
      XNEW5=MAGNT*COS(THETA)
       XNEW6=MAGNT*SIN(THETA)
      J=CMPLX(XNEW5,XNEW6)
      CPLX1=1.0-XNEWB*G-(1.0-XNEWD*G)*(XNEWA/XNEWC)
      CPLX2=J*(CONJG(G)-G)
```

```
      CPLX3=CPLX1/CPLX2
      CPLX4=(J-BPPRM/2.0)/(J+BPPRM/2.0)
      CPLX5=CLOG(CPLX4)
      CPLX6=CPLX3*CPLX5
      XNEW7=REAL(CPLX6)
      XNEW8=XNEWA*(BPPRM/2.0)+XNEW7
      XNEW9=1.0/(2.0*3.1415927*XNEWC)
      INTVL=XNEW8*XNEW9
      CPLX7=((OMEGB-J)/(OMEGB+J))*((OMEGA+J)/(OMEGA-J))
      CPLX8=CLOG(CPLX7)
      CPLX9=(BPRIM-APRIM*G)/(J*(CONJG(G)-G))
      CPLX10=CPLX8*CPLX9
      XNEW10=REAL(CPLX10)
      XNEW11=DELSQ/(OMEGB-OMEGA)
      XNEW12=XNEW11/XNEWC
      PHISQ=XNEW10*XNEW12
      GO TO 90
  150 CONTINUE
      WRITE(6,160)
  160 FORMAT(1H , 13HCASE 3 REGION)
      YNEW1=SQRT(XNEWM-XNEWN)
      RS1=XNEW1+YNEW1
      RS2=XNEW1-YNEW1
      R1=SQRT(RS1)
      R2=SQRT(RS2)
      YNEW2=(1.0/R1)*ATAN(3.1415927*BP/R1)
      YNEW3=(1.0/R2)*ATAN(3.1415927*BP/R2)
      YNEW4=(1.0-XNEWB*RS1)/(RS2-RS1)
      YNEW5=(1.0-XNEWB*RS2)/(RS1-RS2)
      SUBT1=YNEW4*YNEW2+YNEW5*YNEW3
      YNEW6=(1.0-XNEWD*RS1)/(RS2-RS1)
      YNEW7=(1.0-XNEWD*RS2)/(RS1-RS2)
      SUBT2=YNEW6*YNEW2+YNEW7*YNEW3
      SUBT3=XNEWA*3.1415927*BP
      SUBT4=SUBT1-(XNEWA/XNEWC)*SUBT2+SUBT3
      INTVL=SUBT4/(2.0*3.1415927*XNEWC)
      YNEW8=ATAN(OMEGA/R1)
      YNEW9=ATAN(OMEGA/R2)
      YNEW10=ATAN(OMEGB/R1)
      YNEW11=ATAN(OMEGB/R2)
      YNEW12=YNEW11-YNEW9
      YNEW13=YNEW8-YNEW10
      YNEW14=(BPRIM-APRIM*RS2)/R2
      YNEW15=(BPRIM-APRIM*RS1)/R1
      SUBT5=YNEW14*YNEW12+YNEW15*YNEW13
      YNEW16=1.0/(XNEWC*(RS1-RS2))
      YNEW17=DELSQ/(OMEGB-OMEGA)
      YNEW18=YNEW16*YNEW17
      PHISQ=YNEW18*SUBT5
   90 CNRTH=INTVL/(BP*(NU-PHISQ))
      WRITE(6,100)CNRTH,BETA,GAMMA,B,K
  100 FORMAT(1P5E16.6)
      FIT=CNRTH
      RETURN
      END
```

DIGITAL FM DETECTION

CHARACTERISTICS OF PLL AS DIGITAL FM DETECTOR:

1. PLL CAN ACT AS PREDETECTION FILTER + LIMITER + DISCRIMINATOR + AFC.

2. INTEGRATED CIRCUIT IMPLEMENTATION.

3. EASILY SWITCHED FROM ONE BIT RATE TO ANOTHER.

4. EASILY SWITCHED FROM ANALOG TO DIGITAL RECEPTION.

5. ERROR RATES ABOUT THE SAME AS FOR PRED. FILTER + L-D + AFC.

AIM OF DESIGN:

MINIMUM PEAK PHASE ERROR FOR MINIMUM ERROR RATE.

CONSIDER IF LPF WERE INTEGRATOR.

WHAT WOULD PHASE ERROR BE? (SPIKES)

HOW ABOUT FOR A FIRST-ORDER LOOP? (DETECTED OUTPUT)

THIS LEADS TO HIGHLY-DAMPED LOOP, AS OPTIMUM. (LEAST PEAK IN PHASE ERROR) - - - SEE NEXT SHEET.

DATA NEEDED: BIT RATE = R, LONGEST STRING OF IDENTICAL BITS (NRZ) = N, MAX. CENTER FREQ. UNCERTAINTY = Δ F, TIME TO ACQUIRE STEADY-STATE = Tss, AND IN ADDITION ACCEPTABLE HOLD-IN RANGE, PULL-IN RANGE, AND PULL-IN TIME.

HIGHLY-DAMPED SECOND-ORDER LOOP:

IT ACTS LIKE A FIRST-ORDER LOOP FOR THE DIGITAL BASEBAND BUT LIKE A SECOND ORDER LOOP FOR OFFSETS, PULL- AND HOLD-IN RANGES.

USE:

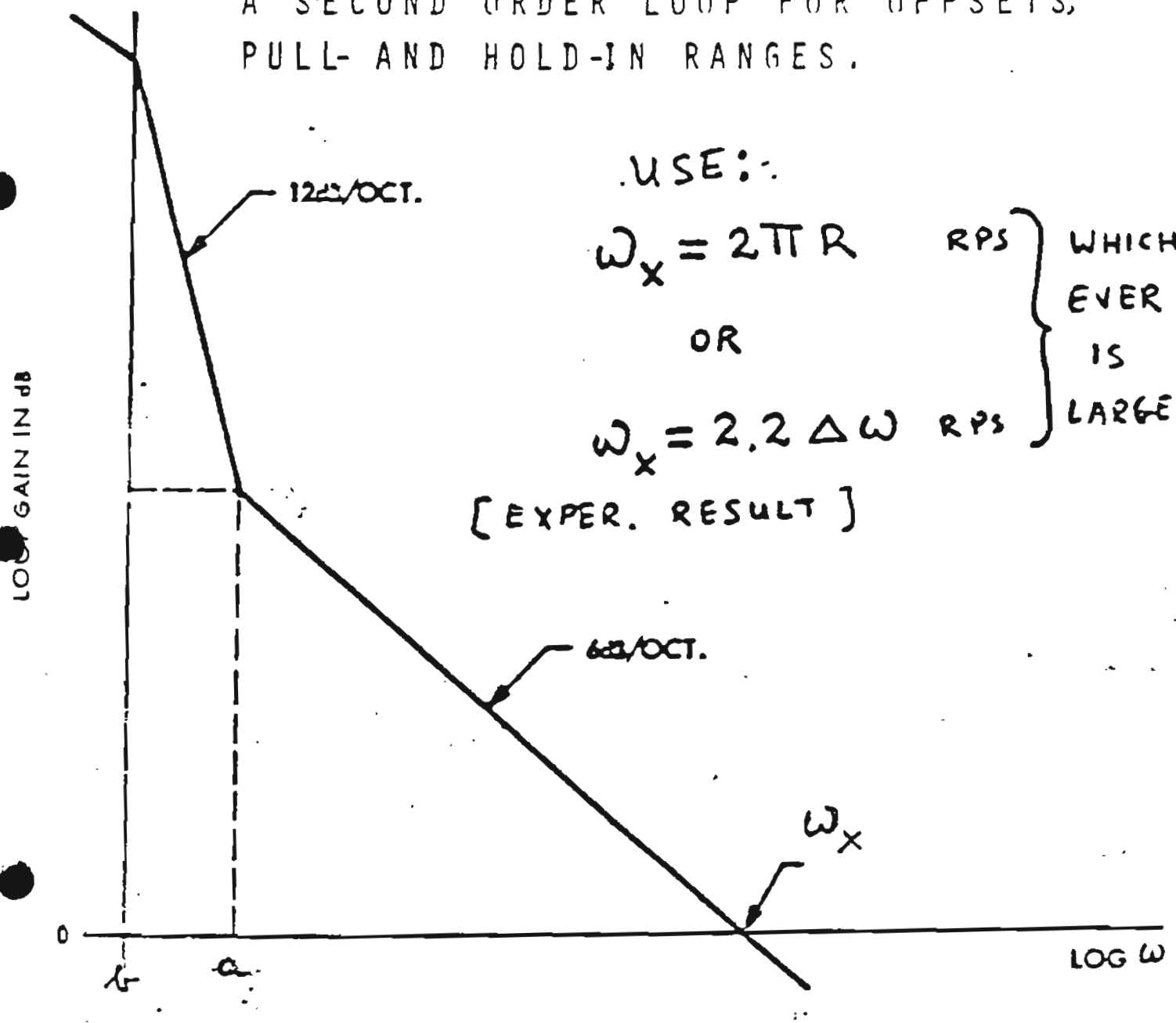
$\omega_x = 2\pi R$ RPS

OR

$\omega_x = 2.2\,\Delta\omega$ RPS

} WHICHEVER IS LARGER

[EXPER. RESULT]



Open-Loop Response

THE ϕ_e FOR A STEP IN FREQUENCY AT THE INPUT, IS (BY LIN. ANALYSIS)

$$\phi_e(t) \approx \frac{\Delta\omega_i}{K}\left[1 + \frac{a}{b}e^{-at} - \frac{a}{b}e^{-\frac{Kb}{a}t}\right]$$

1. TRANSIENT COMPONENT MUCH LARGER THAN STEADY-STATE, BY FACTOR $\frac{a}{b}$.

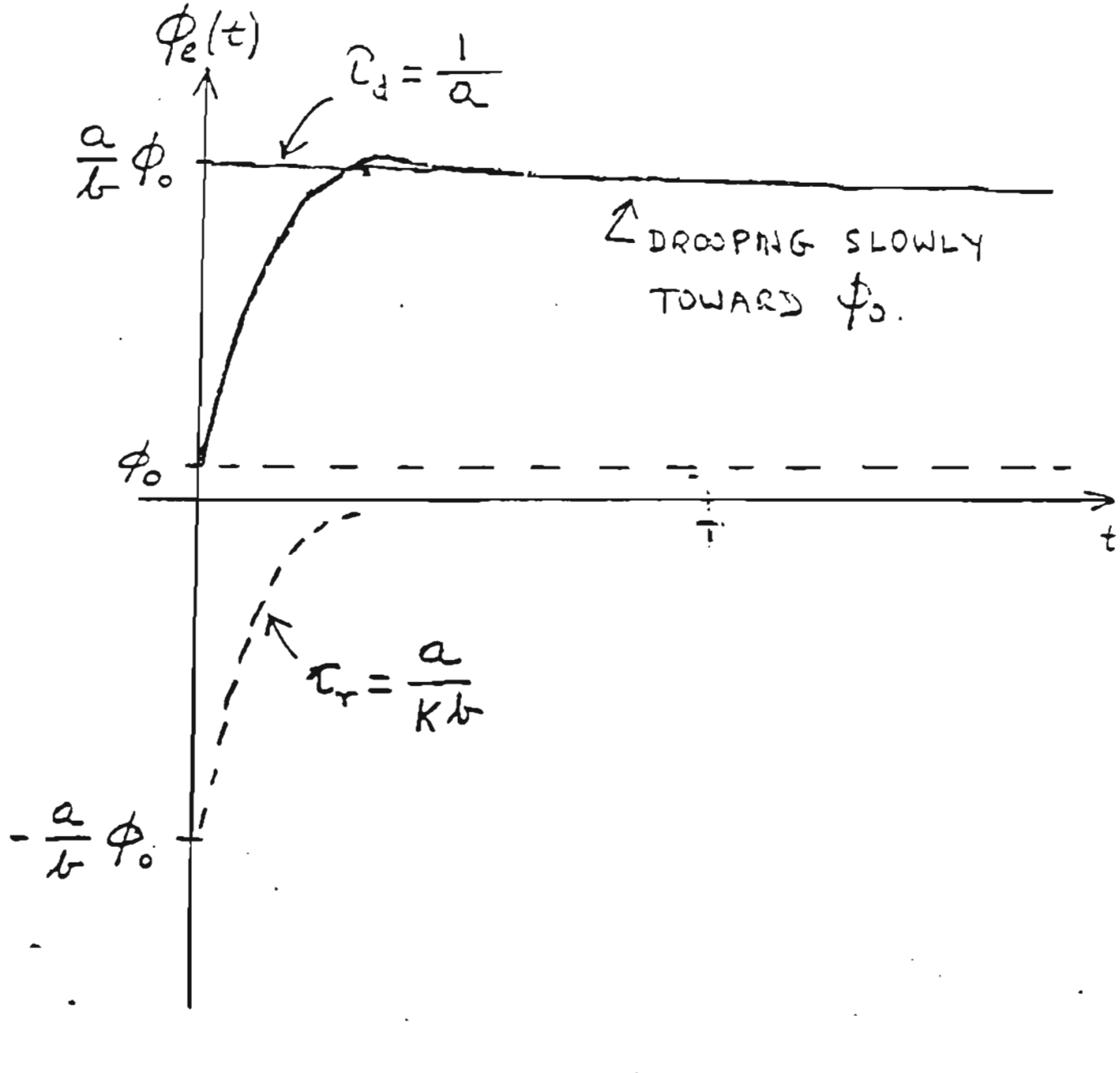
2. THERE ARE 2 PARTS TO TRANSIENT:

ONE RISES RAPIDLY WITH

$$\tau_r = \frac{a}{Kb}$$

THE OTHER DROOPS SLOWLY WITH

$$\tau_d = \frac{1}{a}$$



TRANSIENTS IN ϕ_e FOR HIGHLY-DAMPED SECOND-ORDER LOOP AND FREQUENCY STEP INPUT.

IF FREQ. IS NOT BINARY THEN

$$\phi_e(\infty) = \phi_0 .$$

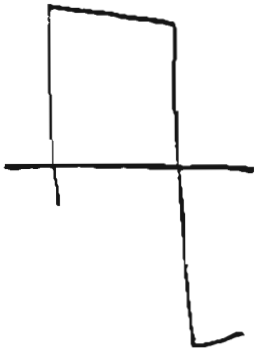
USUAL REQUIREMENTS:

1. RISE TIME SHOULD BE MUCH LESS THAN A BIT LENGTH, i.e.,

$$\frac{a}{Kb} \ll \frac{1}{R} .$$

2. DROOP TIME CONSTANT SHOULD BE VERY LARGE COMPARED TO THE LENGTH OF N IDENTICAL BITS,

i.e. $$\frac{1}{a} \ggg \frac{N}{R}$$



DROOP ADDS TO THE PEAK Φ_e.

3. DROOP TIME CONSTANT SHOULD PERMIT STEADY-STATE DUE TO CENTER FREQUENCY OFFSETS TO BE ACHIEVED WITHIN SPECS. TYPICALLY IT SHOULD BE SMALLER THAN TIME CONSTANT OF DC BLOCK IN POST-DETECTION CIRCUIT.

4. FOR SMALL STEADY-STATE PHASE ERROR, ϕ_0, WE NEED

$$\frac{b}{a} \ll 1$$

5. DURING SIGNAL DROPOUTS, LOOP IS "COASTING" WITH TIME CONSTANT $\frac{1}{b}$.

EXAMPLE

$R = 32$ KB/S, $N = 64$, $D = 0.7$ (OPT.)

OFFSET $\leq$ 100 KHz

SOLUTION:

1. $\omega_x = 2\pi R = 2\pi \times 32{,}000 = 2 \times 10^5$ RPS

2. TIME SPAN FOR 64 BITS IS

$$\tau_N = \frac{64}{32{,}000} = 2 \times 10^{-3} \text{ SEC.}$$

LET US PERMIT A DROOP OF 1% OVER THE 64-BIT SEQUENCE, THEN

$$\tau_N a = 0.01 \qquad \therefore \; a = 5 \text{ RPS}.$$

3. THE TIME CONSTANT TO REACH STEADY-STATE $= \frac{1}{a} = 0.2$ SEC.

4.

FOR ϕ_0 TO BE VERY SMALL, LET

$$\frac{a}{b} = 25 \quad \therefore \quad b = 0.2 \text{ RPS}.$$

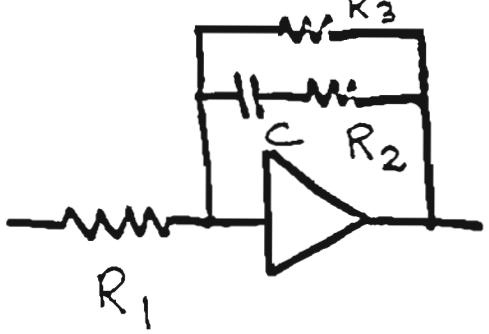
5. $$K = \frac{a\omega_x}{b} = 25 \times 2 \times 10^5 = 5 \times 10^6$$

6. $$\phi_0 = \frac{\Delta\omega_i}{K} = \frac{2\pi \times 10^5}{5 \times 10^6} = 0.125 \text{ rad} = 7.2^\circ.$$

WE CAN NOW ALSO CALCULATE

HIR, PIR, PIT.

7. CONSIDER IMPLEMENTATION SHOWN



$$a = \frac{1}{R_2 C}, \quad b = \frac{1}{(R_2 + R_3)C}$$

LET $C = 10^{-6}$ Fd, THEN $R_2 = 200\text{K}$

$$R_2 + R_3 = \frac{1}{bC} = 5 \text{ Meg} \quad \therefore \quad R_3 = 4.8 \text{ Meg}.$$

Problem on Binary FM Detection

Design a PLL for Binary FM Detection, as follows:

R=4.8 KB/sec , Max. number of consecutive identical bits =32

Droop=7% , Deviation index= $\frac{2\Delta f}{R}=4$

Find w_x, K, a, b, R_2, R_3, C

Answers: $w_x=2\pi x21x10^3$, $K\tilde{=}4x10^6$, a=10, b=0.3 .

Solution to Problem on Binary FM Detection

$\Delta f = 2R = 9{,}600.\ Hz$

$2.2\,\Delta\omega = 2.2 \times 2\pi \times 9{,}600. = \underline{132{,}700\ RPS \doteq \omega_x}$

$\tau_N = \dfrac{32}{4{,}800} = 0{,}0067\ sec.$

For a droop of 7%, $\tau_N a = 0.07$

$\therefore\ a = \dfrac{0.07}{0.0067} \approx \underline{10.\ RPS}$

For small ϕ_o, let $\underline{b = 0.3}$

Then $K = \dfrac{a\omega_x}{b} = \dfrac{10 \times 132{,}700}{0.3} = \underline{4.4 \times 10^6\ RPS}$

Let $C = \underline{10^{-6}\ Fd}$, then $R_2 = \dfrac{1}{aC} = \dfrac{10^6}{10} = \underline{100.K}$

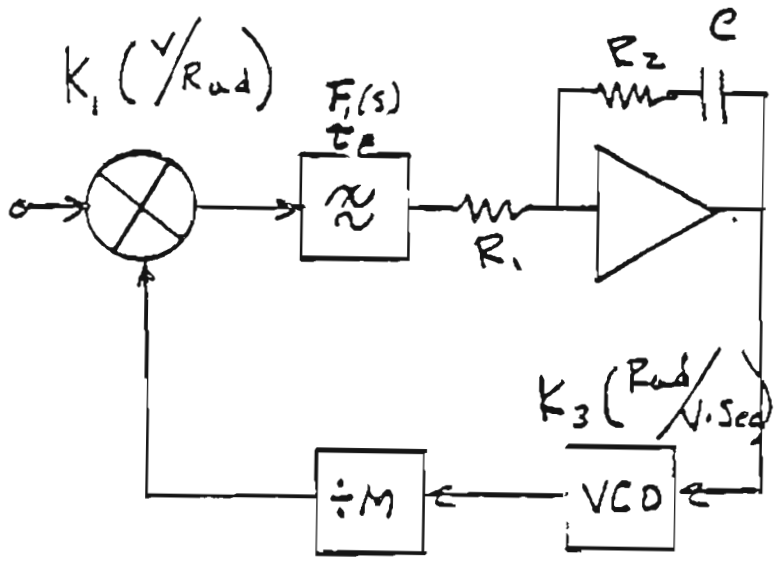
$R_2 + R_3 = \dfrac{1}{bC} = \dfrac{1}{0.3 \times 10^{-6}} = 330.K$

$\therefore\ R_3 = \underline{230.K}$

NOISE/SPURIOUS/STABILITY CONSIDERATIONS

Arnold Newton

F



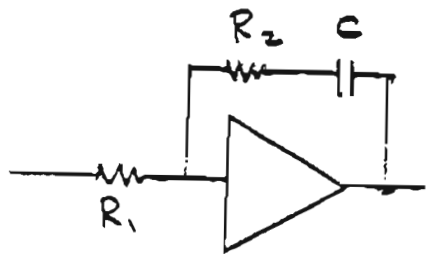
Loop Constant:

$$\tau_1 = R_1 C$$

$$\tau_2 = R_2 C$$

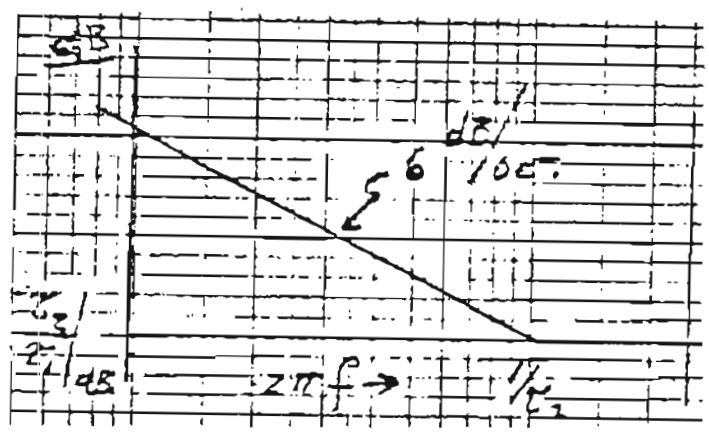
$$K_0 = \frac{K_1 K_3}{M} = \frac{K}{M}$$

Loop Filter



$$F(S) = \frac{S\tau_2 + 1}{S\tau_1}$$

	$F(S)$
$S \to 0$	$\frac{1}{S\tau_1} \to \infty$
$S \to \infty$	$\frac{\tau_2}{\tau_1} \dots \frac{\tau_2}{\tau_1}$



$\frac{1}{F}$

THE PREFILTER SERVES TO SUPPRESS SPURIOUS MODULATION BY THE HARMONICS OF THE REFERENCE FREQUENCY F_r. ITS TRANSFER RESPONSE $F_1(s)$ IS CHARACTERIZED BY A BANDWIDTH B AND A GROUP DELAY τ_F. GENERALLY, THE FOLLOWING CONDITION IS SATISFIED:

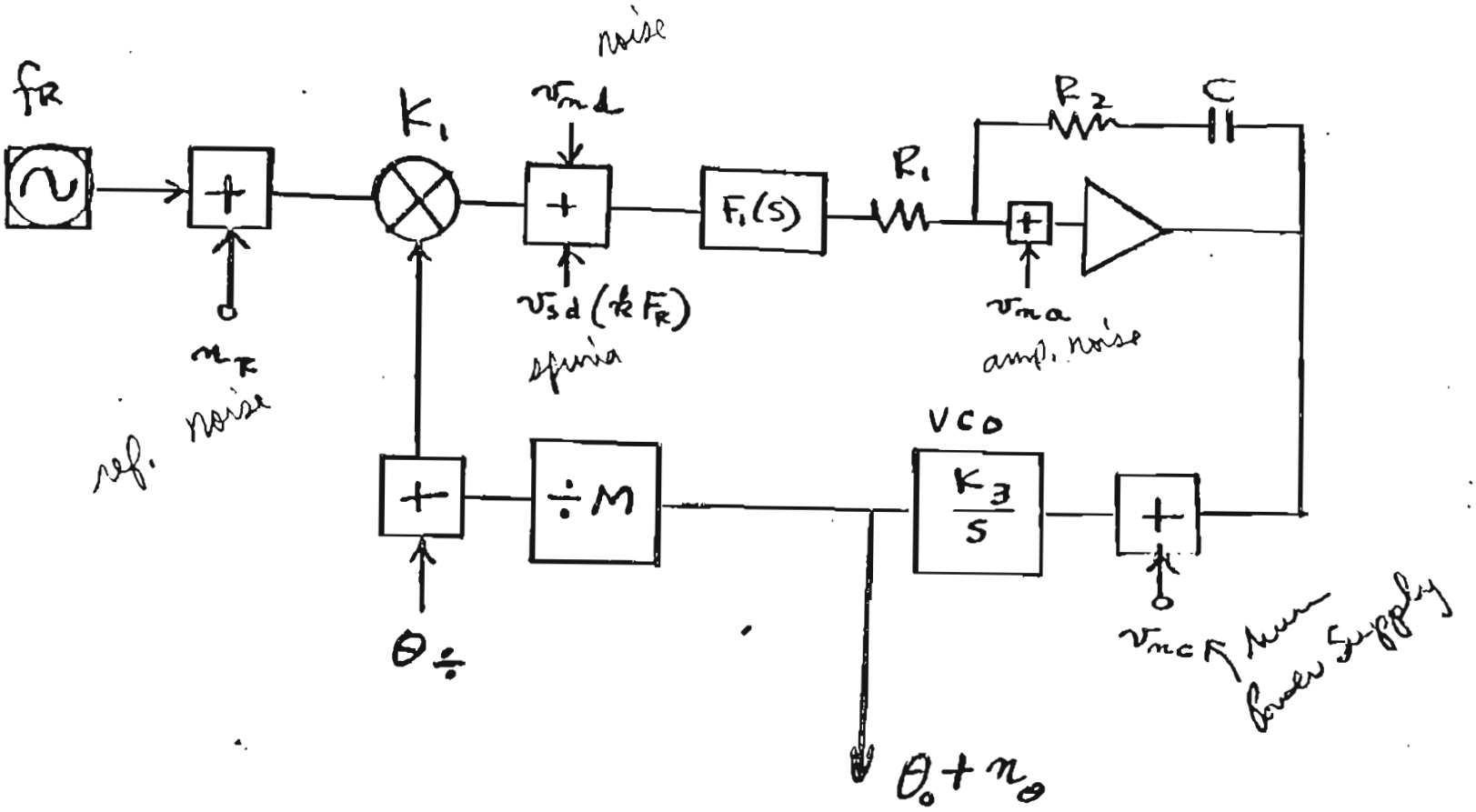
$$F_n \ll B \ll F_r$$

CONSEQUENTLY, WITHIN THE PLL CLOSED LOOP BANDWIDTH A DELAY IS EXPERIENCED:

$$F_1(s) \approx E^{-s\tau_F}$$

SECOND ORDER PLL SUSCEPTIBILITY TO RANDOM NOISE AND SPURIOUS COMPONENTS

Ref. 4



MODEL FOR NOISE AND SPURIOUS INJECTION

Susceptibility to Noise and Spurious; $n_o(\omega) = \sum n_p(\omega)$

source of contribution	Units	Contribution to n_o output noise	In Band contribution $\omega \ll \omega_m$	Out of Band contribution $\omega \gg \omega_m$
Reference Noise	$\theta_R(\omega)$ in Rad^2/Hz	$M^2 \lvert H(j\omega)\rvert^2 \theta_i(\omega)$	$M^2 \theta_R(\omega)$	$\left(\frac{MK}{\omega}\right)^2 \lvert F_1(j\omega)\rvert^2 \theta_R$
Phase Det. Noise	v_{nd} in $V/\sqrt{Hz}$	$\left(\frac{M}{K_1}\right)^2 \lvert H(j\omega)\rvert^2 v_{nd}^2$	$\left(\frac{M}{K_1}\right)^2 \lvert H(j\omega)\rvert^2 v_{nd}^2$	$\left(\frac{MK}{\omega K_1}\right)^2 \lvert F_1(j\omega)\rvert^2 v_{nd}^2$
Phase Det. Spurious	v_{sd} in $V(\text{peak})$	$\left(\frac{M}{K_1}\right)^2 \lvert H(j\omega_s)\rvert^2 v_{sd}^2$	—	$\left(\frac{MK}{\omega_s K_1}\right)^2 \lvert F_1(j\omega_s)$
Op Amp Noise	v_{na} in $V/\sqrt{Hz}$	$\left(\frac{M}{K_1}\right)^2 \left\lvert\frac{H(j\omega)}{F(j\omega)}\right\rvert^2 v_{na}^2$	$\left(\frac{M}{K_1}\right)^2 v_{na}^2$	$\left(\frac{MK}{K_1}\right)^2 \frac{v_{na}^2}{\omega^2}$
Control Noise	v_{nc} in $V/\sqrt{Hz}$	$\left(\frac{K}{K_1}\right)^2 \frac{\lvert 1-H(j\omega)\rvert^2}{\omega^2} v_{nc}^2$	$\left(\frac{K}{K_1\omega_n}\right)^2 \left(\frac{\omega}{\omega_n}\right)^2 v_{nc}^2$	$\left(\frac{K}{K_1}\right)^2 \frac{v_{nc}^2}{\omega^2}$
VCO Jitter	$\theta_o(\omega)$ in Rad^2/Hz	$\lvert 1-H(j\omega)\rvert^2 \theta_o(\omega)$	$\left(\frac{\omega}{\omega_n}\right)^4 \theta_o(\omega)$	$\theta_o(\omega)$
Frequency Divider Noise	$\theta_\div$ in Rad^2/Hz	$M^2 \lvert H(j\omega)\rvert^2 \theta_\div(\omega)$	$M^2 \theta_\div(\omega)$	$\left(\frac{MK}{\omega}\right)^2 \lvert F_1(j\omega)\rvert^2 \theta_\div(\omega)$

COMMON PHASE DET. TYPES

1. PHASE/FREQUENCY DETECTOR

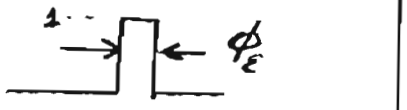
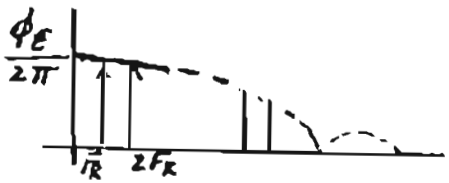
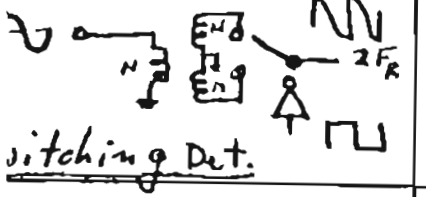
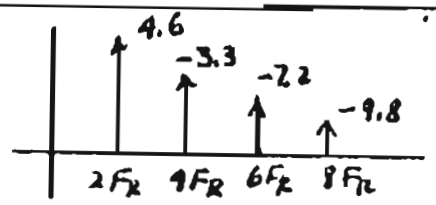
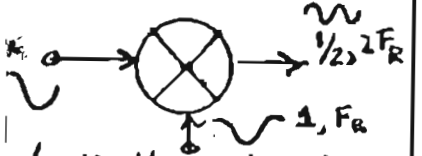
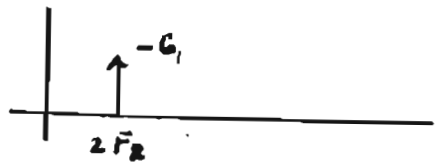
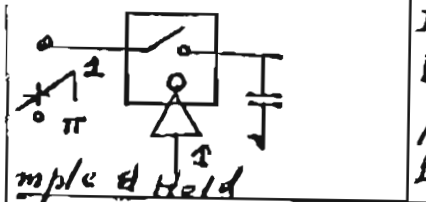
2. SWITCHING PHASE DETECTOR

3. ANALOG MULTIPLIER

4. SAMPLE AND HOLD

REF. 5,6

Phase Detector Characteristics

Phase Detector Type	V_{sd}	K_1	$\frac{K_1}{V_{sd}}$	Spectral Characteristics	Delay τ_d	Phase Jitter
 Base/Frequency Det.	1	$\frac{1}{2\pi}$	$\frac{1}{2\pi}$			(-135 to -142) dBC Typical
 witching Det.	1	$\frac{2}{\pi}$	$\frac{2}{\pi}$			
 log Mult., Bal. Mixer	½	½	1			
 mple & Hold	Ideally-0 Depends on Aperture Effects	$\frac{1}{\pi}$			$\frac{T_R}{2}$ relative to 1	

V_{sd} - Level of spurious emerging from phase detector

The phase detectors are idealized. Practical devices may have scaling factors other than shown.

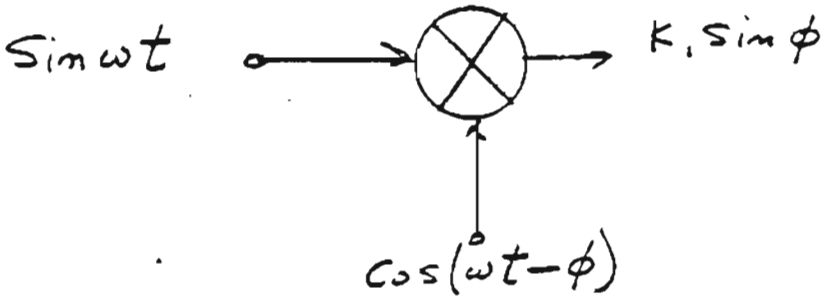
- THE PHASE FREQUENCY DETECTOR OWES ITS POPULARITY TO ITS RELIABLE ACQUISITION PROPERTIES. SPURIOUS ENERGY IS DISTRIBUTED OVER A WIDE SPECTRUM, PRECLUDING THE USE OF SIMPLE TRAPS AND REQUIRING EFFICIENT FILTERS. PHASE JITTER CAN LIMIT ITS USE IN HIGH PERFORMANCE PHASE LOCK SOURCES AND FREQUENCY SYNTHESIZERS.

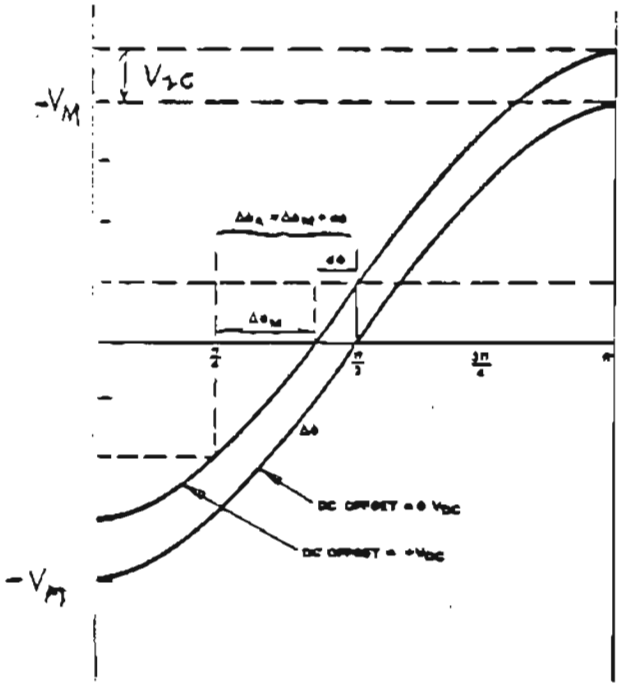
- THE SWITCHING PHASE DETECTOR PROVIDES A LOW DC OFFSET BUT GENERATES HIGH LEVELS OF SPURIOUS. IT IS SUITABLE FOR LOW-FREQUENCY NARROW BANDWIDTH APPLICATIONS.

- THE ANALOG MULTIPLIER OR EQUIVALENTLY THE BALANCED MIXER GENERATES A SPURIOUS AT TWICE THE REFERENCE FREQUENCY AND LENDS ITSELF TO THE USE OF A TRAP. THEREFORE, IT OFFERS LOW-SPURIOUS WIDE BANDWIDTH CAPABILITIES. HOWEVER, IT OFTEN REQUIRES ACQUISITION AID WITH ADDED COMPLEXITY.

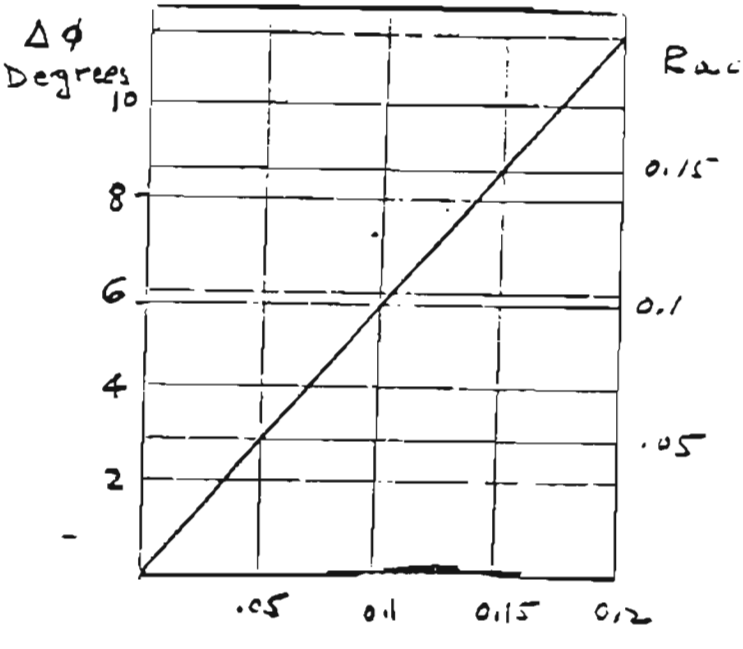
- THE SAMPLE AND HOLD POTENTIALLY OFFERS LOWEST LEVELS OF SPURIOUS. ALTHOUGH THE INHERENT DELAY IS $\frac{TR}{2}$, THE NET DELAY CAN BE LOW BECAUSE OF MODEST PREFILTER REQUIREMENTS. ACQUISITION AIDS ARE REQUIRED.

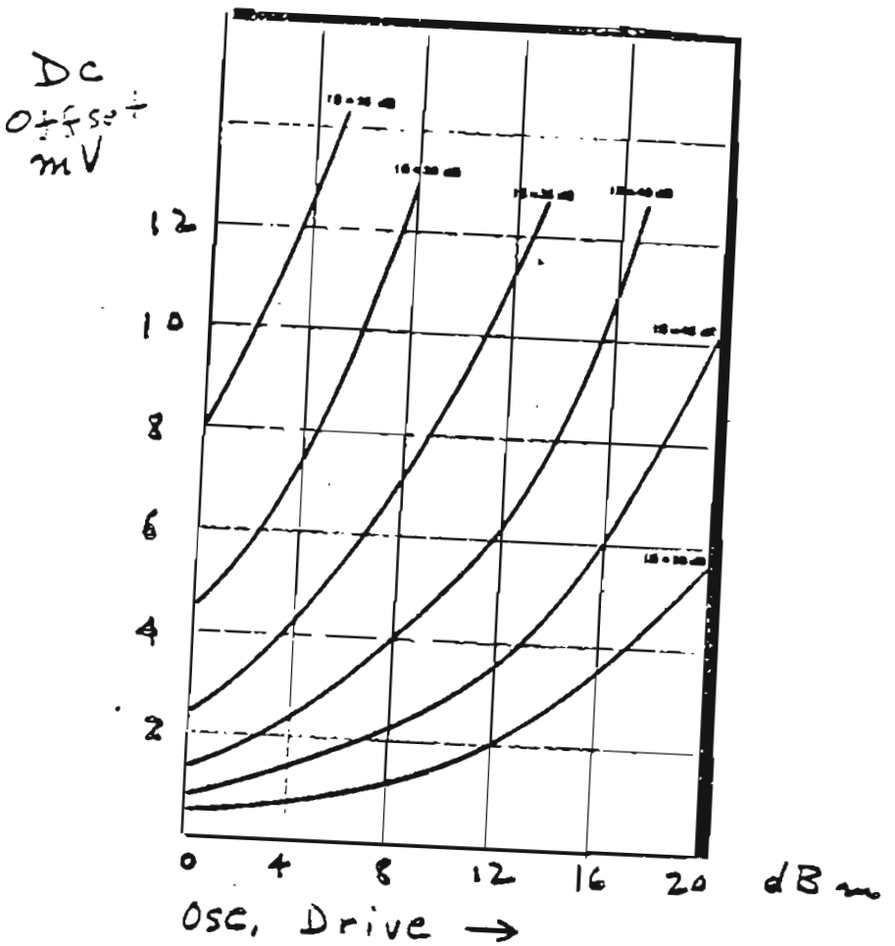
BALANCED-MIXER AS PHASE DETECTOR



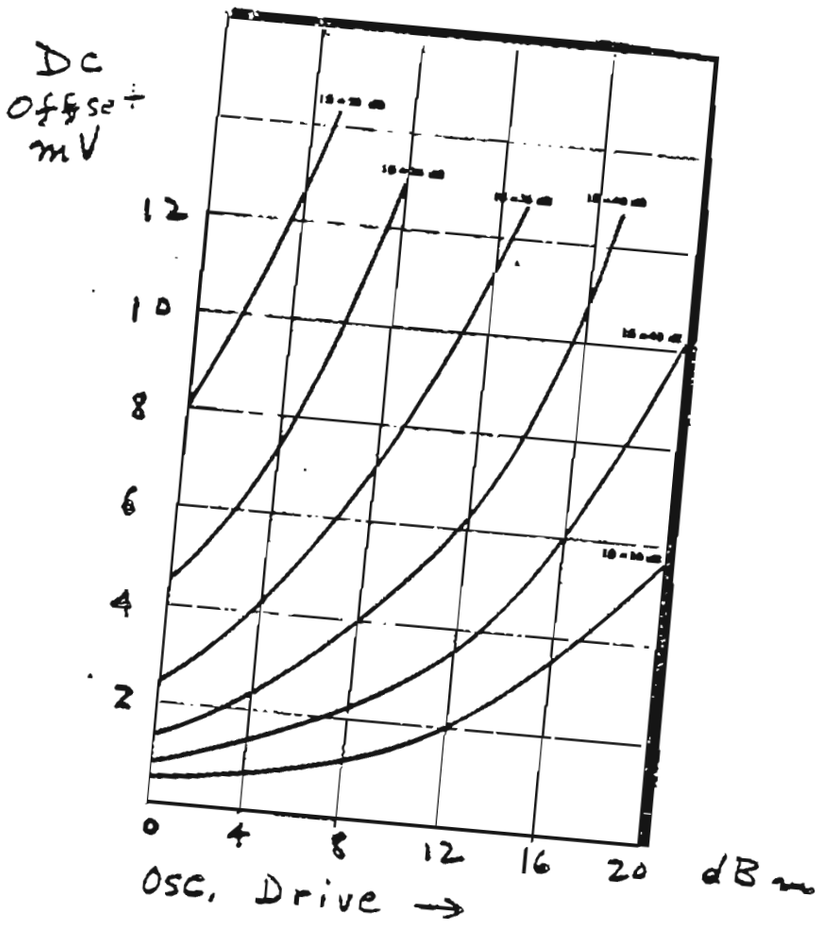


Null phase error due to DC offset.

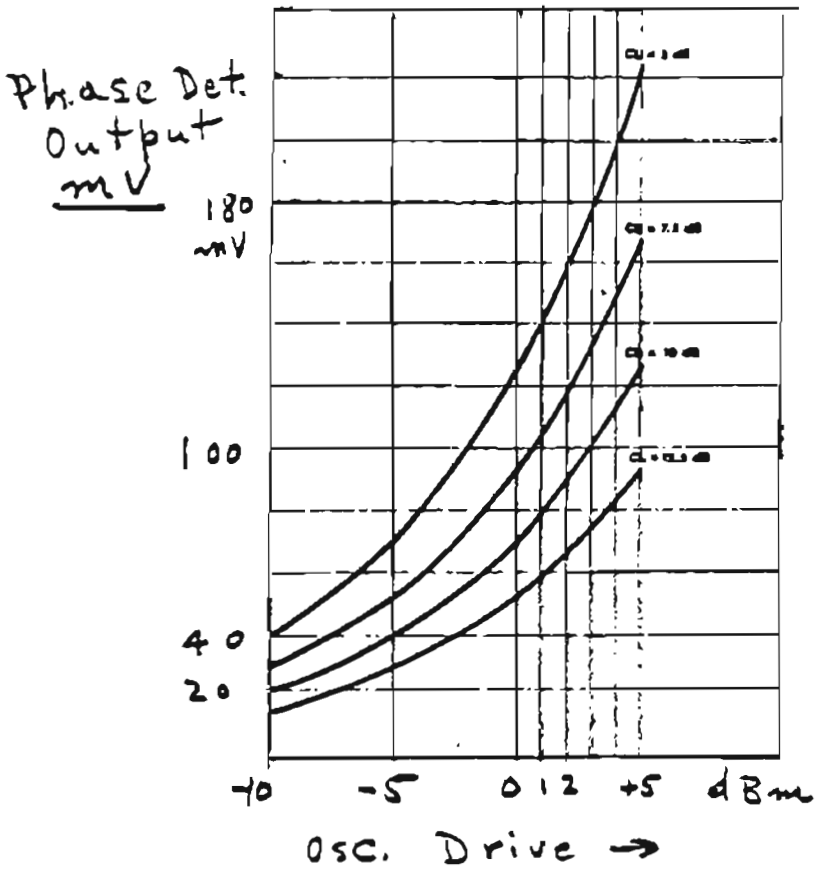




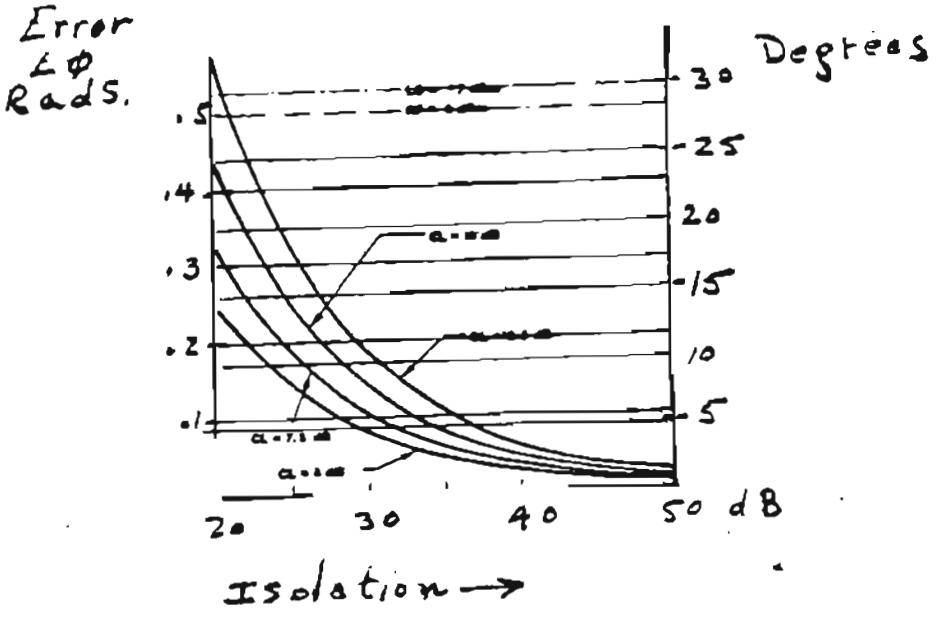
Effect of Osc. Drive and Isolation



Effect of Osc. Drive and Isolation



Detector output as a function of osc. drive and conversion loss CL



Phase error as a function of isolation and conversion loss.

High-Figure-Of-Merit
PHASE DETECTORS

RPD SERIES

MODEL	FREQUENCY	Z(Ohms)	COST
RPD-1	1-100 MHz	50	$15.95(5-24)

DESCRIPTION — These new high efficiency phase detectors offer state-of-the-art performance while still economically priced. These are the only units in the world offering a figure-of-merit greater than 125—at only $15.95.

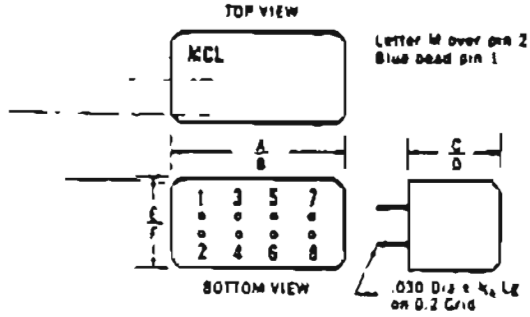
The figure-of-merit M or efficiency of a phase detector can be defined as the ratio of maximum DC output voltage (in mV) divided by the RF power (in dBm). The maximum DC output of the RPD-1 is 1000 mV with +7 dBm applied to the LO and RF ports. Thus, its figure-of-merit M is 143, which represents a highly efficient phase detector. For comparison, a standard phase detector offers 350 mV DC output with the same LO and RF inputs for a figure-of-merit M of 50.

Only 0.40 inches high, the low profile RPD series of phase detectors covers a very broad frequency range from 1 to 100 MHz. Exhibiting a flat frequency response, these units are designed to operate with a 50 ohm impedance at the L & R ports, and 500 ohms at the I port. Output is 1000 mV (typ) and isolation is greater than 50 dB (typ).

Packaged within an RFI shielded metal enclosure and hermetically sealed header, these high performance units have their 8 pins located on a 0.2 inch grid.

High reliability is a characteristic of the RPD series. Each unit carries a one-year guarantee by Mini-Circuits.

DIMENSIONS AND CONNECTIONS



	A	B	C	D	E	F
IN	.3701	.400	.395	.4001	.3701	.400
MM	9.5	10.2	9.7	10.1	9.3	10.1

PIN LAYOUT

Model No.	-1
LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

WEIGHT: 5.2 grams .18 ounces

FEATURES
Broadband, 1-100 MHz
High Output, 1000mV
High Figure-Of-Merit, M, 143 typical
High Isolation, typically greater than 50dB
Low DC Offset, 0.2 mV typical
Miniature, 0.128 in. cu., 0.4 in x 0.8 PC area, 0.4 in. high
High Reliability, 100% tested
Low Cost, $15.95 (5-24)

APPLICATIONS
- Radar
- ECM Systems
- Test instruments
- Phase-lock loops

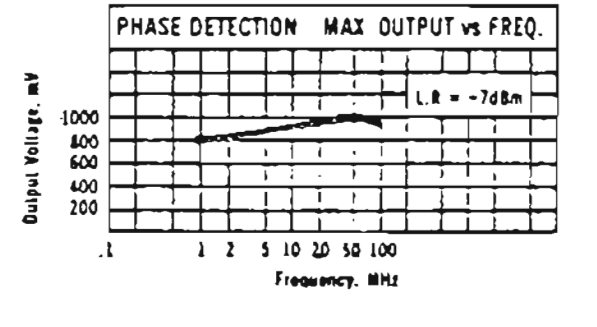
ABSOLUTE MAXIMUM RATINGS

• Input Power:		50 mW
• Peak IF Input Current:		40 mA
• Operating and Storage Temp.:		−55°C to +100°C
• Pin Temperature:	(10 sec.)	+260°C

RPD-1 SPECIFICATIONS

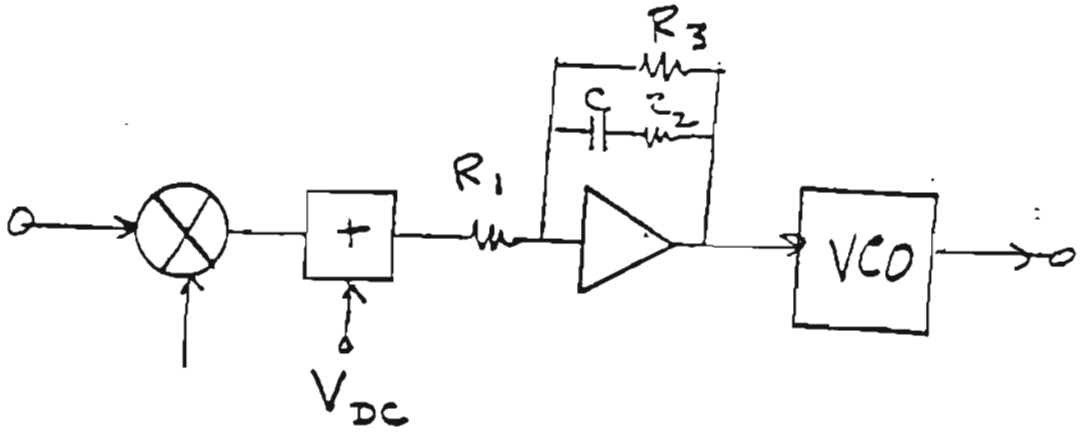
FREQUENCY RANGE: L and R ports Output ports	 1-100 MHz DC-50 MHz
SCALE FACTOR	8 mV/Degree
IMPEDANCE L and R ports I port	 50 ohms 500 ohms
L and R SIGNAL LEVELS	+7 dBm
ISOLATION, L-R	40 dB min
MAXIMUM DC OUTPUT, mV	1000 mV typ 750 mV min
DC OUTPUT POLARITY (L and R in-phase)	 Negative
DC OUTPUT OFFSET VOLTAGE	0.2 mV typ 1 mV max
FIGURE-OF-MERIT, M	143 Typical

MODEL RPD-1



Mini-Circuits 2625 E. 14th St., Brooklyn, NY 11235 (212) 769-0200 Dom. Telex 125460 Int'l. Telex 620156

DC GAIN CONSIDERATIONS



$$\text{DC Gain} \quad K_2 = \frac{R_3}{R_1}$$

OPEN-LOOP FREQUENCY OFFSET DUE TO PHASE DETECTOR DC OFFSET VDC

$$\Delta\omega = K_2 K_3 V_{DC}$$

$$\frac{\Delta\omega}{\omega_0} = K_2 \frac{K_3}{\omega_0} V_{DC}$$

SATURATION WILL PRODUCE HANGUPS WHEN DC OFFSET VDC IN COMBINATION WITH DC GAIN K_2 WILL CAUSE THE VCO TO BE DRIVEN BEYOND ITS TUNING CAPABILITY.

PROBLEM

1. TYPICAL FOR A VCXO ARE THE FOLLOWING PARAMETERS; LINEAR FREQUENCY DEVIATION OF $\pm$ 0.1% FOR A CONTROL VOLTAGE OF $\pm$ 5v AND A LIMITING FREQUENCY DEVIATION OF $\pm$ 0.4%. FOR AN OFFSET V_{DC} OF $\pm$ 2mV DETERMINE MAXIMUM K_2.

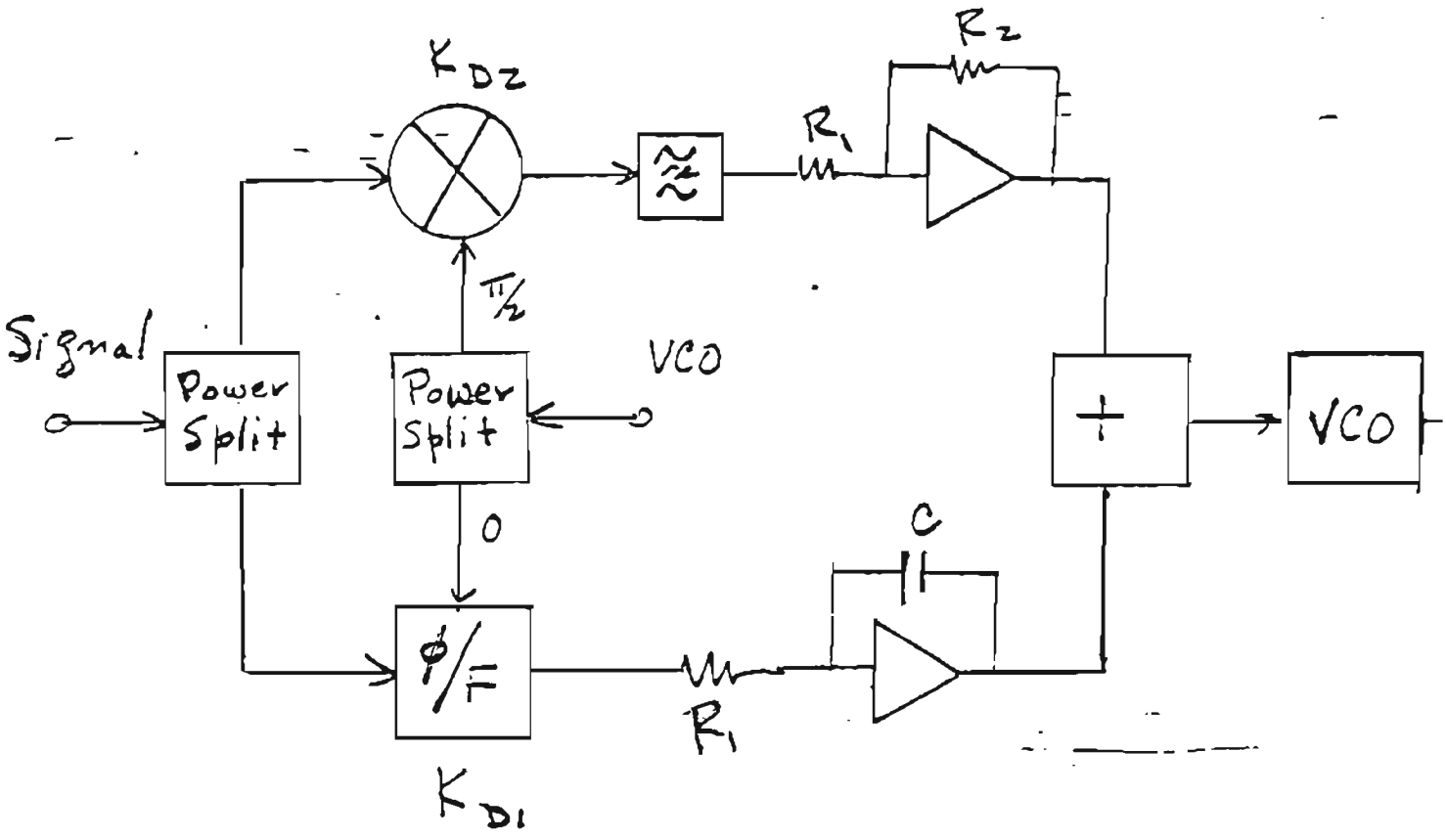
SOLUTION:

$$\frac{\Delta\omega_{max}}{\omega_0} = 4\times10^{-3}, \quad \frac{K_3}{\omega_0} = \frac{10^{-3}}{5} = 2\times10^{-4}$$

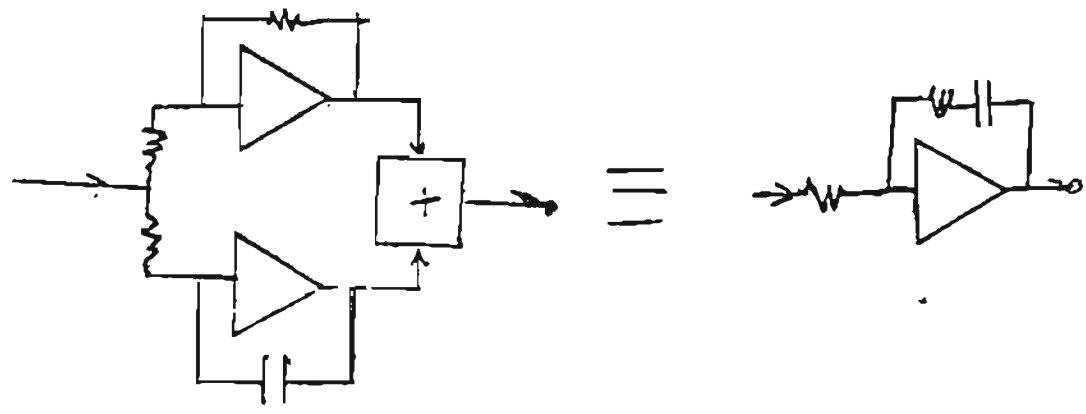
$$V_{DC} = 2\times10^{-3}$$

$$K_{2\,MAX} = \frac{\Delta\omega_{max}}{\omega_0} \Big/ V_{DC}\,\frac{K_3}{\omega_0} = \frac{4\times10^{-3}}{4\times10^{-7}} = 10$$

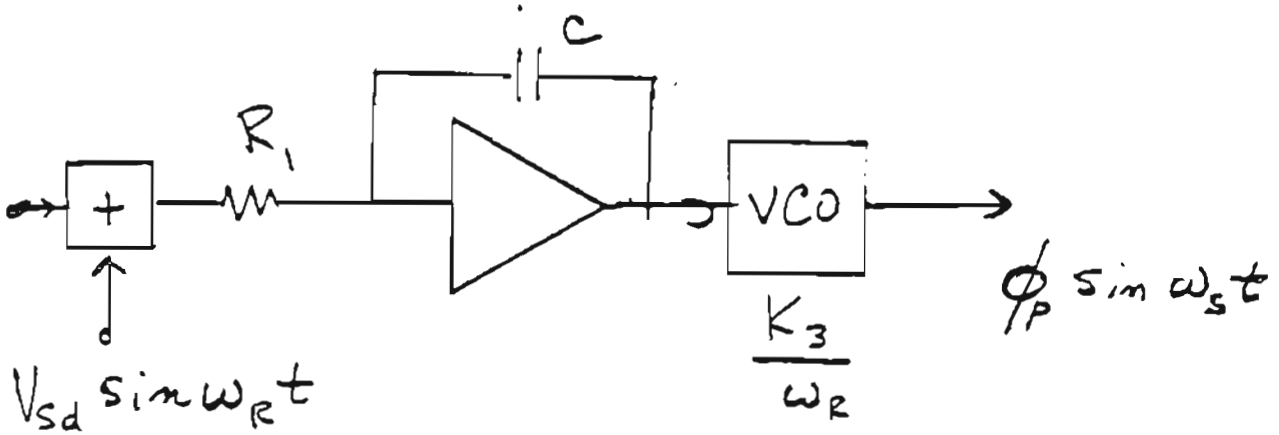
A COMPOUND PHASE DETECTOR FOR REDUCED SPURIOUS SUSCEPTABILITY



FROM: THE EQUIVALENCE OF INTEGRAL PLUS PROPORTIONAL



SUSCEPTABILITY TO FUNDAMENTAL



$$\frac{\phi_p}{V_{sd}} = \frac{1}{\omega_R \tau_1} \cdot \frac{K_3}{\omega_R} \quad \text{in} \quad \frac{\text{Rads}}{V}$$

$$\tau_1 = \frac{K_1 K_3}{M} \frac{1}{\omega_n^2}$$

$$\frac{\phi_p}{V_{sd}} = \left(\frac{\omega_n}{\omega_R}\right)^2 \frac{M}{K_1}$$

REJECTION OF FUNDAMENTAL:

$R = 40 \log \frac{wr}{wn} + 20 \log K, - 20 \log M$

PROBLEM

2. IN THE COMPOUND PHASE DETECTOR, GIVEN T_1 AND T_2 IN THE INITIAL ACTIVE FILTER ASSOCIATED WITH K_{d1}

   (a) DETERMINE THE GAIN FACTOR $\frac{R_2}{R_1}$

   (b) ASSUME THAT fn IS 1/30 of THE REFERENCE FREQUENCY fr, $K_1 = 0.1$ V/RAD and M = 10. DETERMINE REJECTION OF THE FR COMPONENT.

SOLUTION

(a) when fb $\longrightarrow \infty$

$$K_{d1} \frac{T_2}{T_1} = K_{d2} \frac{R_2}{R_1}$$

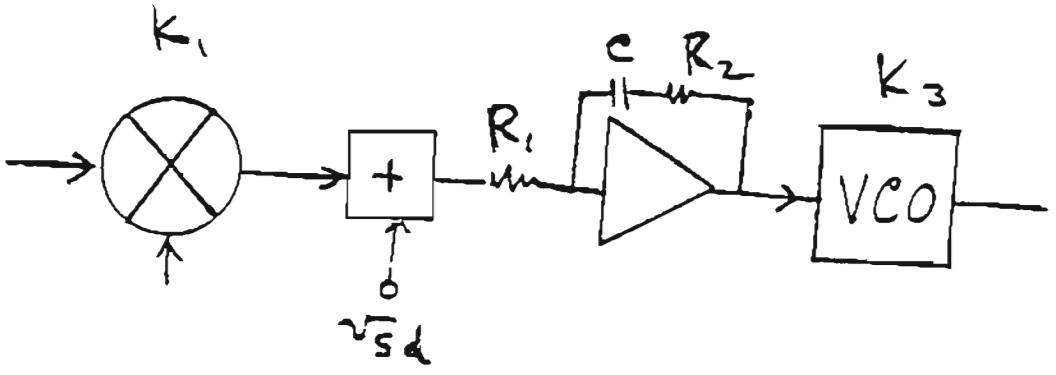
$$\frac{R_2}{R_1} = \frac{K_{d1}}{K_{d2}} \frac{T_2}{T_1}$$

(b) $R = 40 \log 30 + 20 \log 0.1 - 20 \log 10$

$R = 59 - 20 - 20 = 19dB$

OUT OF BAND SPURIOUS SUSCEPTABILITY

IN ABSENCE OF PREFILTER



OUT-OF-BAND

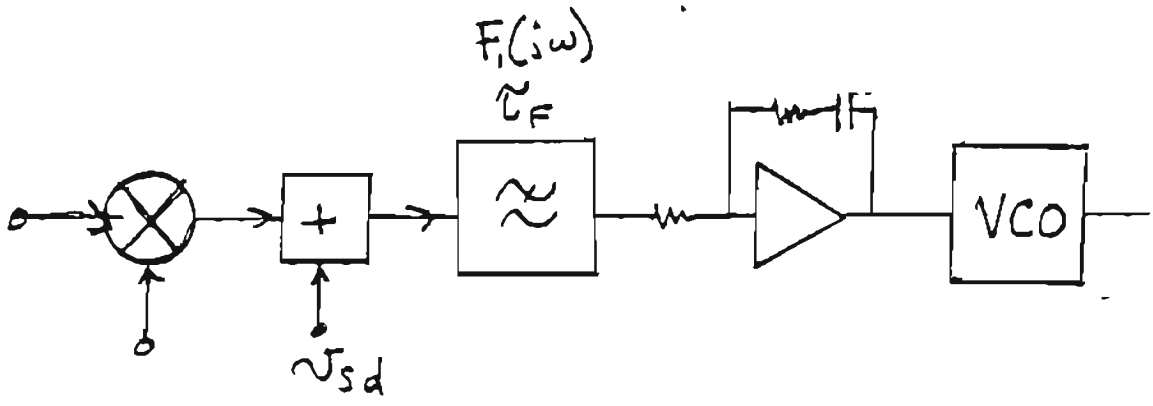
$$\Delta F(t) = A K_3 v_{sd}(t)$$

$$\underset{f \to \infty}{A} = \frac{\tau_2}{\tau_1} = \frac{2\zeta\omega_n}{K_1 K_3} M$$

$$\Delta F(t) = 2\zeta\omega_n M \frac{v_{so}(t)}{K_1}$$

$$\Delta\phi(t) = \int \Delta F(t)\, dt$$

THE PREFILTER



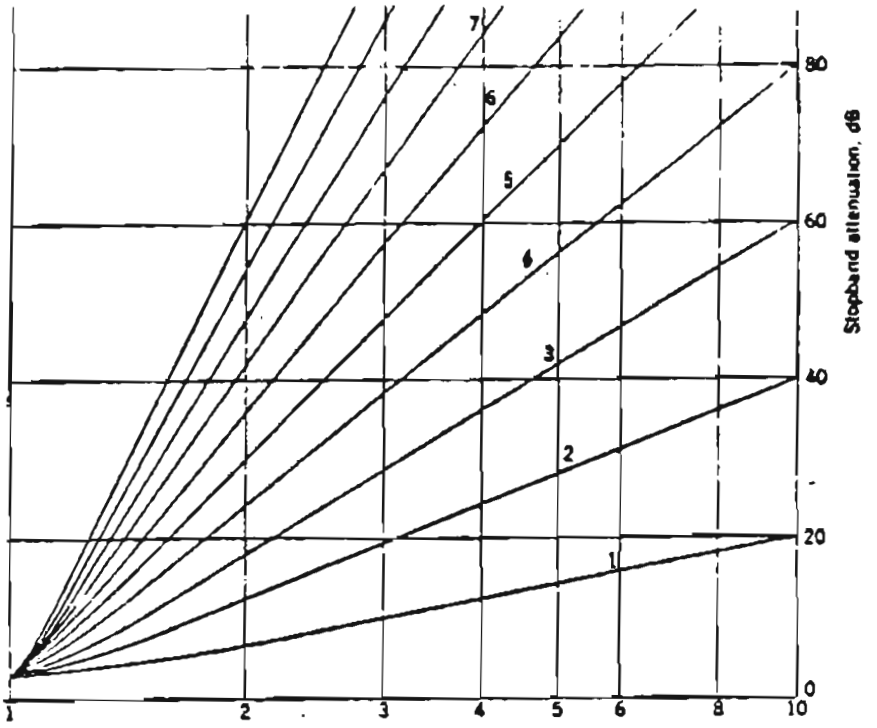
GENERAL CONDITIONS

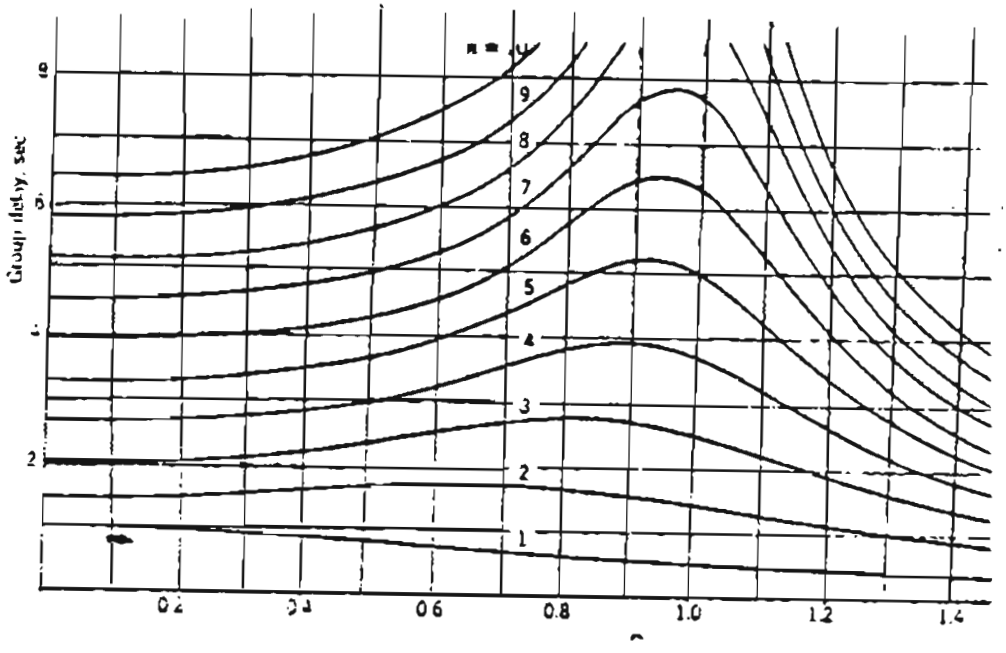
B - NOMINAL BANDWIDTH OF PREFILTER

$$f_n << B << F_r$$

IN-BAND THE FILTER APPEARS AS A DELAY ELEMENT, PRODUCING EXCESS PHASE SHIFT AT BASEBAND;

$$\Delta\theta = w_b T_f$$

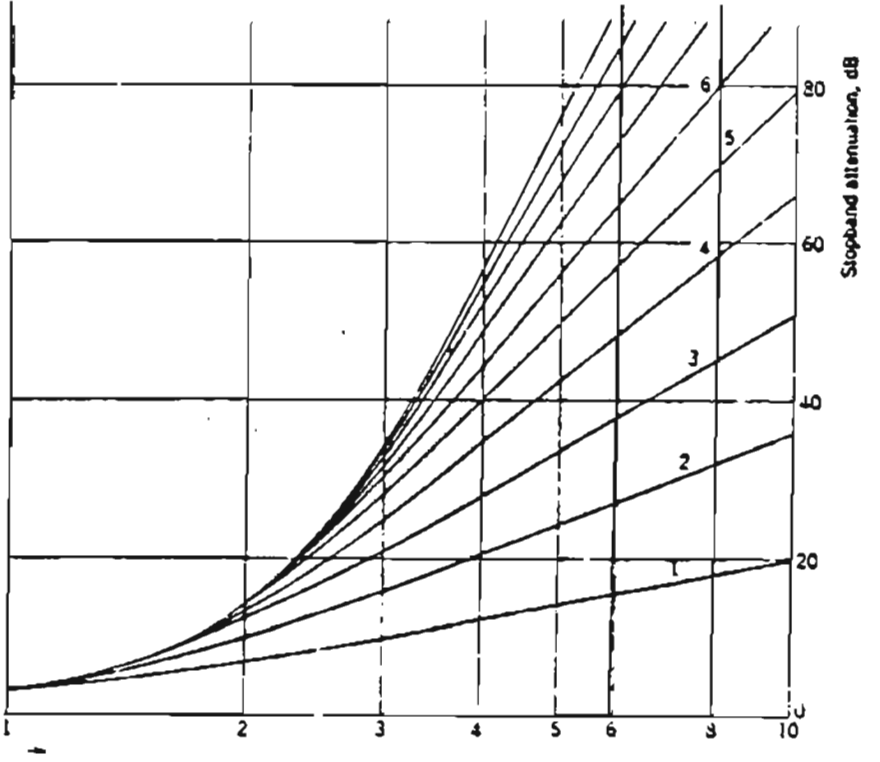


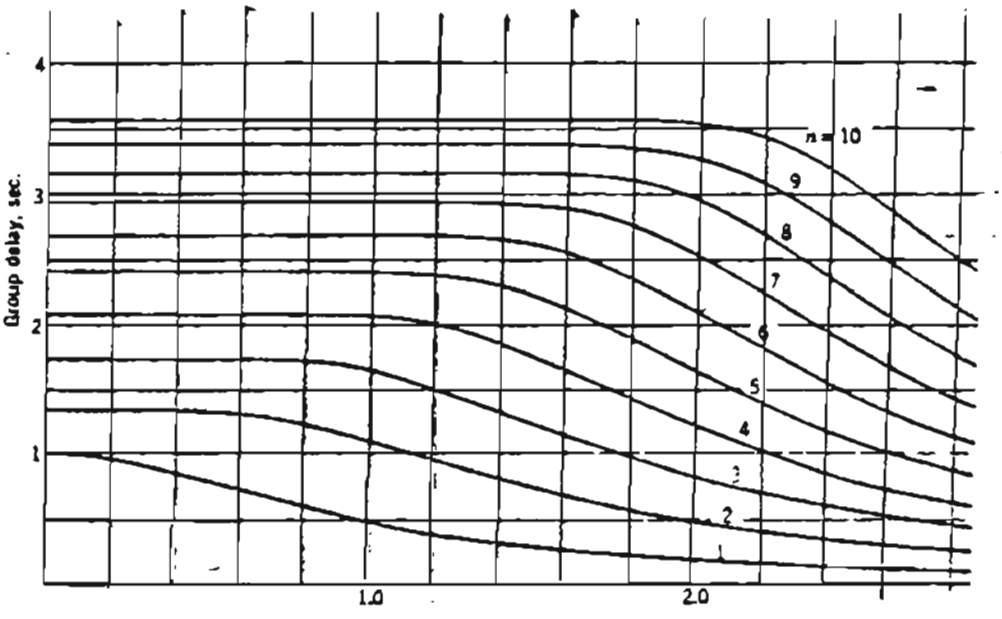


Butterworth Filter Attenuation and Group Delay Characteristics. Normalized to 1 Rad/sec Bandwidth.

27
F

Ref. 11





Bessel Filter Characteristics

FILTER TYPE	PREFILTER DELAY PERFORMANCE Required fundamental rejection-40dB number of poles-3 BANDWIDTH	IN-BAND DELAY, T_f	DELAY PEAK Tp/Tf	PULSE ATT. AT 1 RAD. PHASE ERROR
SYNCHRONOUS RC	0.11	2.15	----	35 dB
BUTTERWORTH	0.2	1.43	1.4	30
0.1 dB CHEBYSHEV	0.25	1.4	1.7	28
0.5 dB CHEBYSHEV	0.29	1.4	1.7	27
6dB GAUSSIAN	0.17	1.59	---	31
12 dB GAUSSIAN	0.17	1.72	---	31
BESSEL	0.15	1.75	---	32

NOTES:
1. Bandwidth normalized to reference freq. Fr
2. Delay normalized to ref. period $\frac{1}{Fr}$
3. When phase error in Ø/F detector is below one RAD, the pulse amplitude attenuation increases at the rate of 20 log $\frac{1}{\emptyset_e}$

FILTER TYPE	PREFILTER DELAY PERFORMANCE Required fundamental rejection-40dB number of poles- ϵ			
	BANDWIDTH	IN-BAND DELAY, T_f	DELAY PEAK Tp/Tf	PULSE ATT. AT 1 RAD. PHASE ERROR
SYNCHRONOUS RC	0.18	1.93	---	30
BUTTERWORTH	0.45	1,37	1.7	23
0.1 dB CHEBYSHEV	0.59	1.35	2.8	21
0.5 dB CHEBYSHEV	0.63	1.27	3.2	20
6dB GAUSSIAN	0.42	1.45	1.6	23.5
12 dB GAUSSIAN	0.31	1.43	1.1	26
BESSEL	0.27	1.58	---	27

NOTES:
1. Bandwidth normalized to reference freq. Fr
2. Delay normalized to ref. period $\frac{1}{Fr}$
3. When phase error in Ø/F detector is below one RAD, the pulse amplitude attenuation increases at the rate of 20 log $\frac{1}{\emptyset_e}$

FILTER TYPE	PREFILTER DELAY PERFORMANCE Required fundamental rejection-60dB number of poles-6			
	BANDWIDTH	IN-BAND DELAY, T_f	DELAY PEAK Tp/Tf	PULSE ATT. AT 1 RAD. PHASE ERROR
SYNCHRONOUS RC	0.11	3.15	----	35 dB
BUTTERWORTH	0.3	1.98	1.7	27
0.1 dB CHEBYSHEV	0.42	1.91	2.8	23.5
0.5 dB CHEBYSHEV	0.48	1.75	3.2	22
6dB GAUSSIAN	0.29	1.57	1.6	27
12 dB GAUSSIAN	0.22	1.57	1.1	29
BESSEL	0.18	2.36	---	31

NOTES:
1. Bandwidth normalized to reference freq. Fr
2. Delay normalized to ref. period $\frac{1}{Fr}$
3. When phase error in Ø/F detector is below one RAD, the pulse amplitude attenuation increases at the rate of 20 log $\frac{1}{Ø_e}$

CONCLUSIONS

WHEN THE FUNDAMENTAL REJECTION IS PREDETERMINED, DELAY IS LEAST WHEN:

1. Typically a multipole filter is better (6-poles is better than 3-poles)

2. A selective filter is preferred (Chebyshev is efficient, RC and Bessel filters are inefficient).

3. In using selective filters, the delay peak must be considered in any particular design.

4. The gaussian filter appears a good compromise choice.

LOOP DELAY, ITS SOURCES AND EFFECTS

SOURCES OF DELAY

- Propagation through divider chains
- Phase detector sampling process
- Group delay in filters
- Spurious poles

NET DELAY $T = Tr + Td + Tf + Ts$

IRREDUCIABLE DELAY IS Tr

$$T > Tr$$

EFFECT ON OPEN LOOP RESPONSE:

$$E^{-sT} \cdot F(s)$$

SIMPLE CORRECTION

Objective: Retain closed loop response associated with 0.707 damping factor. Approximating

$$E^{-sT} \approx \frac{1}{1 + s^T}$$

2nd order loop is transformed into

3rd order loop:

$$H(s) = \frac{K(s+s_2)}{Ts^3 + s^2 + Ks + Ks_2}$$

To retain $\zeta = 0.707$

(a) fn must be reduced

(b) ζ° must be increased

Example: $w_n T = 0.15$

fn is reduced by a factor of 0.87

ζ is increased by 1.01

Ref. 8

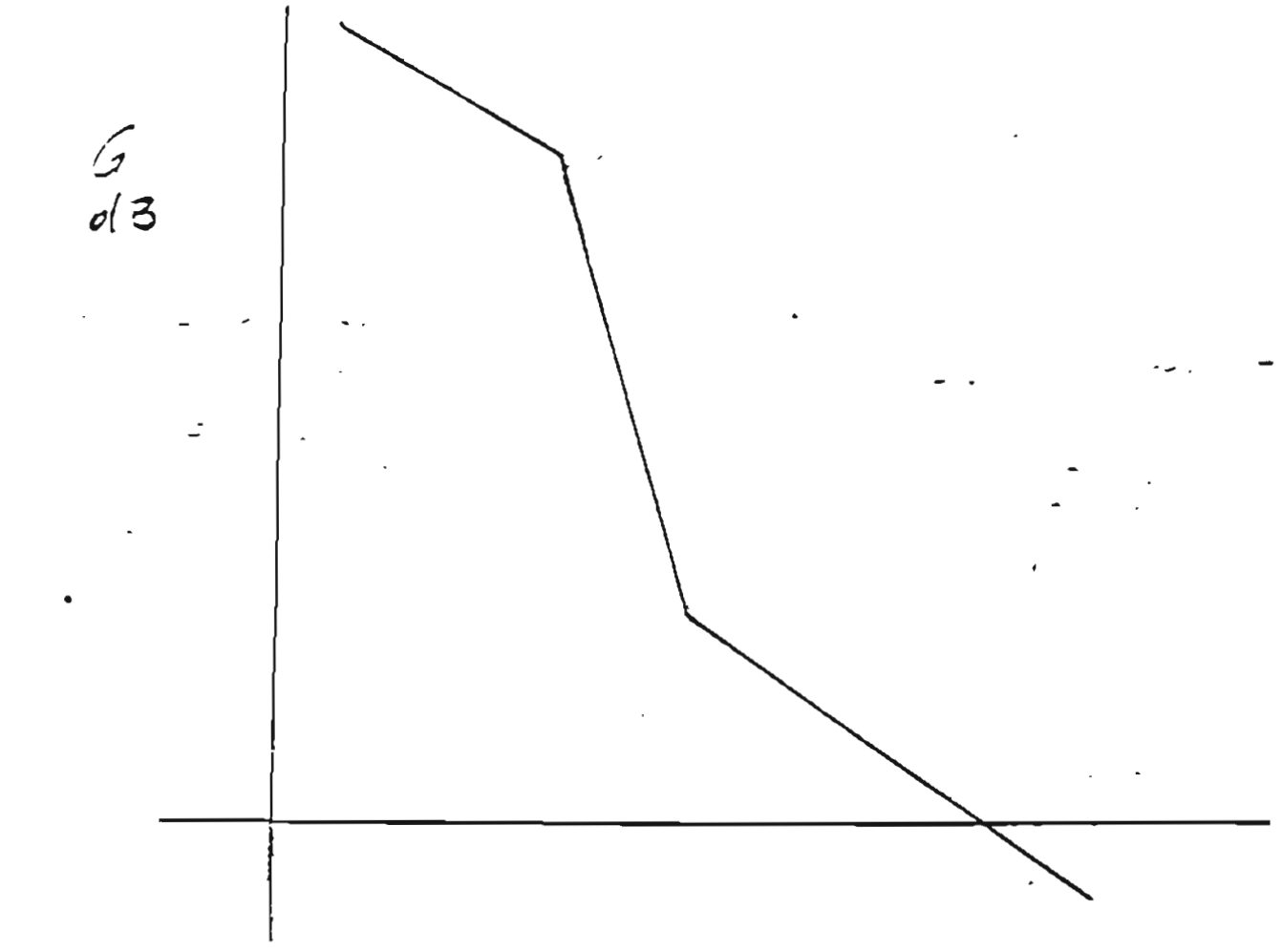
PROBLEM

LET EXCESS PHASE AT wn BE LIMITED TO LESS THAN 0.2 RADS.

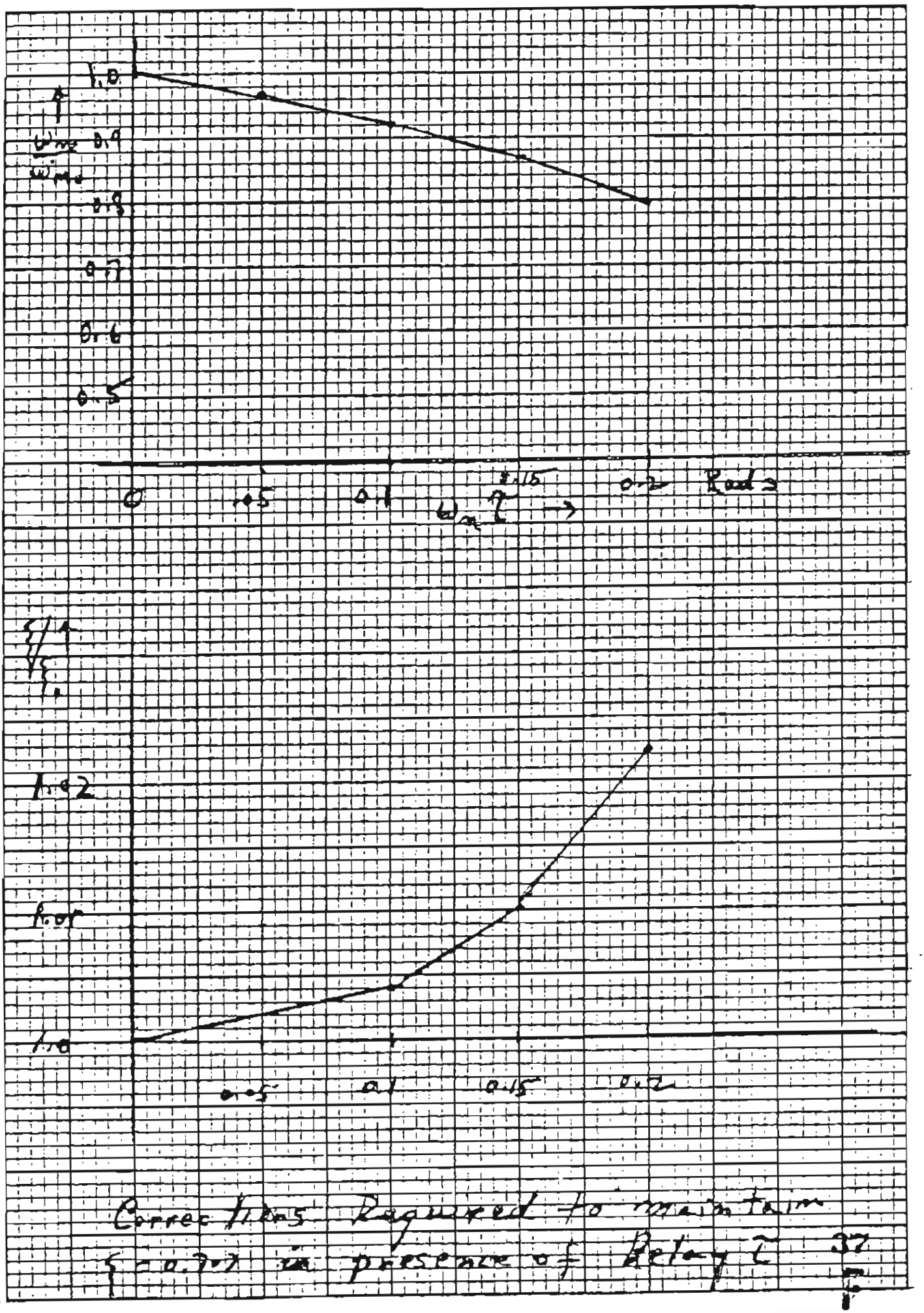
ASSUME THAT SPURIOUS DELAY $T = 1.5\ T_r$, such that the net delay $T_. = T_r + T = 2.5\ T_r$, what is maximum fn?

SOLUTION:

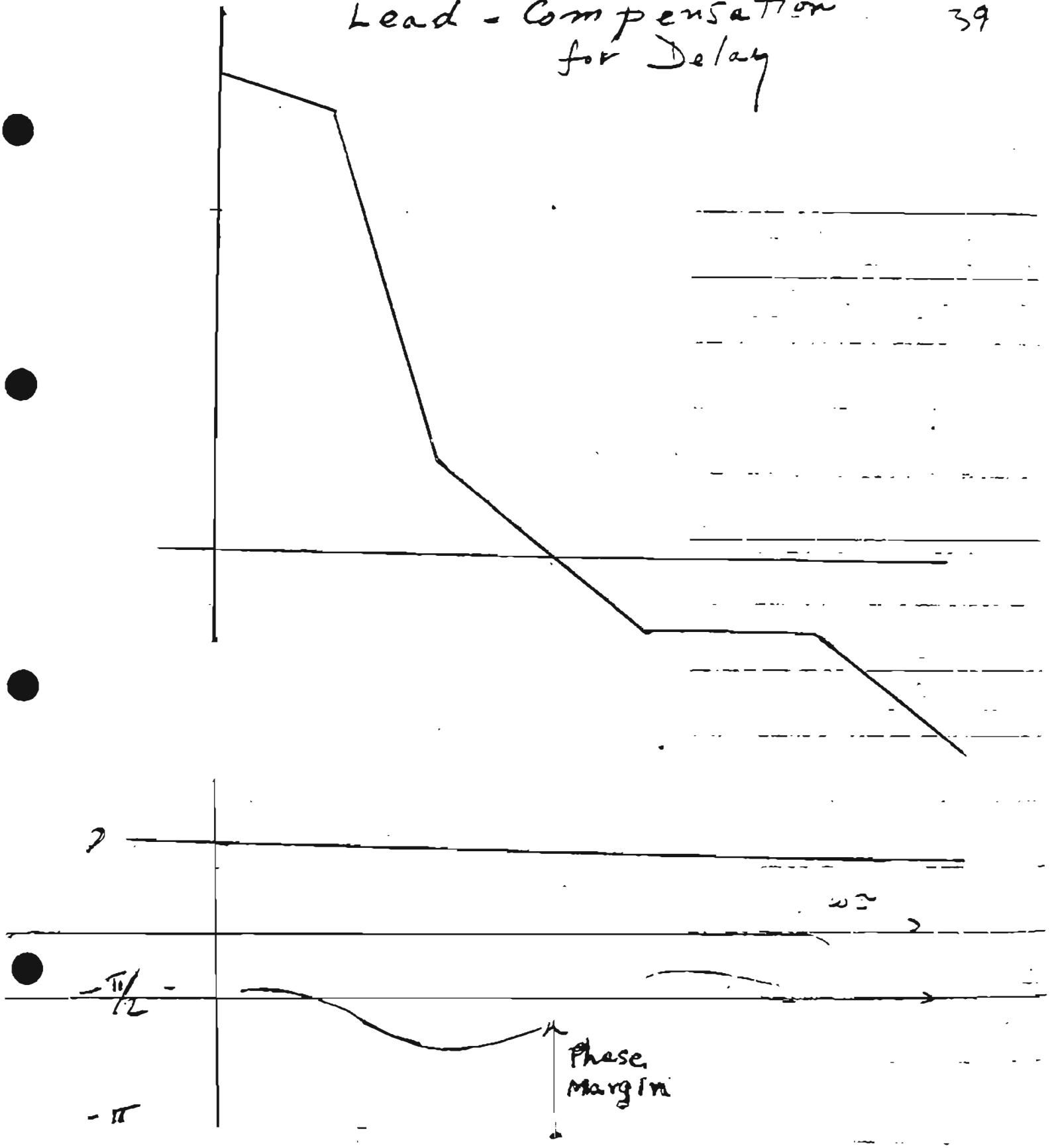
$$fn = \frac{0.2}{2TT \times 2.5T_r} = 0.0127\ F_r$$



Bode - interpretation of delay of . . .



Lead - Compensation for Delay



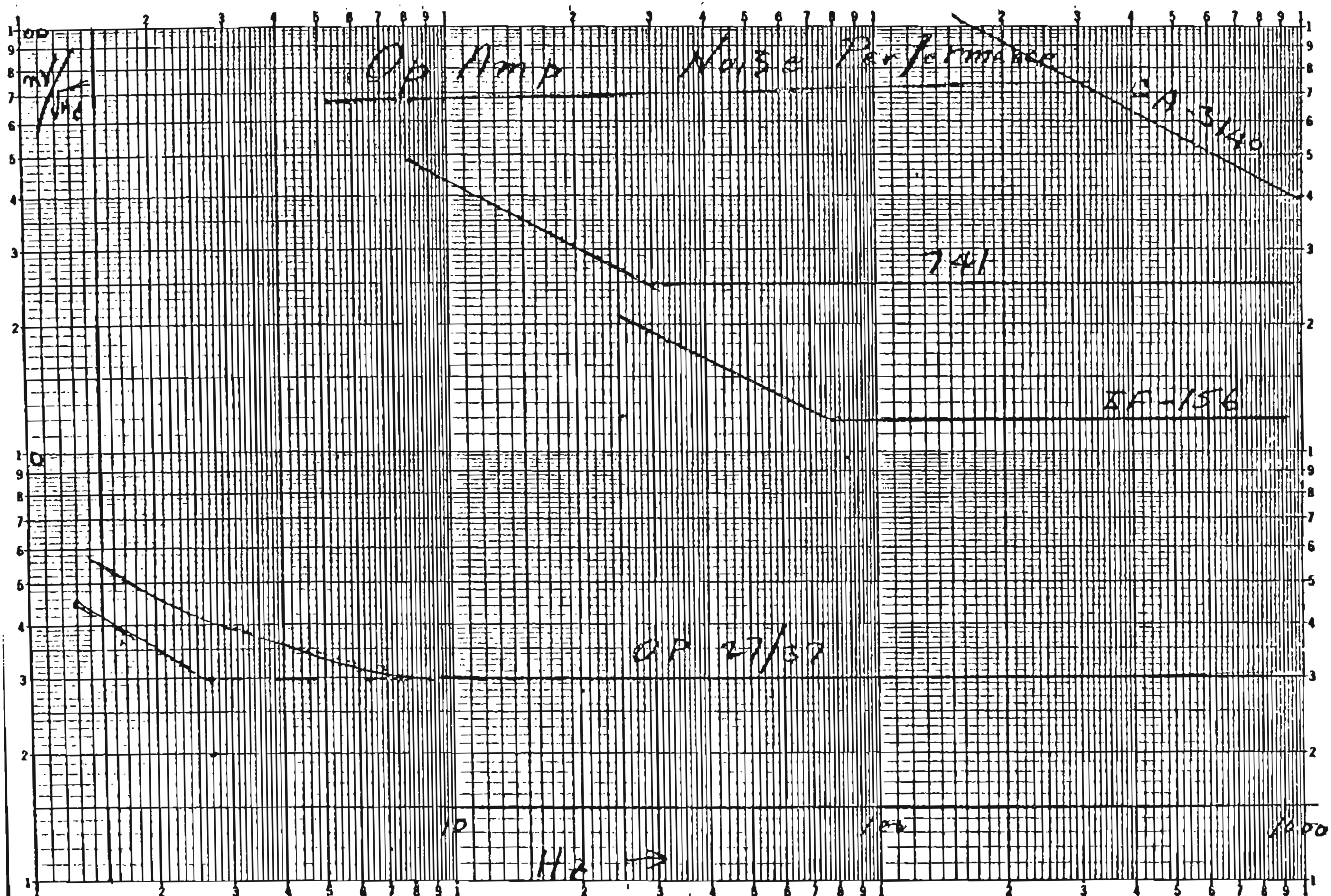
OPERATIONAL AMPLIFIER NOISE SUSCEPTIBILITY

CONTRIBUTION TO VCO NOISE

In-band: $\left(\frac{M}{K_1}\right)^2 \overline{na}^2$

Out-of-band: $\left(\frac{MK}{K_1}\right)^2 \frac{\overline{na}^2}{W_b^2}$

K+E LOGARITHMIC 46 7323
3 X 3 CYCLES MADE IN U.S.A.
KEUFFEL & ESSER CO.



45

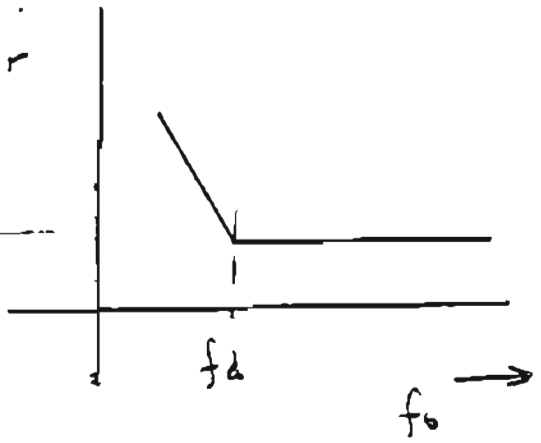
F

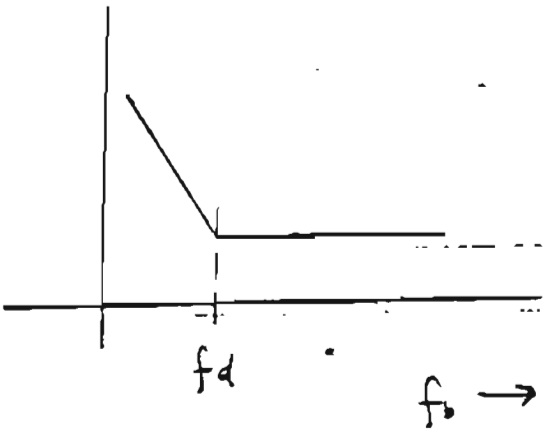
FREQUENCY AND PHASE NOISE POWER SPECTRA

OSCILLATOR

OSCILLATOR & RESONATOR

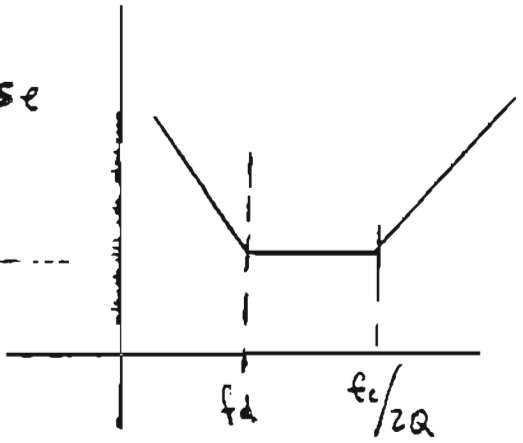
Amplifier Phase Noise

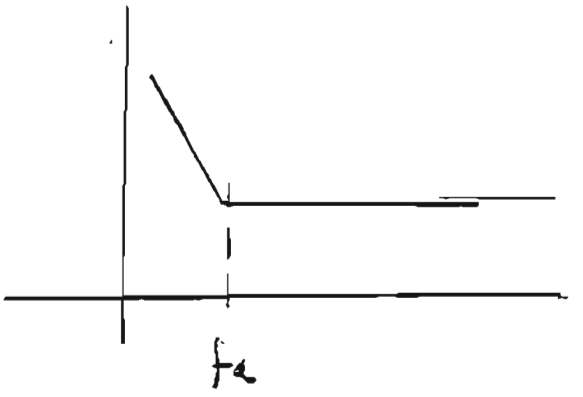




FM Noise

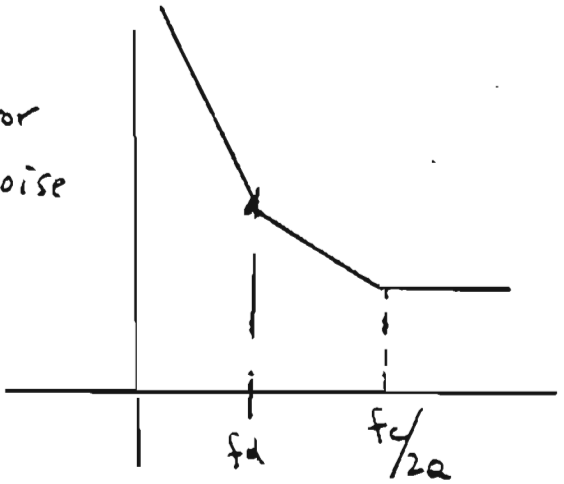
$\eta_f(f_0)$

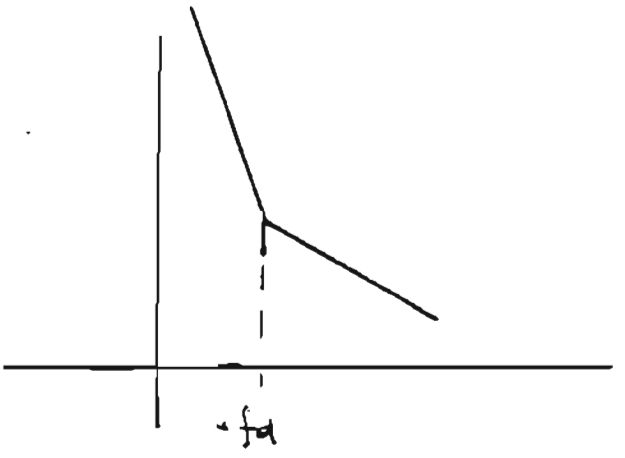




Oscillator Phase Noise

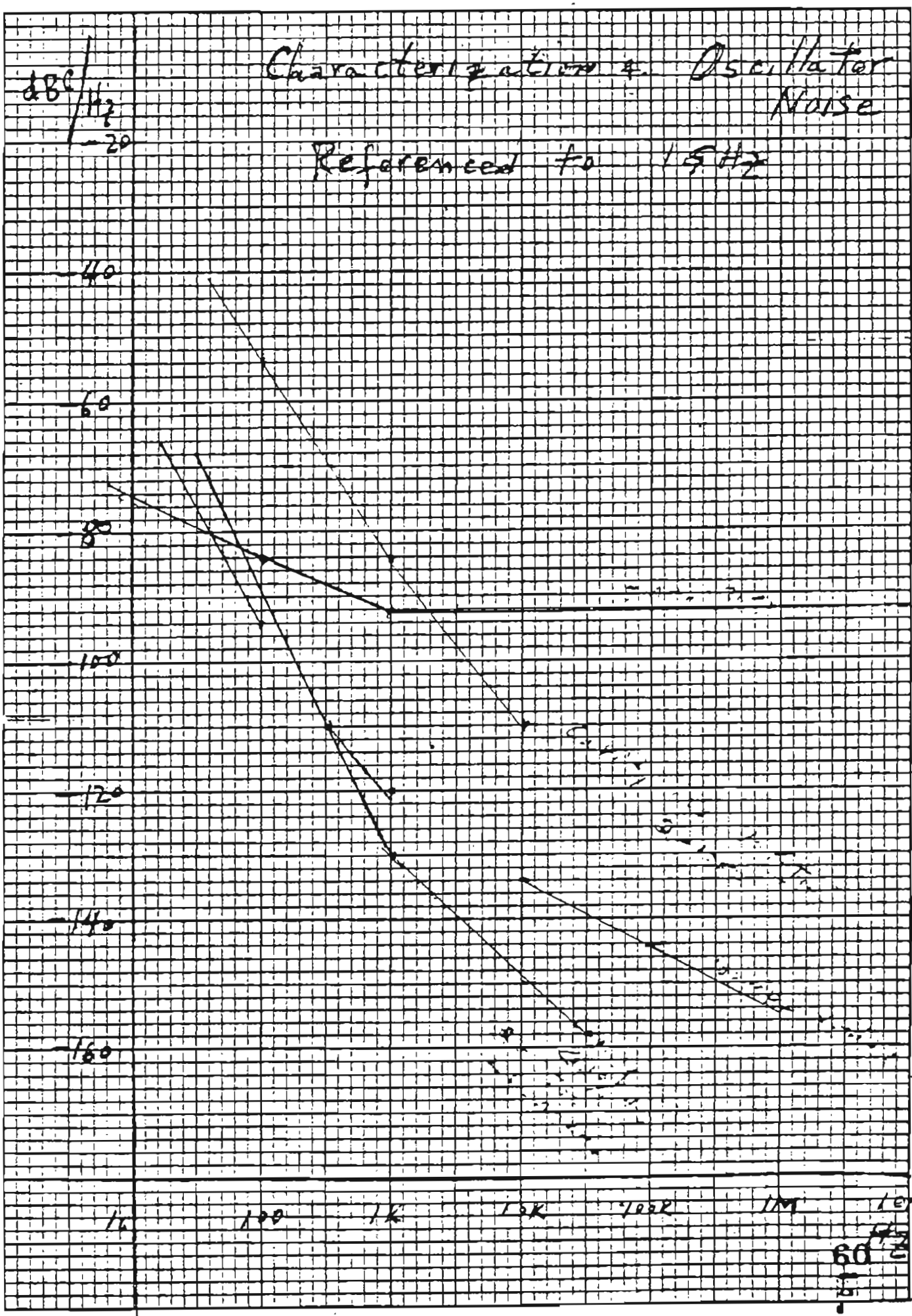
$\eta_\theta(f_3)$



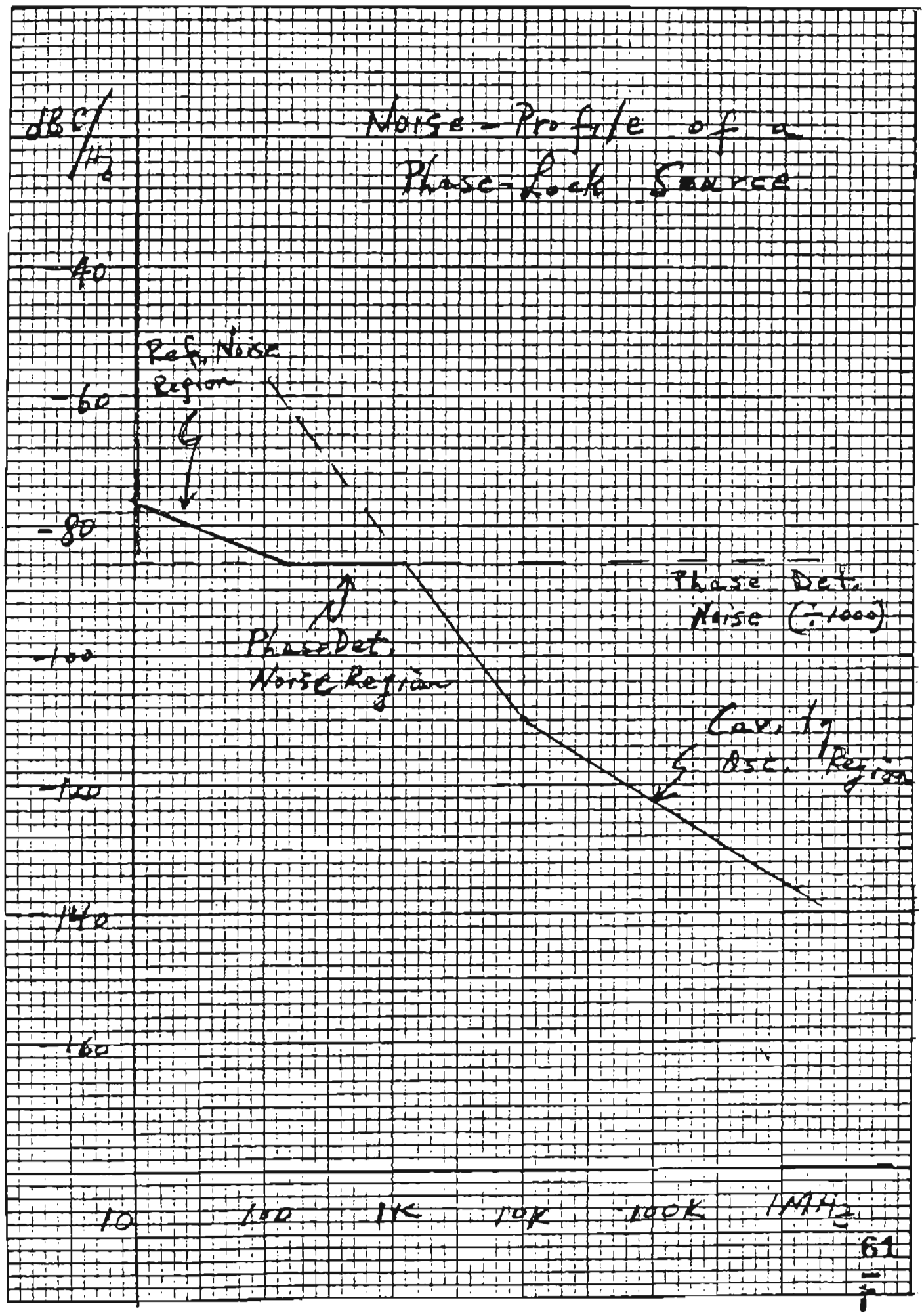


Characterization of Oscillator Noise

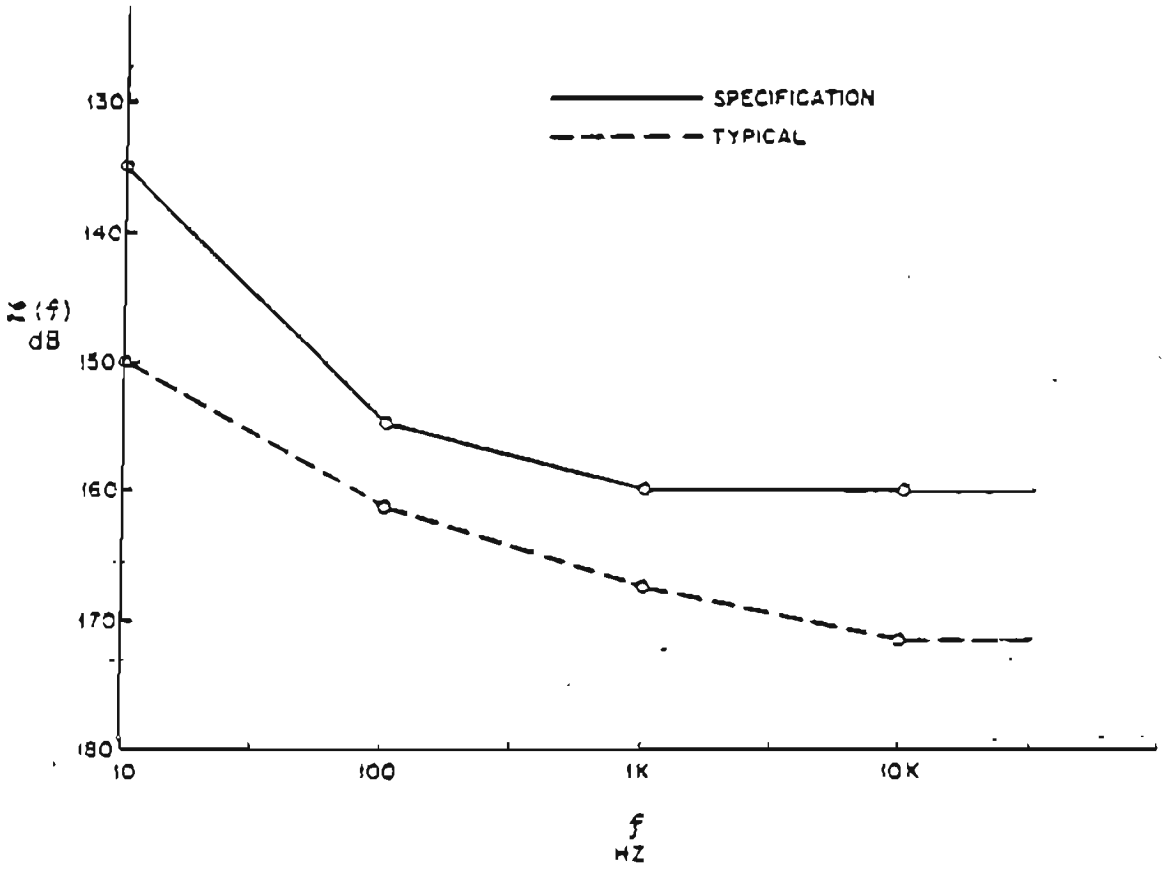
Referenced to 1 GHz



Normalized with respect to 1 GHz


Noise - Profile of a Phase-Lock Source
dBc/Hz
-40
-60
-80
-100
-120
-140
-160
Ref. Noise Region
Phase Det. Noise Region
Phase Det. Noise (÷1000)
Cavity Osc. Region
10
100
1K
10K
100K
1MHz

THE DIVIDER THAT WORKS AT HIGHEST FREQ. HAS HIGHEST NOISE



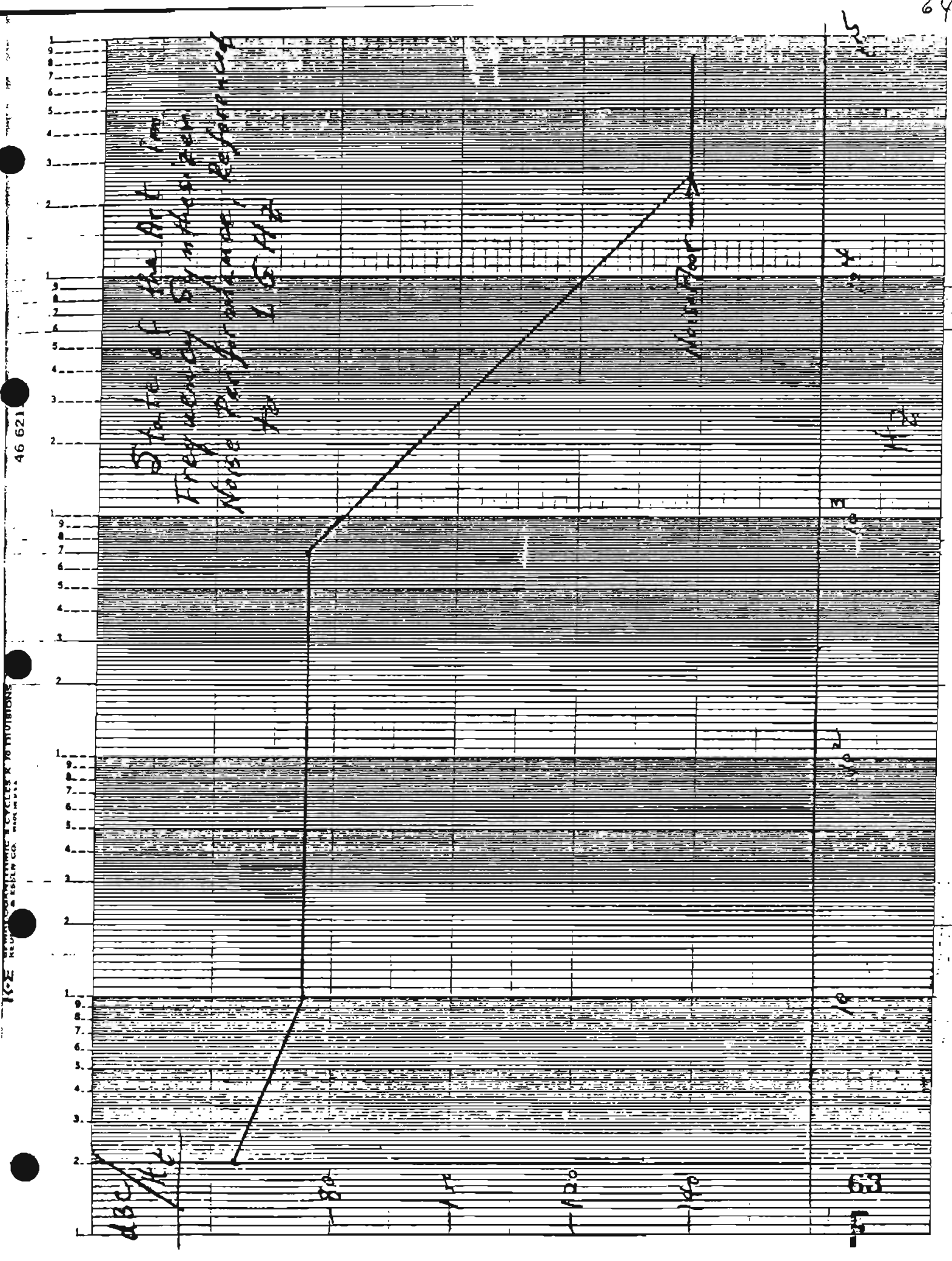
STATE-OF-THE-ART in 10MHz

CRYSTAL OSCILLATOR REFERENCE

Ref. noise is ultimate limit.

Add 40dB to get with respect to 1GHz.

HP now has better reference.


46 6211
63

PROBLEM:

The following characteristics are typical for phase lock components:

ECL DIVIDER:	- 155 dBC/Hz
TTL DIVIDER:	- 170 dBC/Hz
Phase/Frequency DETECTOR:	- 130 to -146 dBC/Hz
	Assume -130 dBC/Hz
10 MHz CRYSTAL REFERENCE:	- 155 dBC/Hz and a corner frequency of 500 Hz

The VCO operates at 1GHz and its spectral characteristics are as follows:

OFFSET FROM CARRIER	dBC/Hz
100 Hz	-46
300 Hz	-60
1 KHz	-80
3 KHz	-90
10 KHz	-100

GIVEN A DIVISION OF ÷ 100

DETERMINE

a - Optimum fn
b - Net Spectral Noise Density
c - Sketch Resultant Spectral Noise Density
d - Estimate Net Integrated Phase Jitter in degrees

SOLUTION

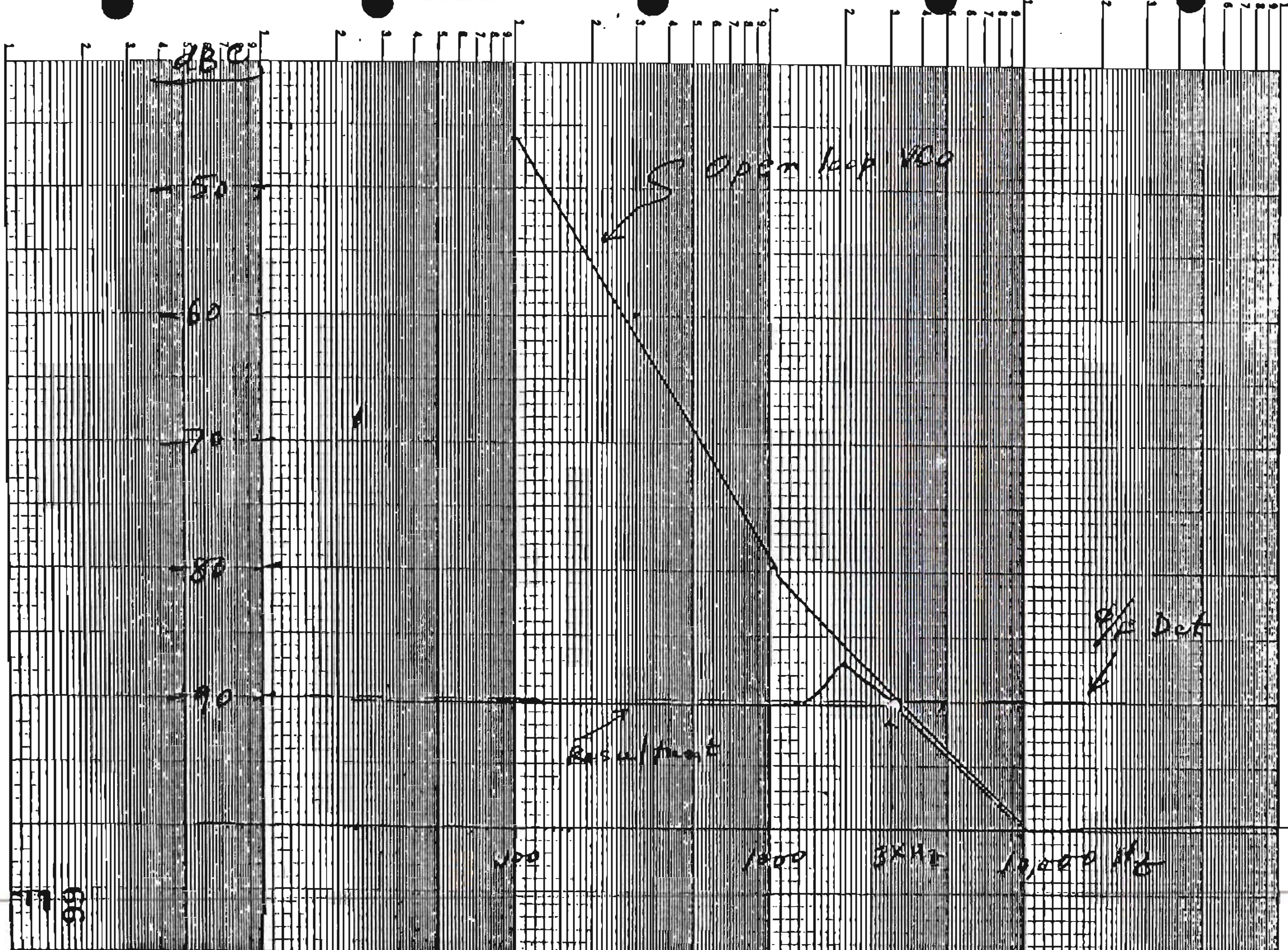
The circuit noise is dominated by the phase / frequency detector contribution which translates to -90 dBC/Hz at 1GHz.

a. From the intersection in the graph, the optimum fn is approximately 3KHz.

b. The net spectral density rises to -87dBC/Hz

d. On the basis of -87dBC/Hz and a 3KHz bandwidth.
The variance is: $2 \times 10^{-8.7} \times 3000\ RAD^2 = 1.2 \times 10^{-5} RAD^2$
The net phase jitter B = 3.5 m Rd = 0.2°

K+E SEMI-LOGARITHMIC 46 6212
5 CYCLES X 70 DIVISIONS
KEUFFEL & ESSER CO.



References

1. Gardner, F. M.: Phaselock Techniques, John Wiley,2nd Ed.

2. Klapper, J., Frankle, J.: Phase Locked and Frequency Feedback Systems, Academic Press, 1972.

3. Blanchard, A.: Phase-Locked Loops, John Wiley, 1976.

4. Gardner, F. M.: Phaselock Up To Date, Seminar, Oct. 1979

5. Kurz, S. R.: Zero in on Mixer Phase Errors, Microwaves, Jan. 1979.

6. Kurz, S. R.: Specifying Mixers as Phase Detectors, Microwaves, Jan. 1979.

7. Zverev, A. I.: Handbook of Filter Synthesis, John Wiley, 1967.

8. Wetenkamp, S.: Combatting Phaselock Loop Transport Lag, MSN, March 1979.

9. Hutchinson, B.H.: Contemporary Frequency Synthesis Techniques, Lincoln Labs MIT Report, March 1972.

10. Altenbach, R. K.: Notes on FM Distortion in VCO, GR Experimenter, Sept. 1969.

11. Pelchat, G. M., et al.:Distortion in Vericap FM Oscillators, IEEE Transactions on Communication, Feb. 1969.

12. Noble, F. W.: Inductor Ups Crystal Bandwidth 2%, Electronic Design, March 1967.

13. Noble, F. W.: Need an Adjustable Crystal Oscillator?, Electronic Design , March 1967.

14. Designing Around Tuning Diode Inductance, Motorola Note #249.

15. Tuning Diode Design Techniques, Motorola Note #551.

16. Niehenke, E. C., Hess, R. D.: A Microstrip Low Noise VCO, IEEE Transactions PGMTT, Dec. 1979.

References, Cont.

17. Leeson, D.B.: A Simple Model of Oscillator Noise, IEEE Proc., Feb. 1966.

18. Kurakawa, K.: Injection Locking of Microwave Solid State Oscillator, IEEE Proc., Oct. 1973.

19. Scherer, D.: Low Noise Design, Microwaves, April/May 1979.

20. Alley, G. D.: An Ultra Low Noise Microwave Synthesizer, IEEE, MTT, Dec. 1979.

21. Payne, J.B.: Synthesizer Designs Depend on Satcom, Microwaves, March 1980.

22. Winchell, D.: Single Loop Synthesizer, Microwaves, March 1980.

23. Telewski, F.: Delay Lines Give RF Generator Spectral Purity, Electronics, Aug. 28, 1980.

24. Egan, W.: Frequency Synthesis by Phaselock, John Wiley, 1980.