PACIFIC MONOLITHICS®

A Division of Richardson Electronics

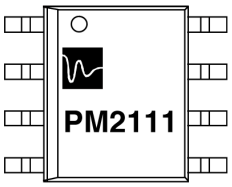
# PM 2111

# DATA SHEET

## Single Supply RFIC Power Amplifier
## 800 - 1675 MHz Operation

## Features

- **>30 dBm Output Power @ 5V**
- **Single 3V to 5V Supply - Class A Operation**
- **Linear Class AB Operation (requires -$V_{GG2}$)**
- **50% Efficiency**
- **Unconditionally Stable**




**SO-8 Plastic Package**

## Applications

- **Wireless Data Collection**
- **Cellular & Cordless Telephones**
- **Mobile Satellite Communications**

### Description

The PM2111 is a two stage high-efficiency GaAs FET RFIC power amplifier designed for wireless applications with 850 MHz to 1650 MHz center frequencies, where greater than 50 MHz bandwidths are achieved using external matching components.

In a single supply mode both stages of the PM2111 are inherently biased for (saturated) Class A operation and the current will remain constant, or increase slightly under input power back-off. By applying a negative voltage to $V_{GG2}$ a more linear, Class AB operation is possible, reducing current consumption when in an idle or backed-off input power mode. Using the PM2111 in this Class AB mode has an advantage over traditional deep depletion mode devices since it does not require two negative supply voltages or sequencing circuits for safe and proper operation.

### Electrical Characteristics

Typical values specified for $f$ = 1675 MHz, $V_{DD}$ = 5.0V, $T_A$ = +25°C, unless otherwise noted.

**Minimum and Maximum Specifications are Guaranteed over Frequency and Temperature.**

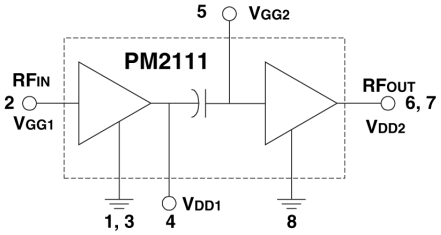
Tested in a 50Ω system using the external circuits shown on page 3.

| Characteristics | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Frequency Range | $f$ | | 800 | | 1675 | MHz |
| Small Signal Gain | G | $P_{IN}$ = -10 dBm | | 29.0 | | dB |
| Input Return Loss | RL | | | -15.0 | | dB |
| Power Output ($P_{1dB}$) | $P_{1dB}$ | | | 29.5 | | dBm |
| Power Output (saturated) | $P_{SAT}$ | $P_{IN}$= +5 dBm, $f$ = 915 MHz | | 31.0 | | dBm |
| Power Output (saturated) | $P_{SAT}$ | $P_{IN}$= +5 dBm, $f$ = 1675 MHz | 29 | 30.5 | | dBm |
| Power Added Efficiency | η | $P_{IN}$= +5 dBm, $f$ = 1675 MHz | 40 | 50 | | % |
| Drain Current | $I_{DD}$ | $P_{IN}$= +5 dBm | | 500 | 600 | mA |
| Load VSWR for Output Stability | VSWR | Source VSWR < 1.2:1 | | 10:1 | | |
| Thermal Resistance | $\theta_{JC}$ | Junction to GND | | 35 | | °C/W |

## Absolute Maximum Ratings

| Characteristics | Symbol | Value | Units |
|---|---|---|---|
| Drain Voltage | $V_{DD}$ | +9.0 | V |
| Power Dissipation | $P_{DISS}$ | 1.9 | W |
| Load VSWR | VSWR | 10:1 | |
| RF Input Power | $P_{IN}$ | +10.0 | dBm |
| Operating Temperature | $T_{OP}$ | -40 to +85 | °C |
| Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | °C |

Caution: Operating beyond the specified rating for any of these parameters may cause permanent damage to device.

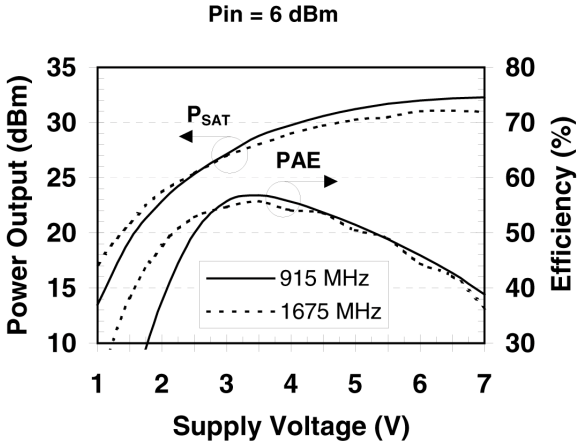



Note: Pins 1, 3 and 8 are common to the metal bottom side of package.

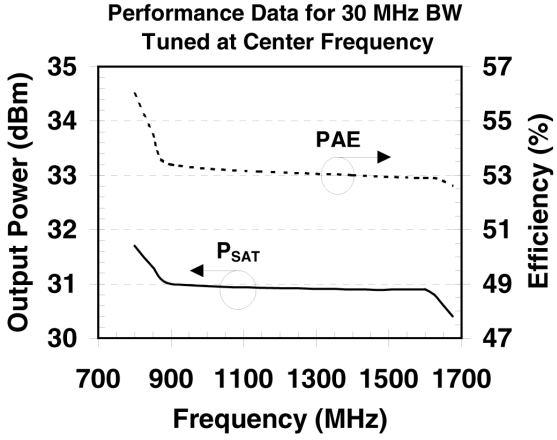
## Typical Performance Characteristics

**Obtained using external circuits shown on page 3.**

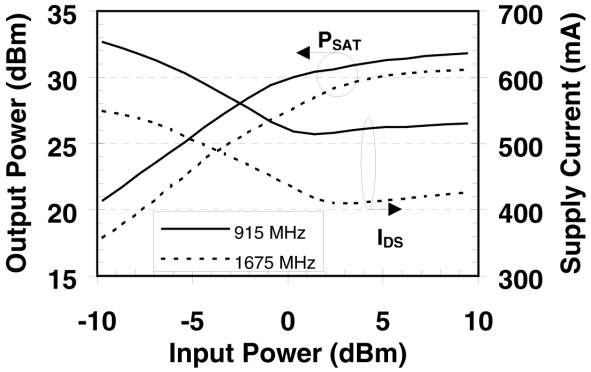
### RF Power and PAE vs. Supply Voltage



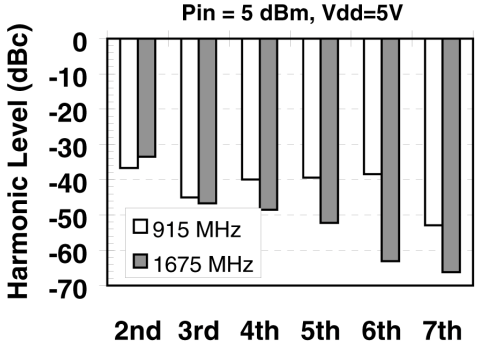

### Power and Efficiency vs. Frequency




### Output Power and Supply Current vs. Input Power

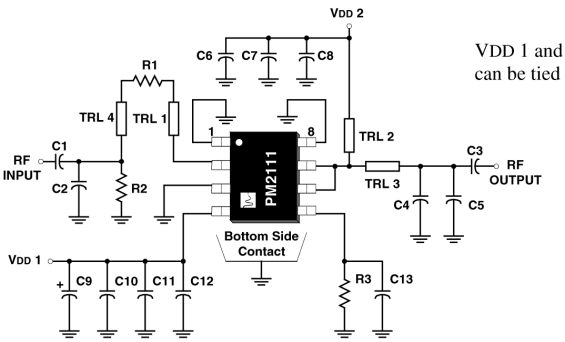



### Harmonic Levels at $P_{SAT}$



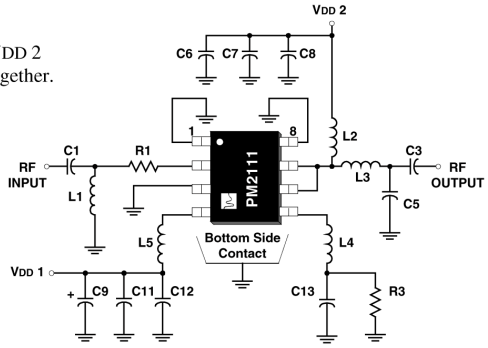
# Recommended Matching Networks for the PM2111

**1550 - 1675 MHz Schematic**



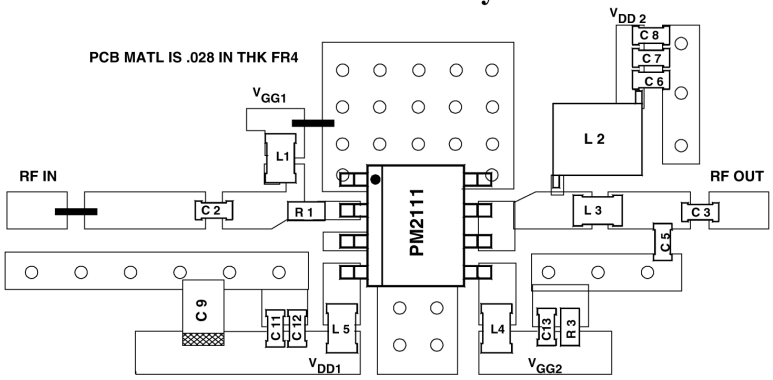

VDD 1 and VDD 2 can be tied together.

**800 - 950 MHz Schematic**

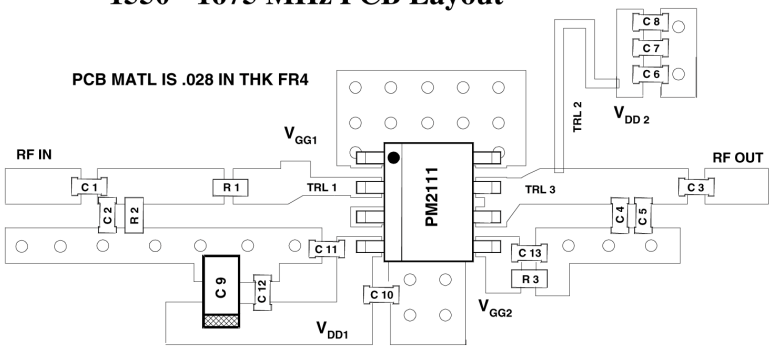



Note: For Class AB Operation R3 is connected to $V_{GG2}$ rather than to ground.

## 800 - 950 MHz PCB Layout




## 1550 - 1675 MHz PCB Layout



## Application Information

The metalized bottom side contact area of the amplifier and the associated matching networks must have a continuous ground plane or the amplifier performance may be degraded. Terminate pins 1, 3, 8 and package base to a common ground pad. This ground pad must provide a connection to the back side of the ground plane with plated via holes. It is important to provide a good thermal path for the PM2111 since the device can dissipate up to 1.9 Watts of continuous average power.

The PM2111 requires external input, output, and interstage matching for proper operation. The input match is accomplished using C2 , L1, R1 and TRL1. R1 also serves to reduce low frequency gain and improve stability. R2 is a DC return for the gate of the first stage FET at 1675 MHz. R3 and C13 limits the gate current and is only required if $P_{IN}$ exceeds 5 dBm. The interstage matching consists of L4 and L5. Output power match is achieved using L3/TRL3, C4, and C5. L2 must be able to support DC current in excess of 700 mA to insure reliable operation. Extensive bypassing is recommended for linear digitally modulated applications requiring good IMD performance. In addition, a negative bias voltage may be applied to $V_{GG2}$ (pin 5) for class-AB operation. In this mode, no power sequencing is required to eliminate excess current draw prior to the application of sufficient gate voltage. The typical pinch-off voltage is -0.6V. $V_{GG2}$ of -0.4V provides idle currents below 200 mA.

### List of Components

| 800-950 MHz | | 1550-1675 MHz | |
|---|---|---|---|
| **Part** | **Value** | **Value** | **Size** |
| C1 | 33 pF | 33 pF | 0603 |
| C2 | | 3.0 pF | 0603 |
| C3 | 33 pF | 3.0 pF | 0603 |
| C4 | | 1.2 pF | 0603 |
| C5 | 5.6 pF | 1.2 pF | 0603 |
| C6 | 33 pF | 33 pF | 0603 |
| C7 | 1000 pF | 1000 pF | 0603 |
| C8 | 0.1 µF | 0.1 µF | 0603 |
| C9 | 6.8 µF | 6.8 µF | 0603 |
| C10 | | 33 pF | 0603 |
| C11 | 33 pF | 33 pF | 0603 |
| C12 | 1000 pF | 0.1 µF | 0603 |
| C13 | 56 pF | 56 pF | 0603 |
| L1 | 12 nH | | 0805 |
| TRL1 | | θ = 15<br>*f* = 1675 MHz<br>Zo = 50Ω | |
| L2/TRL2 | 18.5 nH | θ = 39<br>*f* = 1675 MHz<br>Zo = 95 Ω | 0805 |
| L3/TRL3 | 1.8 nH | θ = 29<br>*f* = 1675 MHz<br>Zo = 50 Ω | 0805 |
| TRL4 | | θ = 16<br>*f* = 1675 MHz<br>Zo = 50 Ω | |
| L4 | 6.8 nH | | 0805 |
| L5 | 4.7 nH | | 0805 |
| R1 | 47 Ω | 5.1 Ω | 0603 |
| R2 | | 680 Ω | 0603 |
| R3 | 20 Ω | 20 Ω | 0603 |

## Package Specifications

### Pin Connections

| Pin # | Function |
|---|---|
| 1 | GND |
| 2 | $RF_{IN}/V_{GG1}$ |
| 3 | GND |
| 4 | $V_{DD1}$ |
| 5 | $V_{GG2}$ |
| 6 | $RF_{OUT}/V_{DD2}$ |
| 7 | $RF_{OUT}/V_{DD2}$ |
| 8 | GND |
| Base | GND |

**Part Number Marking System:**
The PM2111 shall be marked as follows:
Model Number:
PM2111
Lot Date Code:
YYWW

SO-8 Outline Drawing