TAPR FHSS Radio Project Status

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FHSS Radio Status

- **Focus has been on Digital Processor board:**
  - Most functions, parameters, status are controlled by VLSI devices with registers.
  - Need CPU operational to test almost anything.
- **RF board:** high-criticality area is initially the VCO’s - testing looks good.
VCO Status

• Two VCO’s used, alternate each 10 milliseconds.
  – Current settling time is ~ 6 milliseconds.
  – Leaves margin in timing.
  – Matches model developed.

• Spectrum of VCO looks good.

• Most significant sideband is VCO reference frequency.
  – about -60 dBc.
VCO Spectrum (not hopping)

10 dB/div

20 kHz. / div
Processor / Digital Board (Rev 2)
RF Board (Rev 1)
RF + Digital Board Connected
Testing the Digital Board
Software Status

- Ported XINU to TAPR board (currently running from DRAM).
  - Pre-emptive, prioritized, multi-tasking kernel.
  - Next effort is to move it to FLASH
- Ported Comer TCP/IP stack to TAPR board.
  - Re-written Ethernet and Serial device drivers, Timer driver, Initialization code.
  - Gateway router functionality + host interface.
- SNMP code ported to TAPR board (but not tested).
Software Status - 2

• Local console and Ethernet (10-base-T) interfaces are functional.
  – Can ‘PING’ in either direction (received, or console can initiate).

• VLSI device register test code written - implemented as UDP daemon.
  – Is a server to a client on a Win95 / NT host which provides graphical change/display of VLSI device contents.
Toolset

• Development to date has used SDSI compiler / assembler / linker / debugger.
  – Very powerful graphical debug capability through BDM interface.

• Software being ported to GNU environment.
  – GNU non-graphical debugger (BDM)
  – GNU compiler, linker, assembler

• Non-BDM Ethernet loader in development.
To Be Developed

- HTTP 0.9 daemon for initial configuration provisioning:
  - MAC address
  - IP address
  - Subnet mask
  - Default Gateway, etc.

- The radio code itself!