2.4GHz Direct Sequence Wireless LAN Cascade Analysis

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Abstract

The paper describes the cascade analysis of an IEEE 802.11 direct sequence wireless LAN radio in the 2.4GHz ISM band. A step by step approach is taken including: Basic system architecture decisions, gain distribution/IF limiter analysis and finally the complete cascade analysis. Important RF parameters for each function block in both the receive and transmit chains are evaluated and the design trade-offs are explored.

Introduction

Wireless Local Area Network (WLAN) is coming onto the marketplace with a flurry of products of various types and designs. Wireless offers a different paradigm for computer network users and capabilities breaking the tethers of the wired only network. This paper will explore the process of developing the architecture of one such WLAN system.

What should a WLAN radio do? What are the needs of the market place? What performance is possible in the technology? Where should the compromise between cost and performance be made? These are the types of questions one has to answer when setting goals for a new radio architecture.

Fortunately, the IEEE and the worldwide electronics industry have had the foresight to develop the IEEE 802.11 standard to limit the infinite range of possible combinations of performance and protocol. This also provides the customer with the bonus of compatibility between different vendors. The IEEE 802.11 committee has created three standards for wireless LAN communication; Frequency Hop (FH), Direct Sequence (DS), and Infrared. The radio standards FH and DS use two modulation methods that seem to attain similar goals, but that offer special performance advantages in different situations and applications.

This paper will analyze an example of a WLAN solution, a Direct Sequence Spread Spectrum (DSSS) system from Intersil Corporation, the PRISM® chip set.

The Architecture

A basic architecture is shown in the block diagram in Figure 1. The radio design is centered on the expected signal characteristics of the modulation method. A Differential Quadrature Phase Shift Keying (DQPSK) modulation encodes the data in terms of phase with minimal amplitude variation, improving noise immunity. This is joined with the IEEE 802.11 protocol standard Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) and with the FCC requirement for 10dB processing gain, to allow signals to be received with approximately 0dB Signal to Noise Ratio (SNR) for a 10^{-5} Bit Error Rate (BER). The CSMA/CA protocol allows only one user, per channel, at a time (i.e., first come, first serve) making for a quieter medium. The processing gain, achieved by spreading the signal with a PN code, allows a faint signal to be pulled from the noise while suppressing non-correlating interferers.

A single antenna is used, although two antennas are supported for diversity to counter the effects of multi-path fading. From the antenna, the received input is applied to the pre-select filter FL1. This filter is a two pole dielectric design, rejecting interferers outside the 2.4GHz ISM band and providing image rejection.

The T/R switch is integrated into the HFA3925 RF Power Amplifier. The switch in receive mode leads to the HFA3424 Low Noise Amplifier, which is used to set the noise figure for the entire receiver.

Next, the signal enters the HFA3624 RF/IF Converter, first passing through the integrated LNA section and then going off-chip to FL2. Filter FL2 is an inexpensive 2 pole monolithic LC bandpass filter used to suppress image noise.

The signal then enters the downconverter section of the HFA3624. Low-side local oscillator injection is used to mix down to the single intermediate frequency, 280MHz. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50Ω environment.

The IF receive filter FL3, is a Surface Acoustic Wave (SAW) device used for channel selection within the band. The SAW output is reactively matched to the IF input of the HFA3724 Quadrature IF Modulator/Demodulator.

In receive mode, the HFA3724 provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. The two limiting amplifiers or limiters, in cascade with a one pole LC limiter BPF FL4, provide most of the receiver gain, giving the radio it's sensitivity.

For engineers with an analog background, limiters can be thought of as high speed, high gain comparators. They operate on the largest signal present, amplifying it up to a rail to rail output and thus rejecting smaller signals and noise.

After the limiters, the signal is then mixed down to baseband with the quadrature baseband demodulator into the I and Q components. Finally anti-alias filtering is performed before going to the analog to digital converters (ADCs) of the Baseband Processor, HFA3824. The baseband circuit samples the waveform with 3-bit ADCs and then despreads and demodulates the received data.

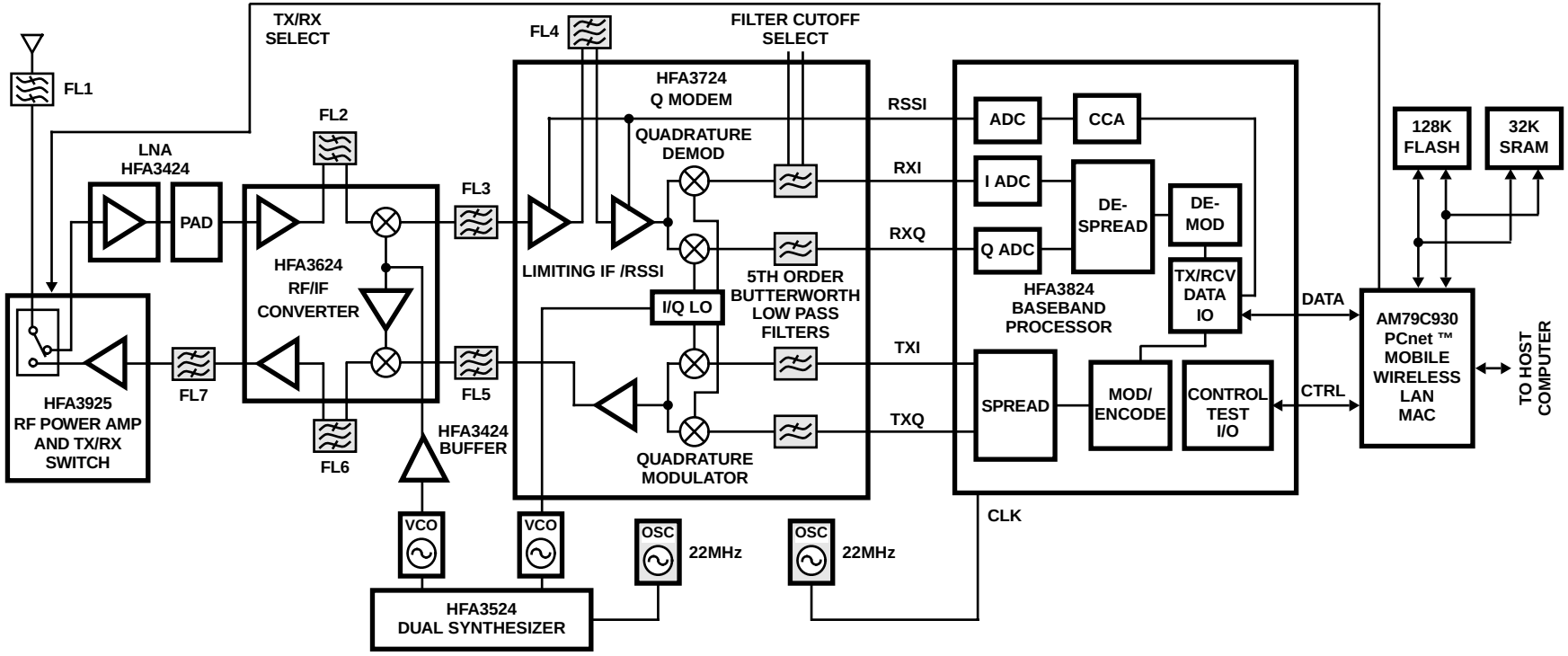

FIGURE 1. PRISM™ PC CARD BLOCK DIAGRAM

PCnet™ is a trademark of AMD, Inc.

General Specifications

- Targeted Standard . . . . . IEEE 802.11 (Draft)
- Data Rate . . . . . 1Mbps DBPSK
  2Mbps DQPSK
- Range. . . . . 400ft Indoor (Typ) (Note 1)
  3700ft Outdoor (Typ) (Note 1)
- Frequency Range . . . . . 2412MHz to 2484MHz
- Step Size 1MHz
- IF Frequency 280MHz
- IF Bandwidth 17MHz
- RX/TX Switching Speed . . . . . .2µs (Typ)
- Operating Voltage . . . . . $4.5V_{DC}$ - $5.5V_{DC}$
- Standby Current . . . . . 190mA at 1µs Recovery (Note 4)
  70mA at 25µs Recovery (Note 4)
  60mA at 2ms Recovery (Note 4)
  30mA at 5ms Recovery (Note 4)
- Operating Temperature Range . . . . 0^oC to 70^oC (Note 2)
- Storage Temperature Range . . . . . .-55^oC to 125^oC
- Mechanical . . . .Type II PC Card, with Antenna Extension
- Antenna Interface . . . . . SMA, 50Ω

Receive Specifications

- Sensitivity . . . . .-93dBm (Typ), 1Mbps, 8E-2 FER (Note 3)
  . . . . . .-90dBm (Typ), 2Mbps, 8E-2 FER (Note 3)
- Input Third Order Intercept Point . . . . . .-17dBm (Typ)
- Image Rejection . . . . . 65dB (Typ)
- IF Rejection . . . . . 80dB (Typ)
- Adjacent Channel Rejection . . . . . 63dB (Typ)
  at 25MHz Offset
- Supply Current . . . . . .287mA (Typ)
  2Mbps, 100% Duty Cycle

Transmit Specifications

- Output Power . . . . . +18dBm (Typ)
- Transmit Spectral Mask . . . . . .-32dBc (Typ)
  at First Side-Lobe
- Supply Current . . . . . .488mA (Typ)
  2Mbps, 100% Duty Cycle

NOTES:

1. Using M/A-COM AND-C-107 omnidirectional antenna.
2. AM79C930 limited to 0^oC to 70^oC.
3. FER = Frame Error Rate or Packet Error Rate.
4. Recovery times do not include MAC recovery.

FIGURE 2. TYPICAL PERFORMANCE

On the Transmit side, data can either be DBPSK or DQPSK modulated at 1MSPS (Mega Symbols Per Second), resulting in a baseband quadrature signal with I and Q components. These digital signals are output to the HFA3724 fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main lobe.

The signals are then quadrature modulated up to IF using the same 2xLO used for the quadrature demodulation. The IF output is reactively matched to FL5, the transmit IF SAW filter. The output of FL5 is terminated in a 200Ω potentiometer that is used for transmit gain control.

The signal then goes to the high impedance input of the HFA3624 upconverting mixer for conversion to the 2.4GHz - 2.5GHz band. The mixer output is filtered with FL6, a 2 pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The pre-amplifier, in the HFA3624, amplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a two pole dielectric bandpass filter, is used to further suppress both transmit LO leakage and the undesired sideband. The HFA3925 RFPA amplifies the transmit signal to approximately +20dBm. This represents a back-off from the 1dB compression of typically 4.5dB. The transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off. Allowing for a 2dB loss in the band select filter FL1, this gives a final output power of +18dBm. Typical radio performance is displayed in Figure 2.

Limiters vs AGCs

Generally limiters and AGCs are used to provide large gains at the IF stage. Automatic Gain Control (AGC) circuits maintain good signal linearity over a wide dynamic range, even amplifying small signals buried in the noise. However, AGCs must settle to a final value quickly. This is especially difficult in a packetized system where AGC settling for packet acquisition must take place in under 2µs.

Limiters are nonlinear devices, eliminating amplitude information, but work well for phase encoded modulation. They provide the added benefit of suppressing secondary signals and so will have up to 6dB advantage over AGCs in a positive SNR environment.

The selection of limiters takes advantage of the modulation scheme, positive SNR of the environment, while reducing cost and complexity.

Receive Chain Gain Distribution Analysis

The IF stage, including the limiters, is of a differential design to improve noise rejection and stability for these high gain stages. The RF front end, on the other hand, is single ended to reduce complexity. A receive chain block diagram is shown in Figure 3.

The minimum limiter 1 and 2 voltage gains are 39dB at 2.7V and 400MHz. The radio design uses the part at a less extreme operating point of 3.5V and 280MHz where the minimum performance is 42dB. The limiter 1 and 2 output limiting voltage is $200mV_{P-P}$ into a differential 500Ω load. Using 3dB loss in the limiter Bandpass Filter (BPF), the limiter chain (LIM1, BPF, LIM2) cascaded voltage gain is 81dB, with typical performance above 90dB. With a $200mV_{P-P}$ output, the input limiting voltage is $17.8\mu V_{P-P}$ or -98dBm at 250Ω source impedance.

This is calculated as follows: since the source and load impedances are different (250Ω vs 500Ω) the input signal is calculated in terms of voltage. Remember that the limiter is a voltage gain device and so gain is independent of source impedance. Substitute the result of Equation 1 into 2 and calculate $V_{IN(P-P)}$.

$$\text{Gain (V/V)} = 10\left(\frac{\text{Gain (dB)}}{20}\right) \quad \text{(EQ. 1)}$$

$$V_{OUT} = \text{Gain (V/V)} \bullet V_{IN} \quad \text{(EQ. 2)}$$

Calculate the input power with a 250W impedance by using Equation (3) to get V_{RMS} and then substitute into (4) with R = 250Ω to get power in Watts. Equation (3) assumes a sinewave crest factor for the $\sqrt{2}$ term. Power in Watts is converted to dBm with Equation (5) to get -98dBm input power at 250Ω source impedance.

$$V_{RMS} = \frac{V_{P-P}}{2 \bullet \sqrt{2}} \quad \text{(EQ. 3)}$$

$$\text{Pwr(Watts)} = \frac{V^2_{RMS}}{4} \quad \text{(EQ. 4)}$$

$$\text{Pwr(dBm)} = 10\log(\text{Pwr(Watts)} \bullet 10^3) \quad \text{(EQ. 5)}$$

The limiters have a noise bandwidth of over 500MHz and so the cascaded limiters will fully limit on their own noise, if no BPF is used between the stages. The thermal noise voltage delivered from the 250W source to the limiters in a 500MHz band is -87dBm, as calculated from Equation (6). This thermal noise adds to the limiter noise figure (NF) of 7dB resulting in an equivalent input noise power of -80dBm, which is significantly higher than the -98dBm required for limiting.

$$P(\text{Watts})_A = kT\Delta f \quad \text{(EQ. 6)}$$

Where:

$P(\text{Watts})_A$ = Available Noise Power

$k = 1.38042 \times 10^{-23}$

Boltzmans Constant

T = 300 Degree Kelvin

Δf = 500MHz

The RF front end 3dB bandwidth is 17MHz, with an estimated noise bandwidth of 20MHz, as defined by the IF SAW filter. This makes the available thermal noise at the limiter input -101dBm and with the 7dB limiter noise figure, is an equivalent -94dBm.

If the limiter BPF was also 20MHz, the front end would only need to supply 7dB of noise floor gain to overcome the limiter noise figure. This would result in a receiver that limits in a 20MHz bandwidth from front end noise with no margin. The 20MHz limiter BPF would require a second SAW filter and therefore, is not cost effective or practical.

The alternative chosen to be implemented is a simple one pole LC BPF with a bandwidth wide enough so that the variability of fixed components do not result in the filter being off frequency. The filter selected has a 3dB bandwidth of 50MHz, and an estimated noise bandwidth of 100MHz. Using this method, the front end gain must be increased to compensate for excess limiter bandwidth.

It is desired that the second limiter to be fully limited on front end noise, as opposed to noise generated in the first limiter. This requires that the front end noise floor must be greater than the sum of the following; the limiter NF of 7dB, the ratio of limiter BPF noise bandwidth to front end IF SAW bandwidth (10log(100MHz/20MHz) or 7dB), and the amount of limiting margin (6dB for -1dB limiting). The front end output noise floor must therefore be greater than 20dB.

The limiting margin was measured on the HFA3724 IF Mod/Demod, with good agreement to a theoretical estimate based upon the hyperbolic tangent response of a bipolar differential limiter. The measurement means that if a non-desired jamming signal, noise in this case, is 6dB below the level of the desired signal, the desired output will be reduced 1dB.

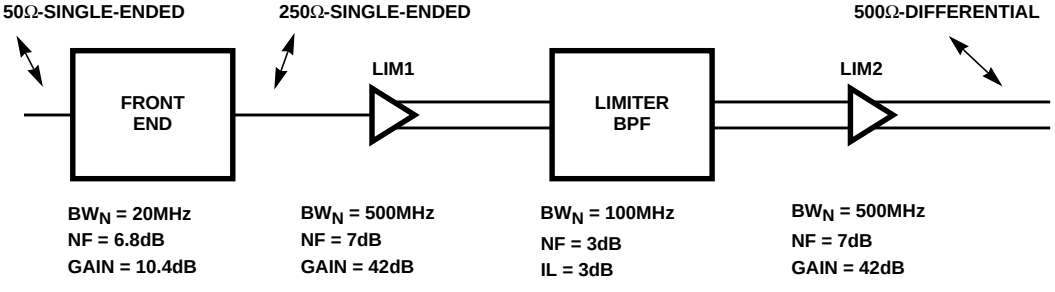

FIGURE 3. RECEIVE CHAIN GAIN DISTRIBUTION DIAGRAM

The front end noise floor was previously calculated for a 20MHz bandwidth as -101dBm, if the required gain is now added, this noise floor becomes -81dBm as shown in Equation (7). Now verify that this level is larger than the minimum signal power required to limit the limiter chain and guarantee that the radio limits on front end noise $(-81dBm > -98dBm)$.

$$(20MHz\ kTB) + NF_{LIM} + BPF_{Noise} + Lim_{Margin} = \text{Front End Noise} \quad \text{(EQ. 7)}$$

i.e.,

-101dBm + 7dB + 7dB + 6dB = -81dBm

Where: (20MHz KTB) is Available Thermal Noise

NF_{LIM} is Noise Figure of Limiter Chain

BPF_{Noise} is Added Noise due to Limiter BPF Bandwidth Wider than Front End

Lim_{Margin} is Front End Margin Required to Guarantee Limiter Jammer Rejection

As will be explored next, the actual front end gain is 10.4dB and the NF is 6.8dB for a front end output noise floor increase of 17.2dB typical, not the desired 20dB. This results in limiting, when no signal is present, on mainly front end noise, but also some limiter broadband noise. This limiter output, although still fully limited, when band filtered will have a slight drop in baseband quadrature output voltage to the HFA3824 ADCs as compared to totally limiting on front end noise due to some of the limiter noise being out of band. The net impact to the system is a small reduction in sensitivity due to reduced ADC signal to full scale. If desired, additional front end gain, or a reduced bandwidth limiter BPF could be used to gain back performance.

Receive Chain Front End Cascade Analysis

The typical receiver performance of the chip set is illustrated in the level diagram analysis shown in Figure 4. Across the top of the figure are descriptions of the blocks in the receive chain. Each block has typical values for Insertion Loss (IL) or Gain (G), Noise Figure (NF) and Output Third Order Intercept Point (OIP3). The noise figure for a passive element is equal to its insertion loss and its OIP3 is set to 100dBm for the purpose of calculation. The left side of the figure lists the parameters to be calculated for each block element; Gain, NF, IIP3 and typical signal level. The entry in each space is the result of the parameter after the effect of the chain element, with the exception of IIP3 where the entry is for the block input. Cascaded parameters may be determined anywhere along the chain, and so this type of analysis can show where a units performance is not being utilized as it should and therefore, has increased the system cost over what it could be.

The receiver front end total gain is 10.4dB for a radio with better than -90dBm sensitivity. This is due to the high gain of the IF limiter stages. Minimizing front end gain is desirable so that IIP3 may be maximized. The front end actually has a significantly larger amount of gain than is indicated by the total. A total of 21.2dB of gain is required, to overcome the insertion loss of the receive filters, particularly the IF SAW filter with an insertion loss of 10dB maximum.

The IF SAW filter is critical to the design because it provides a large amount of ultimate rejection for adjacent channel interferers and sharp band edges to select the desired channel. This allows other channels to operate close by in frequency without interference. Typically this 17MHz bandwidth SAW filter provides adjacent channel rejection of 63dB at 25MHz of frequency offset.

The figure shows that noise figure is dominated by the first LNA, the HFA3424, where it is set to 5.2dB. The rest of the chain only contributes another 1.6dB for a total front end noise figure of 6.8dB. Even a noise figure of 12dB for the downconvert mixer only adds 0.3dB latter in the chain. The reason for this dominance by the first gain stage can be seen from the cascaded noise figure Equation (8). The noise figure of subsequent stages are divided by the total gain of prior stages. This fact makes the selection of the first LNA important because the front end noise figure sets the amount of front end SNR degradation and therefore, contributes to receiver sensitivity.

$$NF_{TOTAL} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + ... \quad \text{(EQ. 8)}$$

Where NF and G (Gain) are Linear Number, i.e.,

Where $NF = 10^{\frac{NF\ (dB)}{10}}$

INPUT POWER	FL1 TOKO RF FILTER IL=2.0	HFA3925 T/R SWITCH IL=1.2 OIP3=34	HFA3424 LNA G=13dB NF=2.0 OIP3=11.1	ATTEN IL=5.0	HFA3624 LNA G=15.6 NF=3.8 OIP3=15	FL2 MURATA RF FILTER IL=3.0	HFA3624 MIXER G=3.0 NF=12.0 OIP3=4.0	FL3 TOYOCOM IF SAW FILTER IL=10.0	HFA3724 IF LIMITER STRIP G=0 NF=7.0
Gain	-2.0dB	-3.2dB	9.8dB	4.8dB	20.4dB	17.4dB	20.4dB	10.4dB	10.4dB
NF	2.0dB	3.2dB	5.2dB	5.5dB	6.0dB	6.0dB	6.3dB	6.4dB	6.8dB
IIP3	-16.8dBm	-18.8dBm	-20.0dBm	-6.9dBm	-11.9dBm	4.0dBm	1.0dBm	NA	NA
-90dBm	-92dBm	-93.2dBm	-80.2dBm	-85.2dBm	-69.6dBm	-72.6dBm	-69.6dBm	-79.6dBm	-79.6dBm

FIGURE 4. PRISM1 RECEIVER LEVEL DIAGRAM

Where the NF calculation is dominated by the first element in the chain, IP3 is typically dominated by the last element, the element with the largest signal. In this case, the downconverting mixer, with an OIP3 of 4dBm, is where the largest signal occurs and is the dominating element for our cascade analysis.

Third Order Intercept (IP3) is a measure of signal distortion, and the equation for cascaded IP3 has the same form as another distortion parameter 1dB compression (P1dB). The equation for cascaded IIP3 is shown in Equation (9).

$$IIP3(Watts)_{TOTAL} = \frac{1}{\frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1G_2}{IIP3_3} + ...} \quad \text{(EQ. 9)}$$

Where IIP3 and G (Gain) are Linear Numbers.

The total receiver front end third order intercept point of -16.8dBm is important in the management of non-desired jamming signals. Jammers can be high power out-of-band signals that make it past the 2.4GHz ISM band pre-select filter or especially in-band signals. In-band jammers can be either intentional (i.e., other radios on the same or another channel) or unintentional (i.e., microwave ovens).

As the power of jamming signals approach the receiver IIP3, harmonics and mixing products of these jammers appear. The risk here is if the jammer itself is not directly in the desired signal channel, it is possible that some of the distortion terms can be. Once the distortion product is in the channel, it can no longer be filtered out and the signal must be rejected through processing gain or limiter suppression.

Another effect from jamming signals related to the IIP3 is receiver desensitizing. The receiver input 1dB compression point may be approximated by subtracting 10dB from the IIP3 resulting in -26.8dBm. A jamming signal larger than this will begin to compress the receiver front end, reducing the front end gain of the large jamming signal along with the desired signal. This desensitizing of the receiver causes a loss of sensitivity and limiter margin, even if the jammer is later filtered out by the IF SAW filter.

A trade-off between noise figure and input intercept point exists in any receiver. The attenuator after the first LNA is used in this trade-off between high gain, for good sensitivity, and lower gain for better IIP3.

The receiver front end circuits have been specially designed to permit input signals as large as 0dBm with the receiver still able to function. This is important because if the designer is not careful, the design may have great sensitivity and range, but when the two radios get close they will not work! The signal is so large that it overdrives the input causing the input amplifier or RF mixer to saturate and stop functioning.

Transmit Chain Front End Cascade Analysis

The transmitter performance analysis is shown in the level diagram in Figure 5. Here again, the function blocks are described across the top, with the only difference being that Output 1dB Compression Point (OP1dB) is listed for each block. The parameter list, on the left side, includes Gain, OP1dB, and Output Power (P_{OUT}).

The large gain in the Power Amplifier, HFA3925, keeps the signal level small for the whole chain before it. This helps conserve supply current and the cost associated with devices that need to handle large signals.

The output power at the RF filter is shown as 18dBm, with the output of the Power Amplifier at 20dBm. The design has been optimized for the best use of supply current and cost of the PA. If the output power was lower, the supply current and cost of the PA could be saved with smaller and cheaper devices. If the output power was higher, the signal will be too close to the P1dB and the signal will have excessive distortion, causing regrowth of the side lobes. The transmitted signal must suppress side lobes to -30dB to meet the 802.11 spectral mask specification.

Therefore, the output power needs to be controlled very carefully. The run to run variation in gain and insertion loss of the elements in the transmit chain requires either a manual power adjustment or an active power adjustment feedback circuit. In this design, a manual potentiometer is used to adjust output power and side lobe performance on each unit during manufacturing. For purposes of this analysis, the variable attenuator shows 0dB loss and the Modulator output as -10.4dBm. This was done for illustration purposes only, in actuality the Modulator output (HFA3724) has a relatively large output (200mV_{P-P}) that needs to be significantly attenuated to the level indicated.

OUT POWER	FL1 TOKO RF FILTER IL=2.0	HFA3925 PWR AMP G=28dB P1dB=24.5	FL7 TOKO RF FILTER IL=2.0	HFA3624 PRE AMP G=12.3 P1dB=5.6 NF=5.7	FL6 MURATA RF FILTER IL=3.0	HFA3624 MIXER G=2.1 P1dB = -10.5 NF=14.5 Z_I=1kΩ Z_O=50Ω	ATTN IL= VAR	FL5 TOYOCOM IF SAW FILTER IL=10 MAX IL=7.0(TYP) Z_O=270Ω	HFA3724 MOD OUT Z_O=270Ω
Gain	35.4dB	37.4dB	9.4dB	11.4dB	-0.9dB	2.1dB	-	-	-
OP1dB	19.2dBm	21.2dBm	-4.0dBm	-2.0dBm	-13.5dBm	-10.5dBm	-	-	-
P_{OUT}	18dBm	20dBm	-8dBm	-6dBm	-18.3dBm	-15.3dBm	-17.4dBm	-17.4dBm	-10.4dBm

FIGURE 5. PRISM1 TRANSMITTER LEVEL DIAGRAM

Typically it is desirable for the last element in the transmit chain to set the P1dB of the system. The Cascaded 1dB Compression Point is calculated as shown in Equation (10) for Input P1dB or Equation (11) for Output P1dB.

$$IP1dB(Watts)_{TOTAL} = \frac{1}{\frac{1}{IP1dB_1} + \frac{G_1}{IP1dB_2} + \frac{G_1G_2}{IP1dB_3} + ...} \quad \text{(EQ. 10)}$$

Where IP1dB (Input 1dB Compression Point) and G (Gain) are linear numbers.

$$0P1dB(Watts)_{TOTAL} = \frac{G_{TOTAL}}{\frac{G_1}{0P1dB_1} + \frac{G_1G_2}{0P1dB_2} + \frac{G_1G_2G_3}{OP1dB_3} + ...} \quad \text{(EQ. 11)}$$

Where OP1dB (Input 1dB Compression Point) and G (Gain) are linear numbers.

Comparing the system P1dB at the Power Amplifier, 21.2dBm, with the P1dB of the PA itself, 24.5dBm, it is apparent that other elements in the transmit chain are affecting P1dB and therefore, contributing to the regrowth of side-lobes early. Measurements have determined that a 6dB margin, between signal power and the P1dB of a device will result in 1dB of side-lobe regrowth. In the level diagram the upconvert mixer has only 4.8dB headroom setting the P1dB of the system from the mixer to the PA. If the upconvert mixer were to have 2dB higher P1dB or if the transmit chain had 2dB additional gain, virtually all the side lobe regrowth could be made to occur at the PA. This would allow the PA to be driven for a larger output power signal, closer to the P1dB.

Conclusion

Through a detailed analysis of an existing radio design, this paper has presented useful tools and methods for the design and implementation of a 2.4GHz DS Wireless LAN radio. These tools include; “Receive Chain Gain Distribution/Limiter Analysis”, the “Receive Chain Front End Cascade Analysis”, and the “Transmit Chain Front End Cascade Analysis”.

The paper shows how the radio design is shaped from early decisions about the modulation scheme, protocol, and environment. The basic decision of what will provide the majority of receiver gain, AGCs or Limiters. The use of a typical block diagram, such as the Intersil PRISM chip set, in the piecing together or setting goals for a new design or understanding an existing one. Finally the cascade analysis reveals strong and weak points in the design that may be improved to reduce cost or gain performance.

The cascade analysis was performed using “AppCAD Version 1.02 by HewlettPackard”. This freeware is no longer available but many cascade analysis tools exist with advanced capabilities and that are easy to use.

References

For Intersil documents available on the internet, see web site www.intersil.com/
Intersil AnswerFAX (321) 724-7800.

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