KENWOOD

SERVICE MANUAL

R-2000 DCK-1

COMMUNICATIONS RECEIVER

CONTENTS

SPECIFICATIONS

Frequency Range: 150 kHz ~ 30 MHz
150 kHz ~ 26 MHz (W2 type)
2 MHz ~ 30 MHz (X type)
Mode: AM, FM, SSB (USB/LSB), CW
Sensitivity: (0 dBμ = 1 μV)

Mode \ Frequency	150 kHz ~ 2 MHz	2 MHz ~ 30 MHz
SSB/CW (S+N/N 10 dB)	Less than 2 μV	Less than 0.4 μV
AM (S+N/N 10 dB)	Less than 20 μV	Less than 4 μV
FM (S+N/N 20 dB)	–	Less than 1 μV

Selectivity:

Mode \ Selectivity	Selectivity	
AM-WIDE	6 kHz (–6 dB)	18 kHz (–50 dB)
AM-NARROW	2.7 kHz (–6 dB)	5 kHz (–50 dB)
SSB/CW	2.7 kHz (–6 dB)	5 kHz (–50 dB)
CW-NARROW	500 Hz (–6 dB)*	820 Hz (–60 dB)*
FM	15 kHz (–6 dB)	30 kHz (–50 dB)

*: with YG-455C optional CW crystal filter

Symbol	Destination
K	U. S. A
M	General market
T	Britain
W	Europe
X	Australia & New Zealand

Image Ratio: Better than 70 dB
IF Rejection: Better than 70 dB
Frequency Stability: Within ±300 Hz during the first hour after 1 minute of warm-up.
Within ±50 Hz during any 30 minutes period thereafter.
Frequency Accuracy: $\pm 10 \times 10^{-6}$ or better (at normal temperatures)
Squelch Sensitivity: (threshold, 0 dBμ = 1 μV)
AM/SSB/CW = Less than 3.12 μV
FM = Less than 0.5 μV
Audio Load Impedance: 4Ω to 16Ω
Audio Output Power: 1.5W (8Ω load, 10% distortion)
Antenna Impedance: 50Ω/500Ω
Power Consumption: (at no signal) = 14W AC
13.8V DC, 0.6A (with optional DCK-1)
(at Memory Back-up) = 3W AC
13.8V DC, 0.1A (with optional DCK-1)
Power Requirements: 100/120/220/240V AC, 50/60 Hz
13.8V DC (with optional DCK-1)
Dimensions: 375 (14.8) W × 115 (4.5) H × 210 (8.3) D mm (inch)
Weight: 5.5 kg (12.1 lbs.) approx.

CIRCUIT DESCRIPTION

RX unit X55-1340-00

R-2000 is a triple conversion general coverage receiver with a first IF of 45.85 ~ 45.90 MHz, 9.85 ~ 9.90 MHz second IF and a 455 kHz third IF.

Both low (50Ω) or high (500Ω) impedance antenna terminals are provided for all bands.

The signal supplied through the antenna terminal goes to the antenna fuse (100 mA) and three step RF attenuator (10, 20, and 30 dB). It next enters the BPF (Band Pass Filter), which divides the 0.15 ~ 30 MHz range into 6 bands; 0.15 MHz ~ 1 MHz, 1 MHz ~ 2 MHz, 2 MHz ~ 4 MHz, 4 MHz ~ 8 MHz, 8 MHz ~ 17 MHz and 17 MHz ~ 30 MHz. Q58: SN74LS145N converts the BCD band data signal from the PLL control circuit to select the appropriate BPF for the frequency selected.

Exiting the BPF, the signal, is fed to RF amp Q1: 3SK73(GR), first IF trap (operating at 40.875 MHz) and emitter follower Q2: 2SC1815 (Y).

The RF signal is mixed with the first local oscillator 45.9 ~ 75.85 MHz and converted to the 45.85 ~ 45.90 MHz first IF by balanced mixer Q3 and Q4: 3SK73(GR).

Q3 and Q4 drain voltage is supplied through a switching circuit consisting of Q5 and Q6 controlled by Q47 and Q48: 2SC1815 (Y) will turn off when the VHB signal is applied from the PLL control circuit in the (optional) VHF reception mode. At the same time, the first IF circuit input is switched to the converter by switching diodes D13 and D14: 1S2588.

After passing the first IF LC filter the signal is converted to the 9.85 ~ 9.90 MHz second IF by the second balanced mixer Q7 and Q8: 3SK74(L) using the 36 MHz second local oscillator injection signal.

The second IF signal passes through ceramic filter F1 (f_o: 9.875 MHz) and is converted to the 455 KHz third IF by the third balanced mixer Q9 and Q10: 3SK73(GR) using the 9.445 ~ 9.395 MHz third local oscillator injection signal.

The signal is applied to the NB gate D15, 16. A part of the signal is also applied to the NB (Noise Blanker) amplifiers on the PLL unit via buffer Q11: 2SC1815(Y). The signal output from the NB gate is switched to the appropriate bandwidth third IF filter (F2 ~ F5 of 455 kHz), then fed to the third IF amplifiers.

The IF filter bandwidths are: F3; 2.7 kHz, F4; 6 kHz and F5; 15 kHz. Filter F3 is used in the AM narrow, SSB and CW wide modes, F4 in the AM wide mode and F5 in the FM mode. Filter position F2 is provided for the CW narrow mode and an optional YG-455C or YG-455CN filter can be used.

The third IF amplifiers are divided into two systems; one for the FM mode and one for all other modes.

In the FM mode, the signal passing through F5 is amplified by Q32: TA7060P, Q33: 2SC1675(L) and Q34: μPC577H, then detected by ceramic discriminator F6, and diodes D41 and 42.

The noise component of the detected signal is amplified by Q35 and Q36: 2SC1775(E), rectified (D44 and 45), DC amplified (Q37 and 38), then applied to squelch gate switch Q41: 2SC1815(Y), center stop control Q40: 2SC1815(Y) and BUSY LED switch Q42 and Q43: 2SC1815(Y).

The DC voltage which is generated from the discriminator (F6) is fed to window comparator Q39: NJM4558D which forms an AND circuit together with Q40 and generates the Program Scan center stop signal which is applied to the PLL control circuit via Q46: 2SC1815(Y). The FM IF signal from Q33 is amplified by Q59: 2SC1815(Y) and detected by D39 and D40: 1N60 to drive the S meter.

In all modes other than FM, the signal which has passed F2 through F4 are amplified by Q12 and Q13: 3SK73(GR). A sample of the IF signal is buffer by Q14: 2SC1815(Y) and is AM detected by D29: 1N60, buffered by Q15, and diode switched by D30 to the squelch-controlled switch Q16. Output from Q14 is also rectified by D37 and D38: 1N60. This signal is also split: the rectified output is both AGC amplified by Q23: 2SC1815(Y) and squelch amplified by Q28: 2SC1815(Y), Q29: 2SK192A(GR), Q30: 2SA1015(Y) and Q31: 2SC1815(Y). Q24 (CW and SSB) and Q25 (AM) 2SC1815(Y) select the AGC slow time constant by mode. AGC is applied dack to the RF and IF amplified. The AGC voltage is also amplified by Q50: 2SK192A(GR) and Q51: 2SA1015(Y) to drive the S meter. Q26 and Q27: 2SC1815(Y) switch off power to the AM, CW, and SSB IF amplifiers and squelch amplifiers in the FM mode. The output of the squelch amplifiers (Q31) is applied to the BUSY LED switch Q44: 2SC1815(Y), scan stop switch Q45: 2SC1815(Y) and squelch gate Q16: 2SC2240(GR).

Q21: 2SC1815(Y) is the BFO circuit oscillator and Q22: 2SC1815(Y) the buffer. The BFO output is applied to the product detector D25 ~ D28 (1N60). Q20: 2SC1815(Y) is the LSB frequency shift switch.

The AM signal detected by D29 is buffered by Q15: 2SC2240(GR), and the audio signal is selected according to mode by either D30 (for AM) or D31 (for SSB and CW). This is fed through switch Q16 to audio amplifier Q17: 2SC2240(GR). The FM audio signal passes squelch gate Q52: 2SC2240(GR) and then goes to Q17.

Audio amplified by Q17 is first fed to the VOLUME and TONE controls. Q18: 2SC2240(GR) provides output to the REC jack.

The audio signal, having passed the VOLUME and TONE controls, is power amplified by Q57: HA1368R to drive the speaker.

As accessory circuits, a BEEP oscilator circuit (Q55 and 56) and standby mute circuit (Q49, 60 and 61) are provided.

In the mute mode, Q49: 2SC1815(Y) decreases the RB (receive B+) line to −6V to mute all modes except FM. The RB line then controls Q60 and 61 to disrupt FMB (FM B+) to Q33, which effectively mutes the FM mode.

The power supply circuits consists of a 9V AVR (automatic voltage regulator) Q54: AN7809 and a 14V ripple filter Q53.

Item	Rating
Nominal center frequency	within 9.875 MHz ± 30 kHz
3 dB bandwidth	within 130 ± 30 kHz
20 dB bandwidth	350 kHz or less
Loss	8 dB or less
Spurious response (within 9.875 ± 2 MHz) (within 8.965 ± 25 KHz)	 30 dB or more 40 dB or more
Input and output impedance	330Ω

Table 1. Ceramic filter (L72-0338-05) RX unit F1

CIRCUIT DESCRIPTION

Item	Rating
Center frequency	455 kHz ±0.6 kHz
6 dB band width	2.8 ±0.3 kHz
40 dB band width	5.5 kHz or less
Insertion loss (at maximum output)	6.0 dB or less
Guaranteed attenuation (within 455 ±100 kHz)	55 dB or more
Spurious attenuation (within 0.1 to 1.0 MHz) for 600 to 700 kHz	45 dB or more 40 dB or more
I/O matching impedance	2.0 kΩ

Table 2. Ceramic filter (L72-0332-05, RX unit F3) SSB, AM-N, CW-W

Item	Rating
Nominal center frequency	455 kHz
6 dB band width	±3 kHz or more (from 455 kHz)
50 dB band width	±9 kHz or less (from 455 kHz)
Ripple (within 455 ±2 kHz)	2 dB or less
Insertion loss	6 dB or less
Guaranteed attenuation (within 455 ±100 kHz)	60 dB or more
I/O matching impedance	2.0 kΩ

Table 3. Ceramic filter (L72-0319-05, RX unit F4) AM-W

Item	Rating
Nominal center frequency	455 kHz
6 dB bandwidth	±7.5 kHz or more
50 dB bandwidth	±15 kHz or less
Ripple (within 455 ± 5 kHz)	3 dB or less
Loss	6 dB or less
Guaranteed attenuation (within 455 ± 100 kHz)	35 dB or more
Input and output impedance	1.5 kΩ

Table 4. Ceramic filter (L72-0316-05, RX unit F5) FM

Item	Rating
Center frequency f_o	455.7 kHz
Center frequency deviation	f_o ±50 Hz at 6 dB
6 dB bandwidth	±250 Hz or more
60 dB bandwidth	±425 Hz or less
Ripple	2 dB or less
Loss	6 dB or less
Guaranteed attenuation	80 dB or more at 100 Hz to 455.1 kHz and 456.3 kHz to 2 MHz
Imput and output impedance	2 kΩ // 15 pF

Table 5. CW Crystal filter (L71-0206-05) YG-455C (Option)

Item	Rating
Center frequency quency f_o	455.7 kHz
Center frequency deviation	f_o ±50 Hz at 6 dB
6 dB bandwidth	±125 Hz or more
60 dB bandwidth	±250 Hz or less
Ripple	2 dB or less
Loss	6 dB or less
Guaranteed attenuation	80 dB or more at 100 Hz to 455.3 kHz and 456.1 kHz to 2 MHz
Input and output impedance	2 kΩ // 15 pF

Table 6. CW Crystal filter (L71-0207-05) YG-455CN (Option)

PLL (Phase locked loop) unit X50-1920-00

The PLL unit houses the PLL oscillator circuit, microprocessor control circuit and the NB amplifier circuits. In the PLL circuit, there is a 9 MHz reference frequency crystal oscillator, the first local oscillator (45.90 ~ 75.85 MHz), second local oscillator (36 MHz) and third local oscillator (9.395 ~ 9.445 MHz), which are output to the Receiver unit.
The digital circuit peripheral to the microprocessor controls the PLL circuit frequency, display, clock/timer, input interface, rotary encoder mode (speed) and memory.

1. **PLL circuit**
   1) Reference frequency oscillator
      Q1 operates at a reference frequency of 9 MHz, which is supplied to the second and third local oscillator circuits through buffer Q2.
      Via buffer Q3, a 4.5 MHz signal divided 1/2 by IC1 is supplied through buffer Q4 to the first local oscillator PLL circuit. The reference frequency is also buffered (Q6) and divided down to 1 kHz by IC2 for use as a clock reference signal.
   2) First local oscillator circuit (LO1)
      The first local oscillator is obtained from the PLL (Phase Locked Loop) circuit. Three VCOs (Voltage Controlled Oscillator) controlled by the microprocessor through Q20 ~ 22 cover the 45.90 ~ 75.85 MHz frequency range. The VCO output is amplified by Q26, Q27 and Q28. Part of the signal is applied to buffer Q16: 2SC1907 and PLL IC5: MN6147C. The spurious component is eliminated from the remaining signal by a BPF and is output via buffer Q29 and Q30: 2SC1707 as the LO1 signal.
      IC5: MN6147C consists of a programmable frequency divider, reference frequency divider and phase comparator which compares the reference and VCO frequencies (comparision frequency; 25 kHz). The programmable divider's ratio (1836 ~ 3034; only even number) is controlled by the microprocessor.
      The phase error signal from the comparator is applied to the VCO by active filter Q17, Q18 and Q19: 2SC1775.
   3) Second local oscillator (LO2)
      The reference frequency is quadrupled by Q5: 2SC1815 to obtain the 36 MHz second local oscillation frequency.

CIRCUIT DESCRIPTION

4) Third local oscillator (LO3)
This circuit consists of PLL IC2: MN6147C which incorprates a 5 kHz PLL and mixer. One VCO is provided; the frequency range is 39.505 ~ 44.500 MHz and the dividing ratio range is 7901 ~ 8900. This PLL circuit is composed of VCO Q11: 2SC1923, PLL IC2: MN6147C and a loop filter consisting of Q8, Q9 and Q10: 2SC1775. The VCO output is buffered (Q12), divided 1/100 to 395.05 ~ 455.00 kHz by IC3: MN54459L, buffered (Q13) and mixed with the 9 MHz reference signal by IC4: SN16913P to obtain the 9.39505 ~ 9.445 MHz third local oscillator frequency. This is filtered (CF1) and amplified (Q15), then sent to the Receiver unit.

5) Unlock muting
The output from PLL IC2 pin 2 (unlock) becomes an unlock signal through IC21: TA7324P and Q71, and is used to control the audio muting circuit on Switch unit "B" to reduce or eliminate any pulse noise which may be generated when the frequency is changed and the PLL momentarily resets.

2. Control unit

1) Rotary encoder input circuit
On the Encoder unit, a 50 slit rotary disc and 2 photointerruptors generate 2 clock signals having a 90° phase difference, which are input to the Control unit via the EN1 and EN2 lines. These clock signals are waveform shaped by IC6, quadrupled by the gate circuit consisting of IC7 and 8 (the 50 pulse/rev signal is changed to a 200 pulse/rev signal), and applied IC12, through Flip-Flop IC9 1/4 to the microprocessor pin No. 39 (T1 port). At the same time, the encoder's rotational dirction is detected from the clock pulses by the FF circuit IC9 1/4 and is input to microprocessor pin 29 (Port 37). The waveforms at each point are shown in Fig. 1.

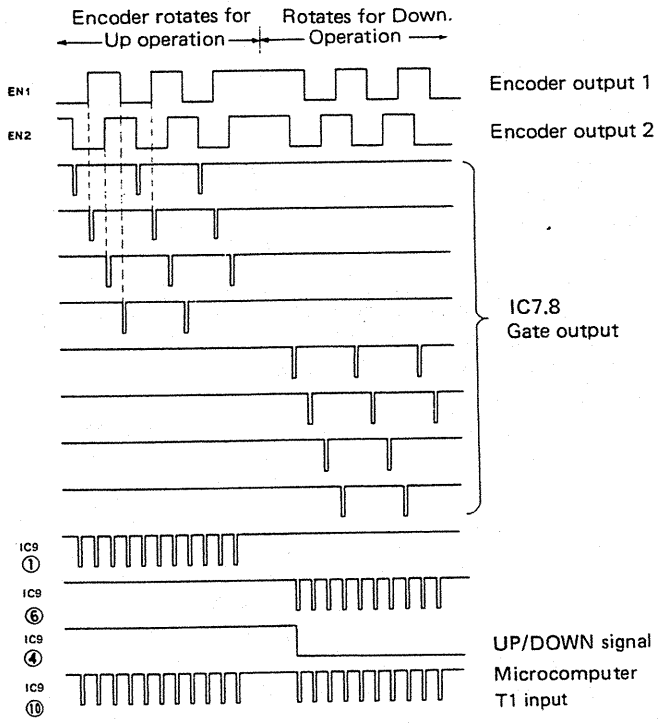

Fig. 1 Encoder output to micro-processor input timing and waveforms

2) Program scan circuit
IC10 on the Control circuit is an astable multivibrator circuit controlled by the PG. SCAN switch. Both its output, and the clock signal are applied to the microprocessor T1 port.
During scan, the multivibrator oscillators output pulse train is accessed by ICs 9 1/4, 10 1/4 and 11 1/2, while the oscillator stops in the HOLD mode and only the Encoder clock pulse is available.
The oscillator frequency is determined by C173, C174, R145 and VR1. When the tuning speed is SLOW or MID, the oscillator frequency is approximately 10 ~ 18 Hz. When it is FAST, Q34 turns on and the oscillator frequency is approximately 5 ~ 9 Hz.

3) Clock circuit
A 1 kHz clock signal is output from PLL IC2 (pin 6), waveform shaped by IC17 1/4 and applied to the microprocessor INT port (pin No. 6) to count the time.
When the HOUR and MINUTE switches are depressed simultaneously the time display shows 00:00. In CLOCK 1 mode, the time display stops flashing and the clock begins counting the seconds (which are not shown) when the switches are depressed. When the display is flashing, the HOUR and MINUTE switches cannot be used to set the time.
When the Function switch is set to any position other than FREQUENCY, depressing the HOUR switch will increment the HOUR digit by one. When the HOUR switch is held ON, the Hours digit increases continuously. The Minutes digit does not change during HOURS set.
Each time the MINUTE switch is depressed, the Minutes digit increases by one. When the switch is held ON, the Minutes digit advances. The Hours digit does not change during Minutes set.
To program the timer, set the timer ON time and place the timer switch ON. Receiver power remains off until the timer preset time is reached, when the relay is activated and the power is switched on.
When the timer OFF time is programmed, the power is turned off at that preset time. When the timer switch is ON, the power switch is inoperative. The timer relay output is available at the Remote control terminals on the rear panel.

4) Microprocessor power supply circuit
When the microprocessor IC12: μPD80C49C is in operation, 5V should be applied to Vcc pin No. 40.
When the microprocessor is in the back-up standby mode, 2V should be applied. When the power switch is turned off, Q35 and Q36 change the level of RESET pin No. 4 to low to protect the RAM, the V_{DD} pin No. 26 becomes low to stop the oscillator and the contents of the RAM are maintained by the low standby voltage (Vcc).
When the power is turned on, 5V is applied to the Vcc pin, the V_{DD} pin becomes high while the RESET pin is held low to activate the oscillator, then the RESET pin returns to a logic high and the program is reset.

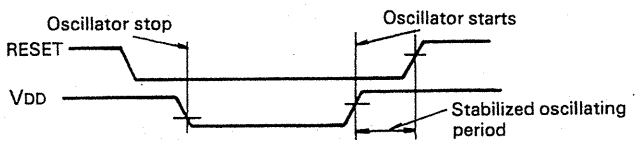

Fig. 2 Micro-processor power supply circuit

CIRCUIT DESCRIPTION

5) Dimmer circuit
The dimmer functions by controlling power to the DC/DC converter. When the main power is on, approximately 12V is supplied to Q41 and Q42 by Q61, Q72, Q73 and D40. When the main power is off or the DIMMER switch is ON, Q73 turns off, and the voltage to Q41 and Q42 is decreased to approximately 8.5V to reduce the display voltage, resulting in a dimmed display.

6) Display circuit
The seven segment and digit signals are output from IC14 to drive the 8-digit display. As the output current is active low, IC15, IC16, Q38, Q39 and Q40 are used.

3. Noise blanker circuit
Pulse noise is obtained through Q11 on the Receiver unit. It is amplified by Q62, Q63 and Q64, rectified by D43 and D44 and DC amplified by Q66 to drive the Receiver unit NB gate circuit. The NB is ON when Q66 is emitter is grounded through D45 varistor.
Q65 is the NB AGC amplifier.

Item	Rating
Nominal center frequency	within 9.420 MHz ± 30 kHz
3 dB bandwidth	within 130 ± 30 kHz
20 dB bandwidth	350 kHz or less
Loss	8 dB or less
Spurious response (within 9.420 ± 2 MHz) (within 8.510 ± 25 KHz)	 30 dB or more 40 dB or more
Input and output impedance	330Ω

Table 7. Ceramic filter (L72-0337-05) PLL unit CF1

Microprocessor Operational Description

1. Digital VFO

1) Reception frequency
The VFO continuously covers 100 kHz - 29,999.95 kHz and stops at the end.
W2 type: 150 kHz - 25.99995 MHz
X type : 2 MHz - 29.99995 MHz

2) Frequency step

	Step	One VFO cycle
FAST	5 kHz	1 MHz
MID	500 Hz	100 kHz
SLOW	50 Hz	10 kHz

The step changeover frequency does not change.
When the VFO is operated with an increased step frequency, frequencies lower than the step frequency are rounded and the VFO scans up or down referring to that frequency.

Example: SLOW step → FAST step

1
3,160.45 MHz
(3,160.4 MHz) → 3,165.00 MHz (3,165.0 MHz) UP
3,155.00 MHz (3,155.0 MHz) DOWN

2
3,163.45 MHz
(3,163.4 MHz) → 3,170 MHz (3,170.0 MHz) UP
3,160.00 MHz (3,160.0 MHz) DOWN

3
3,168.45 MHz
(3,168.4 MHz) → 3,170.00 MHz (3,170.0 MHz) UP
3,160.00 MHz (3,160.0 MHz) DOWN

The above frequencies are displayed frequency; the 10 Hz digits are not displayed.

3) BAND function
The frequency changes by a 1 MHz step when the BAND switch is operated. When the switch is kept depressed, the frequency changes continuously every 0.2 seconds. A beep signal sounds every step. The BAND function stops at the fequency limit and the beep signal does not sound.
When the down operation below the receivable range, the final displayed freuency is the minimum receivable frequency.
Example:

DOWN		UP		
1,034.6 kHz	→	0,100.0 kHz	→	1,100.0 kHz

4) F. LOCK
The VFO and BAND switch operation stop when the F. LOCK switch is set to ON.

5) BACK UP
When the memory is not backed up, the unit enters 15,000.00 kHz MODE (AM) after initial setting.
When the memory is backed up, the unit enters the last reception frequency mode.

2. MODE function

With the mode select operation, the 1st local oscillation frequency is shifted and the displayed frequency is received.

	1st local oscillation frequency shift width
AM	0 (Reference)
FM	0
USB	+1.7 kHz
LSB	−1.7 kHz
CW	+0.7 kHz

3. MEMORY function

1) Memory contes
Built-in 10-channel memory (Frequency and mode information is stored.)

2) M. IN function
When M.CH 1 - 0 switch is pressed with the M.IN switch kept pressed the selected memory channel data is displayed, the beep signal sounds and the displayed frequency and mode are stored. At that time, the previously stored data i replaced with new data.

3) MR function
When M.CH 1 - 0 is pressed, the stored memory contents are recalled to the VFO, enabling frequency shifting.

4) AUTO.M function
When the AUTO.M switch is pressed, the AUTO.M indicator lights and the auto memory function turns on.
When the switch is pressed again, the indicator goes off and the auto memory function turns off.
Auto memory ON: The shifted frequency and mode are stored in the displayed memory channel.
Auto memory OFF: The displayed memory channel contents are not changed even when the frequency is shifted or the mode is changed.

CIRCUIT DESCRIPTION

Example:

frequency change MR
3.235.00 (AM) → 4.182.00 (USB) → 3.235.00 (AM)
(CH5) (CH5)

4. M.SCAN function

1) ALL scan
When the M.S switch is pressed, the M.S indicator lights. When the switch is released, the scanning operation starts. The scanning interval is 1.5 seconds.
M1 → M2 → M3 → ····· → M9 → M0 → M1 → ·····
start
When the M.S switch is pressed again, the M.S indicator goes off, the scanning operation stops and the unit displayes the frequency and mode which were displayed before the scanning operation was started.

2) Select scan
When the desired M.CH switch is pressed with the M.S switch kept pressed, the stored data is recalled. When the switch is released, only the selected memory frequency is scanned.
When the desired M.CH switch is pressed twice in succession, the M.CH display shows "C" and memory frequency scanning is cancelled.

Example:

CH6 cancelled.
M.CH
M.S → 2 → 8 → 6 → 6 → 4 → M.S
(Keep pressed.) Released.
Then scan starts.

Scan: M2 → M4 → M8 → M2 → M4 → M8 → M2

The scanning release operation is the same as that in all scan and the selected memory channel is cleared.

3) HOLD
When the HOLD switch is pressed during the memory scan operation, the HOLD indicator lights and the scanning operation stops.
In the hold mode, the mode can be changed and memory storage is possible. The memory data does not change without memory input even when the mode is changed.

4) When the FUNCTION switch is set to a position other than FREQUENCY during the memory scanning operation or the POWER switch is set to OFF the scanning operation is released and the unit displayes the reception frequency and mode which were displayed before the scanning operation was started.

5. P.SCAN function

1) Scan
When the P.S switch is pressed, the P.S indicator lights and the data stored in channel 9 is recalled. When the switch is released, the frequencies between channel 9 and channel 0 are scanned.
The reception mode stored in channel 9 is used as a reference and the scanning direction is from channel 9 to 0.
When the scanning operation reaches channel 0, it starts from channel 9 again. At that time, a beep signal sounds to indicate that the P.SCAN operation has finished one cycle.
The scan step can be selected with scan step switch and the reception mode can be changed. When the mode is change, the mode does not change until one cycle of P.SCAN operation is finished.
When the P.SCAN operation is finished.
When the P.SCAN switch is pressed again, the P.SCAN indicator goes off, the scanning operation stops and the unit displays the frequency and mode which were displayed before the scanning operation was started.

2) HOLD
When the HOLD switch is pressed during P.SCAN operation, the HOLD indicator lights, the scanning operation stops and the VFO shifts the frequency within the range of the P.SCAN frequency. At the end frequency, the operation stops.
In the HOLD mode, memory storage is possible. When new data is input to channel 9, the stored data can be used as the P.SCAN range.
When the HOLD switch is pressed again, the HOLD indicator goes off and the scanning operation is resumed.

3) BUSY signal stop
When the squelch is opened during the P.SCAN operation, the BUSY indicator lights and the scanning operation stops. When the squelch is closed, the BUSY indicator goes off and the scanning operation starts again. Pressing the BAND UP/DOWN switch when the scanning scanning is stopped due to the squelch function will restart the scanning operation. When the BAND UP/DOWN switch is kept pressed, the scanning operation does not stop even when the squelch opens.
The BUSY signal stop functions in all modes.

4) When the FUNCTION switch is set to a position other than FREQUENCY or the POWER switch is set to OFF, the scanning operation stops and the unit displays the received frequency and mode which were displayed before the scanning operation was started.

5) When a converted is connected and the data stored in both channels 9 and 0 is not an HF or VHF frequency, the M.CH display shows "E" and the P.SCAN does not function. When the M.CH display of the channels 9 and 0 shows "E", P.SCAN does not function.

6. Clock function

1) When the FUNCTION switch is set to CLOCK-1 or CLOCK-2, the unit display the time.
CLOCK-1: Reference time
CLOCK-2: Dual time
When power is supplied, the clock indication blinks.
When CLOCK-1 is reset, the indication stops the blinking.

2) Setting time
Reset CLOCK-1 to stop the blinking. At that time, the seconds digit is set to 0. When the indication is blinking, the time cannot be set. Resetting CLOCK-2 does not stop the indication blinking.

Function	Hour	Minute	Operation
CLOCK-1	ON	ON	Reset to 0:00 (0 sec.).
	ON	OFF	The minutes digits are maintained, the hours digit is incremented and the seconds digits count.
	OFF	ON	The hours digit is maintained, the minutes digits are incremented and the seconds digits count.

CIRCUIT DESCRIPTION

Function	Hour	Minute	Operation
CLOCK-2	ON	ON	Reset to 0:00 and the seconds digits count.
	ON	OFF	The minutes digits are maintained, the hours digit is incremented and the seconds digits count.
	OFF	ON	The hours digit is maintained, the minutes digits are incremented and the seconds digits count.

The clock employs the 24-hour system.
0.00 ···→ 23,59 → 0.00 ···→ 3.15 → 3.16 ···
Each time the HOUR or MINUTE switch is pressed, the corresponding digit is incremented by 1. When the switch is kept pressed, the digit is continuouly incremented at an interval of 0.12 seconds.

3) When the power is shut off, the CLOCK-1 and CLOCK-2 are reset to 0:00. When the power is supplied again, the indication blinks.

7. Timer function

1) TIMER switch
When the TIMER switch is set to ON regardless of the POWER switch setting, the power is turned off and the timer functions. The CLOCK-1 and ON TIME are compared and power is supplied when the set times coincide. Then the CLOCK-2 and OFF time are compared and power is shut off when the set times coincide.
When the ON and OFF times are the same, the power is not turned on.
When CLOCK-1 indication blinks, setting the TIMER switch ON will not operate the timer and the TIMER ERROR indicator will lights.

2) Time setting

Function	Hour	Minute	Operation
ON/OFF	ON	ON	Reset to 0:00.
TIME	ON	OFF	The minutes digits are maintained and the hours digits are incremented.
	OFF	ON	The hours digit is maintained and the minutes digits are incremented.

The HOUR and MINUTE switches function in the same way as for the clock.

3) The CLOCK and ON/OFF TIME are displayed regardless of the POWER switch setting.

8. BACK UP

When the memory back up lithium battery is loaded, the data (frequency and mode) stored in the memory, last reception frequency and mode and ON/OFF TIME are backed up even when the power is shut off.

9. Dimmer function

When the DIMMER switch is set to ON or the POWER switch is set to OFF, the brightness of the digital display and meter decreases, resulting in a dimmer effect.

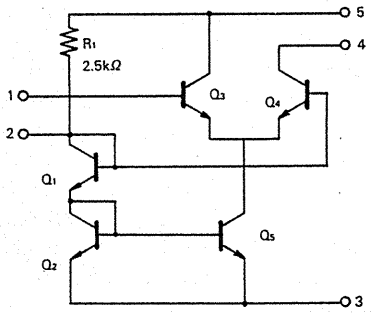

Fig. 3 TA7060P (RX unit Q32)

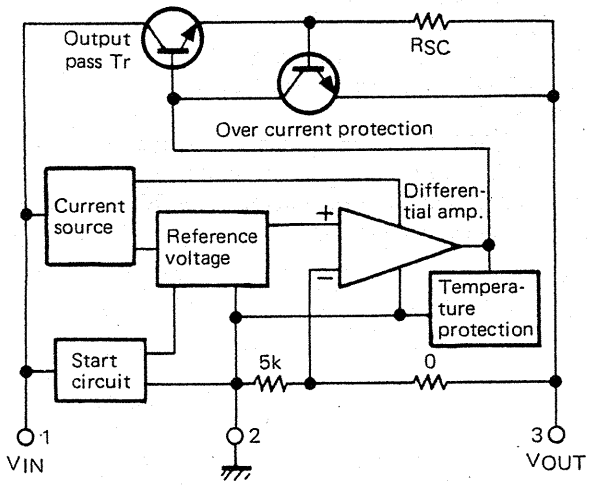

Fig. 4 AN7809 (RX unit Q54, PLL unit IC20)
AN7805 (PLL unit IC18, 19)

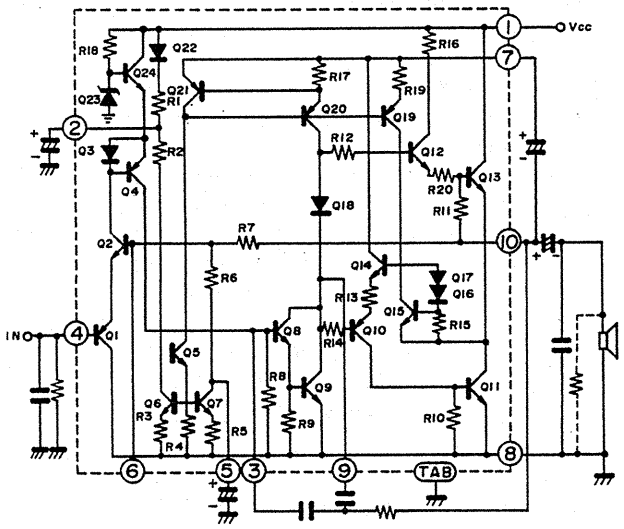

Fig. 5 HA1368R (RX unit Q57)