Three Charge Sensitive Amplifier Circuits

This paper describes three charge sensitive amplifier circuits – two commercial models and a new experimental circuit. Charge sensitive amplifiers take an input current pulse and deliver an output voltage proportional to the total charge contained in the input pulse. This performs several useful functions: the integration performed by the amplifier serves to filter high frequency noise, and the output pulse can be many times longer than the input pulse. This last feature is very useful when used with fast plastic scintillators. These scintillators have an output pulse decay time of 3-5 nsec, so the pulse stretching performed by a charge sensitive amplifier can make amplitude discrimination much easier. A further advantage of a charge sensitive amplifier is that all output pulses have the same shape and decay time constant, assuming that the input pulse is much shorter than the decay time constant. This makes subsequent pulse processing much easier. A simple diagram of a charge sensitive amplifier is shown in Figure 1. The major circuit elements are an inverting amplifier, a feedback charge storage capacitor and a reset circuit. . The capacitor stores charge from input pulses so that a voltage appears on the output proportional to the total charge in the input pulse. The reset network discharges the capacitor between pulses. Without the reset circuit, the output voltage is essentially a step function, with an extremely long decay time dependent on the amplifier offset voltage, input bias current, and miscellaneous leakage currents. In simple implementations of this circuit, the reset network is a large value resistor. Other more complex circuits use an optically coupled FET to reset the charge storage capacitor. The circuits discussed in this paper all use resistor reset.

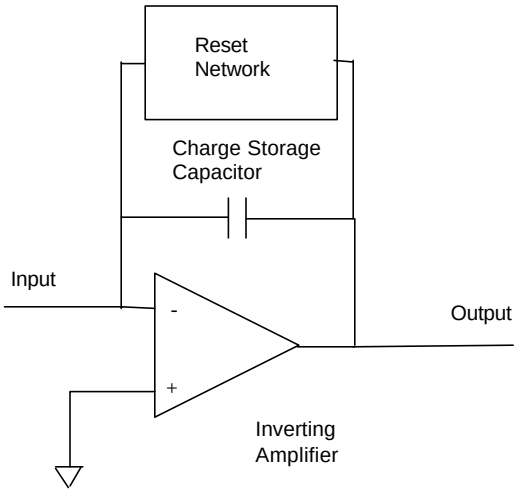

Figure 1. Basic Implementation of Charge Sensitive Amplifier

Ortec 109a Charge Sensitive Amplifier

A schematic for the charge sensitive amplifier front end of the Ortec 109a preamplifier is shown in Figure 2. The heart of this circuit is a jfet common source amplifier (Q1). The gate of Q1 is AC coupled to the input via high voltage blocking capacitor C3, in order to block any DC detector bias. C3 is included inside the amplifier AC feedback loop to avoid errors arising from the capacitive voltage divider formed between the blocking capacitor and the preamplifier input shunt capacitance. Source resistor R9 helps to set quiescent current in Q1. This resistor is bypassed by C5 to boost high frequency gain. The Q1 drain is held at a constant potential by cascode transistor Q2, thus greatly reducing the effects of Q1 drain-to-gate

capacitance. This allows both a high gain and wide bandwidth to be obtained in a single stage. R4 provides collector loading for Q1. Q3 buffers the inverting output obtained at R4 and applies it to emitter follower Q4. Q5 provides current source loading at the emitter of Q4. Current source loading is a common technique for increasing the linearity of an emitter follower stage. R11, R12, and R14 set the quiescent current in Q5. R11 bypasses the voltage divider formed by R11 and R12. Capacitor C6 provides "bootstrap" drive from the output of the amplifier back to the Q2 collector. Bootstrapping helps to provide extra output voltage swing by forcing the Q1 collector higher or lower than the positive supply rail. R5 isolates the Q1 collector and load resistor from the positive rail so that the bootstrapping can take place. R44 drops some voltage to help reduce the dissipation in Q4 and Q5, as the total voltage across these transistors is 48V. R44 is bypassed by C8 so that the negative pulsed drive capability of Q5 is not reduced by R44. R15, 16, C9, and C11 provide filtering and bypass for the +/-24V rails. The overall sense of the amplifier is inverting, with voltage gain provided entirely by Q1. Charge storage capacitor C4 is connected between the input and output of the amplifier. Resistors R8 and R36 help to set the overall bias levels of the amplifier and also reset C4 between pulses. The purpose of C10 is not entirely clear to this observer. It may be present to boost the open loop AC gain of the circuit by allowing any variation in positive bus voltage due to the interaction of the amplifier front end with decoupling resistor R15 to affect the bias current in Q5. Removing C10 would probably have a minimal effect on circuit operation.

The amplifier sensitivity is 1V/picocoulomb, determined by C4. The output pulse fall time is determined by C1, R8, and R36. In a perfect circuit, these elements alone would determine the output pulse fall time, which would be the RC time constant of the 3 components (57 usec). However, actual output pulse fall time is specified as 50 usec. The extra resistance is added to compensate for the effects of leakage currents from the input FET, the printed circuit board, and capacitor C4 itself. The correspondence between theoretical and actual fall times for this circuit is actually very precise for a practical circuit. In actual circuits, the difference between theoretical and actual fall times is often as much as 5X because of miscellaneous leakage currents for non-optimal circuit implementations. Q1 is different from the original Ortec 109 (2N3819), and may have been selected for low leakage.

Bicron Charge Sensitive Amplifier

The circuit in Figure 3 is taken from a Bicron on-line document describing photomultiplier tube bases and preamplifiers. This circuit is based on the same principles as the Ortec 109 preamplifier, but incorporates some interesting variations. It is designed to operate on –24V, as opposed to the +/- 24V supplies for the Ortec 109. As in the previous circuit, the input stage is a common source jfet amplifier (Q1). Resistor R17 at the drain of Q1 helps to prevent high frequency parasitic oscillation. C7 decouples the amplifier input from the photomultiplier HV bias. Q1 quiescent current is set by R19, which is in turn bypassed to the ground rail by C8 to boost high frequency gain. Drain loading is accomplished via cascode transistor Q8 and Resistor R21. This is a single ended version of a folded cascode circuit, commonly used in modern nuclear preamplifiers to increase gain-bandwidth product. The voltage at the Q1 collector is set via voltage divider R22 and R24. C9 bypasses the voltage divider. R23 sets the DC quiescent current in Q8. C10 bypasses R23 so that it does not interfere with the high frequency action of Q8. L1 allows DC current to pass unimpeded but causes any AC signal in Q1 to modulate the current to Q8. R18 and R20 damp high frequency parasitic oscillations. The output at R21 is buffered by a discrete darlington amplifier (Q3 and Q4) to minimize loading of the gain stage. R26 at the emitter of Q3 is a high value (150k) to provide high impedance at the Q3 base and minimize loading. R27, R28, and R29 fix the bias current in Q4, but R27 is bypassed by C12 to remove it from the AC gain path. R28 provides a 50 ohm output impedance for the amplifier. This circuit is somewhat unusual in that the current for all stages is funneled through output resistors R28 and R29, possibly to slightly increase the open loop AC gain. It also somewhat complicates calculating overall circuit bias levels, though these can be readily determined empirically or by computer simulation. The circuit would probably work just as well if the preceding amplifier stages were returned to the negative rail instead of R28. R25 and C11 provide compensation to prevent oscillation or ringing. C13 and R30 provide supply filtering and decoupling. R15 provides DC feedback to help set DC bias levels and resets charge storage capacitor C6 between pulses. This circuit has a specified gain of 667 millivolts/picocoulomb, which corresponds precisely with the C6 value. The specified pulse time is 33 microseconds, which is exactly the time constant of C6 and R15.

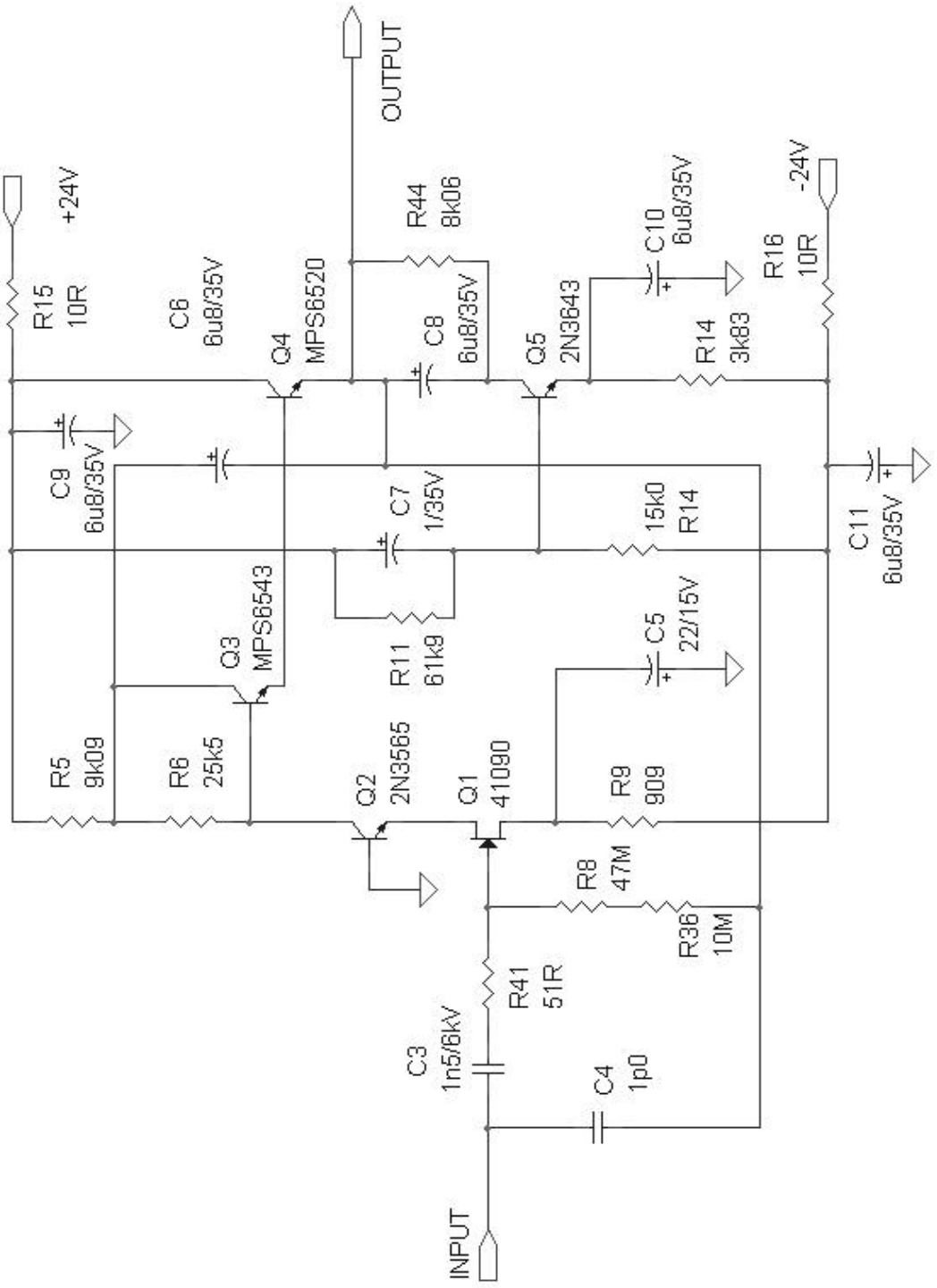

Figure 2. Ortec 109A Charge Sensitive Amplifier Schematic

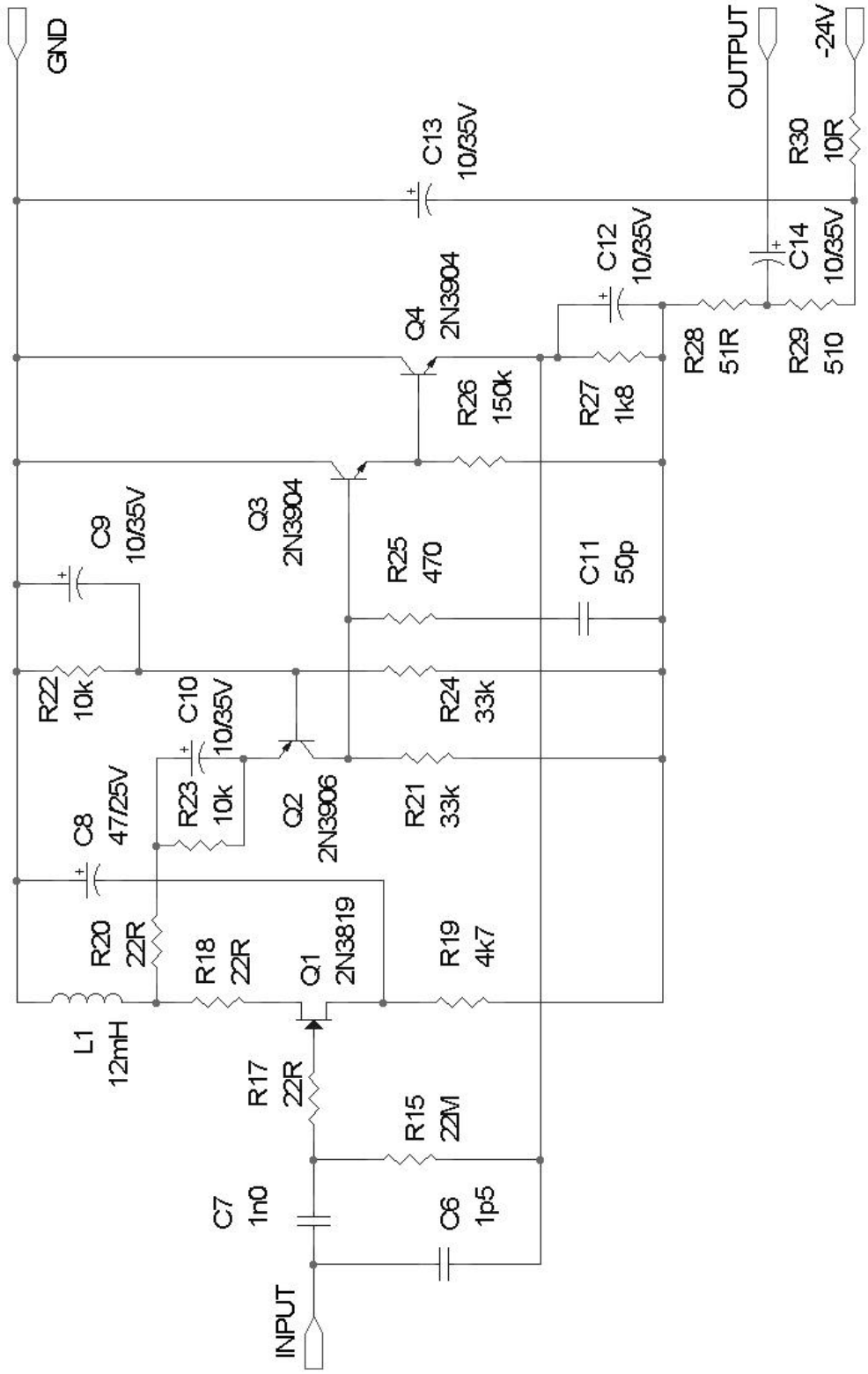

Figure 3 Bicron Charge Sensitive Amplifier schematic

Experimental Charge Sensitive Amplifier and Pulse Shaper

The circuit shown in Figure 4 is an experimental charge sensitive amplifier/pulse shaper based on the preceding two circuits, but with refinements making the quiescent bias easier to predict. As in the previous circuit, a common source amplifier (Q1) is the input stage and main gain element. Quiescent current in Q1 is set by current sink Q3. The current source is bypassed by C5 for maximum high frequency open loop gain. Series resistor R4 counteracts any instability introduced by C5. Gate resistor R5 is used to suppress extremely high frequency (>100MHz) parasitic oscillation. Current source Q2 provides current to both Q1 and cascode transistor Q4. Q4 acts to pin the Q1 drain at a constant potential set by LED voltage references D1 and D2. This serves to counteract the effect of drain to source capacitance in Q1, greatly extending its gain-bandwidth product. R6 slightly spoils the effect of cascode transistor Q4, reducing the ultimate gain-bandwidth product and helping to prevent very high frequency oscillation. As in the previous Bicron circuit, this is a single ended example of a folded cascode circuit, commonly used in modern high-speed nuclear instrumentation. The circuit operates in current differencing mode. R2 and D1 set the current in Q3 to approximately 2.7 ma. Q3 sets the current drawn by Q1 in the absence of an input signal to approximately 2mA. The remainder of the current flows in Q4. A signal applied to Q1 will vary the current drawn by it, thus changing the current directed into Q4. R8 is the actual load resistor for Q1, and sets the gain of the input stage. Instead of a discrete darlington amplifier, a small-signal N-channel mosfet is used as an output buffer. R7 prevents parasitic oscillation that can occur when a mosfet is operated in its linear region. R9 sets the quiescent current in Q5. The DC feedback loop is closed via R1, which also serves to reset charge storage capacitor C2. C1 provides input coupling and DC blocking. C1 is currently a 100nF, 63V film capacitor in the experimental prototype. In practice, this capacitor would be a much smaller high voltage part, and the junction of C1 and C2 would be connected directly to the anode resistor of a PMT, or to the biasing resistor of a semiconductor detector. LEDs D1-D3 are used as forward voltage references. They are an inexpensive method of providing a low noise, low voltage reference with much lower incremental impedance than a comparable zener diode. Red GaAsP LEDs provide almost exactly 1.6V drop at 10mA bias current. Green GaP LEDs provide almost exactly 2V drop at the same bias current. If the amplifier is used in the same enclosure as a PMT, the LEDs should be shielded with black paint or Glyptal to prevent interference with the PMT. The overall sense of the amplifier is inverting, and the gain is 21mV/picocoulomb, set by C2. The theoretical pulse fall time is 103 usec, the RC time constant of R1 and C2

The second half of the circuit is a two-pole pulse shaper. The exponential output waveform of a charge sensitive amplifier is not optimal for amplitude discrimination, as it spends very little time at maximum amplitude. It is common to cascade several integrator stages to stretch the pulse into a more suitable shape at the price of some amplitude loss. Since the process of shaping rounds the pulse profile, a very modest post amplifier can be used to recover lost signal amplitude or to further boost the signal. With a large number of cascaded integrator stages (7-8 stages) the pulse assumes a gaussian profile. A Gaussian profile is optimum for amplitude discrimination and less susceptible to pulse pile-up, as the tail time is reduced in proportion to the high amplitude portion of the waveform. Two stages are used in this example as a compromise to reduce parts count. In this circuit, the pulse shaping is performed by a unity gain second order low pass filter, implemented with P-channel mosfet source follower Q7. The cutoff frequency of the filter is set such that its time constant equals the decay time constant of the preceding charge sensitive amplifier. This condition is satisfied when the cutoff frequency of the filter, f_C, is equal to $1/\tau$, where τ is the decay time constant of the charge sensitive amplifier output pulse. C8-10 and R11-12 set the filter cutoff frequency. The filter elements are selected for Bessel alignment, for a well-damped pulse response. R13 suppresses parasitic oscillation in mosfet Q7. Bias for Q7 is provided by current source Q6. Using a current source instead of the customary resistor as the load for a source follower improves its linearity and helps make the bias level independent of supply voltage. The output is AC coupled via C12. Capacitors C3-4, C6-7, and C11 provide power supply bypassing

Input and output waveforms for the Figure 4 circuit are shown in Figures 5 and 6. The amplifier input was driven with a CMOS pulser modified to better approximate a current source. This helps to show the behavior of the amplifier with an actual detector, as both PMTs and silicon diode detectors are current output devices. The input waveform is shown in the upper trace of Figure 5. This waveform is the voltage

output of the pulser before voltage-current conversion. The pulse decay time constant (~ 200 nsec) was chosen to approximate the output from a ZnS(Ag) based fast neutron scintillator or a NaI(Tl) gamma scintillator, both of which have similar pulse relaxation times. The bottom trace of Figure 5 shows the leading edge of the CSA output waveform. Much of the leading edge ringing is caused by difference in grounding position between the input and output oscilloscope probes and a less than optimal connection between the pulser and the CSA. This ringing is completely filtered out by the following pulse shaping stage. The CSA and Pulse shaper outputs are shown together in Figure 6. The bottom trace is the CSA output, while the top trace shows the pulse shaper output. As can be seen, the shaper stretches the high amplitude region of the CSA output pulse, making accurate amplitude discrimination much easier. The pulse shaper output shows some baseline shift due to the capacitor coupled output and a relatively high pulse repetition rate (~1kHz). This counting rate would not bee seen in practice with a typical fusor. Pole-zero cancellation could also be used to help eliminate the baseline shift at high counting rates. The theoretical output pulse fall time of the CSA is the time constant of C2 and R1 (103 usec). The actual pulse fall time is about 44 usec, or less than half the predicted value. During the initial evaluation of this circuit the actual fall time difference between theoretical and actual values was five times shorter than the theoretical value. This “fall time deficit” was found to be due to several factors. Printed circuit board and input FET gate leakage currents can discharge C1at a rate faster than R1. Mounting C1, C2, R3, R5, and the Q1 gate lead on teflon push-in standoffs greatly reduced the effect of printed circuit board leakage current on the output pulse fall time. Using a mosfet instead of a jfet for Q1 also helped bring the pulse fall time more in line with expected values, though a jfet was used again in the final circuit version. Making C1 relatively large reduces the effect of leakage current on output fall time, though it also correspondingly reduces the output pulse amplitude. These measures reduced the discrepancy to its current value of 2X. Much of the remaining discrepancy is probably due to the fact that the pulser used to drive the CSA is only an approximation of a true current source. A PMT or silicon detector will deliver a current pulse and then go essentially open circuit, with only the bias resistors to provide any reverse current into the amplifier input. Unfortunately, the pulser provides a certain amount of positive drive between the negative output pulses, which acts to reset C1 faster than the predicted value. Actual input from a PMT or semiconductor detector will probably show fall times more in accordance with predicted values. In the works is a pulser specially designed to drive a charge sensitive amplifier, for circuit testing without the inconvenience of using an actual detector setup.

References

Glenn F. Knoll, Radiation Detection and Measurement, Third Edition

Helmuth Spieler Instrumentation Notes: www-physics.lbl.gov/~spieler

Don Lancaster, Active Filter Cookbook

www.hep.ph.ic.uk/~hallg/instrumentation/lectures

www.mssl.ucl.uk/~pdt/lectures/3C64/strand1

The last two URLs host a series of lecture notes covering nuclear instrumentation and electronics. They cover some of the same topics as the Spieler notes, but in condensed, easy to absorb form. They also mention some practical details not covered by Spieler.

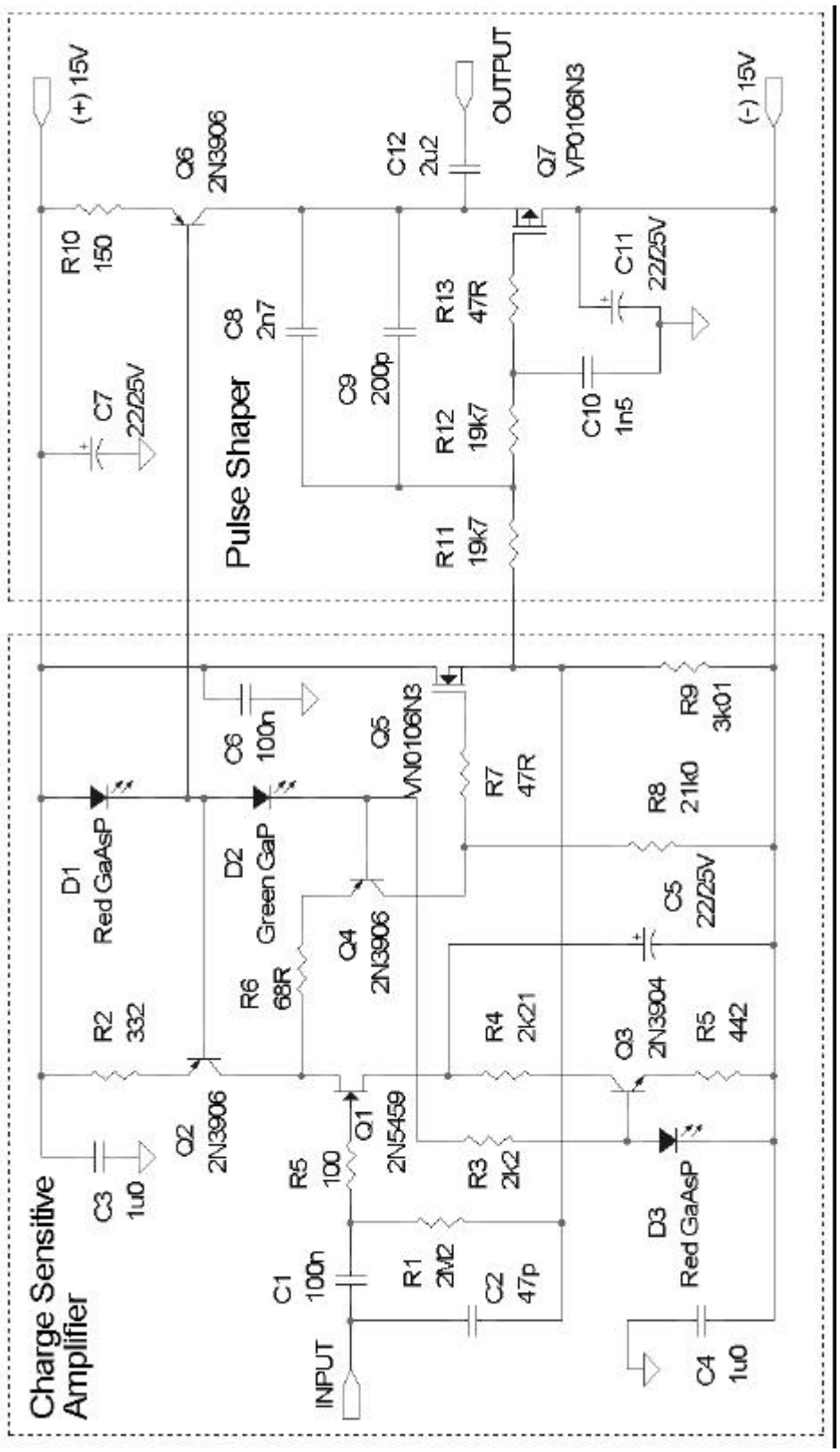

Figure 4. New Charge Sensitive Amplifier with Pulse Shaper

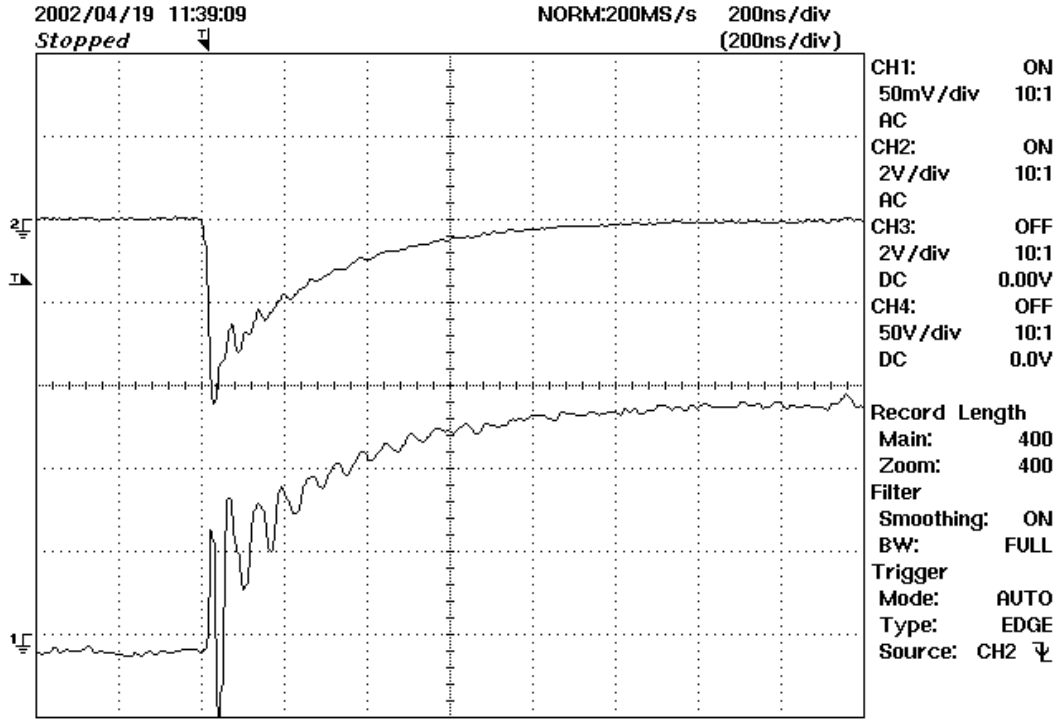

Figure 5. Upper Trace: Charge Sensitive Amplifier Input Pulse 2V and 200 nsec/div
Lower Trace: Charge Sensitive Amplifier Output Leading Edge 50 mV and 200 nsec/div:

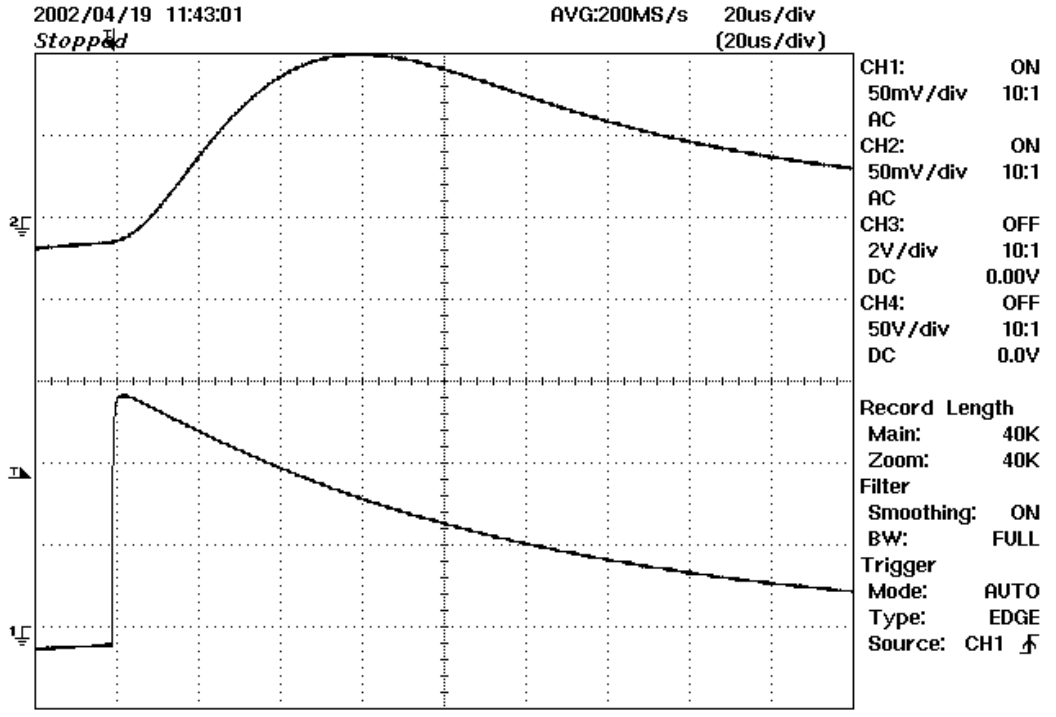

Figure 6. Upper Waveform: Pulse Shaper Output 50mV and 20 usec/div
Lower Waveform: Charge Sensitive Amplifier Output 50mV and 20 usec/div