ECEN 325 Final Project: BJT Design

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1 Objective

The objective of this project is to design and construct a working three stage amplifier using the NPN 2N2222 type bipolar junction transistors. This amplifier must have a gain of 50 (34 dB), with an input impedance of greater than 200kΩ. The amplifier should be designed such that it operates off of a 5V DC supply with a maximum input signal of 5mV. Harmonic distortions should be kept below -30dB, in order to preserve the fidelity of the signal. The amplifier should be designed with a 50Ω load in mind.

2 Design

As suggested, this amplifier was first designed at the output stage. Subsequent stages were designed to achieve the necessary voltage gain and the input stage was designed to achieve the input impedance. Resistors must be chosen for the standard values. (In practice the values of the resisters vary anyways) For this design assume the 2N2222 transistors have a $\beta = 150$. I use the convention that resistors connected between base and ground are R_{B2}, base and V_{CC} R_{B1}, collector R_C, and emitter R_E. The load seen by a stage is denoted by R_L.

2.1 Output stage

Since the load is 50Ω the output stage must have a low output impedance. Using BJT's, a common collector configuration will satisfactorily drive low output impedances with a high current gain and a voltage gain of less than unity. Since the load resistance is already know, this circuit needs to be designed with three resistors in mind: R_{B1},R_{B2}, and R_E.

So that g_m will be larger, let the collector current $I_{CQ} = 10\text{mA}$. For the output to accommodate the 250mV maximum swing, V_E must be at least 250mV, preferably higher. For the transistor to remain in the saturation region $V_{CE} > 300\text{mV}$ as well. Considering this along with the input impedance of the circuit, R_E is chosen as 200Ω, putting $V_E = 2\text{V}$.
Let $R_{B2} = 1\text{Meg}\Omega$, so that R_{B1} can be solved from the mesh:

$$\frac{5 \cdot 1\text{M}}{1\text{M} + R_{B1}} = 2 + 0.7 + \frac{10\text{mA}}{150}\frac{1\text{M} \cdot R_{B1}}{1\text{M} + R_{B1}} \tag{1}$$

Solving this equation, we find that $R_{B1} = 33\text{k}\Omega$
Knowing all the resistors, the gain, input impedance, and DC simulations may be found. The gain is just:

$$A_v = \frac{R_L||R_E}{R_L||R_E + 1/g_m} \tag{2}$$

$R_L||R_E = 200||50 = 40$ and $g_m = 10\text{mA}/26\text{mV} = 0.3846$ such that $A_v = 0.939$.
The input impedance is found to be:

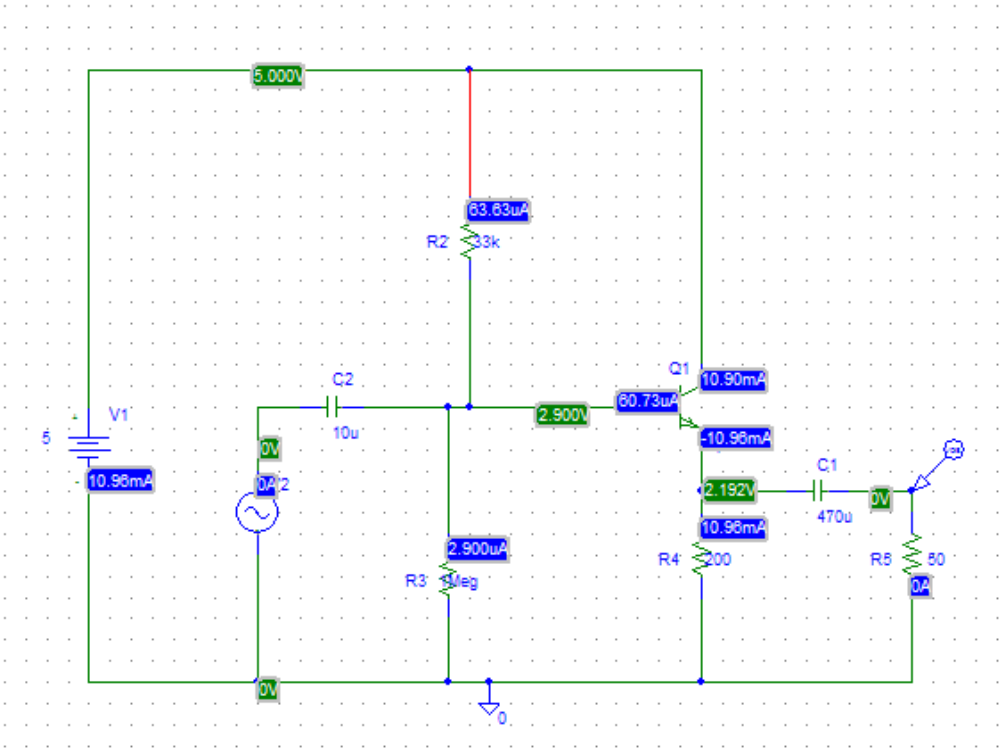
$$A_{v3} = \frac{R_L||R_E}{R_L||R_E + 1/g_m} \tag{3}$$

$$Z_{in} = R_{B1}||R_{B2}||(r_\pi + (1+150)R_E||R_L) \tag{4}$$

$(r_\pi + (1+150)R_E||R_L) = (\frac{26 \cdot 150}{10} + 151 \cdot 40) = 6\text{k}$.

$Z_{in} = 1\text{M}||33\text{k}||6\text{k} = 5.356\text{k}$. This impedance will aid in the design of the next stage.

Pictured is the Pspice schematic of the output stage. The DC bias voltages are as expected, within reasonable tolerance. AC and transient simulations (not pictured) confirm the gain of the amplifier. Capacitors were chosen for an appropriate passband.



2.2 Middle stage

This stage must have appreciable voltage gain, so a common emitter configuration is employed, and the emitter resistance seen by AC voltages is kept low using an emitter capacitance along with two emitter resistors. Let $I_{CQ} = 1\text{mA}$. For $V_E = 1\text{V}$, let $R_E = R_{E1} + R_{E2} = 91 + 910 = 1.001\text{k}\Omega$.

Let $R_{B2} = 1\text{Meg}\Omega$, so that $g_m = 1/26 = 0.0384$ The base mesh then satisfies:

$$\frac{5 \cdot 1\text{M}}{1\text{M} + R_{B1}} = 1 + 0.7 + \frac{1\text{mA}}{150} \frac{1\text{M} \cdot R_{B1}}{1\text{M} + R_{B1}} \tag{5}$$

Solving for R_{B1} we have R_{B1} =400kΩ. For common-emitter type amplifiers the voltage gain is:

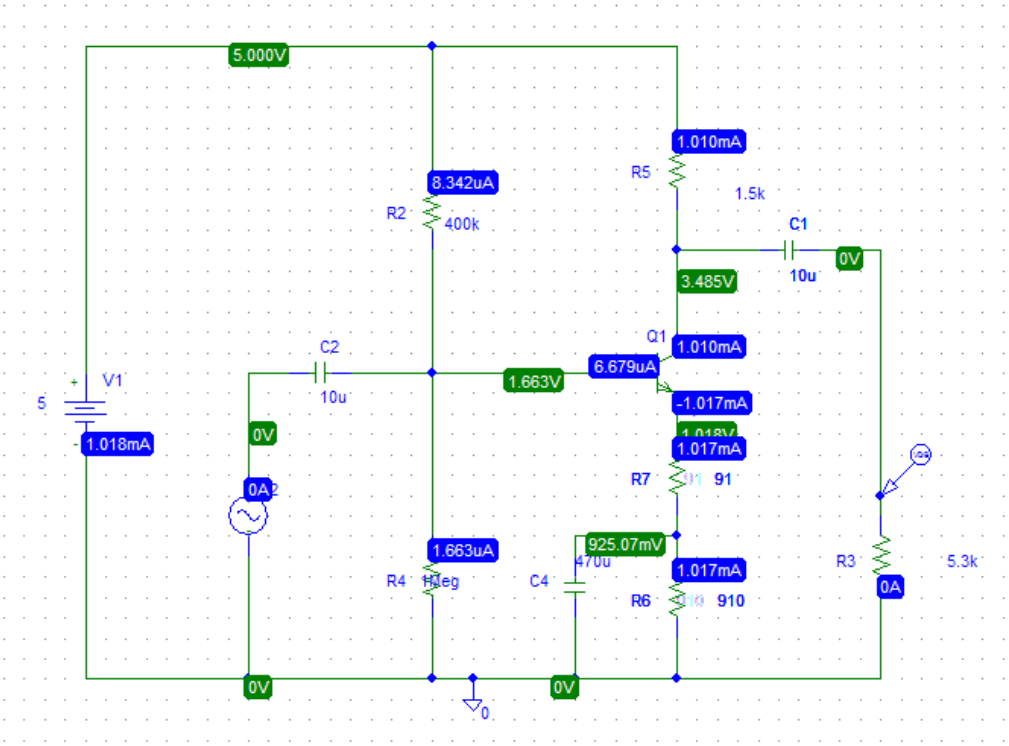
$$A_{v2} = \frac{g_m R_C || R_L}{1 + g_m R_{E1}} \tag{6}$$

With the malice of forethought, the gain of this stage shall be set at 9.98 V/V. Solving (6), we get that $R_C = 1.8\text{k}\Omega$. The input impedance is similar to the output stage, such that:

$(r_\pi + (1 + 150)R_{E1}) = (\frac{26 \cdot 150}{1} + 151 \cdot 91) = 17.6\text{k}.$

$Z_{in} = 1\text{M}||400\text{k}||17.6\text{k}= 16.57\text{k}.$

With that there is now a complete description of the middle stage. The collector voltage is maintained at 3.485V, so that V_{CE} is much in excess of 300mV, ensuring the transistor is operating properly. The input impedance of the output stage is included in the simulation, and the simulation agrees closely with the calculations.



2.3 Input stage

Again a common emitter configuration is used. This stage must be designed carefully in order to have an input impedance exceeding 200kΩ. Specifically, the emitter resistance must be very high for the input impedance to be high. Using a low current operating point will allow the transistor to operate with tolerable voltages and will also increase r_π. Thus, let $I_{CQ} = 0.1$mA, so that $g_m = 0.00384$. With consideration to the input impedance, R_E is chosen as 2kΩ, such that $V_E = 0.2V$. Using the same procedure as in previous stages, choose $R_{B1} = 1$MΩ and solve for R_{B2}:

$$\frac{5 \cdot R_{B2}}{1\text{M} + R_{B2}} = 0.2 + 0.7 + \frac{1\text{mA}}{150}\frac{1\text{M} \cdot R_{B2}}{1\text{M} + R_{B2}} \tag{7}$$

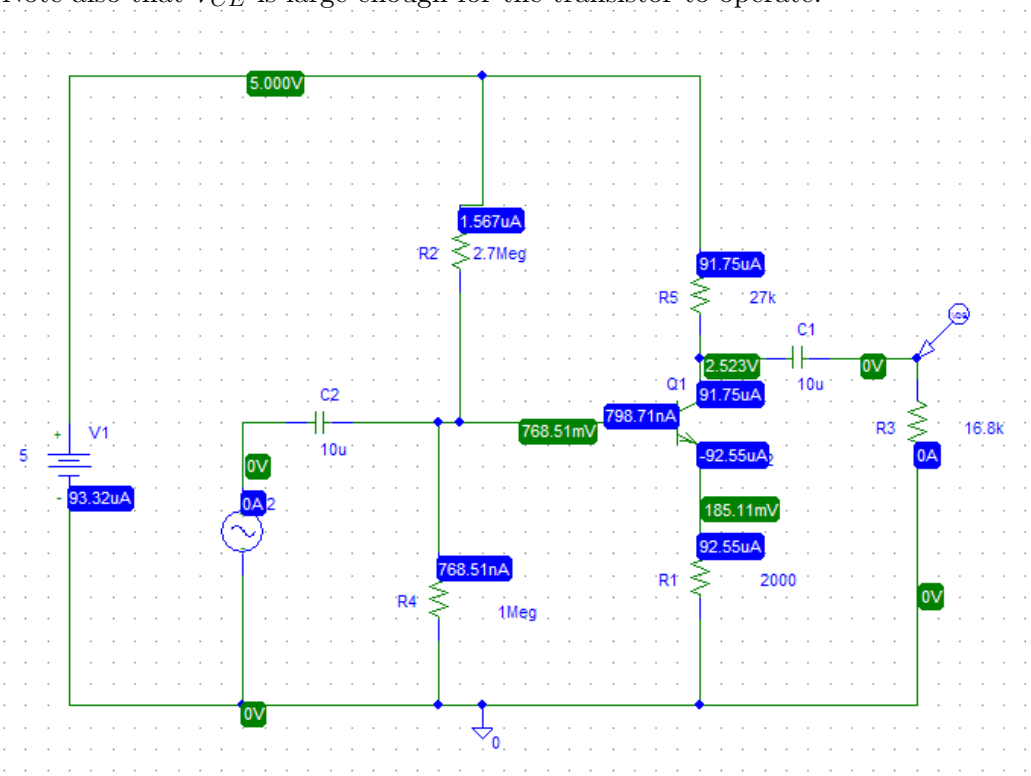
$R_{B2} = 2.7$MΩ, after solving. The gain of this circuit must be set so that the overall gain is 50V/V. The combined gain is $50 = 0.939 \cdot 9.98 \cdot A_{v1}$. This means A_{v1} need only be about 5.33V/V. Since we know the gain, g_m, and R_E, then R_C may be solved from the gain:

$$A_{v1} = \frac{g_m R_C || R_L}{1 + g_m R_E} \tag{8}$$

$R_C = 27$k from this analysis. Lastly, we check the input impedance of this stage:

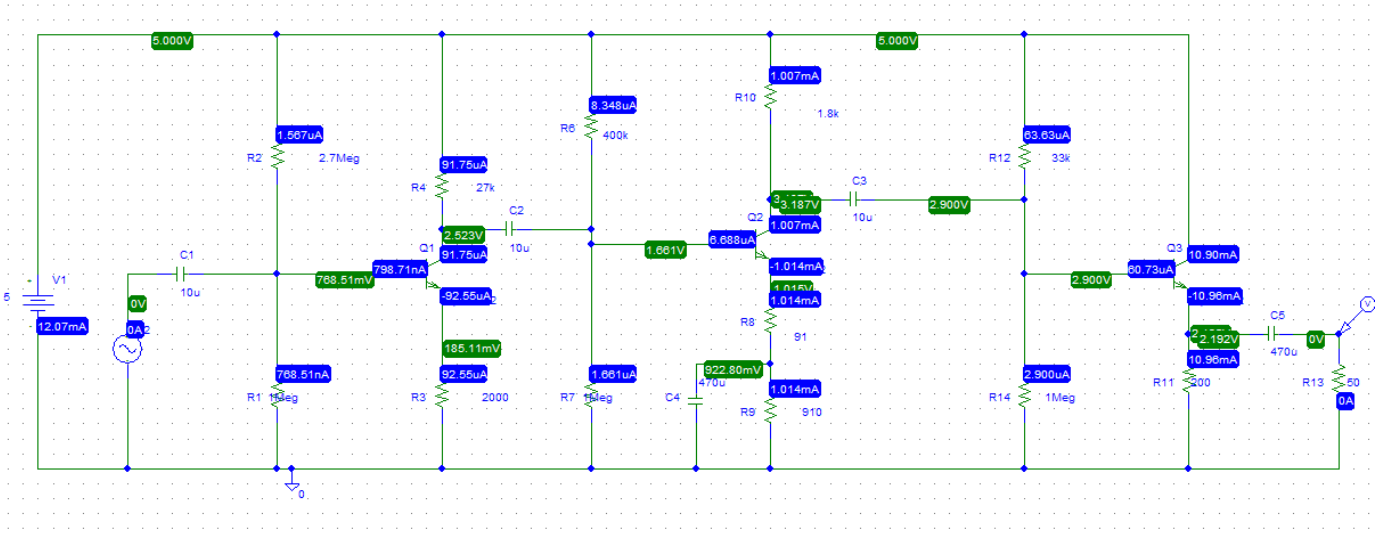
$(r_\pi + (1 + 150)R_E) = (\frac{26 \cdot 150}{0.1} + 151 \cdot 2k) = 17.6$k.

$Z_{in} = 1\text{M}||2.7\text{M}||17.6\text{k} = 232.4$k.
This is good, since an input impedance of greater than 200kΩ was specified. Checking the DC bias in Pspice, we see that I_{CQ} is a little off, but the gain characteristic (not shown) is appropriate. Note also that V_{CE} is large enough for the transistor to operate.

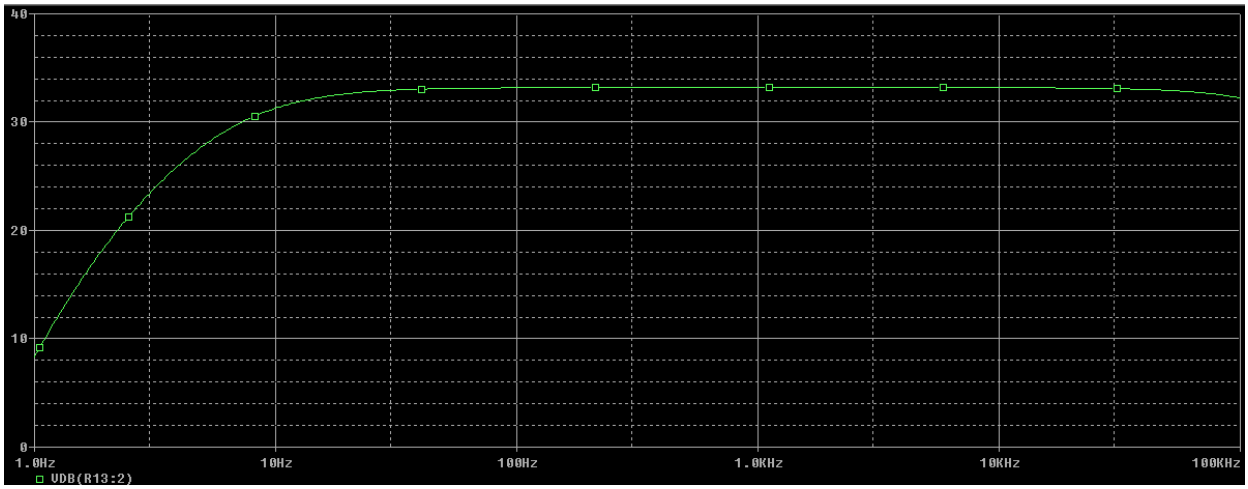


3 Simulations

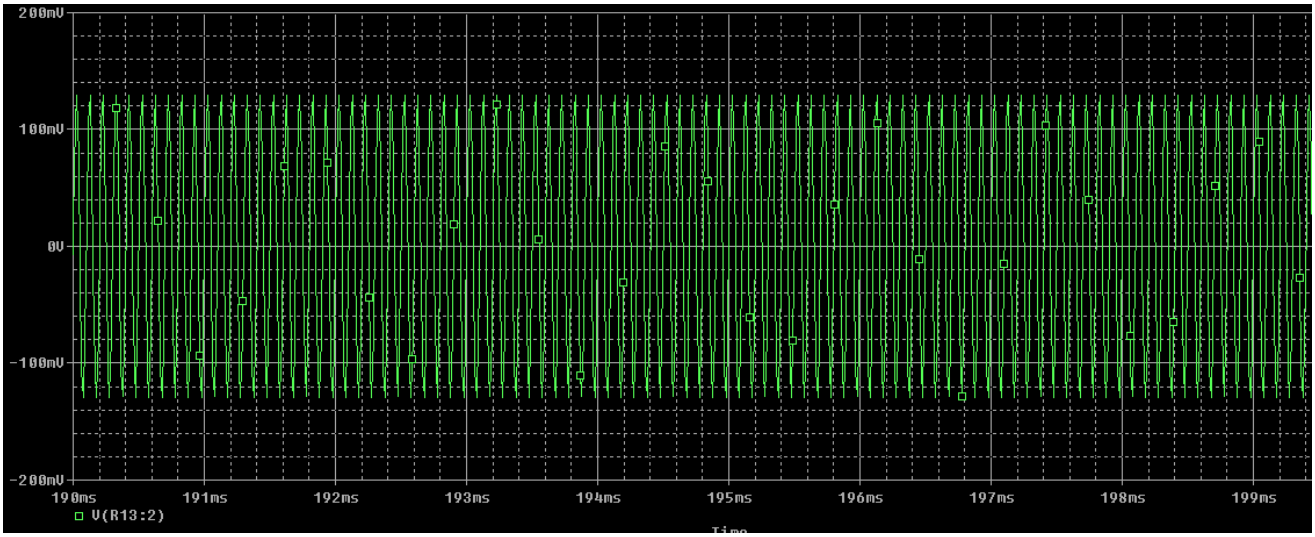
This is the final circuit, with the DC bias voltages and currents shown. Note that the DC values remained unaffected when the stages are connected, due to coupling capacitors.



Running an AC analysis reveals the transfer function of the circuit. This amplifier will operate with 34dB (about 50V/V) of gain in the passband. The low corner frequency is at just under 10Hz and the high frequency corner is at around 100kHz, so that the amplifier will operate appropriately in the audio region.

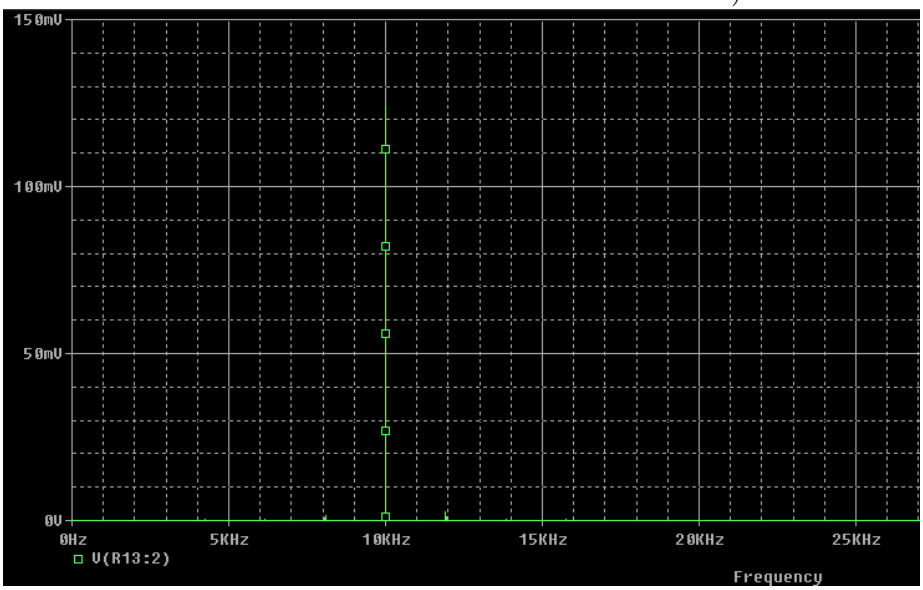


This is a transient simulation of a 10kHz input with an amplitude of 2.5mV. As expected, the output has an amplitude of 125mV.



It was found in further transient simulations that the amplifier behaved properly for input signals up to 6mV, putting it safely within the design constraint of a 5mV maximum input.

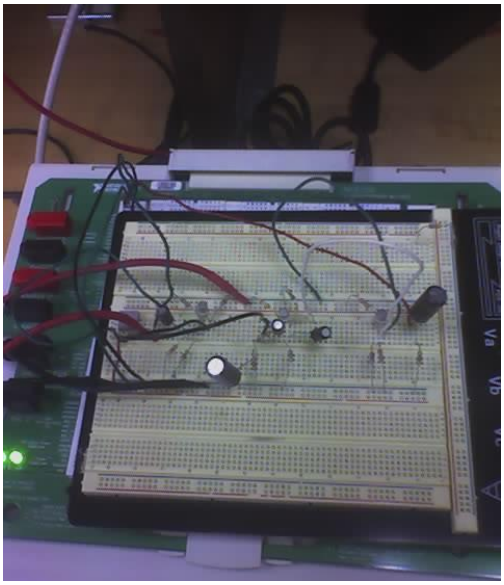
The last simulation result is the FFT of the transient simulations.As expected, the harmonic distortions in simulation are greater than -30dB below the fundamental. (In fact, using the Pspice cursors the first order harmonic could not even be found.)



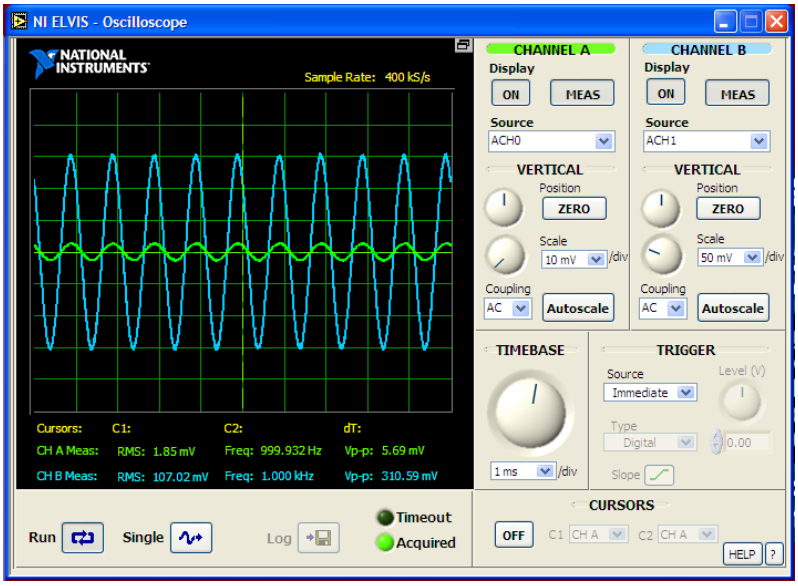
4 Laboratory Results

The circuit was then built in the lab for testing. Building it was straightforward and it worked immediately using the values of resistance and capacitance specified in the design. Pictured below is the complete circuit. The signal input came from a HP function generator and was reduced by using a 1MΩ potentiometer as a voltage divider. All measurements were made using the NI ELVIS

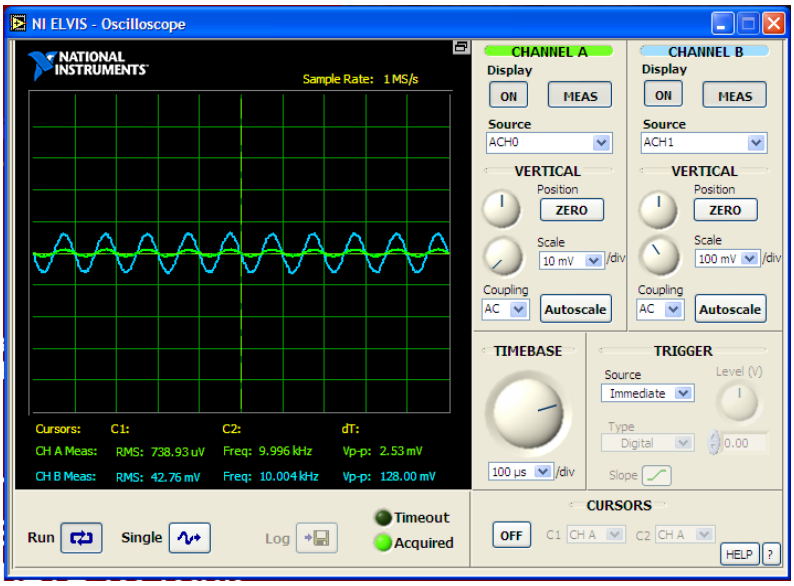
oscilloscope and dynamic signal analyzer.



Transient measurement for a 5mV$_{pp}$ 10kHz input signal:

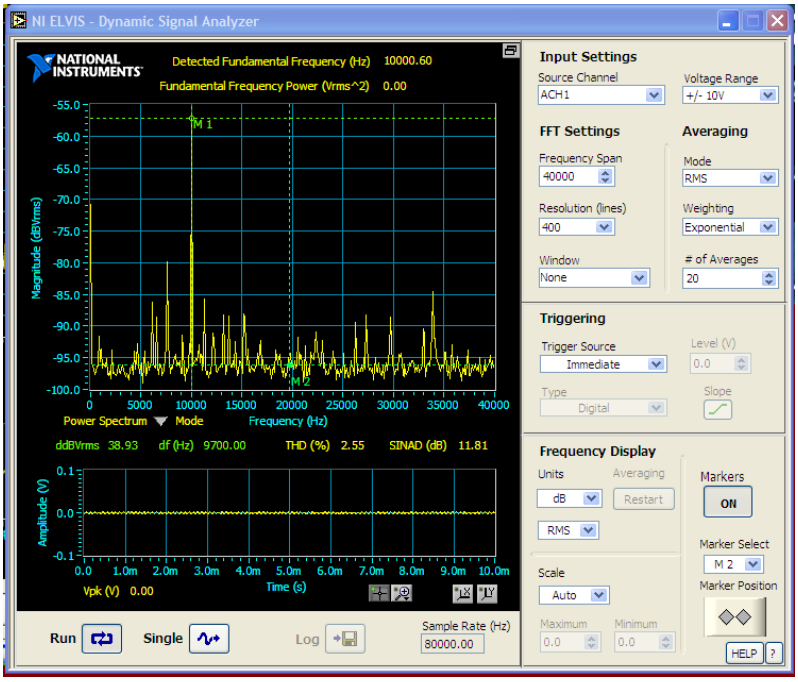


With a 2.5 mV$_{pp}$ 10kHz input signal:



The measured gain is then $128\text{mV}_{pp}/2.53\text{mV}_{pp} = 50.59\text{V/V}$, and similarly for the 5mV_{pp} signal. This is quite good, considering the specified voltage gain needed to be 50V/V. The measured value is only 1.17% off of specification.

The other measurement made in the lab was the distortion analysis for a 10kHz input signal. Pictured below is the result. This is result is quite good, as the first harmonic is well below the -30dB specified. In fact, it's about 40 dB below the fundamental (Using the cursors as a guide).



5 Conclusions

Using a stage-by-stage design, an amplifier with desired voltage gain and imput impedance was constructed using 2N2222 BJT's. A robust amplifier can be designed in this manner, as evidenced by the ease of construction in the lab. The small-signal model used for design works quite well in practice, considering the results. This design also is fairly insensitive to changes in the transistor's β, so that the characteristics of the circuit are contingent only on the external network of resistors and capacitors. Amplifiers of this type have real-world applications, particularly in audio circuits.

ELEN 325 LAB

Spring 2008

Lab No. Final Project

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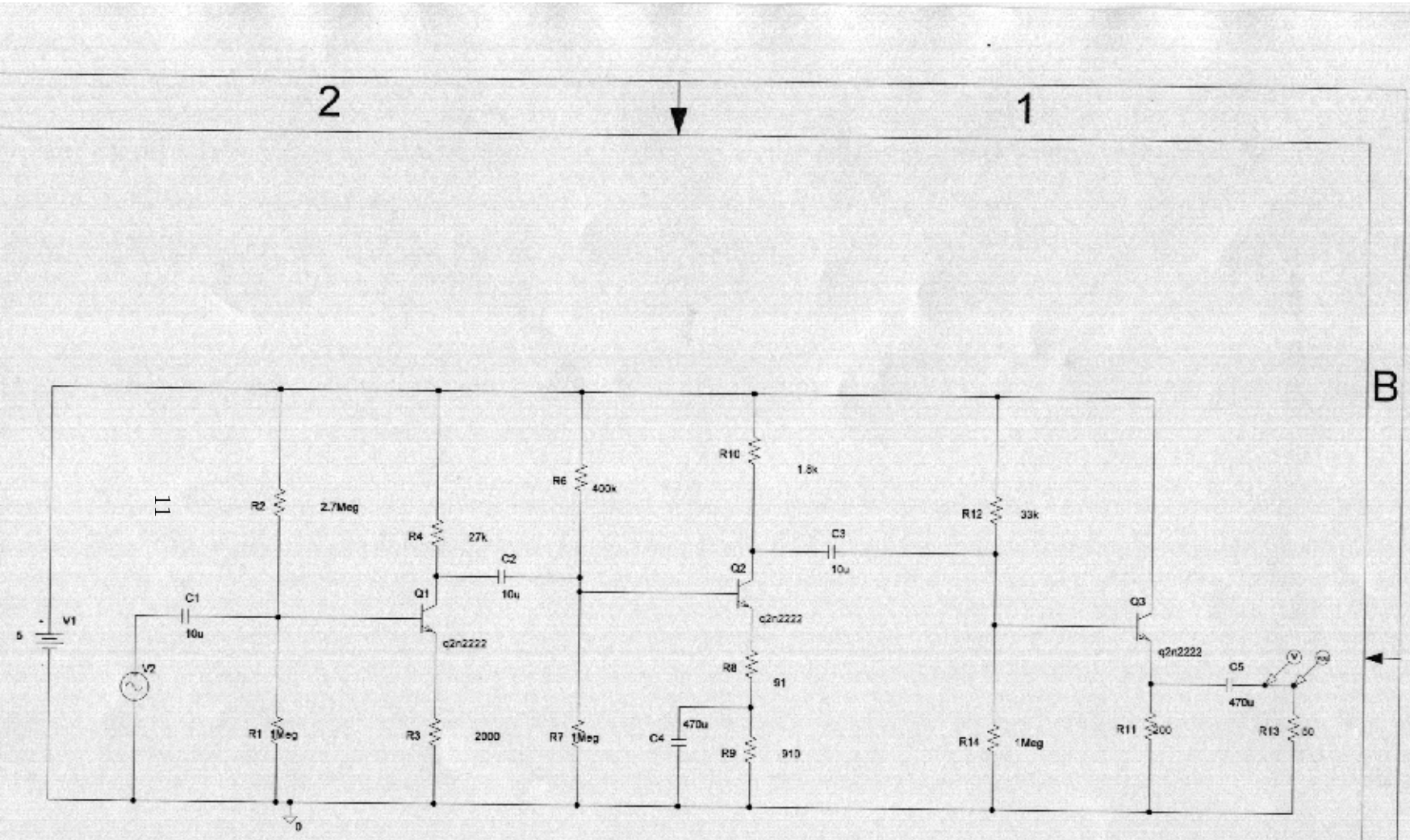
Comments: Everything work fine



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