# DATA SHEET

*( DOC No. HX8357-C01-DS )*

Temporary Version

## HX8357-C01

320RGB x 480 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

*Temporary version 01 April, 2011*

**Himax Technologies, Inc.**
http://www.himax.com.tw

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# 1. General Description

This document describes Himax's HX8357-C01 supports HVGA resolution driving controller. The HX8357-C01 is designed to provide a single-chip solution that combines a source driver, power supply circuit to drive a TFT-LCD panel with 320RGBx480 dots at maximum.

The HX8357-C01 can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-C01 also supports various functions to reduce the power consumption of a TFT-LCD panel via software control.

The HX8357-C01 supports several interface modes, including MPU MIPI DBI Type B interface mode, MIPI DPI/DBI Type C interface mode, MIPI DSI (Display Serial Interface) interface mode and MDDI interface. The interface mode is selected by the external hardware pins IM2~0.

The HX8357-C01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

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# 2. Features

## 2.1 Display

- Resolution:
  - 320(H) x RGB(H) x 480(V)
- Display Color modes
  - Normal Display Mode On
    1. DBI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
    2. DPI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
    3. MDDI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
    4. MIPI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
  - Idle Mode On
    – 8 (R(1),G(1),B(1)) colors

## 2.2 Display module

- Frame Memory area 320 (H) x 480 (V) x 18 bits
- On module DC/DC converter
- VSP = 5.2 V for two time pump (Power supply for driver circuit range)
- VSP = 6.2 V for three time pump (Power supply for driver circuit range)
- VSN = -5.2 V for two time pump (Power supply for driver circuit range)
- VSN = -6.2 V for three time pump (Power supply for driver circuit range)
- VSPR =3.3V to 5.8V (Positive Source output voltage range)
- VSNR= -3.3V to -5.8V (Negative Source output voltage range)
- VGH = +9.0 to +16.5V (Positive Gate output voltage range)
- VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- VCOM=-2.5V to 0V

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## 2.3 Display Control interface

- MIPI-DBI 8-/9-/16-/18-bit MPU parallel interface.
- MIPI-DBI Serial data transfer interface.
- MIPI-DPI 8-/16-/18-data lines parallel video (RGB) interface.
- MIPI-DSI interface.(for Display Serial Interface Version 1.01 and D-PHY Version 1.00)
- MDDI (Mobile Display Digital Interface) interface.(Support VESA Mobile Display Digital Interface Standard Version 1.2)

## 2.4 Input power

- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V(TBD)

## 2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- One chip solution for COG assembly
- Support 1-dot/2-dot/4-dot/column inversion/Zig-Zag inversion
- Support Area scrolling
- Support Partial display mode
- Support Deep standby mode
- Support normal black/normal white LCD
- Support wide view angle display
- On-chip OTP (One-time-programming) and MTP(four-time-programming for ID and VCOM register)
- Built-in internal OTP power
- Support Content Adaptive Brightness Control(CABC) function
- Support Digital 3-Gamma function
- Operating temperature range : -40℃~ 85℃

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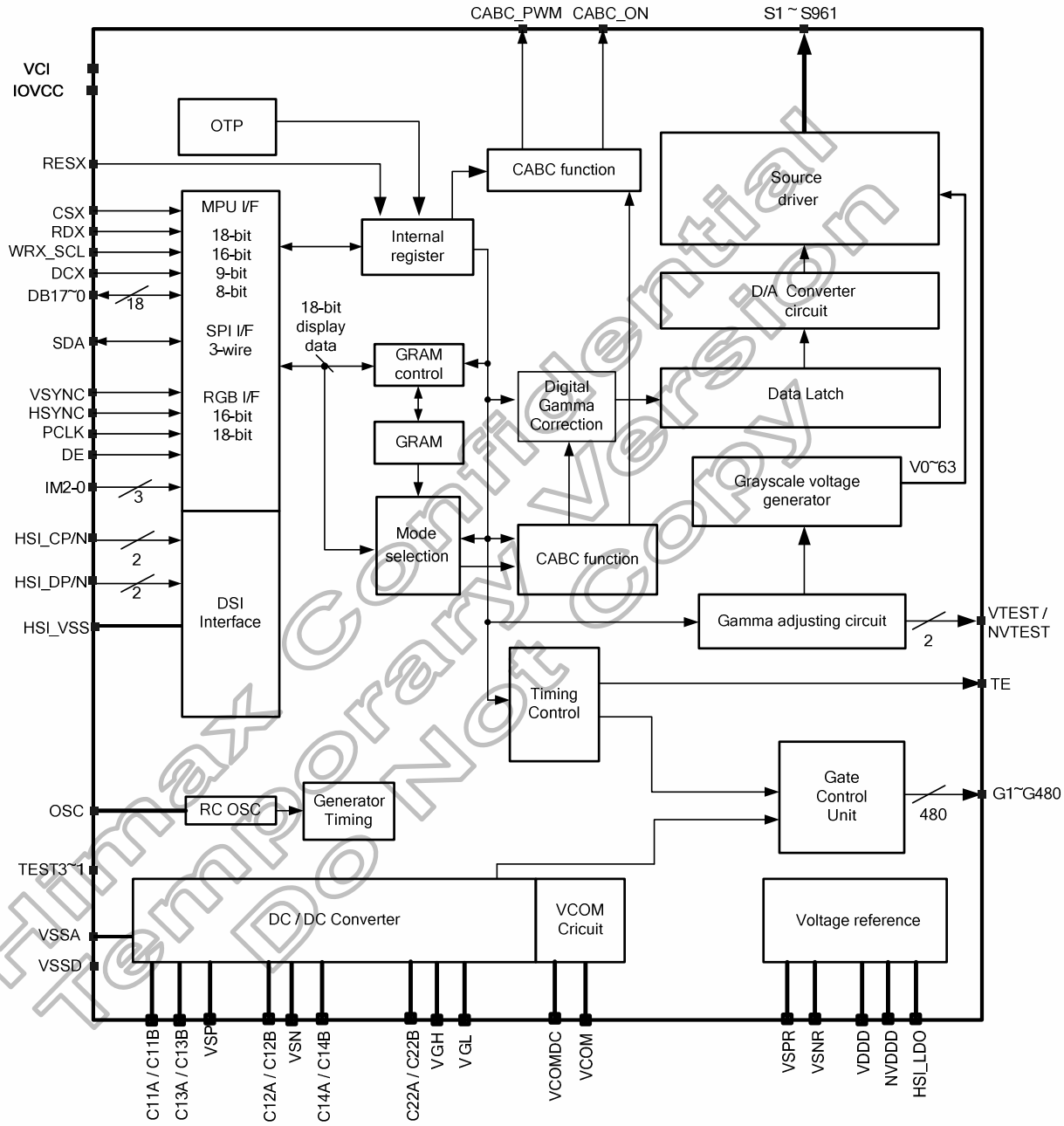
# 3. Block Diagram

## 3.1 Block diagram

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## 3.2 Pin description

<table>
<tr><th colspan="5">Interface Logic Pin</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM2,IM1,IM0</td><td>I</td><td>3</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI TYPE-B 18-bit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI TYPE-B 9-bit</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI TYPE-B 16-bit</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI TYPE-B 8-bit</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MDDI + DBI TYPE-C Option 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI TYPE-C Option 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI DSI</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI TYPE-C Option 3</td></tr>
</table></td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.<br>Low: chip can be accessed;<br>High: chip cannot be accessed.</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B mode: Serves as a write signal and write data at the low level.<br>DBI Type-C mode: it servers as SCL (Serial Clock)<br>Fix it to IOVCC or VSSD level when not used.</td></tr>
<tr><td>RDX</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B: Serves as a read signal and read data at the low level.<br>If not used, please fix this pin at IOVCC or GND level</td></tr>
<tr><td>DCX</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B, Type-C Option 3: Data / Command Selection pin<br>If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Vertical synchronizing signal in DPI interface.<br>Let to open or connected to VSSD.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Horizontal synchronizing signal in DPI interface.<br>Let to open or connected to VSSD.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in DPI I/F mode.<br>Let to open or connected to VSSD.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Data enable signal in DPI interface.<br>Let to open or connected to VSSD.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>DIN_SDA</td><td>I/O</td><td>1</td><td>MCU</td><td>Serial data input pin and output pin in serial bus system interface.<br>The data is inputted on the rising edge of the SCL signal.<br>If not used, please let it open</td></tr>
<tr><td>DOUT</td><td>O</td><td>1</td><td>MPU</td><td>Serial data output.<br>If SDO_EN=0, DOUT is not use.<br>If SDO_EN=1, DOUT is serial data output.<br>Let it to open in MPU interface mode.</td></tr>
<tr><td>DB17~0</td><td>I/O</td><td>18</td><td>MPU</td><td>24-bit bi-directional data bus.<br>The unused pins let to open or connected to VSSD.</td></tr>
</table>

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| Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| S1~S961 | O | 961 | LCD | Output voltages applied to the liquid crystal. |
| G1~G480 | O | 480 | LCD | Gate driver output pins. These pins output VGH, VGL.(If not used, should be open). |
| VCOM | O | 13 | TFT common electrode | The power supply of common voltage in TFT driving. Connect this pin to the common electrode in TFT panel. |
| TE | O | 1 | MPU | Tearing effect output.<br>If not used, please open this pin. |
| CABC_PWM1/<br>CABC_PWM2 | O | 1/1 | Backlight Circuit | CABC backlight control PWM signal output. |
| CABC_ON | O | 1 | Backlight Circuit | LED Driver Enable Signal.<br>If not used, please open this pin. |

| Input/Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| C11A,C11B<br>C13A, C13B | I/O | 11,11<br>10,10 | Step-up Capacitor | Connect to the step-up capacitors for step up circuit 1 operation (VSP). |
| C12A,C12B<br>C14A,C14B | I/O | 6,6<br>13,14 | Step-up Capacitor | Connect to the step-up capacitors for step up circuit 3 operation (VSN). |
| C22A,C22B | I/O | 12,13 | Step-up Capacitor | Connect to the step-up capacitors for step up circuit 1 operation (VGH/VGL). |

| Power Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| IOVCC | P | 7 | Power Supply | Digital IO Pad power supply. |
| VCI | P | 22 | Power Supply | Analog power supply. |
| VSSD | P | 13 | Ground | Digital ground. |
| VSSA | P | 8 | Ground | Analog ground. |
| VDDD | O | 11 | Stabilizing capacitor | For internal logic voltage. Connect to a stabilizing capacitor. |
| NVDDDOUT | O | 10 | Open | For internal logic voltage |
| VSPROUT | O | 4 | Open | Internal generated stable power for source driver unit. |
| VSNROUT | O | 7 | Open | Internal generated stable power for source driver unit. |
| VSP | O | 9 | Stabilizing capacitor | An output from the step-up circuit1.<br>Connect a stabilizing capacitor between VSSA and VSP. |
| VSN | O | 11 | Stabilizing capacitor | An output from the step-up circuit3.<br>Connect a stabilizing capacitor between VSSA and VSN. |
| VGH | O | 8 | Stabilizing capacitor | A positive power output from the step-up circuit 2 for the gate line drive circuit.<br>Connect a stabilizing capacitor between VSSA and VSN. |
| VGL | O | 10 | Open | A negative power output from the step-up circuit 2 for the gate line drive circuit. |
| VCOMDC | O | 3 | Stabilizing capacitor | An output of VCOM level.<br>Do not use VCOMDC as VCOM that supplies voltage to panel. |

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| High speed interface parts | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| HSI_DP, HSI_DN | I/O | 2/2 | DSI Host / MDDI Host | High speed interface data differential signal input/output pins. If not used, please open or connect it to VSSA |
| HSI_CP, HSI_CN | I | 2/2 | DSI Host / MDDI Host | High speed interface CLOCK differential signal input pins. If not used, please open or connect it to VSSA |
| HSI_VSS | P | 4 | Ground | High speed interface analogy ground. HSI_VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise. |
| HSI_LDO | O | 3 | Capacitor | High speed interface regulator output pin. Connect to a stabilizing capacitor between HSI_VSS and HSI_LDO If not used, please open these pins. |

| Test pin and others | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| TEST1 | I | 1 | Open | Test pin input (Internal pull low). If not used, please open or connect it to VSSA |
| TEST2 | I | 1 | Open | Test pin input (Internal pull low). If not used, please open or connect it to VSSA |
| TEST3 | I | 1 | Open | Test pin input (Internal pull low). If not used, please open or connect it to VSSA |
| OSC | I | 1 | Open | A test pin. Please let it open |
| DB18<br>TS0_DB19<br>TS1_DB20<br>TS2_DB21<br>TS3_DB22<br>TS4_DB23 | I/O | 6 | Open | A test pin. Please let it open |
| TESTDP | O | 1 | Open | A test pin. Please let it open |
| VTEST | O | 1 | Open | A test pin. Please let it open |
| NVTEST | O | 1 | Open | Gamma voltage of Panel test pin output. Must be left open. |
| DUMMY1~30 | - | 18 | Open | Dummy pads. Please let it open |
| DUMMY_VCL | - | 9 | Open | Dummy pads. Please let it open |

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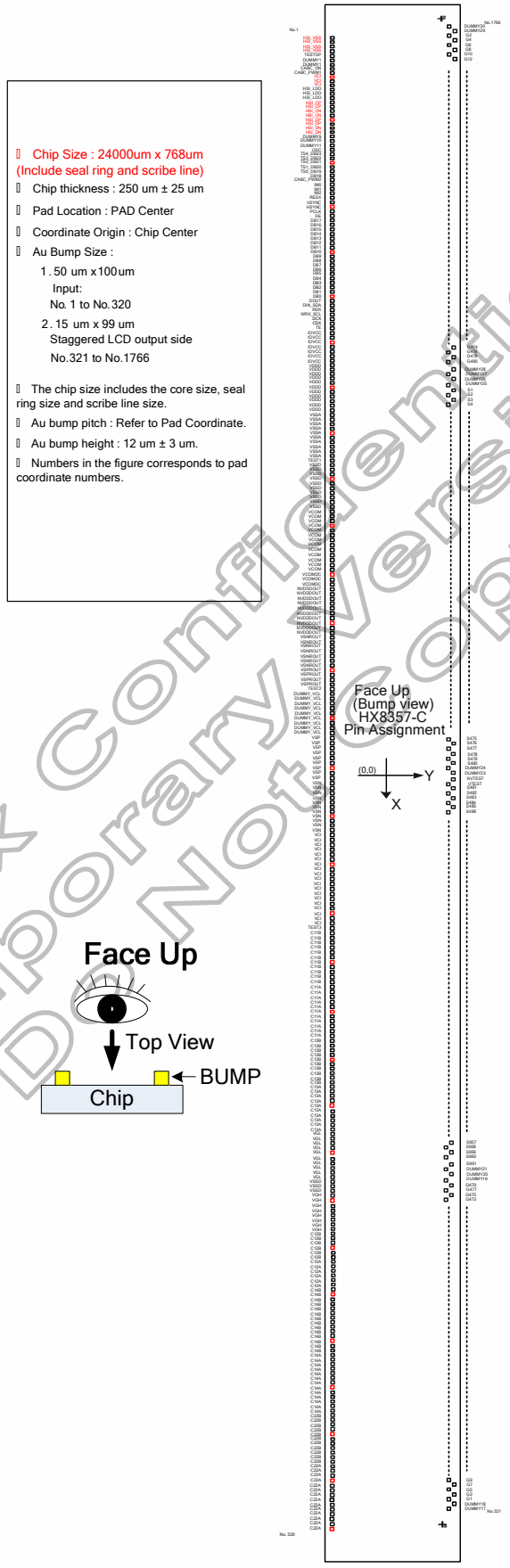
## 3.3 Pin assignment

- Chip Size : 24000um x 768um (Include seal ring and scribe line)
- Chip thickness : 250 um ± 25 um
- Pad Location : PAD Center
- Coordinate Origin : Chip Center
- Au Bump Size :
  1. 50 um x 100 um
     Input:
     No. 1 to No. 320
  2. 15 um x 99 um
     Staggered LCD output side
     No.321 to No.1766
- The chip size includes the core size, seal ring size and scribe line size.
- Au bump pitch : Refer to Pad Coordinate.
- Au bump height : 12 um ± 3 um.
- Numbers in the figure corresponds to pad coordinate numbers.







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## 3.4 PAD coordinates

| No. | Name | X | Y | Bump size |
|---|---|---|---|---|
| 1 | HSI_VSS | -11165 | -286 | 50*100 |
| 2 | HSI_VSS | -11095 | -286 | 50*100 |
| 3 | HSI_VSS | -11025 | -286 | 50*100 |
| 4 | HSI_VSS | -10955 | -286 | 50*100 |
| 5 | TESTDP | -10885 | -286 | 50*100 |
| 6 | DUMMY1 | -10815 | -286 | 50*100 |
| 7 | DUMMY1 | -10745 | -286 | 50*100 |
| 8 | CABC_ON | -10675 | -286 | 50*100 |
| 9 | CABC_PWM1 | -10605 | -286 | 50*100 |
| 10 | VCI | -10535 | -286 | 50*100 |
| 11 | VCI | -10465 | -286 | 50*100 |
| 12 | VCI | -10395 | -286 | 50*100 |
| 13 | HSI_LDO | -10325 | -286 | 50*100 |
| 14 | HSI_LDO | -10255 | -286 | 50*100 |
| 15 | HSI_LDO | -10185 | -286 | 50*100 |
| 16 | HSI_CP | -10115 | -286 | 50*100 |
| 17 | HSI_CP | -10045 | -286 | 50*100 |
| 18 | HSI_CN | -9975 | -286 | 50*100 |
| 19 | HSI_CN | -9905 | -286 | 50*100 |
| 20 | HSI_DP | -9835 | -286 | 50*100 |
| 21 | HSI_DP | -9765 | -286 | 50*100 |
| 22 | HSI_DN | -9695 | -286 | 50*100 |
| 23 | HSI_DN | -9625 | -286 | 50*100 |
| 24 | DUMMY9 | -9555 | -286 | 50*100 |
| 25 | DUMMY10 | -9485 | -286 | 50*100 |
| 26 | DUMMY11 | -9415 | -286 | 50*100 |
| 27 | OSC | -9345 | -286 | 50*100 |
| 28 | TS4_DB23 | -9275 | -286 | 50*100 |
| 29 | TS3_DB22 | -9205 | -286 | 50*100 |
| 30 | TS2_DB21 | -9135 | -286 | 50*100 |
| 31 | TS1_DB20 | -9065 | -286 | 50*100 |
| 32 | TS0_DB19 | -8995 | -286 | 50*100 |
| 33 | DB18 | -8925 | -286 | 50*100 |
| 34 | CABC_PWM2 | -8855 | -286 | 50*100 |
| 35 | IM0 | -8785 | -286 | 50*100 |
| 36 | IM1 | -8715 | -286 | 50*100 |
| 37 | IM2 | -8645 | -286 | 50*100 |
| 38 | RESX | -8575 | -286 | 50*100 |
| 39 | VSYNC | -8505 | -286 | 50*100 |
| 40 | HSYNC | -8435 | -286 | 50*100 |
| 41 | PCLK | -8365 | -286 | 50*100 |
| 42 | DE | -8295 | -286 | 50*100 |
| 43 | DB17 | -8225 | -286 | 50*100 |
| 44 | DB16 | -8155 | -286 | 50*100 |
| 45 | DB15 | -8085 | -286 | 50*100 |
| 46 | DB14 | -8015 | -286 | 50*100 |
| 47 | DB13 | -7945 | -286 | 50*100 |
| 48 | DB12 | -7875 | -286 | 50*100 |
| 49 | DB11 | -7805 | -286 | 50*100 |
| 50 | DB10 | -7735 | -286 | 50*100 |
| 51 | DB9 | -7665 | -286 | 50*100 |
| 52 | DB8 | -7595 | -286 | 50*100 |
| 53 | DB7 | -7525 | -286 | 50*100 |
| 54 | DB6 | -7455 | -286 | 50*100 |
| 55 | DB5 | -7385 | -286 | 50*100 |
| 56 | DB4 | -7315 | -286 | 50*100 |
| 57 | DB3 | -7245 | -286 | 50*100 |
| 58 | DB2 | -7175 | -286 | 50*100 |
| 59 | DB1 | -7105 | -286 | 50*100 |
| 60 | DB0 | -7035 | -286 | 50*100 |

| No. | Name | X | Y | Bump size |
|---|---|---|---|---|
| 61 | DOUT | -6965 | -286 | 50*100 |
| 62 | DIN_SDA | -6895 | -286 | 50*100 |
| 63 | RDX | -6825 | -286 | 50*100 |
| 64 | WRX_SCL | -6755 | -286 | 50*100 |
| 65 | DCX | -6685 | -286 | 50*100 |
| 66 | CSX | -6615 | -286 | 50*100 |
| 67 | TE | -6545 | -286 | 50*100 |
| 68 | IOVCC | -6475 | -286 | 50*100 |
| 69 | IOVCC | -6405 | -286 | 50*100 |
| 70 | IOVCC | -6335 | -286 | 50*100 |
| 71 | IOVCC | -6265 | -286 | 50*100 |
| 72 | IOVCC | -6195 | -286 | 50*100 |
| 73 | IOVCC | -6125 | -286 | 50*100 |
| 74 | IOVCC | -6055 | -286 | 50*100 |
| 75 | VDDD | -5985 | -286 | 50*100 |
| 76 | VDDD | -5915 | -286 | 50*100 |
| 77 | VDDD | -5845 | -286 | 50*100 |
| 78 | VDDD | -5775 | -286 | 50*100 |
| 79 | VDDD | -5705 | -286 | 50*100 |
| 80 | VDDD | -5635 | -286 | 50*100 |
| 81 | VDDD | -5565 | -286 | 50*100 |
| 82 | VDDD | -5495 | -286 | 50*100 |
| 83 | VDDD | -5425 | -286 | 50*100 |
| 84 | VDDD | -5355 | -286 | 50*100 |
| 85 | VDDD | -5285 | -286 | 50*100 |
| 86 | VSSA | -5215 | -286 | 50*100 |
| 87 | VSSA | -5145 | -286 | 50*100 |
| 88 | VSSA | -5075 | -286 | 50*100 |
| 89 | VSSA | -5005 | -286 | 50*100 |
| 90 | VSSA | -4935 | -286 | 50*100 |
| 91 | VSSA | -4865 | -286 | 50*100 |
| 92 | VSSA | -4795 | -286 | 50*100 |
| 93 | VSSA | -4725 | -286 | 50*100 |
| 94 | VSSA | -4655 | -286 | 50*100 |
| 95 | VSSA | -4585 | -286 | 50*100 |
| 96 | TEST1 | -4515 | -286 | 50*100 |
| 97 | VSSD | -4445 | -286 | 50*100 |
| 98 | VSSD | -4375 | -286 | 50*100 |
| 99 | VSSD | -4305 | -286 | 50*100 |
| 100 | VSSD | -4235 | -286 | 50*100 |
| 101 | VSSD | -4165 | -286 | 50*100 |
| 102 | VSSD | -4095 | -286 | 50*100 |
| 103 | VSSD | -4025 | -286 | 50*100 |
| 104 | VSSD | -3955 | -286 | 50*100 |
| 105 | VSSD | -3885 | -286 | 50*100 |
| 106 | VSSD | -3815 | -286 | 50*100 |
| 107 | VCOM | -3745 | -286 | 50*100 |
| 108 | VCOM | -3675 | -286 | 50*100 |
| 109 | VCOM | -3605 | -286 | 50*100 |
| 110 | VCOM | -3535 | -286 | 50*100 |
| 111 | VCOM | -3465 | -286 | 50*100 |
| 112 | VCOM | -3395 | -286 | 50*100 |
| 113 | VCOM | -3325 | -286 | 50*100 |
| 114 | VCOM | -3255 | -286 | 50*100 |
| 115 | VCOM | -3185 | -286 | 50*100 |
| 116 | VCOM | -3115 | -286 | 50*100 |
| 117 | VCOM | -3045 | -286 | 50*100 |
| 118 | VCOM | -2975 | -286 | 50*100 |
| 119 | VCOM | -2905 | -286 | 50*100 |
| 120 | VCOMDC | -2835 | -286 | 50*100 |

| No. | Name | X | Y | Bump size |
|---|---|---|---|---|
| 121 | VCOMDC | -2765 | -286 | 50*100 |
| 122 | VCOMDC | -2695 | -286 | 50*100 |
| 123 | NVDDDOUT | -2625 | -286 | 50*100 |
| 124 | NVDDDOUT | -2555 | -286 | 50*100 |
| 125 | NVDDDOUT | -2485 | -286 | 50*100 |
| 126 | NVDDDOUT | -2415 | -286 | 50*100 |
| 127 | NVDDDOUT | -2345 | -286 | 50*100 |
| 128 | NVDDDOUT | -2275 | -286 | 50*100 |
| 129 | NVDDDOUT | -2205 | -286 | 50*100 |
| 130 | NVDDDOUT | -2135 | -286 | 50*100 |
| 131 | NVDDDOUT | -2065 | -286 | 50*100 |
| 132 | NVDDDOUT | -1995 | -286 | 50*100 |
| 133 | VSNROUT | -1925 | -286 | 50*100 |
| 134 | VSNROUT | -1855 | -286 | 50*100 |
| 135 | VSNROUT | -1785 | -286 | 50*100 |
| 136 | VSNROUT | -1715 | -286 | 50*100 |
| 137 | VSNROUT | -1645 | -286 | 50*100 |
| 138 | VSNROUT | -1575 | -286 | 50*100 |
| 139 | VSNROUT | -1505 | -286 | 50*100 |
| 140 | VSPROUT | -1435 | -286 | 50*100 |
| 141 | VSPROUT | -1365 | -286 | 50*100 |
| 142 | VSPROUT | -1295 | -286 | 50*100 |
| 143 | VSPROUT | -1225 | -286 | 50*100 |
| 144 | TEST2 | -1155 | -286 | 50*100 |
| 145 | DUMMY_VCL | -1085 | -286 | 50*100 |
| 146 | DUMMY_VCL | -1015 | -286 | 50*100 |
| 147 | DUMMY_VCL | -945 | -286 | 50*100 |
| 148 | DUMMY_VCL | -875 | -286 | 50*100 |
| 149 | DUMMY_VCL | -805 | -286 | 50*100 |
| 150 | DUMMY_VCL | -735 | -286 | 50*100 |
| 151 | DUMMY_VCL | -665 | -286 | 50*100 |
| 152 | DUMMY_VCL | -595 | -286 | 50*100 |
| 153 | DUMMY_VCL | -525 | -286 | 50*100 |
| 154 | VSP | -455 | -286 | 50*100 |
| 155 | VSP | -385 | -286 | 50*100 |
| 156 | VSP | -315 | -286 | 50*100 |
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| 334 | G23 | 11010 | 278.5 | 15*99 |
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| 573 | S954 | 7275 | 154.5 | 15*99 |
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| 575 | S952 | 7245 | 154.5 | 15*99 |
| 576 | S951 | 7230 | 278.5 | 15*99 |
| 577 | S950 | 7215 | 154.5 | 15*99 |
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| 586 | S941 | 7080 | 278.5 | 15*99 |
| 587 | S940 | 7065 | 154.5 | 15*99 |
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| 591 | S936 | 7005 | 154.5 | 15*99 |
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| 594 | S933 | 6960 | 278.5 | 15*99 |
| 595 | S932 | 6945 | 154.5 | 15*99 |
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| 604 | S923 | 6810 | 278.5 | 15*99 |
| 605 | S922 | 6795 | 154.5 | 15*99 |
| 606 | S921 | 6780 | 278.5 | 15*99 |
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| 608 | S919 | 6750 | 278.5 | 15*99 |
| 609 | S918 | 6735 | 154.5 | 15*99 |
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| 647 | S880 | 6165 | 154.5 | 15*99 |
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| 719 | S808 | 5085 | 154.5 | 15*99 |
| 720 | S807 | 5070 | 278.5 | 15*99 |

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| 727 | S800 | 4965 | 154.5 | 15*99 |
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| 730 | S797 | 4920 | 278.5 | 15*99 |
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| 736 | S791 | 4830 | 278.5 | 15*99 |
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| 790 | S737 | 4020 | 278.5 | 15*99 |
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| 792 | S735 | 3990 | 278.5 | 15*99 |
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| 796 | S731 | 3930 | 278.5 | 15*99 |
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| 836 | S691 | 3330 | 278.5 | 15*99 |
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| No. | Name | X | Y | Bump size |
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| 845 | S682 | 3195 | 154.5 | 15*99 |
| 846 | S681 | 3180 | 278.5 | 15*99 |
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| 849 | S678 | 3135 | 154.5 | 15*99 |
| 850 | S677 | 3120 | 278.5 | 15*99 |
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| 857 | S670 | 3015 | 154.5 | 15*99 |
| 858 | S669 | 3000 | 278.5 | 15*99 |
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| 884 | S643 | 2610 | 278.5 | 15*99 |
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| 899 | S628 | 2385 | 154.5 | 15*99 |
| 900 | S627 | 2370 | 278.5 | 15*99 |

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| 902 | S625 | 2340 | 278.5 | 15*99 |
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| 926 | S601 | 1980 | 278.5 | 15*99 |
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| 936 | S591 | 1830 | 278.5 | 15*99 |
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| 951 | S576 | 1605 | 154.5 | 15*99 |
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| No. | Name | X | Y | Bump size |
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| 969 | S558 | 1335 | 154.5 | 15*99 |
| 970 | S557 | 1320 | 278.5 | 15*99 |
| 971 | S556 | 1305 | 154.5 | 15*99 |
| 972 | S555 | 1290 | 278.5 | 15*99 |
| 973 | S554 | 1275 | 154.5 | 15*99 |
| 974 | S553 | 1260 | 278.5 | 15*99 |
| 975 | S552 | 1245 | 154.5 | 15*99 |
| 976 | S551 | 1230 | 278.5 | 15*99 |
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| 979 | S548 | 1185 | 154.5 | 15*99 |
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| 1079 | S452 | -600 | 278.5 | 15*99 |
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| No. | Name | X | Y | Bump size |
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| 1145 | S386 | -1590 | 278.5 | 15*99 |
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| 1167 | S364 | -1920 | 278.5 | 15*99 |
| 1168 | S363 | -1935 | 154.5 | 15*99 |
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| 1179 | S352 | -2100 | 278.5 | 15*99 |
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| 1192 | S339 | -2295 | 154.5 | 15*99 |
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| 1196 | S335 | -2355 | 154.5 | 15*99 |
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| 1203 | S328 | -2460 | 278.5 | 15*99 |
| 1204 | S327 | -2475 | 154.5 | 15*99 |
| 1205 | S326 | -2490 | 278.5 | 15*99 |
| 1206 | S325 | -2505 | 154.5 | 15*99 |
| 1207 | S324 | -2520 | 278.5 | 15*99 |
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| 1209 | S322 | -2550 | 278.5 | 15*99 |
| 1210 | S321 | -2565 | 154.5 | 15*99 |
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| 1215 | S316 | -2640 | 278.5 | 15*99 |
| 1216 | S315 | -2655 | 154.5 | 15*99 |
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| 1260 | S271 | -3315 | 154.5 | 15*99 |

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| 1266 | S265 | -3405 | 154.5 | 15*99 |
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| 1314 | S217 | -4125 | 154.5 | 15*99 |
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| 1353 | S178 | -4710 | 278.5 | 15*99 |
| 1354 | S177 | -4725 | 154.5 | 15*99 |
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| 1367 | S164 | -4920 | 278.5 | 15*99 |
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| 1370 | S161 | -4965 | 154.5 | 15*99 |
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| 1439 | S92 | -6000 | 278.5 | 15*99 |
| 1440 | S91 | -6015 | 154.5 | 15*99 |

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| 1442 | S89 | -6045 | 154.5 | 15*99 |
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| 1450 | S81 | -6165 | 154.5 | 15*99 |
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| No. | Name | X | Y | Bump size |
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| 1509 | S22 | -7050 | 278.5 | 15*99 |
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| 1511 | S20 | -7080 | 278.5 | 15*99 |
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| 1514 | S17 | -7125 | 154.5 | 15*99 |
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| 1552 | G446 | -7845 | 154.5 | 15*99 |
| 1553 | G444 | -7860 | 278.5 | 15*99 |
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| 1558 | G434 | -7935 | 154.5 | 15*99 |
| 1559 | G432 | -7950 | 278.5 | 15*99 |
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| No. | Name | X | Y | Bump size |
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| 1563 | G424 | -8010 | 278.5 | 15*99 |
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| 1565 | G420 | -8040 | 278.5 | 15*99 |
| 1566 | G418 | -8055 | 154.5 | 15*99 |
| 1567 | G416 | -8070 | 278.5 | 15*99 |
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| 1569 | G412 | -8100 | 278.5 | 15*99 |
| 1570 | G410 | -8115 | 154.5 | 15*99 |
| 1571 | G408 | -8130 | 278.5 | 15*99 |
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| 1574 | G402 | -8175 | 154.5 | 15*99 |
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| 1585 | G380 | -8340 | 278.5 | 15*99 |
| 1586 | G378 | -8355 | 154.5 | 15*99 |
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| 1588 | G374 | -8385 | 154.5 | 15*99 |
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| 1620 | G310 | -8865 | 154.5 | 15*99 |

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| No. | Name | X | Y | Bump size |
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| 1728 | G94 | -10485 | 154.5 | 15*99 |
| 1729 | G92 | -10500 | 278.5 | 15*99 |
| 1730 | G90 | -10515 | 154.5 | 15*99 |
| 1731 | G88 | -10530 | 278.5 | 15*99 |
| 1732 | G86 | -10545 | 154.5 | 15*99 |
| 1733 | G84 | -10560 | 278.5 | 15*99 |
| 1734 | G82 | -10575 | 154.5 | 15*99 |
| 1735 | G80 | -10590 | 278.5 | 15*99 |
| 1736 | G78 | -10605 | 154.5 | 15*99 |
| 1737 | G76 | -10620 | 278.5 | 15*99 |
| 1738 | G74 | -10635 | 154.5 | 15*99 |
| 1739 | G72 | -10650 | 278.5 | 15*99 |
| 1740 | G70 | -10665 | 154.5 | 15*99 |
| 1741 | G68 | -10680 | 278.5 | 15*99 |
| 1742 | G66 | -10695 | 154.5 | 15*99 |
| 1743 | G64 | -10710 | 278.5 | 15*99 |
| 1744 | G62 | -10725 | 154.5 | 15*99 |
| 1745 | G60 | -10740 | 278.5 | 15*99 |
| 1746 | G58 | -10755 | 154.5 | 15*99 |
| 1747 | G56 | -10770 | 278.5 | 15*99 |
| 1748 | G54 | -10785 | 154.5 | 15*99 |
| 1749 | G52 | -10800 | 278.5 | 15*99 |
| 1750 | G50 | -10815 | 154.5 | 15*99 |
| 1751 | G48 | -10830 | 278.5 | 15*99 |
| 1752 | G46 | -10845 | 154.5 | 15*99 |
| 1753 | G44 | -10860 | 278.5 | 15*99 |
| 1754 | G42 | -10875 | 154.5 | 15*99 |
| 1755 | G40 | -10890 | 278.5 | 15*99 |
| 1756 | G38 | -10905 | 154.5 | 15*99 |
| 1757 | G36 | -10920 | 278.5 | 15*99 |
| 1758 | G34 | -10935 | 154.5 | 15*99 |
| 1759 | G32 | -10950 | 278.5 | 15*99 |
| 1760 | G30 | -10965 | 154.5 | 15*99 |
| 1761 | G28 | -10980 | 278.5 | 15*99 |
| 1762 | G26 | -10995 | 154.5 | 15*99 |
| 1763 | G24 | -11010 | 278.5 | 15*99 |
| 1764 | G22 | -11025 | 154.5 | 15*99 |
| 1765 | G20 | -11040 | 278.5 | 15*99 |
| 1766 | G18 | -11055 | 154.5 | 15*99 |
| 1767 | G16 | -11070 | 278.5 | 15*99 |
| 1768 | G14 | -11085 | 154.5 | 15*99 |
| 1769 | G12 | -11100 | 278.5 | 15*99 |
| 1770 | G10 | -11115 | 154.5 | 15*99 |
| 1771 | G8 | -11130 | 278.5 | 15*99 |
| 1772 | G6 | -11145 | 154.5 | 15*99 |
| 1773 | G4 | -11160 | 278.5 | 15*99 |
| 1774 | G2 | -11175 | 154.5 | 15*99 |
| 1775 | DUMMY29 | -11190 | 278.5 | 15*99 |
| 1776 | DUMMY30 | -11205 | 154.5 | 15*99 |

| Alignment Mark | X | Y | |
|---|---|---|---|
| A1 | -11300 | -280 | |
| A2 | 11300 | -280 | |

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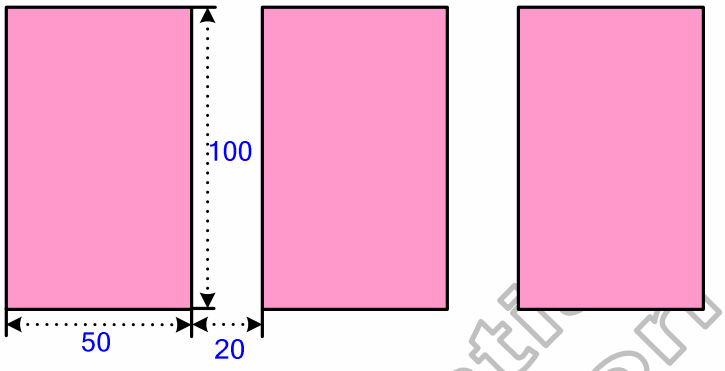
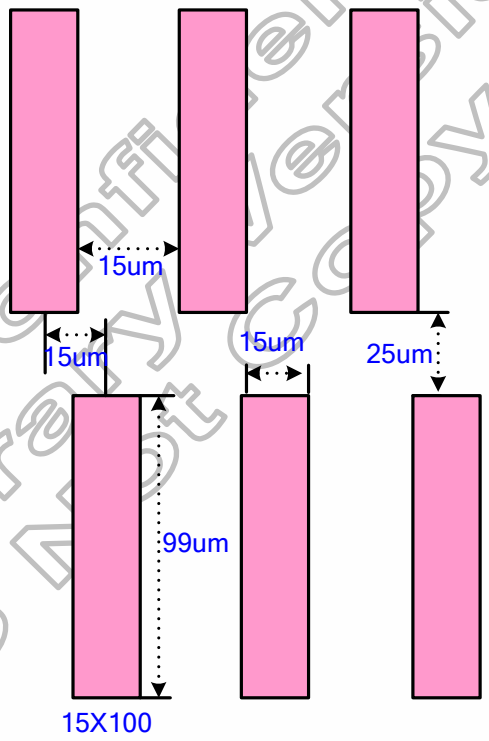
### 3.5 Bump arrangement

| | |
|---|---|
| Input Pad (No.1~320) |  |
| Output Pad (No.321~1776) |  |

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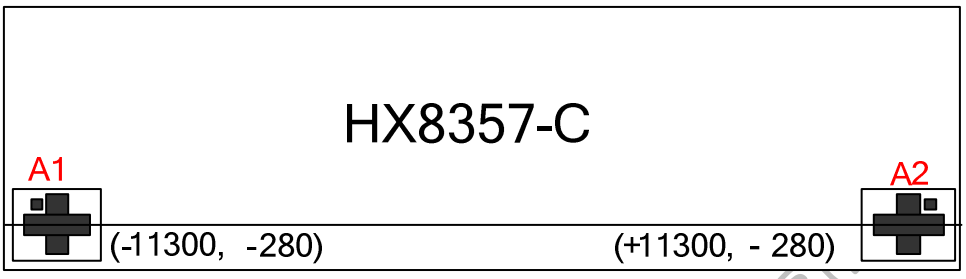
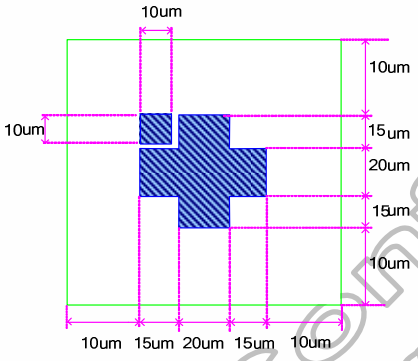
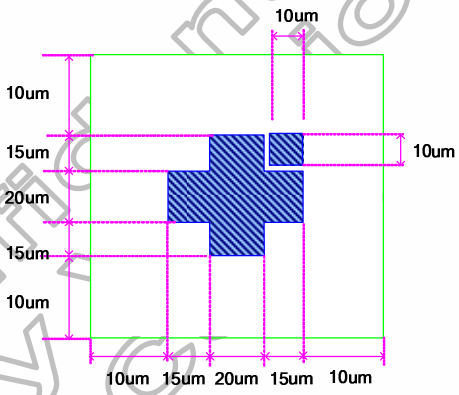
## 3.6 Alignment mark




A_MARK (A1)




A_MARK (A2)

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# 4. Interface

The HX8357-C supports MIPI interfaces: DBI (Display Bus Interface), DPI (Display Pixel Interface), DSI (Display Serial Interface) and MDDI (Mobile Display Digital Interface). Where DBI supports (18-/16-/9-/8-bit interface) Parallel Interface (Type B) and Serial interface (Type C Option 1/ Option 3). The interface mode can be selected by IM2-0 pins setting as show in Table 4.1.

| IM2 | IM1 | IM0 | Interface | WRX_SCL | Data Bus use | |
|---|---|---|---|---|---|---|
| | | | | | Command/Parament | GRAM |
| 0 | 0 | 0 | DBI TYPE-B 18-bit | WRX | DB7-DB0 | DB17-DB0: 18-bits Data |
| 0 | 0 | 1 | DBI TYPE-B 9-bit | WRX | DB7-DB0 | DB8-DB0: 9-bits Data |
| 0 | 1 | 0 | DBI TYPE-B 16-bit | WRX | DB7-DB0 | DB15-DB0: 16-bits Data |
| 0 | 1 | 1 | DBI TYPE-B 8-bit | WRX | DB7-DB0 | DB8-DB0: 8-bit Data |
| 1 | 0 | 0 | MDDI + DBI TYPE-C Option 1 | SCL | HSI_CP/N , HSI_D0P/N | |
| 1 | 0 | 1 | DBI TYPE-C Option 1 | SCL | SDA | |
| 1 | 1 | 0 | MIPI DSI | - | HSI_CP/N , HSI_D0P/N | |
| 1 | 1 | 1 | DBI TYPE-C Option 3 | SCL | SDA | |

**Table 4.1: Interface selection**

The HX8357-C includes an index register (IR), which is stored the index data of internal control register and GRAM. When DCX="L", the command via DBI interface write into register. When DCX="H", GRAM data via R2Ch register can be written through data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the read data in data bus in first read operation is invalid, and the read data is valid from second read in data bus.

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## 4.1 MIPI DBI-B Interface

The selection of DBI interface IM2~IM0 pin to select DBI interface mode. The parallel interface timing diagram is described in Figure 4.1 and Figure 4.2.

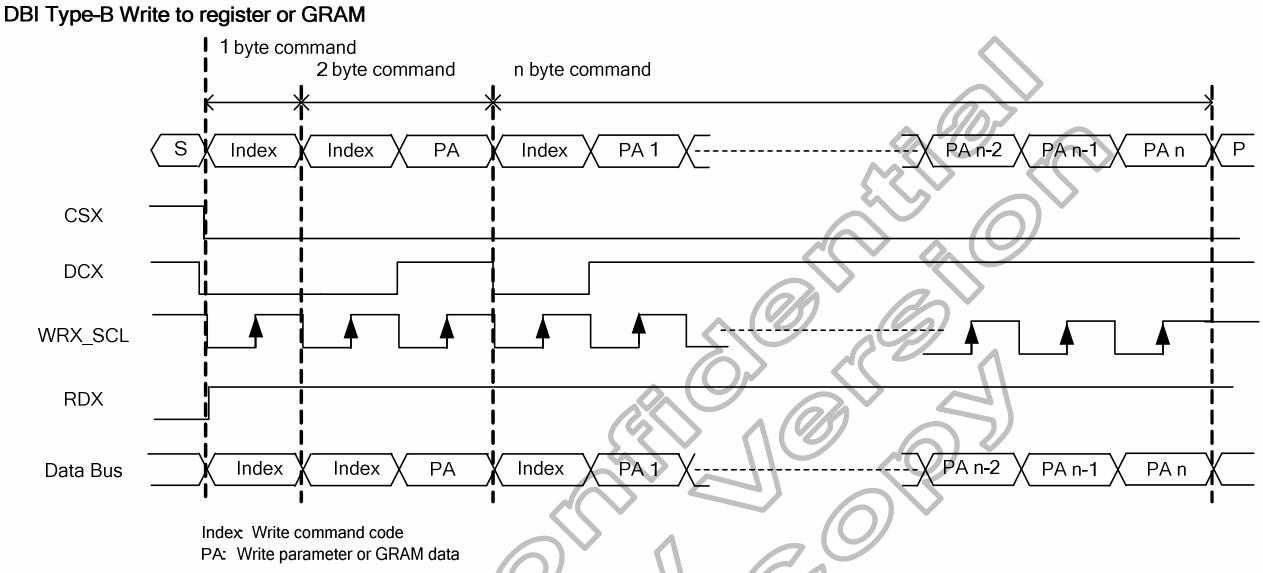


**Figure 4.1: DBI-B System interface protocol, write to register or GRAM**

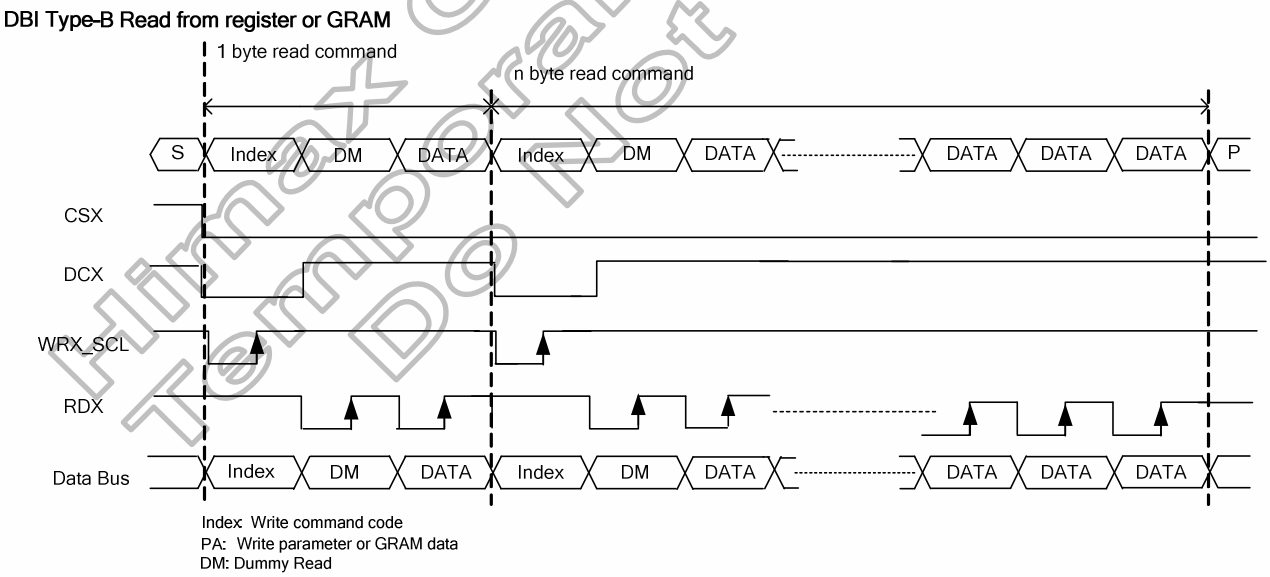


**Figure 4.2: DBI-B System interface protocol, read from register or GRAM**

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## DBI TYPE-B 8-bit Parallel Bus System Interface

The DBI-B system 8-bit bus parallel data transfer can be used by setting “IM2-0” pins to “011”. The Figure4.3 is the example of interface with 8-bit DBI-B microcomputer system interface.

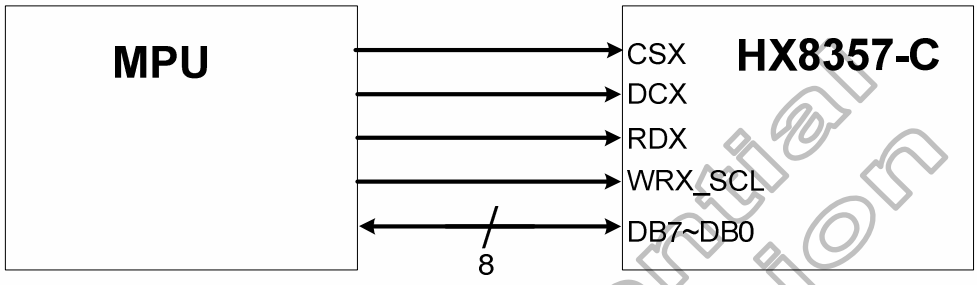


**Figure 4.3: Example of DBI-B System 8-bit bus Interface**

8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH=”05h”
There is 1-pixel (3 sub-pixels) per 2-bytes.

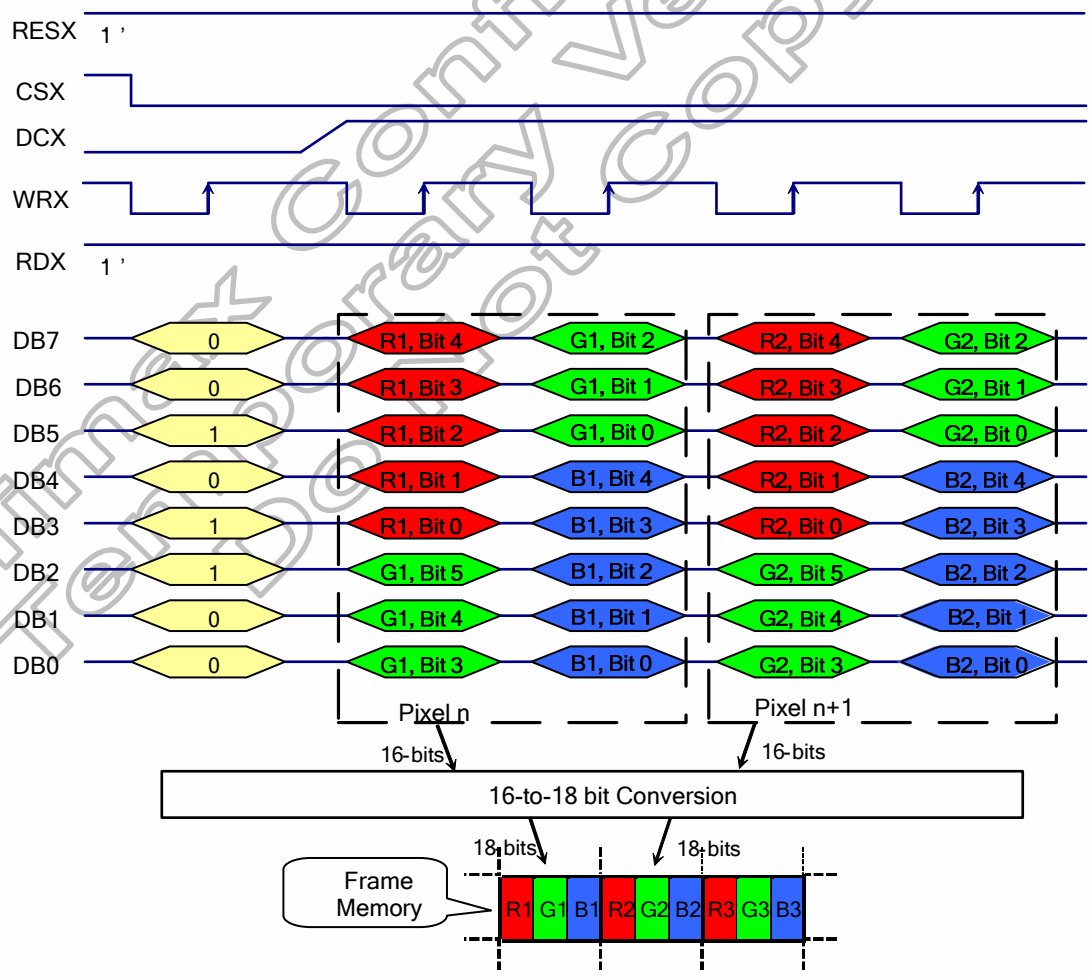


**Figure 4.4: Write data for RGB 5-6-5 (65k colors) bits input in 8-bit parallel Interface**

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8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 3-bytes.

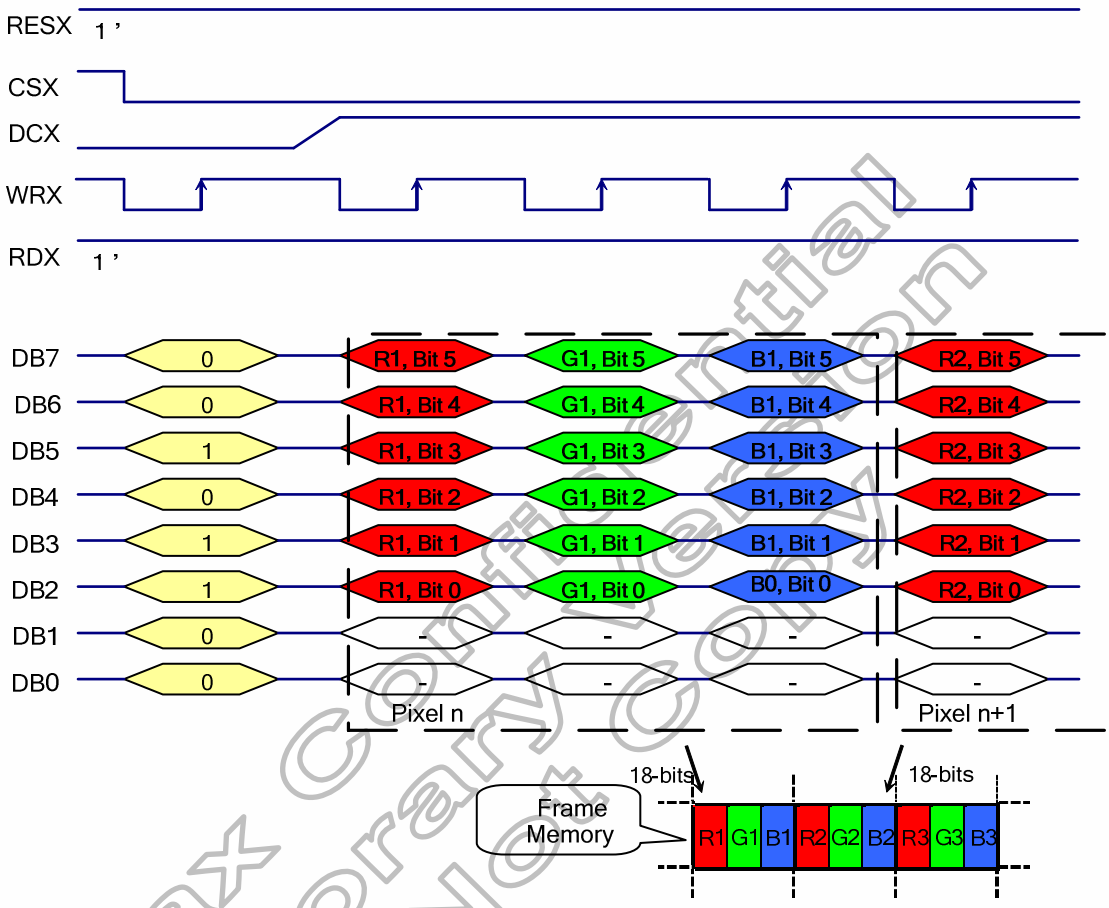


**Figure 4.5: Write data for RGB 6-6-6-bits(262k colors) input in 8-bit parallel Interface**

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## DBI TYPE-B 9-bit Parallel Bus System Interface

The DBI-B system 9-bit bus parallel data transfer can be used by setting “IM2-0” pins to “001”. The Figure4.9 is the example of interface with 9-bit DBI-B microcomputer system interface.

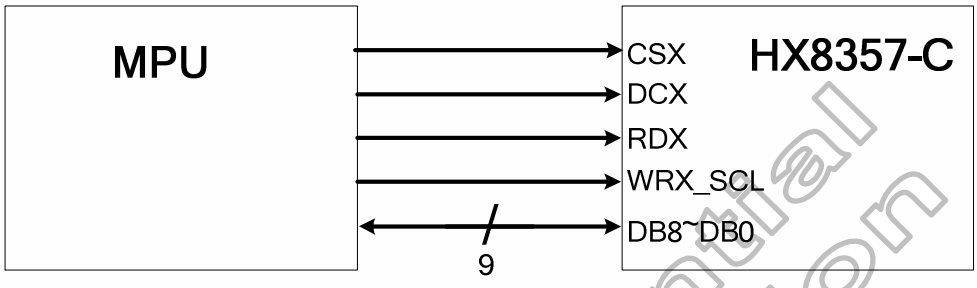


**Figure 4.6: Example of DBI-B System 9-bit bus Interface**

9-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH=”05h”
There is 1-pixel (3 sub-pixels) per 2-bytes.

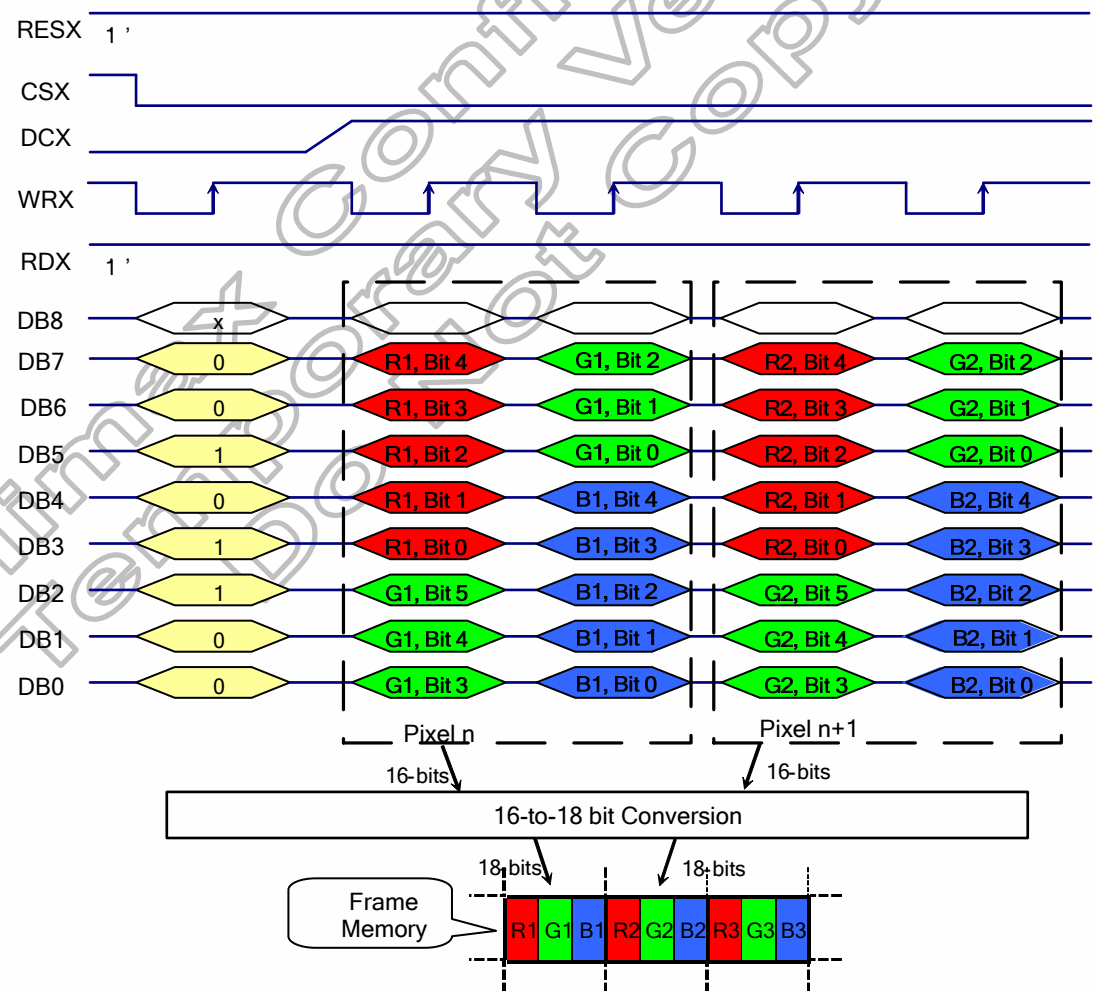


**Figure 4.7: Write data for RGB 5-6-5 (65k colors) bits input in 9-bit parallel Interface**

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9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 2-bytes

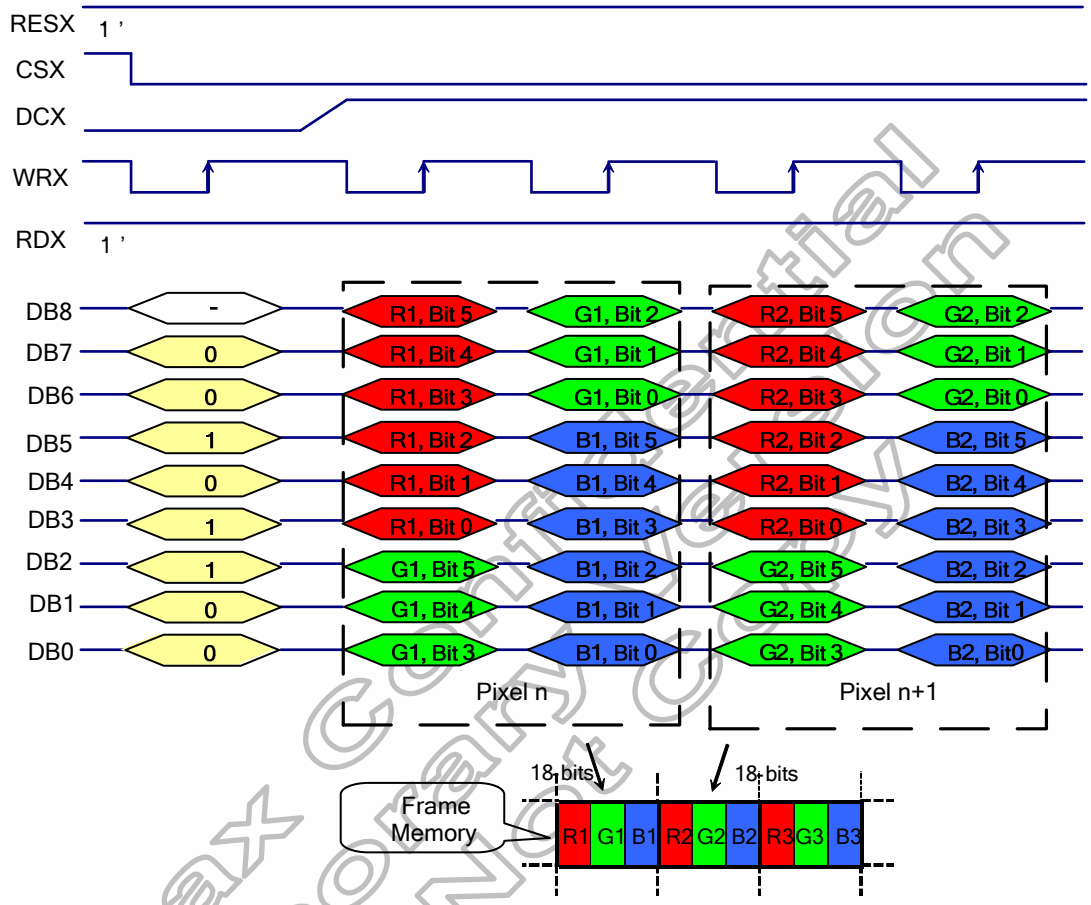


**Figure 4.8: Write data for RGB 6-6-6 (262k colors) bits input in 9-bit parallel Interface**

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## DBI TYPE-B 16-bit Parallel Bus System Interface

the DBI-B system 16-bit bus parallel data transfer can be used by setting “IM2-0”pins to “010”. The Figure4.11 is the example of interface with 16-bit DBI-B microcomputer system interface.

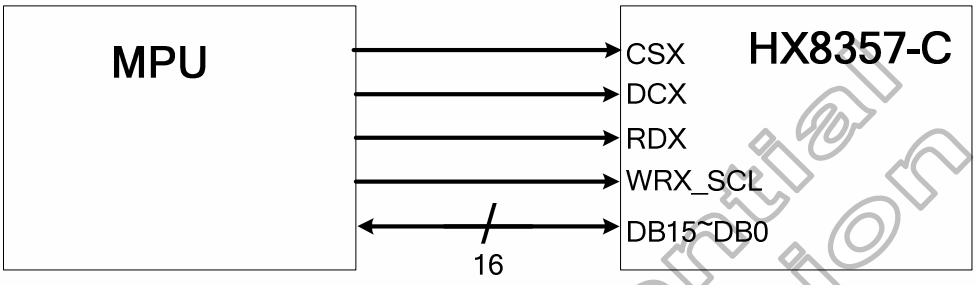


**Figure 4.9: Example of DBI-B System 16-bit bus Interface**

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16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH="05h"
There is 1-pixel (3 sub-pixels) per 1-byte

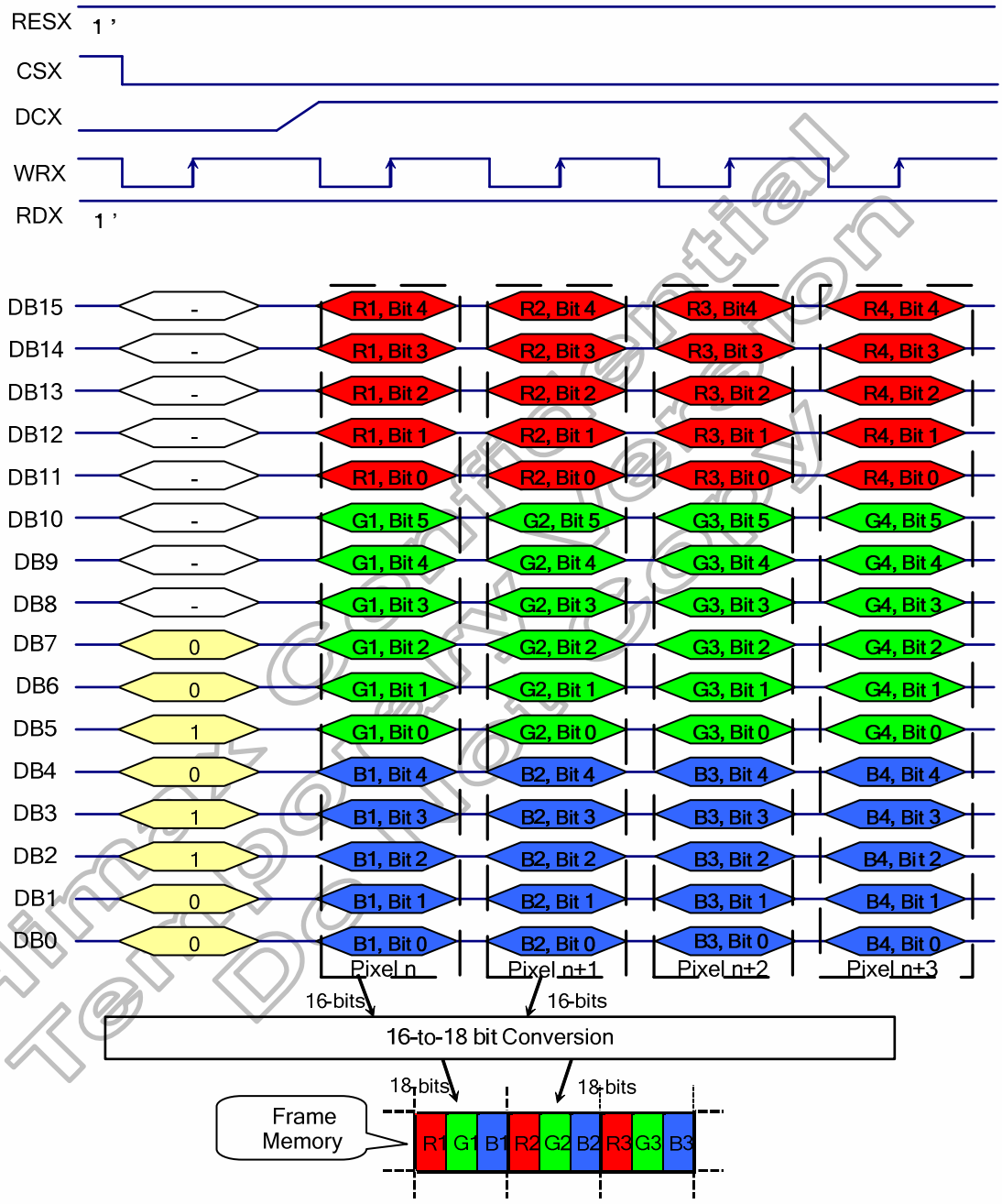


**Figure 4.10: Write data for RGB 5-6-5 (65k colors) bits input in 16-bit parallel Interface**

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16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There are 2-pixels (6 sub-pixels) per 3-bytes

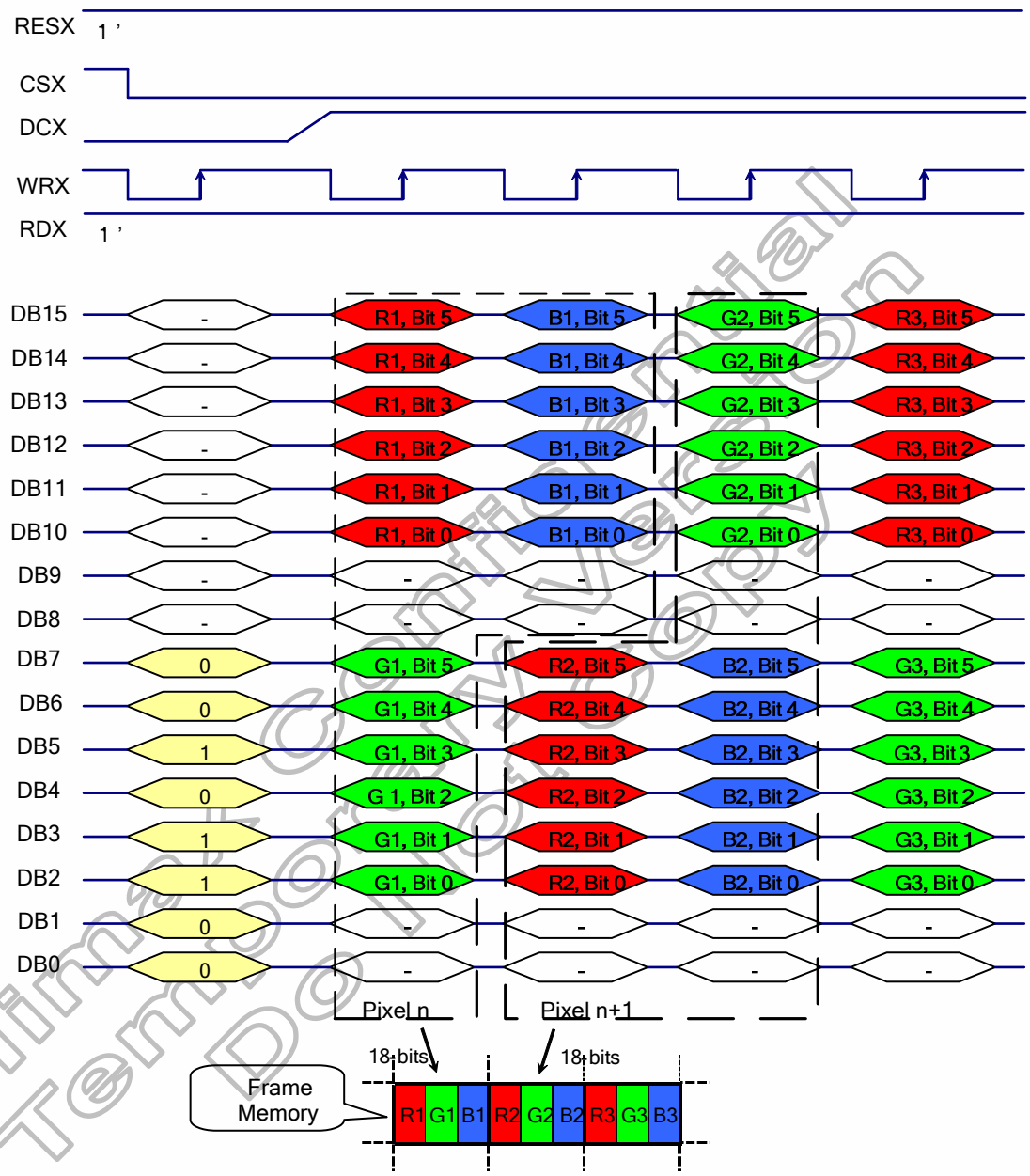


**Figure 4.11: Write data for RGB 6-6-6 (262k colors) bits input in 16-bit parallel Interface**

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## DBI TYPE-B 18-bit Parallel Bus System Interface

The DBI-B system 18-bit bus parallel data transfer can be used by setting “IM2-0”pins to “000”. The Figure 4.15 is the example of interface with 18-bit DBI-B microcomputer system interface.

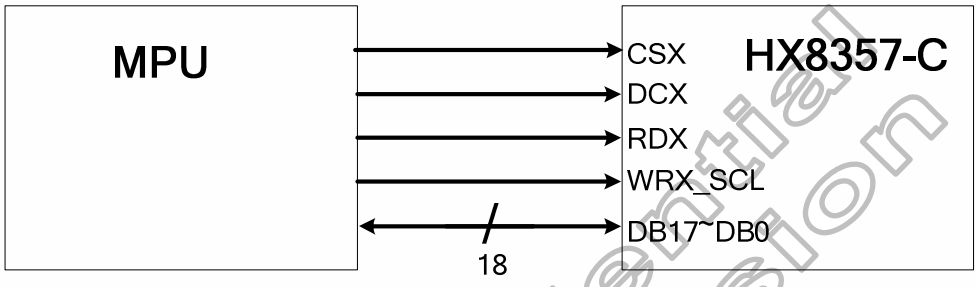


**Figure 4.12: Example of DBI-B System 18-Bit Parallel Bus Interface**

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18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (6 sub-pixels) per 1-byte

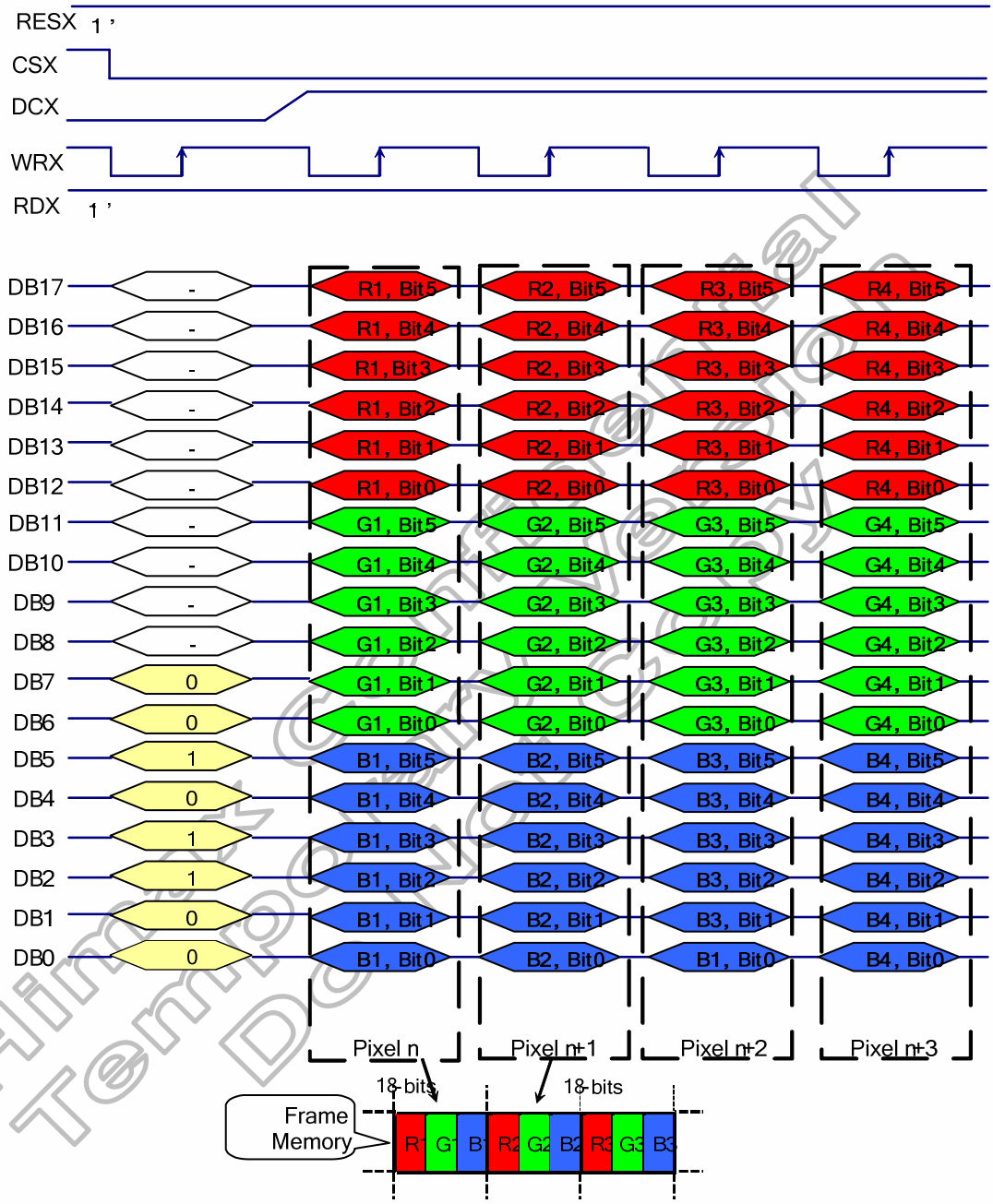


**Figure 4.13 Write data for RGB 6-6-6 (262k colors) bits input in 18-bit parallel Interface**

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## _Paralle Interface Data Color Coding

Data Color Coding for GRAM data ***Write***

- Parallel 8-Bits Bus Interface (IM2,IM1,IM0="011")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| 05h | x | x | x | x | x | x | x | x | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 65K-Color (1-pixel/ 2-bytes) |
| | x | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | |
| 06h | x | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | 262K-Color (1-pixel/ 3bytes) |
| | x | x | x | x | x | x | x | x | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | x | x | x | x | x | x | x | x | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

**Table 4.2: 8-Bits Interface GRAM Write Table**

- Parallel 9-Bits Bus Interface (IM2,IM1,IM0="001")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| 05h | x | x | x | x | x | x | x | x | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 65K-Color (1-pixel/ 2-bytes) |
| | x | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | |
| 06h | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 262K-Color (1-pixel/ 2bytes) |
| | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | |

**Table 4.3: 9-Bits Interface GRAM Write Table**

- Parallel 16-Bits Bus Interface (IM2,IM1,IM0="010")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| 05h | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | 65K-Color |
| 06h | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | 262K-Color (2-pixels/ 3bytes) |
| | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

**Table 4.4: 16-Bits Interface GRAM Write Table**

- Parallel 18-Bits Bus Interface (IM2,IM1,IM0="000")

| **Register Command** | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color |
| 06h | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | **262K-Color** |

**Table 4.5: 18-Bits Interface GRAM Write Table**

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## Data Color Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface (IM2,IM1,IM0="011")

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | Dummy Read |
| | x | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | 262K-Color (1-pixel/ 3bytes) |
| | x | x | x | x | x | x | x | x | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | x | x | x | x | x | x | x | x | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

**Table 4.6: 8-bit parallel interface GRAM read table**

- Parallel 16-Bits Bus Interface (IM2,IM1,IM0="010")

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | Dummy Read |
| | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | 262K-Color (2-pixels/ 3bytes) |
| | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

**Table 4.7: 16-bit parallel interface GRAM read table**

- Parallel 9-Bits Bus Interface (IM2,IM1,IM0="001")

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | Dummy Read |
| | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 262K-Color (1-pixel/ 2bytes) |
| | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | |

**Table 4.8: 9-bit parallel interface GRAM read table**

- Parallel 18-Bits Bus Interface (IM2,IM1,IM0="000")

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register Command** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
| | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | Dummy Read |
| | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 262K-Color |

**Table 4.9: 18-bit parallel interface GRAM read table**

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## 4.2Serial Data Transfer Interface(MIPI DBI TYPE-C)

The HX8357-c supports DBI Type C option 1(3-wire) and option 3(4-wire) serial data transfer interface, the interface selection by setting IM2-0 pins, The IM2-0 set “101” is select option1 3 wire serial bus. The IM2-0 set “110” is select option3 4 wire serial bus.

The 3 wire serial bus is use: chip select line (CSX), serial input/output data (SDA) and the serial transfer clock line (WRX_SCL).

The 4 wire serial bus is use: chip select line (CSX), data/command select (DCX), serial input/output data (SDA/SDO) and the serial transfer clock line (WRX_SCL).

### 4.2.1 Serial data write mode

The 3-Pin serial data packet contains a control bit D/CX and a transmission byte If D/CX is low, the transmission byte is command byte. If D/CX is high, the transmission byte is stored in to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDA/SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

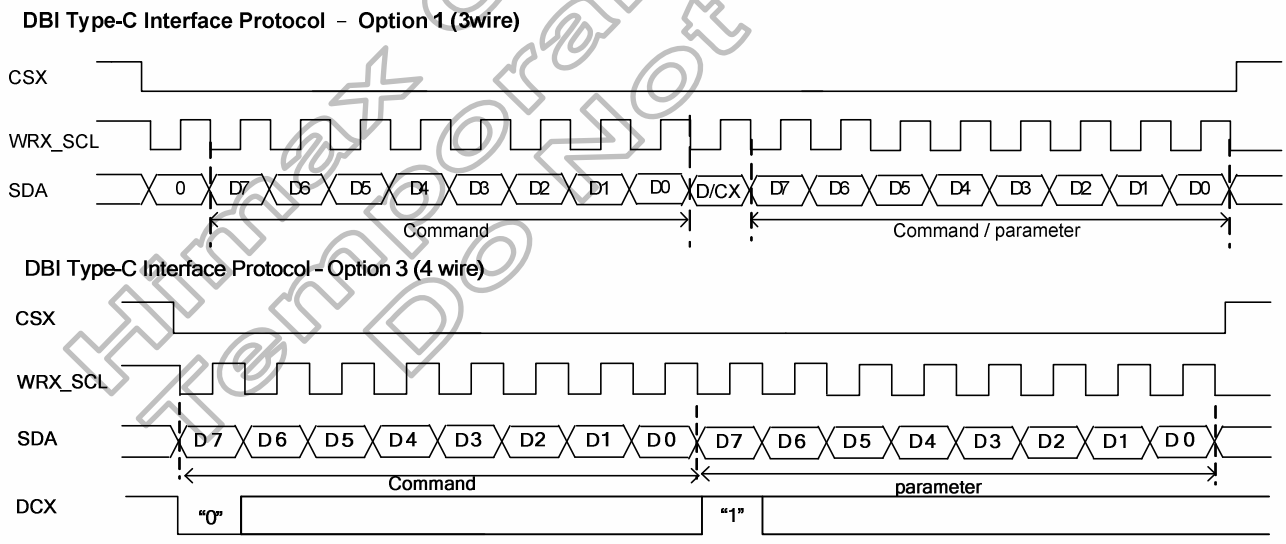


**Figure 4.14: DBI Type C – Serial Interface protocol 3 wire/ 4 wire, write mode**

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### 4.2.2 Read operation in serial peripheral interface

In serial peripheral interface read operation, the host controller first has to send a command and then the following byte is transmitted to host controller in the SDA. The read mode has two type command data read (8-/Over 8-bit) and one type GRAM data read.

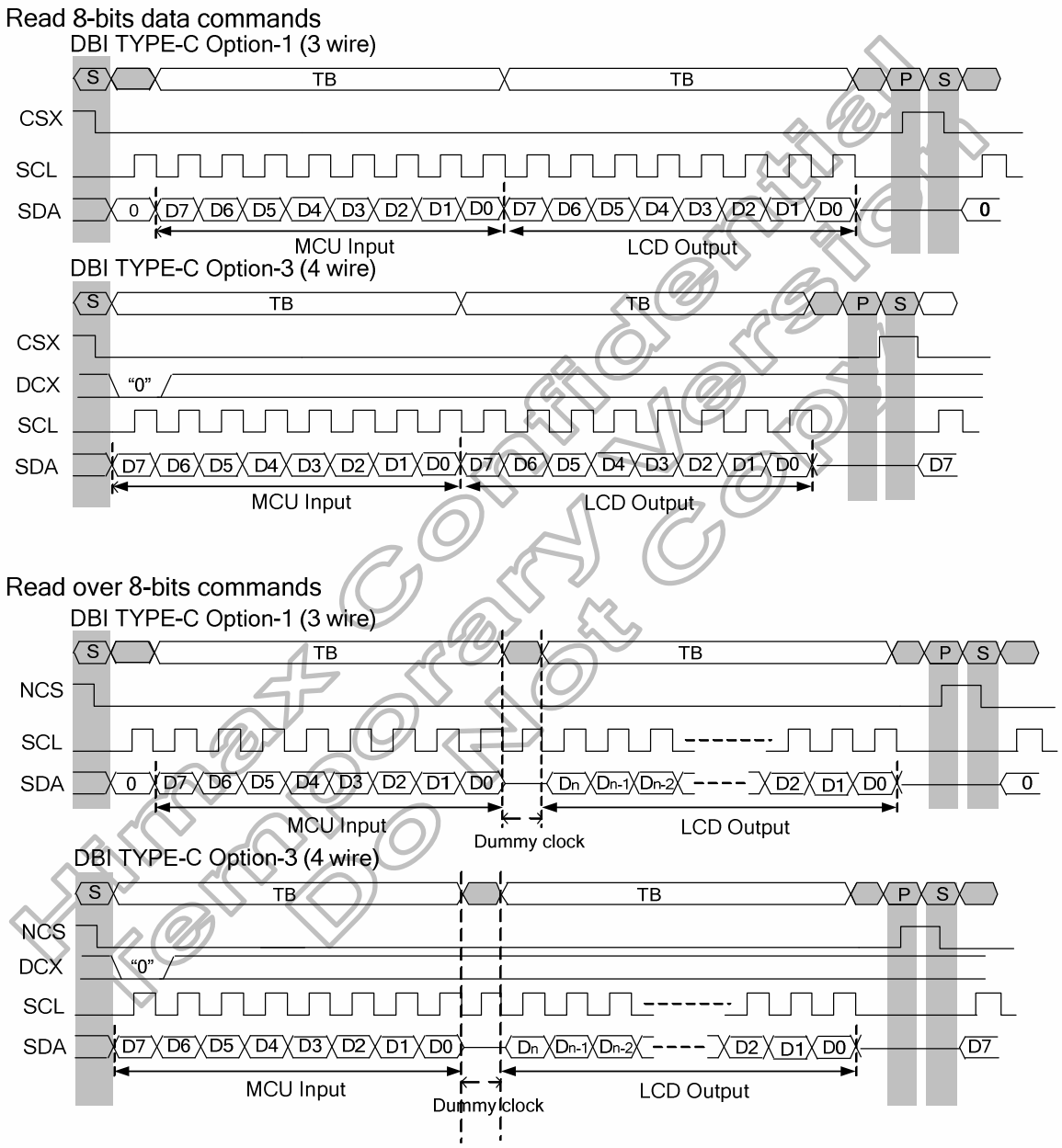


**Figure 4.15: Command Read Operation in Serial Peripheral Interface**

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### 4.2.3 DBI TYPE-C Interface Data Color Coding

There are two types data format to write display data at Serial data bus Interface and it is as same as 8-bit bus Interface.

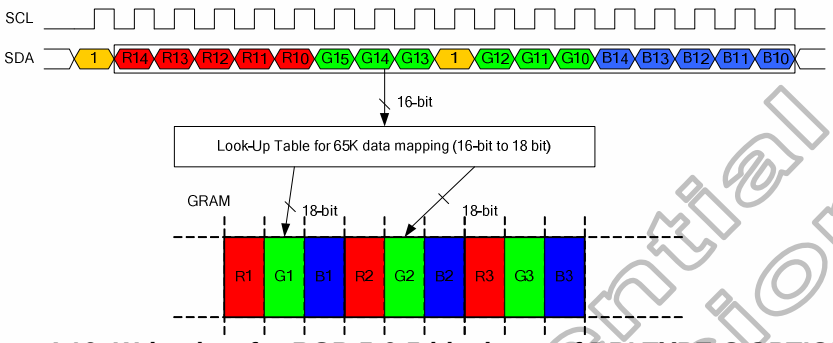


**Figure 4.16: Write data for RGB 5-6-5-bits input of DBI TYPE-C OPTION 1**

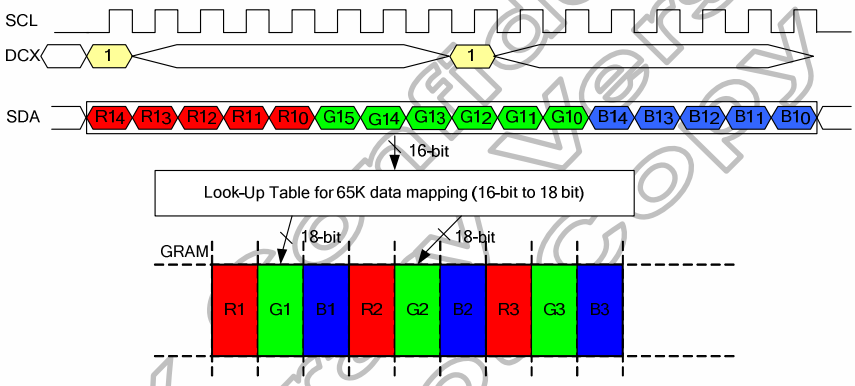


**Figure 4.17: Write data for RGB 5-6-5-bits input of DBI TYPE-C OPTION 3**

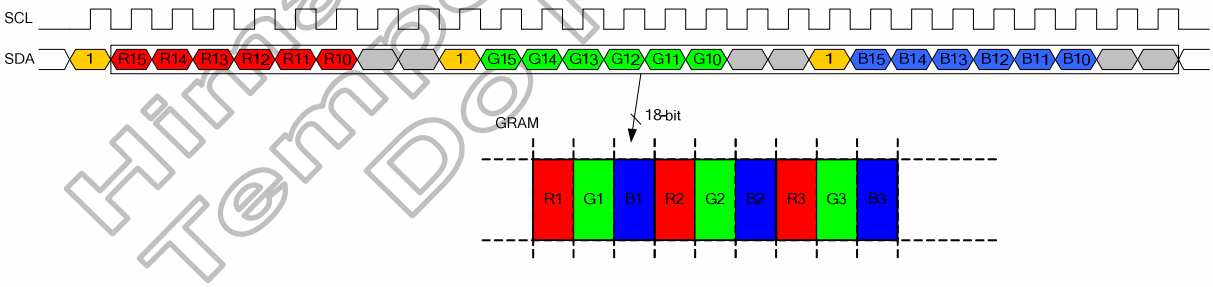


**Figure 4.18: Write data for RGB 6-6-6-bits input of DBI TYPE-C OPTION 1**

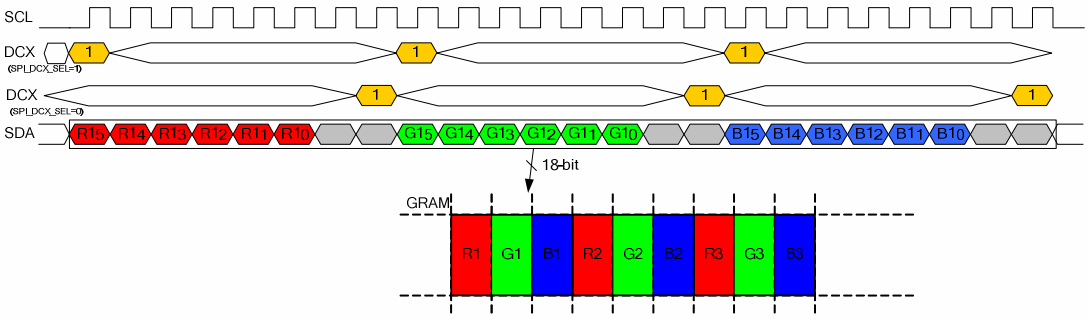


**Figure 4.19: Write data for RGB 6-6-6-bits input of DBI TYPE-C OPTION 3**

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| Register Command | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
|---|---|---|---|---|---|---|---|---|---|
| 3Ah | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| 05h | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 65K-Color (1-pixel/ 2-transfer) |
| | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | |
| 06h | R5 | R4 | R3 | R2 | R1 | R0 | x | x | 262K-Color (1-pixel/ 3-transfer) |
| | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

**Table 4.10: DBI TYPE-C Interface GRAM write Table**

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### 4.2.4 Break and Pause Sequences

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

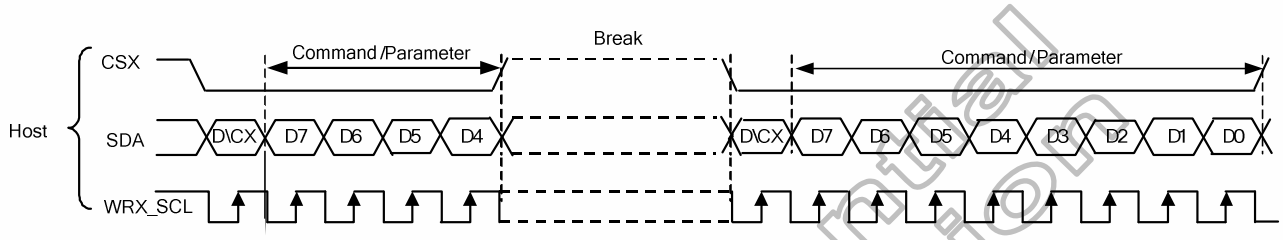


**Figure 4.20: Display Module Data Transfer Recovery**

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

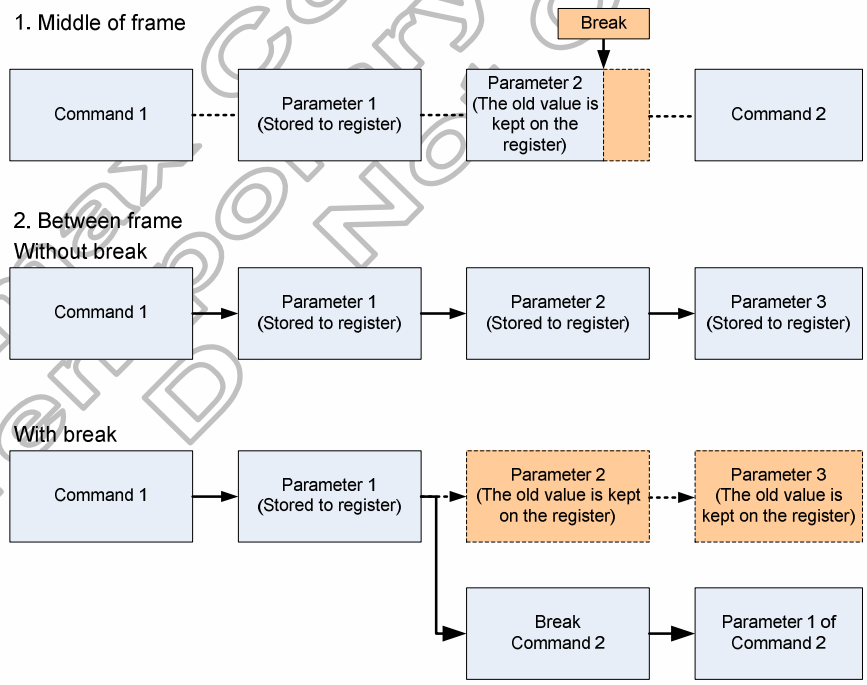


**Figure 4.21: Break durig parameter**

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The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the write sequence at the point where the sequence was paused.

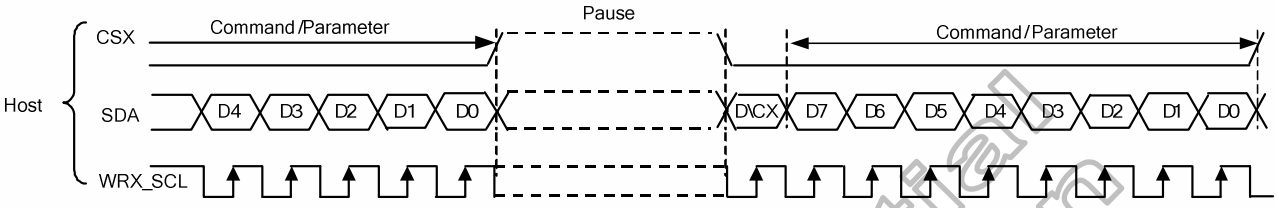


**Figure 4.22: Display Module Data Transfer Pause**

There are 4 cases where there is possible to see this kind of pause:

1. Command – Pause – Command
2. Command – Pause – Parameter
3. Parameter – Pause – Command
4. Parameter – Pause – Parameter

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## 4.3MIPI DPI interface (Display Pixel Interface)

The HX8357-c uses 8, 16, 18-bit parallel DPI interface which includes: HSYNC, VSYNC, DE, PCLK, DB17~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB17~DB0 –lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (‘+’, ‘1’, high) active and its state is read to the display module by a rising edge of the PCLK-line. DB pin 18 bit: DB17-DB12(R5-R0), DB11-DB6(G5-G0) and DB5-DB0(B5-B0); 16 bit: DB15-DB11(R4- R0), DB10-DB5(G5-G0) and DB4-DB0(B4-B0); 8 bit: DB7-DB0(R7-R0, G7-G0, B7-B0)) are used to tell what is the information of the image that is transferred on the display (when DE =1 and there is a rising edge of PCLK). DB17~DB0 – lines can be set to “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.

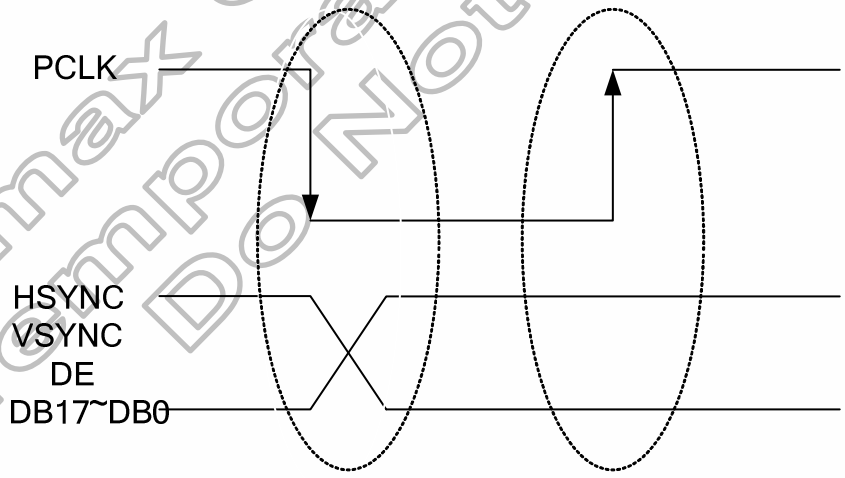


**Figure 4.23: PCLK cycle**
Note: PCLK is an unsynchronized signal (It can be stopped).

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**General Timing Diagram**

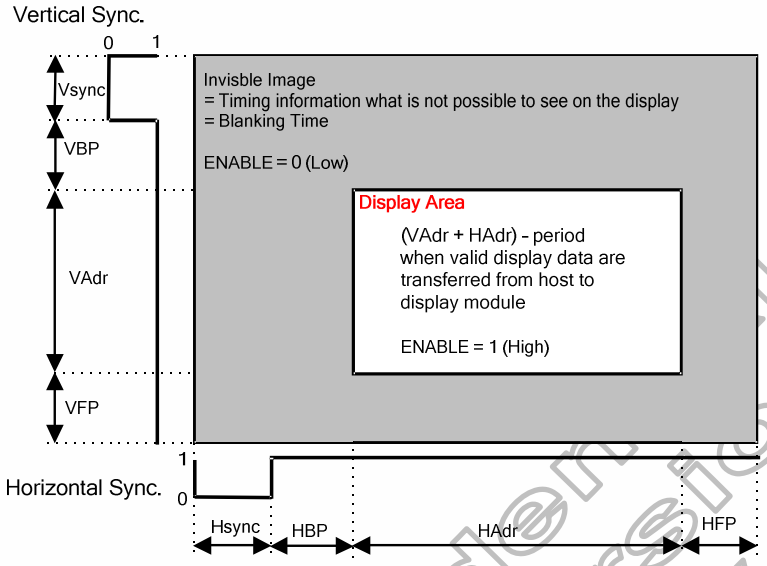


**Figure 4.24: General Timing Diagram**

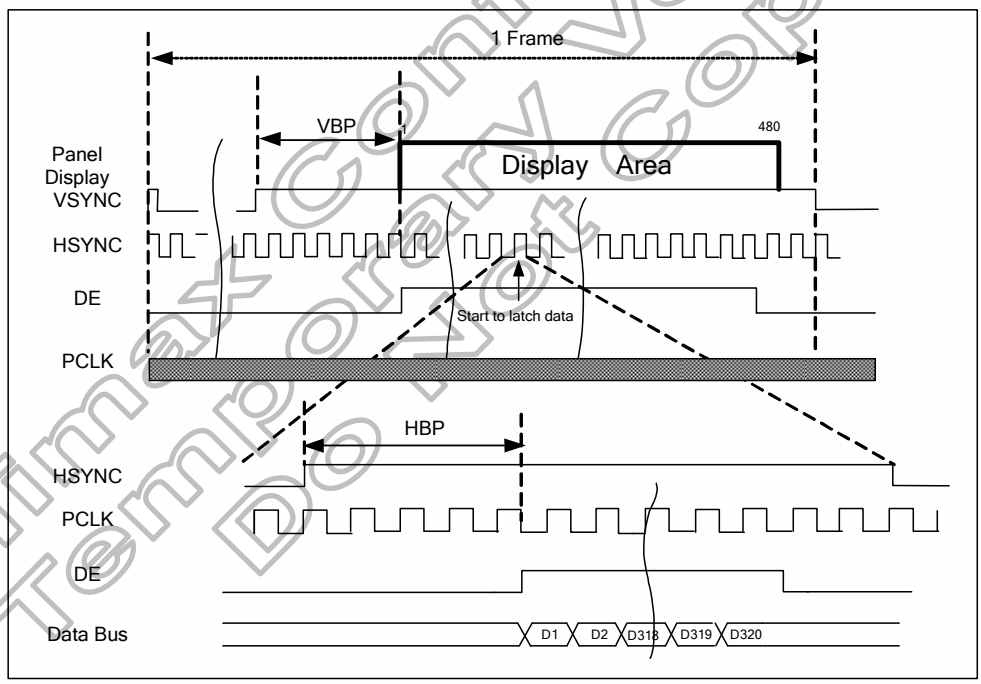


**Figure 4.25: DPI timing diagram**

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

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**DPI Interface Data Color Coding**

The MIPI DPI interface includes three types which are 16-/ 18-bit data format by register 3Ah (set_pixel_format) to select.

| Register 3Ah | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | DPI Interface mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 50h | | | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | 16-bit 65K-Color |
| 60h | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 18-bit 262K-Color |

**Table 4.11: 16-/18- DPI Color mapping**

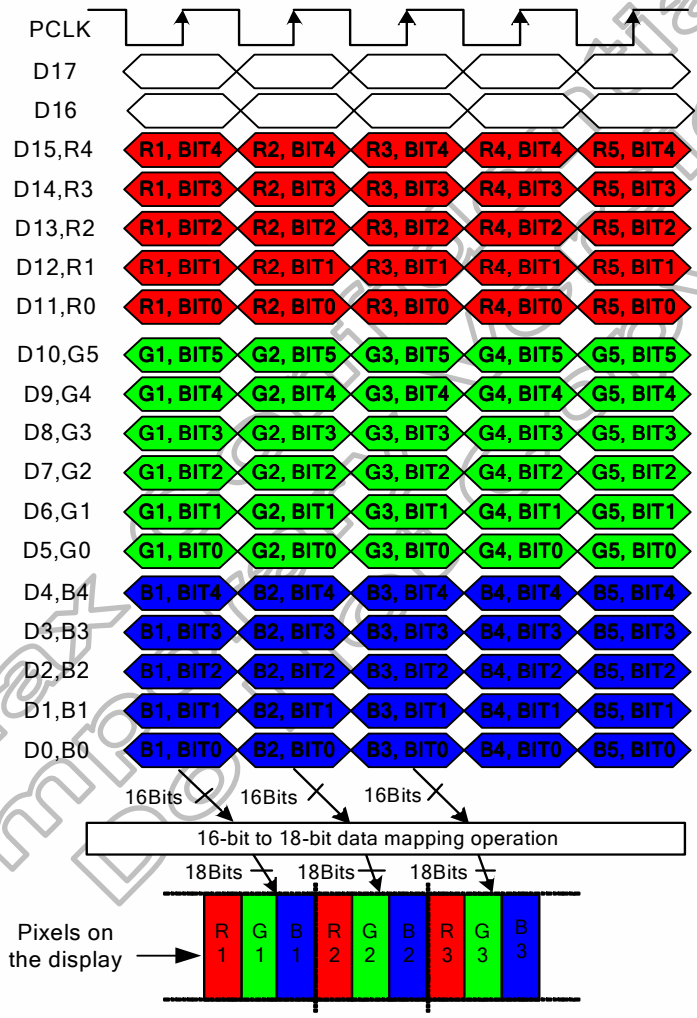


**Figure 4.26: 16 bit data bus color order on DPI interface**

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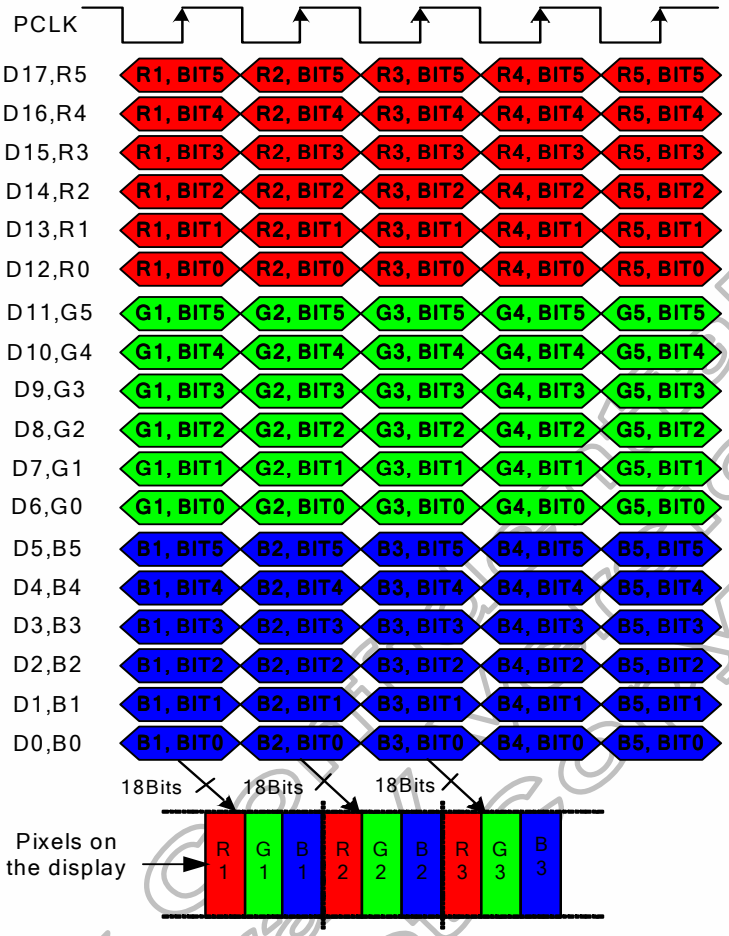


**Figure 4.27: 18 bit data bus color order on DPI interface**

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DPI interface displaying moving pictures can be selected to by register **DM** and **RM.**

RM The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation.

**RM** setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

| RM | Interface for RAM access |
|---|---|
| 0 | DBI Interface (MPU) |
| 1 | DPI Interface (RGB) |

**DM** bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.

| DM | Display Mode |
|---|---|
| 0 | Internal oscillation clock |
| 1 | DPI interface |

| Operation Mode | Frame Memory Access Setting (RM) | Display Operation Mode (DM) |
|---|---|---|
| Internal clock operation (displaying still pictures) | MPU interface (RM=0) | Internal clock operation (DM=0) |
| DPI interface (displaying moving pictures) | DPI interface (RM=1) | DPI interface (DM=1) |

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## 4.4DSI system interface

The selection of interface is by IM(2-0) =”110 “, the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.30 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

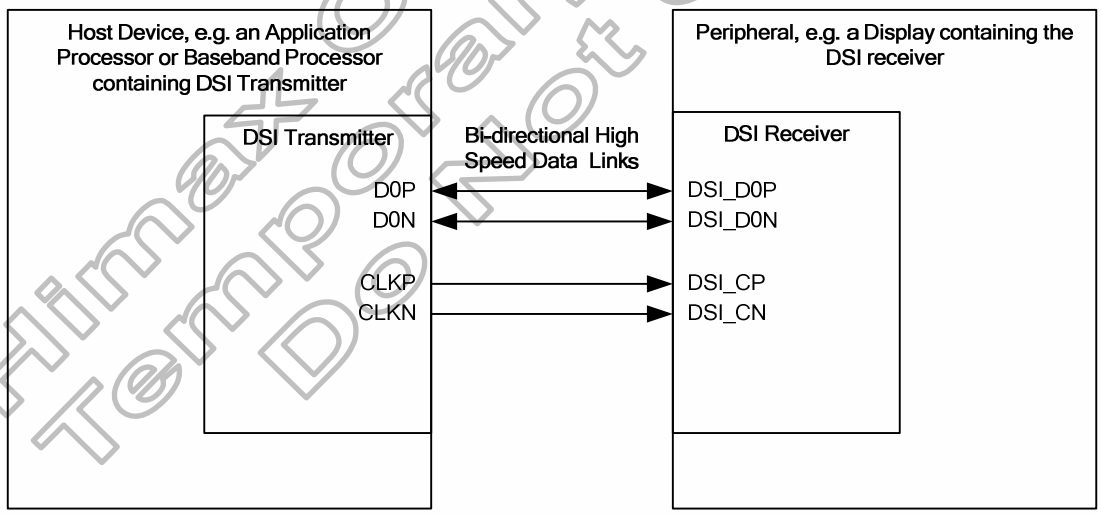


**Figure 4.28: DSI transmitter and receiver interface**

Please refer to “**MIPI Alliance Standard for DSI”** for DSI detailed specifications.

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### 4.4.1 DSI layer definitions

According Figure 4.31 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

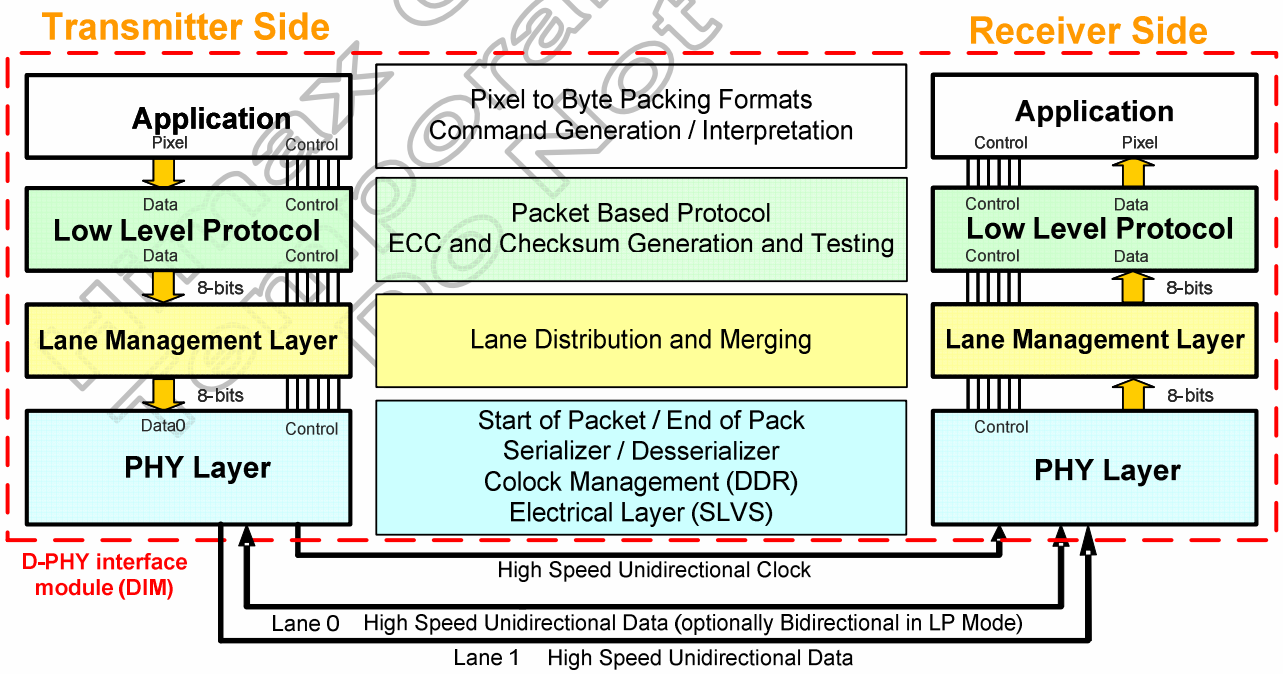


**Figure 4.29: Transmitter and receiver interface**

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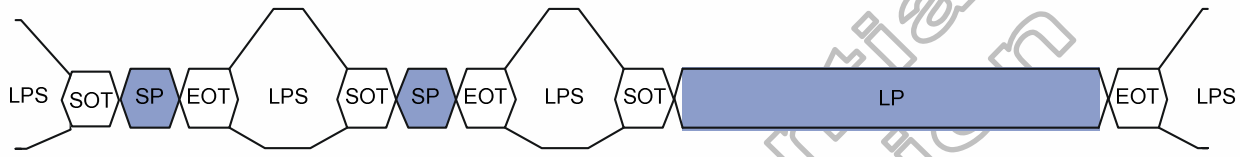
### 4.4.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.32 illustrates multiple HS Transmission packets.

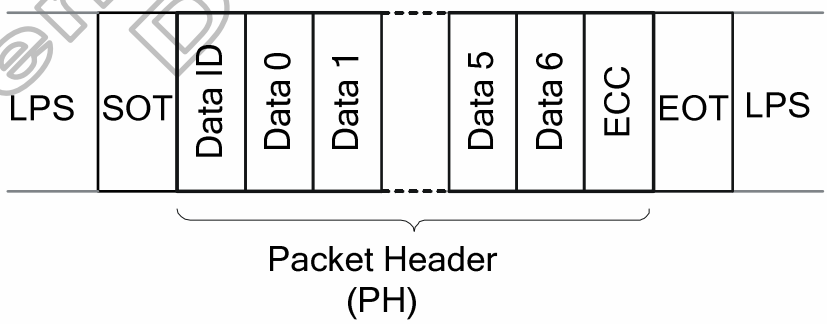



LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

**Figure 4.30: DSI Multiple HS transmission packets**

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

***Short packets*** specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Figure 4.33 shows the structure of the Short packet.




**DI(Data ID)**：Contain Virtual Channel Identifier and Data Type.
**ECC(Error Correction Code)**：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

**Figure 4.31: Structure of the short packet**

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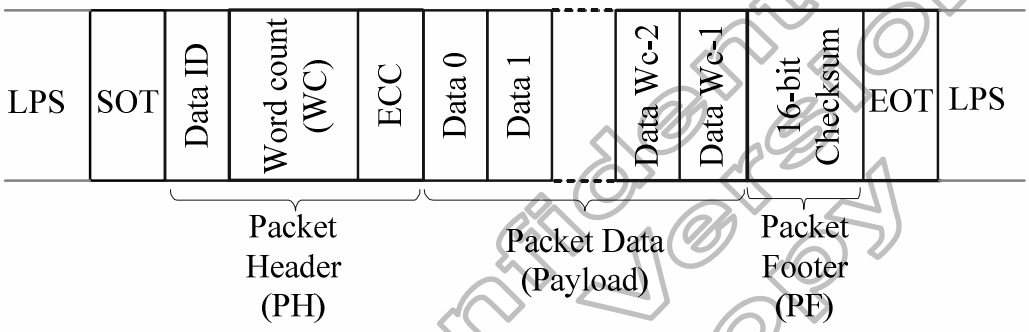
***Long packets*** specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.. Figure 4.43 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF




**DI (Data ID)：**Contain Virtual Channel Identifier and Data Type.
**WC (Word Count)：**The receiver use WC to define packet end.
**ECC (Error Correction Code)：**The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
**PF(Packet Footer)：**Mean 16-bit Checksum.

**Figure 4.32: Structure of the long packet**

According to packet form, basic elements include DI and ECC. Figure 4.44 the shows format of Data ID.

| DI7 | DI6 | DI5 | DI4 | DI3 | DI2 | DI1 | DI0 |
|---|---|---|---|---|---|---|---|
| VC (Virtual Channel) | | DT (Data Type) | | | | | |

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

**Figure 4.33: The format of data ID.**

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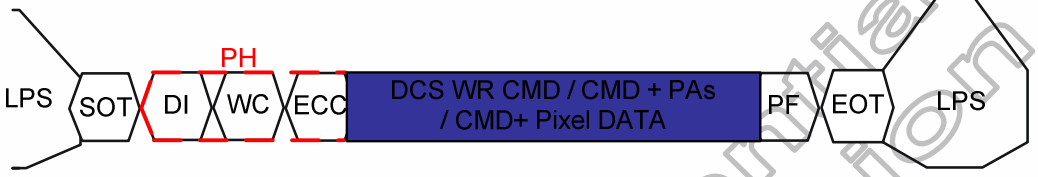
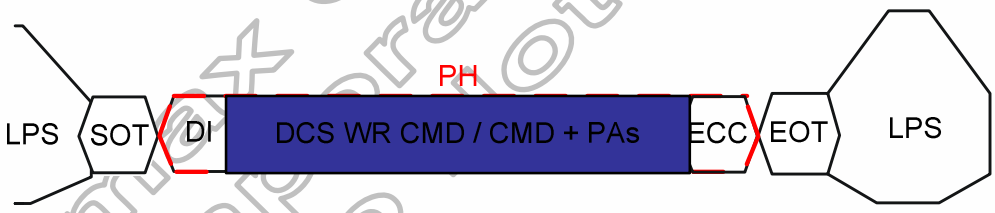
Due to Data Type (DT) mean format of transmission type, Figure 4.36 show Short- / Long-packet transmission command sequence.

Long packet write Command / Parameters / Pixel Datas




DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet write Command / Parameters




DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

**Figure 4.34: Show Short- / Long-packet transmission command sequence**

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#### 4.4.2.1 Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.12 Data Types for Processor-sourced Packets.

| Data type, hex | Data type, binary | Description packet | Size |
|---|---|---|---|
| 01h | 00 0001 | Sync Event, V Sync Start | Short |
| 11h | 01 0001 | Sync Event, V Sync End | Short |
| 21h | 10 0001 | Sync Event, H Sync Start | Short |
| 31h | 11 0001 | Sync Event, H Sync End | Short |
| 02h | 00 0010 | Color Mode (CM) Off Command | Short |
| 12h | 01 0010 | Color Mode (CM) On Command | Short |
| 22h | 10 0010 | Shut Down Peripheral Command | Short |
| 32h | 11 0010 | Turn On Peripheral Command | Short |
| 06h | 00 0110 | DCS READ, no parameters | Short |
| 37h | 11 0111 | Set Maximum Return Packet Size | Short |
| 09h | 00 1001 | Null Packet, no data | Long |
| 19h | 01 1001 | Blanking Packet, no data | Long |
| 39h | 11 1001 | DCS Long Write/write_LUT Command Packet | Long |
| 0Eh | 00 1110 | Packed Pixel Stream, 16-bit RGB, 5-6-5 Format | Long |
| 1Eh | 01 1110 | Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 2Eh | 10 1110 | Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 3Eh | 11 1110 | Packed Pixel Stream, 24-bit RGB, 8-8-8 Format | Long |
| X0h and XFh, unspecified | xx 0000<br>xx 1111 | DO NOT USE<br>All unspecified codes are reserved | - |

**Table 4.12: Data types for processor-sourced packets**

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Under tables list all detail function of all data types

| Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h) | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 01h | V Sync start, Start of VSA pulse. | 2 bytes (DI + ECC) |
| 11h | V Sync End, End of VSA pulse. | |
| 21h | H Sync Start, Start of HSA pulse. | |
| 31h | H Sync End, End of HSA pulse. | |
| **Note:** V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively. | | |

| Color mode status (Color Mode On, Color Mode Off) | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 02h | Color Mode On that switches a Video Mode display module to a low-color mode for power saving. | 2 bytes (DI + ECC) |
| 12h | Color Mode Off that switches a Video Mode display module from low-color display to normal display. | |

| Display status (shutdown command, turn-on command ) | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 22h | Shutdown Peripheral command that turns off the display in a Video Mode display for power saving. | 2 bytes (DI + ECC) |
| 32h | Turn On Peripheral command that turns on the display in Video Mode display for normal display. | |
| **Note**: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command. | | |

| DCS command setting | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 06h | DCS Read command, the returned data may be of Short or Long packet format. | 3 bytes (DI + DCS CMD. + ECC) |
| 39h | DCS Long Write/ Write_LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set. | Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF ) |

**NOTE:** (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.

(2) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

- If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(4) **One byte <= Length of payload DATA <= $2^{WC}$-1**

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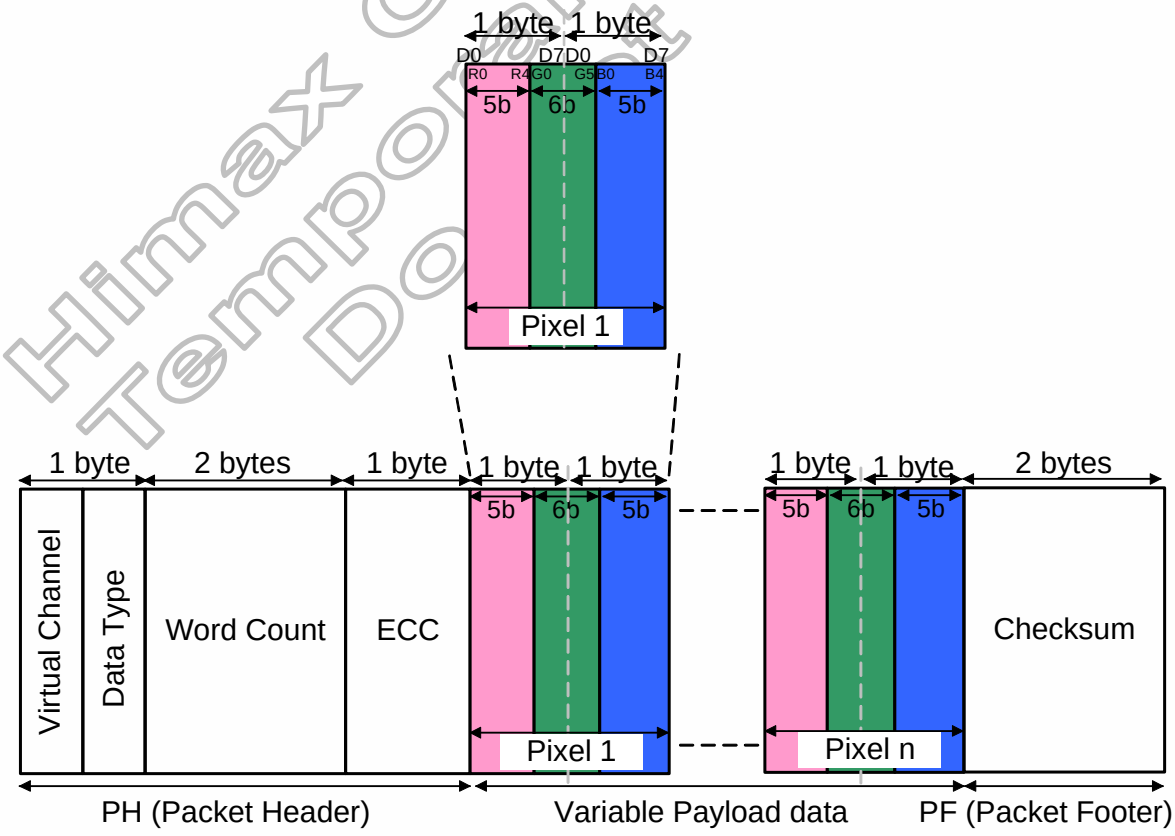
| Return packet size setting | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 37h | Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor. | 4 bytes<br>(DI + WC + ECC) |
| **Note:** The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one. | | |

| Variable data packet | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 09h | Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data. | Up to 65541 bytes<br>( DI + WC + ECC<br>+ DCS CMD.<br>+ Payload DATA +<br>PF ) |
| 19h | Blanking packet is used to convey blanking timing information in a Long packet. | |
| **Note:** (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.<br>(2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display, | | |

| Data stream format – 16bit Format | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 0Eh | Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue". | Up to 65541 bytes<br>( DI + WC + ECC<br>+ DCS CMD.<br>+ Payload DATA + PF ) |




**Note:** Within a color component, the "LSB is sent first, the MSB last ".

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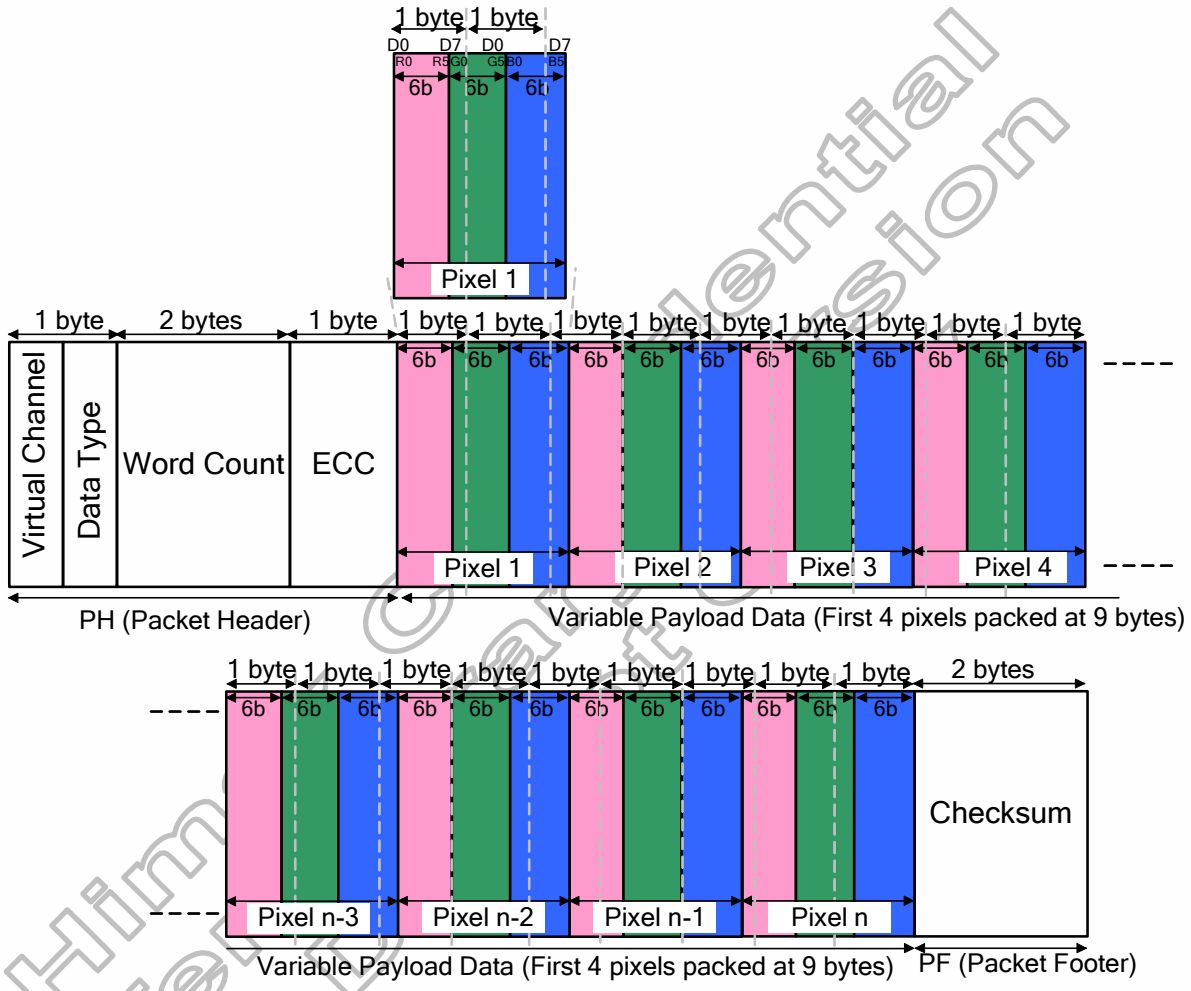
| Data stream format – 18bit Format | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 1Eh | Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue". | Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF ) |




**Note:** Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

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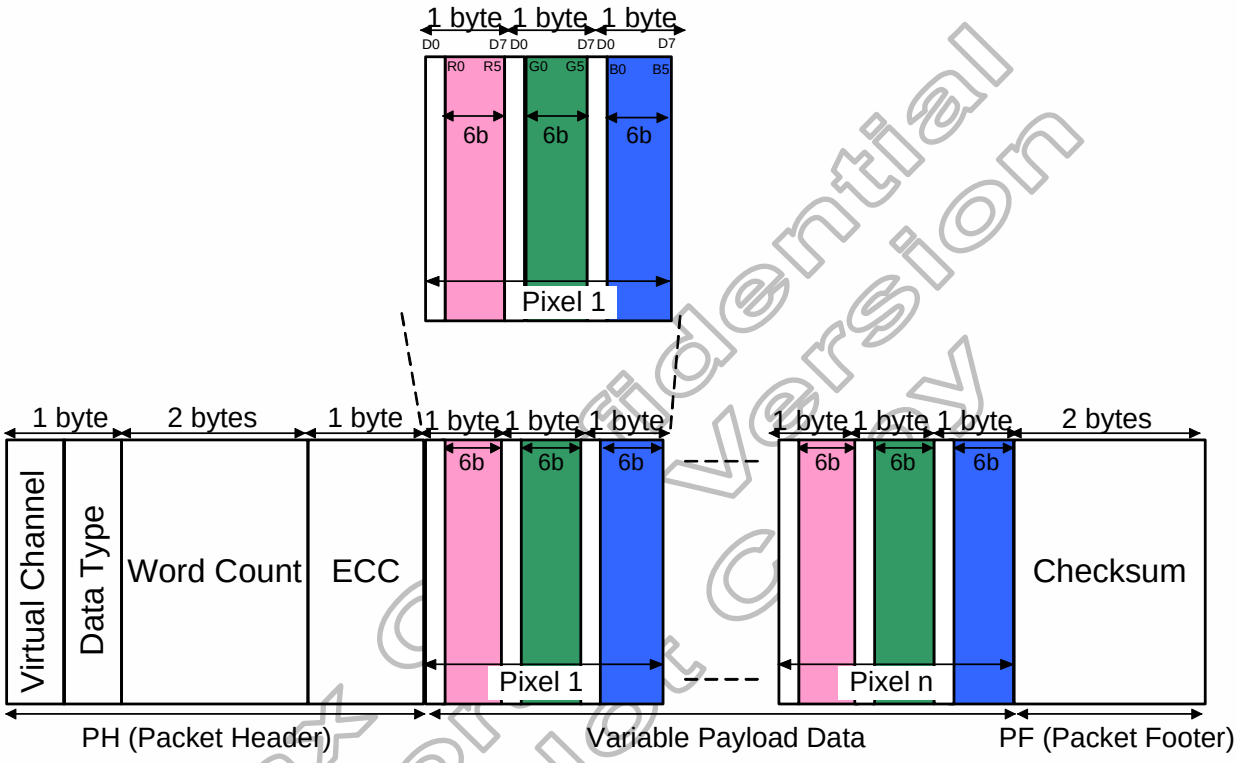
| Data stream format – 18bit Format | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 2Eh | Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”. | Up to 65541 bytes<br>( DI + WC + ECC<br>+ DCS CMD.<br>+ Payload DATA + PF ) |




**Note:** Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

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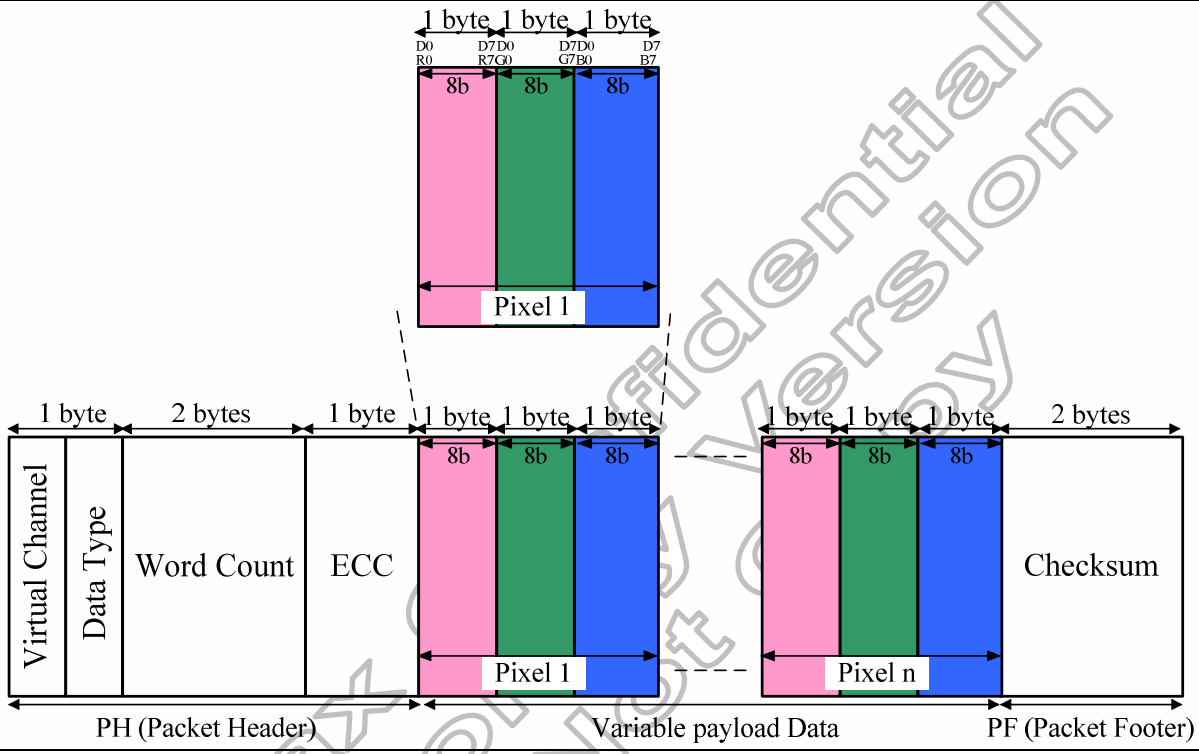
| Data stream forma – 24bit Format | | |
|---|---|---|
| **Data Type, Hex** | **Function Description** | **Number of bytes** |
| 3Eh | Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue. | Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF ) |




**Note:** Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

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#### 4.4.2.2 Peripheral to processor (reverse direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

*A.*Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
*B.Acknowledge* is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
*C.Acknowledge and Error Report* is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
*D.Response to Read Request* may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

A.Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
B.Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
C.Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report*)* packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
D.Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report*)* packet, the Error Report shall have the ECC Error flag set.
E.Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

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Which,

A. “Acknowledge” includes 2 bytes which are DI (VC + Acknowledge Data Type) and ECC.
B. “Acknowledge with Error Report” include 4 bytes which are DI, 2 bytes Error report and ECC.
C. “Response to Read Request” contains 2 types which are Short packet and long packet.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.16 shows the Error Report Bit Definitions. And Table 4.16 list complete set of peripheral-to-processor Data Types.

| Bit | Description |
|---|---|
| 0 | SoT Error |
| 1 | SoT Sync Error |
| 2 | EoT Sync Error |
| 3 | Escape Mode Entry Command Error |
| 4 | Low-Power Transmit Sync Error |
| 5 | HS Receive Timeout Error |
| 6 | reserved |
| 7 | reserved |
| 8 | ECC Error, single-bit (detected and corrected) |
| 9 | ECC Error, multi-bit (detected, not corrected) |
| 10 | Checksum Error (long packet only) |
| 11 | DSI Data Type Not Recognized |
| 12 | DSI VC ID Invalid |
| 13 | reserved |
| 14 | reserved |
| 15 | reserved |

**Table 4.13: Shows the error report bit definitions.**

| Data type, hex | Data type, binary | Description packet | Size |
|---|---|---|---|
| 02h | 00 0010 | Acknowledge with Error Report | Short |
| 08h | 00 1000 | End of Transmission (EoT) packet | Short |
| 1Ch | 01 1100 | DCS Long READ Response | Long |
| 21h | 10 0001 | DCS Short READ Response, 1 byte returned | Short |
| 22h | 10 0010 | DCS Short READ Response, 2 bytes returned | Short |
| Others (00h→3Fh) | | Reserved | - |

**Table 4.14: The complete set of peripheral-to-processor data types.**

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| Acknowledge types | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 02 | Get Acknowledge with Error report when Error occurs from processor transmission. | 4 bytes |
| **Note:**When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error➔Acknowledge with error report, Without error➔ Acknowledge. | | |

| DCS Read types | | |
|---|---|---|
| **Data type, hex** | **Function description** | **Number of bytes** |
| 21h, 22h | This is the DCS Short Read Response, 1 or 2 bytes, respectively. | 4 bytes |
| 1Ch | This is the long-packet response to DCS Long Read Request. | Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF ) |
| **Note:** If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent. | | |

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## 4.5MDDI Interface (Mobile Display Digital Interface)

### 4.5.1 Introduction of MDDI

The HX8357-C support MDDI, which is a differential serial interface with high-speed、low voltage swing characteristics. Both command and display image data can be transferred by MDDI. The devices connected by Data and STB link are host and client part.

Host transfer data to client in “forward” direction, client transfer data to host in “reverse” direction. The Data line is Dual direction, both command and image data are all send through the Data line. The STB line send strobe signal from host to client.

Data transferred in MDDI link are encoded as packet type.

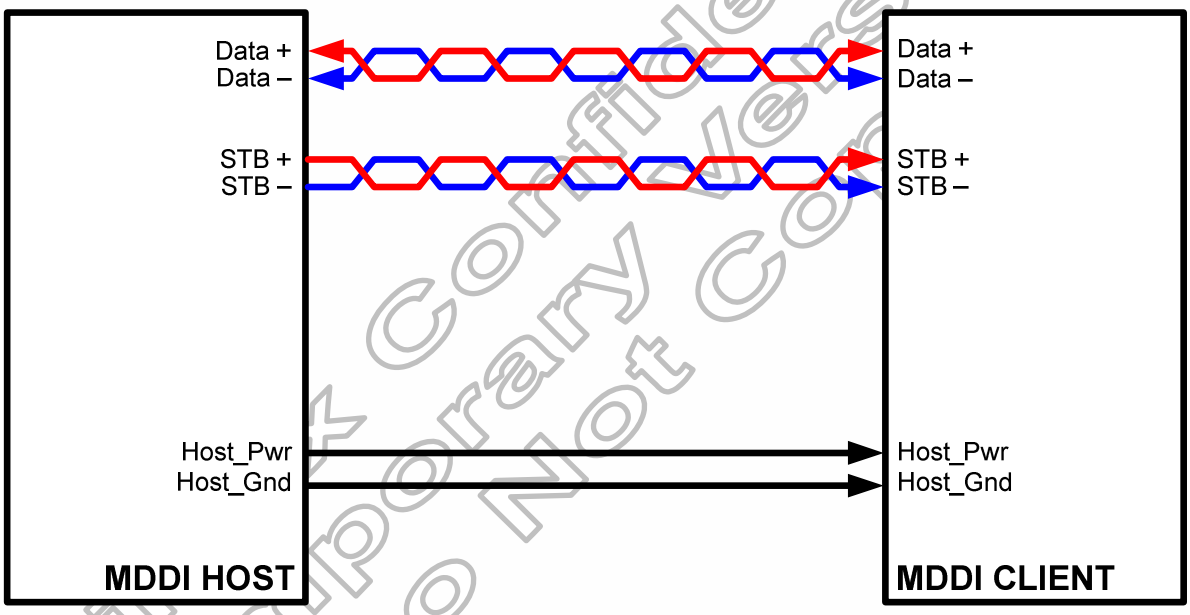


**Figure 4.35: Physical Connection of MDDI Host and Client**

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### 4.5.2 Terminology

The devices connected by the MDDI link are called the host and client. Data going from the host to the client travels in the ***forward*** direction, and data from the client to the host travels in the ***reverse*** direction.

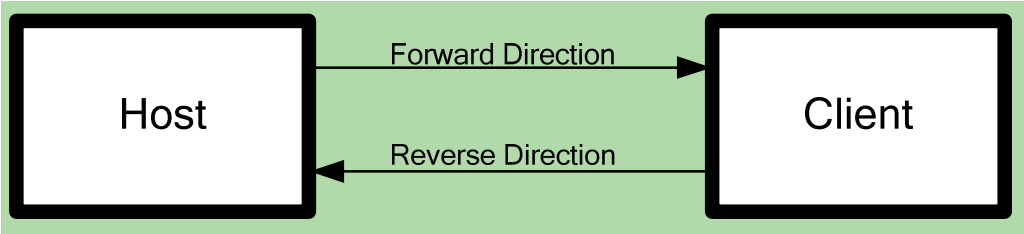


**Figure 4.36: MDDI Terminology**

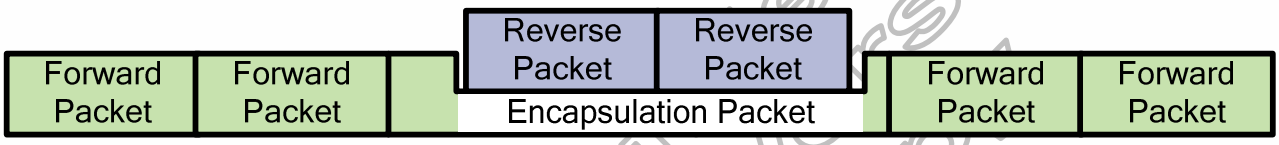


**Figure 4.37: Example of Bi-Directional MDDI Communication**

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### 4.5.3 Order of Data Transmission

All fields are transmitted with the LSB first and the MSB transmitted last. Parameters that are more than one byte in length are transmitted in little-endian format, i.e. the least significant byte first. The data fields of each packet are transmitted in the exact order that they are defined in the subsequent sections below, with the first field listed being transmitted first, and the last field described being transmitted last.

MDDI_Data0 is always aligned with bit 0 of bytes transmitted on the interface in any mode: Type 1, Type 2, Type 3, or Type 4.

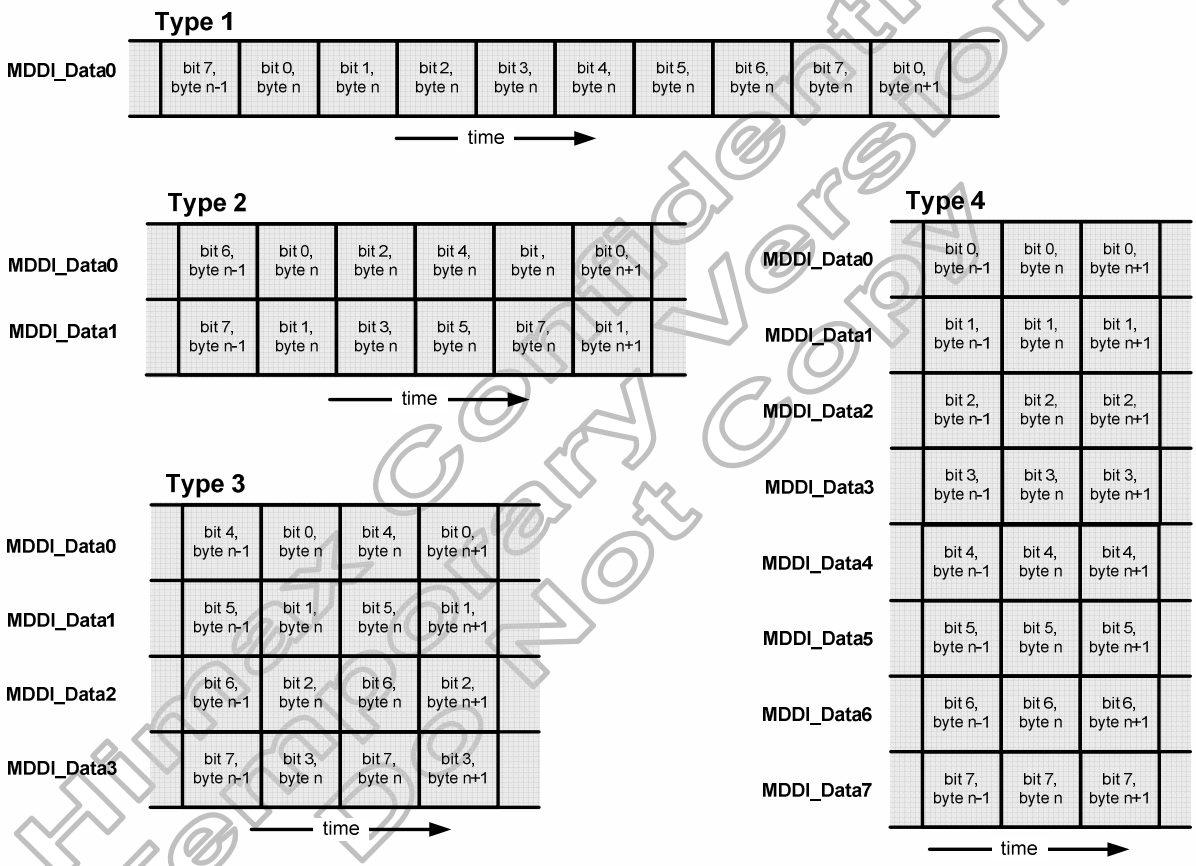


**Figure 4.38: Transmission Bit Ordering For Each Type**

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### 4.5.4 Data-STB Encoding

Data is encoded using a DATA-STB format. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure 4.5 illustrates how the data sequence “1110001011” is transmitted by using DATA-STB encoding.

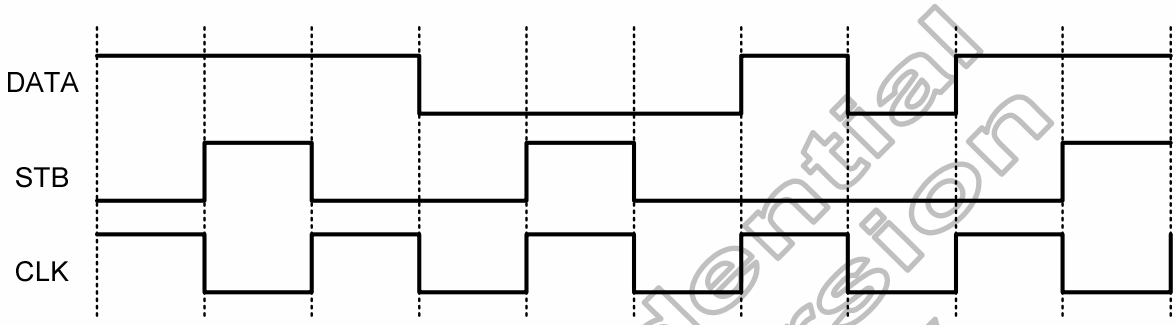


**Figure 4.39: Data-STB Encoding**

Figure 4.42 shows a sample circuit to generate DATA and STB from input data, and then decodes the DATA and STB to the Output Data.

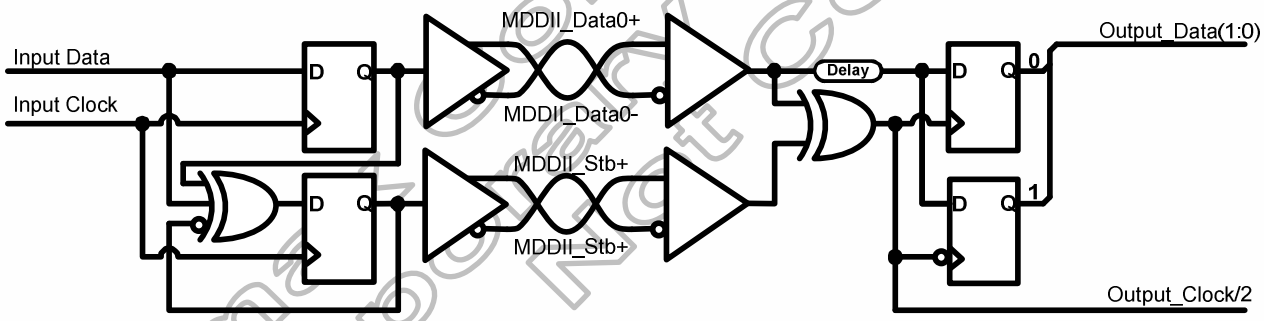


**Figure 4.40: Data / STB Generation & Recovery Circuit**

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### 4.5.4.1 MDDI Data/STB

The MDDI_DATA (HSI_D0P/N) and MDDI_STB (HSI_CLKP/N) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

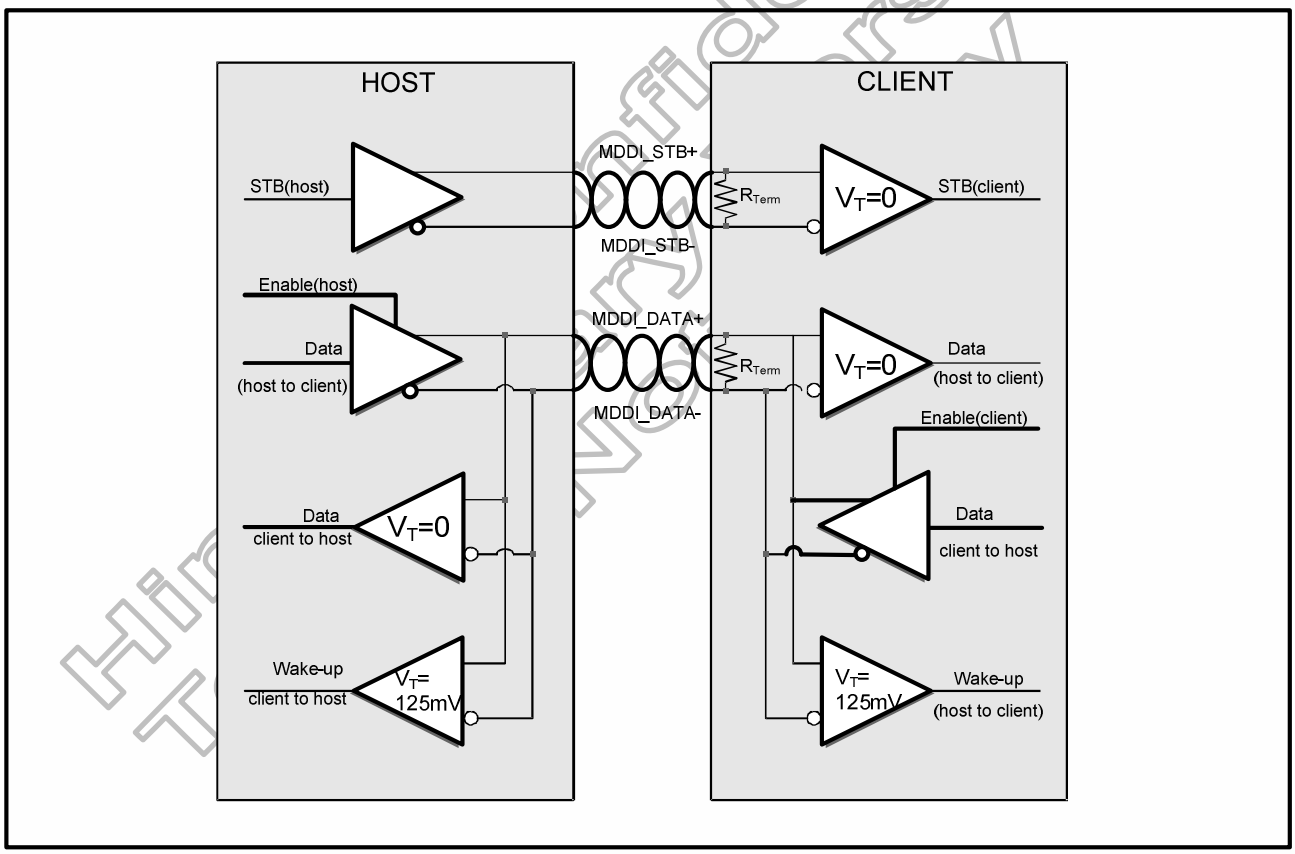


**Figure 4.41: Differential Connection between Host and Client**

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### 4.5.4.2 MDDI Packet

Data transmission over the MDDI link is grouped into packets. Several packets format is supported in HX8357-C. Most packets are in forward direction, transferred from host to client; reverse encapsulation packet is in reverse direction, transferred from MDDI client to host. A number of packets, started by sub-frame header packet, construct one sub frame.

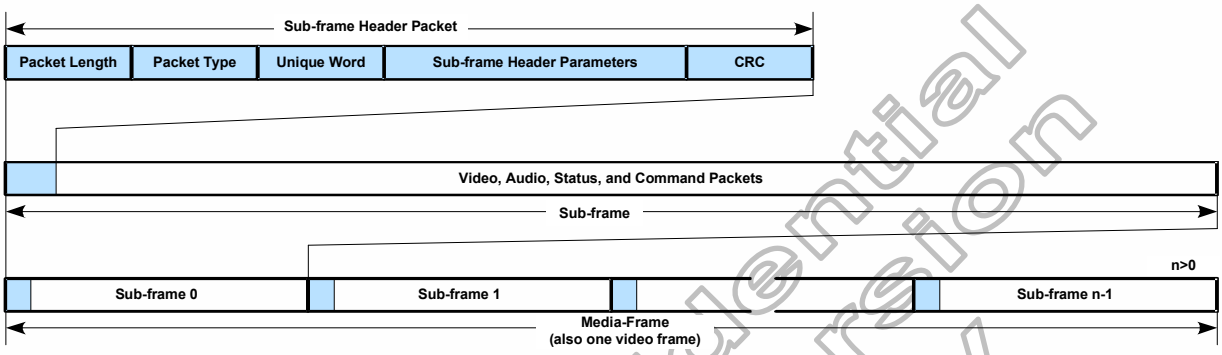
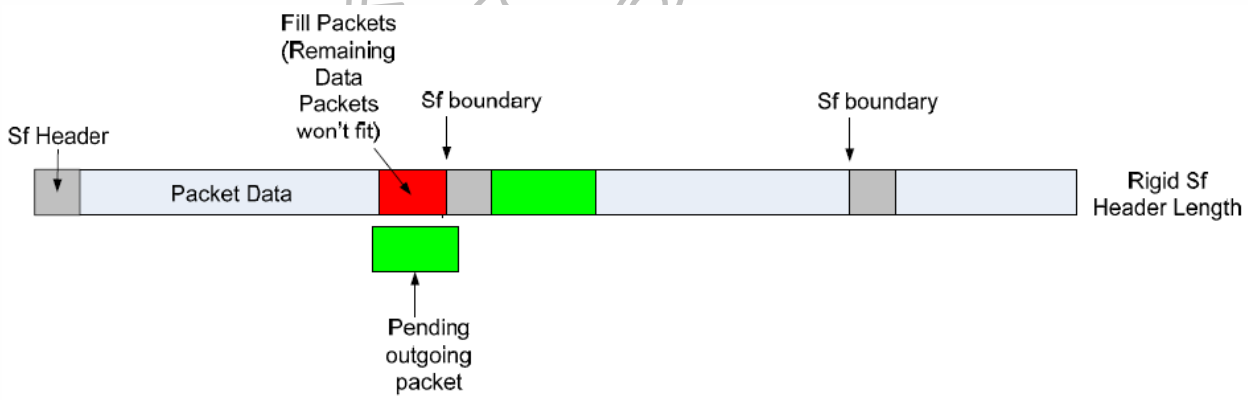



**Figure 4.42: MDDI Packet Structure**

Refer to MDDI frame structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frames make up a media-frame.

The length of sub-frame has three modes Fixed, Flexible and Unlimited.

Fixed sub-frame length means the total byte in a sub-frame will meet the value which defined in the sub-frame header packet in front of a sub-frame.




In flexible sub-frame when a packet is requested to be transmitted, it will never be blocked. This may cause a packet to cross a sub-frame boundary. The host therefore must maintain the sub-frame timing within its core to keep track of sub-frames that have lengths greater than the target length, to then transmit a matched number and length of sub-frames that are less than the target sub-frame length to ensure an average sub-frame length that matches the target length.

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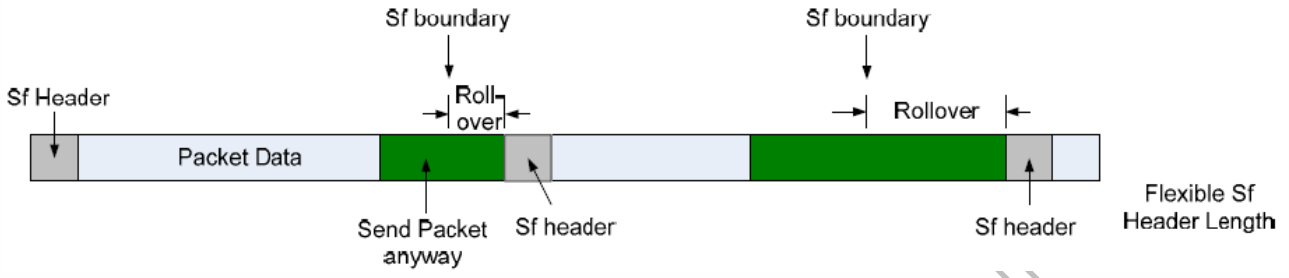
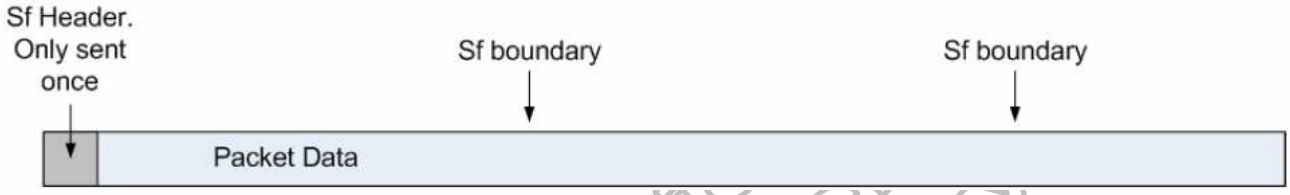



Hibernation to help the client sync up with the unique word pattern. The MDDI host is allowed to transmit a sub-frame at any time if it wishes, however it is not required.




HX8357-C support these packets, which described in the table below.

| Packet | Function | Direction |
|---|---|---|
| Sub-frame header packet | Header of each sub frame | Forward |
| Register access packet | Register setting | Forward |
| Video stream packet | Video data transfer | Forward |
| Windowless Video stream packet | Video data transfer | Forward |
| Flexible Video stream packet | Video data transfer | Forward |
| Filler packet | Fill empty packet space | Forward |
| Reverse link encapsulation packet | Reverse data packet | Reverse |
| Round-trip delay measurement packet | Host→client→host delay check | Forward/Reverse |
| Enhanced Round-trip delay measurement packet | Host→client→host delay check | Forward/Reverse |
| Client capability packet | Capability of client check | Reverse |
| Client request and status packet | Information about client status | Reverse |
| Forward Link Skew Calibration Packet | Use to Calibrate the delay skew | Forward |
| Perform Type Handoff Packet | Change operate Type | Forward |
| Link shutdown packet | End of frame | Forward |

**Table 4.15: List of Supported MDDI Packet**

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### Sub-frame Header Packet

| Packet Length | Packet type =0x3bffh | Unique word =0x005a | Reserved 1 | Sub-frame length | Protocol Version | Sub-frame Count | Media-frame Count | CRC |
|---|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes |

| | | |
|---|---|---|
| packet length | : | total number of bytes in the packet not including the packet length field, always 20 |
| packet type | : | packet type, 0x3bffh for sub-frame header packet |
| unique word | : | link packet type to form a 32-bit unique word for good autocorrelation. |
| reserved 1 | : | not used(all zero) |
| sub-frame length | : | In fixed Sub-Frame mode, this value specifies number of bytes per sub-frame.<br>In the Flexible Sub-Frame mode ,this value represents the target length.<br>In the unlimited Sub-Frame mode, the value is set to zero |
| | : | All zero define the length of the sub-frame is undefined. |
| protocol version | : | set all zero |
| sub-frame count | : | specifies number of sub-frame header packet. |
| media frame count | : | specifies number of media frame |
| CRC | : | error check |

### Register Access Packet

| Packet Length | Packet type =146 | bClient ID | Read/Write Info | Register Address | Parameter CRC | Register Data list | Register Data CRC |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes | P_length-14 bytes | 4 bytes |

| | | |
|---|---|---|
| packet length | : | total number of bytes in the packet not including the packet length field |
| packet type | : | packet type, 146(decimal) for register access packet |
| bClient ID | : | set all zero |
| Read/Write Info | : | when write value to register, bit[15:14] = “00” |
| | | when request data from register, bit[15:14]=“10” |
| | | when data from client, bit[15:14] = “11” |
| | | bit[13:0] : A 14-bit unsigned integer that specifies the number of 32-bit register<br>Data List items to be transferred in the Register Data List field |
| register address | : | Register address is set written here. |
| parameter CRC | : | To error check from packet length to register address |
| register data list | : | A list of 4-byte register data values. |

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## Video Stream Packet

| Packet Length | Packet type =16 | bClient ID | video data format descriptor | pixel data attributes | X left edge | Y top edge | X right edge | Y bottom dedge | X start | Y start |
|---|---|---|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| pixel count | parameter CRC | pixel data | pixel data CRC |
|---|---|---|---|
| 2 bytes | 2 bytes | packet length - 26 bytes | 2 bytes |

packet length
packet type
bClient ID
video data format descriptor

- total number of bytes in the packet not including the packet length field
- packet type, 16 (decimal) for register access packet
- set all zero

| [15:12] | [11:8] | [7:4] | [3:0] | |
|---|---|---|---|---|
| 0x05 | 0x05 | 0x06 | 0x05 | 16bpp RGB format |
| | 0x06 | 0x06 | 0x06 | 18bpp RGB format |
| | 0x08 | 0x08 | 0x08 | 24bpp RGB format |

pixel data attributes

- bits [1:0] =11 (fixed value), others are all zero

X left edge
- X coordinate of the left edge of the active window filled by the Pixel Data field.

X top edge
- Y coordinate of the top edge of the active window filled by the Pixel Data field

X right edge
- X coordinate of the right edge of the active window filled by the Pixel Data field.

Y bottom edge
- Y coordinate of the bottom edge of the active window filled by the Pixel Data field.

X start
- X coordinate of the first pixel in the Pixel Data field below

Y start
- X coordinate of the first pixel in the Pixel Data field below

Pixel count
- Write number of pixel

Patameter CRC
- To error check from packet length to pixel count

pixel data
- pixel data info. Number of pixel data must not be over 65509

pixel data CRC
- To pixel data error check.

## Windowless Video stream packet

| Packet Length | Packet type =22 | bClient ID | video data format descriptor | pixel data attributes | pixel count | parameter CRC | pixel data | pixel data CRC |
|---|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | packet length - 14 bytes | 2 bytes |

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 22 (decimal) for register access packet
bClient ID : set all zero
video data format descriptor : bits[15:13]=010, raw RGB format (fixed value)
bit[12]=1,only packed type is available (fixed value)
bits[11:0]=number of bits per pixel,
bits[11:8]=for Red,bits[7:4]=for Green,bits[3:0]=for Blue
pixel data attributes : bits[1:0]=11, displayed both eyes (fixed value)
others are all zero
Pixel count : Write number of pixel
Patameter CRC : To error check from packet length to pixel count
pixel data : pixel data info. Number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

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## Flexible Video stream packet

| Packet Length | Packet type =20 | bClient ID | Field Present Flags | video data format descriptor | pixel data attributes | X left edge | Y top edge | X right edge | Y bottom dedge | X start | Y start |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| pixel count | parameter CRC | pixel data | pixel data CRC |
|---|---|---|---|
| 2 bytes | 2 bytes | packet length – present header bytes | 2 bytes |

| | | |
|---|---|---|
| **packet length** | **:** | **total number of bytes in the packet not including the packet length fie** |
| **packet type** | **:** | **packet type, 16 (decimal) for register access packet** |
| **bClient ID** | **:** | **set all zero** |
| **Field Present Flags** | **:** | **A value of '1' for each bit indicates that the field is present in the packet.<br>A value of '0' for the bit indicates that the field is not present.<br>o Bit 0 indicates the presence of the Video Data Format Descriptor field.<br>o Bit 1 indicates the presence of the Pixel Data Attributes field.<br>o Bit 2 indicates the presence of the X Left Edge field.<br>o Bit 3 indicates the presence of the Y Top Edge field.<br>o Bit 4 indicates the presence of the X Right Edge field.<br>o Bit 5 indicates the presence of the Y Bottom Edge field.<br>o Bit 6 indicates the presence of the X Start field.<br>o Bit 7 indicates the presence of the Y Start field.<br>o Bit 8 indicates the presence of the Pixel Count field.<br>o Bits [15:9] must be set to '0'.** |
| **video data format descriptor** | **:** | **bits[15:13]=010, raw RGB format (fixed value)<br>bit[12]=1,only packed type is available (fixed value)<br>bits[11:0]=number of bits per pixel,<br>bits[11:8]=for Red,bits[7:4]=for Green,bits[3:0]=for Blue** |
| **pixel data attributes** | **:** | **bits[1:0]=11, displayed both eyes (fixed value)<br>others are all zero** |
| **X left edge** | **:** | **X coordinate of the left edge of the active window filled by the Pixel D** |
| **X top edge** | **:** | **Y coordinate of the top edge of the active window filled by the Pixel D** |
| **X right edge** | **:** | **X coordinate of the right edge of the active window filled by the Pixel** |
| **Y bottom edge** | **:** | **Y coordinate of the bottom edge of the active window filled by the Pix** |
| **X start** | **:** | **X coordinate of the first pixel in the Pixel Data field below** |
| **Y start** | **:** | **X coordinate of the first pixel in the Pixel Data field below** |
| **Pixel count** | **:** | **Write number of pixel** |
| **Patameter CRC** | **:** | **To error check from packet length to pixel count** |
| **pixel data** | **:** | **pixel data info. Number of pixel data must not be over 65509** |
| **pixel data CRC** | **:** | **To pixel data error check.** |

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**Perform Type Handoff Packet**

| Packet Length | Packet type =77 | Interface Type | Reserved1 | Delay filler | CRC |
|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 1 byte | 1 byte | Packet Length – 6 bytes | 2 bytes |

| | | |
|---|---|---|
| packet length | : | total number of bytes in the packet not including the packet length field |
| packet type | : | packet type, 77(decimal) for perform type handoff packet |
| interface type | : | contain the new type to be used.<br>Bit[2:0], define the forward link<br>1: handoff to type1<br>2: handoff to type2<br>others: not used.<br>Bit[5:3], define the reverse link<br>1: handoff to type1<br>others not used<br>bit[7:6], set all zero. |
| Reserved1 | : | Set all zero |
| delay filler | : | Set all zero<br>Forward link is Type1, Delay filler is 16byte<br>Forward link is Type2, Delay filler is 32byte |
| CRC | : | To error check |

**Forward Link Skew Calibration Pack**

| Packet Length | Packet type =83 | hClient ID | CRC | All Zero1 | Calibration Data Sequence | All Zero2 |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 8 bytes | Packet Length - 22 bytes | 8 bytes |

| | | |
|---|---|---|
| packet length | : | total number of bytes in the packet not including the packet length field |
| packet type | : | packet type, 83(decimal) for perform type handoff packet |
| hClient ID | : | contain the new type to be used. |
| CRC | : | To error check |
| All Zero 1 | : | Set all zero |
| Calibration Data Sequence | : | a data sequence that causes the MDDI_Data signals to toggle at every data period.<br>o Type 1 – (64 byte data sequence) AAh, AAh … or 55h, 55h…<br>o Type 2 – (128 byte data sequence) CCh, CCh … or 33h, 33h… |
| All Zero 2 | | Set all zero |

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### Filler Packet

| Packet Length | Packet type =0 | filler bytes (all zero) | CRC |
|---|---|---|---|
| 2 bytes | 2 bytes | packet length – 4 bytes | 2 bytes |

packet length  total number of bytes in the packet not including the packet length field
packet type  packet type, 0 (decimal) for register access packet
filler bytes  set to all zero (The size is under packet length available)
CRC  To error check

### Link Shutdown Packet

| Packet Length | Packet type =69 | CRC | All zeros |
|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 16 bytes |

packet length  total number of bytes in the packet not including the packet length field
packet type  packet type, 16 (decimal) for register access packet
CRC  To error check
All zeros  write all zero (size is 16 bytes, because MDDI for HX8369-A is type 1)

Fixed Value

For more information about MDDI packet refer to VESA MDDI spec.

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### 4.5.4.3 Hibernation / Wake up

HX8357-C MDDI provides the hibernation mode to reduce the power consumption. The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption. In hibernation mode, hi-speed drivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

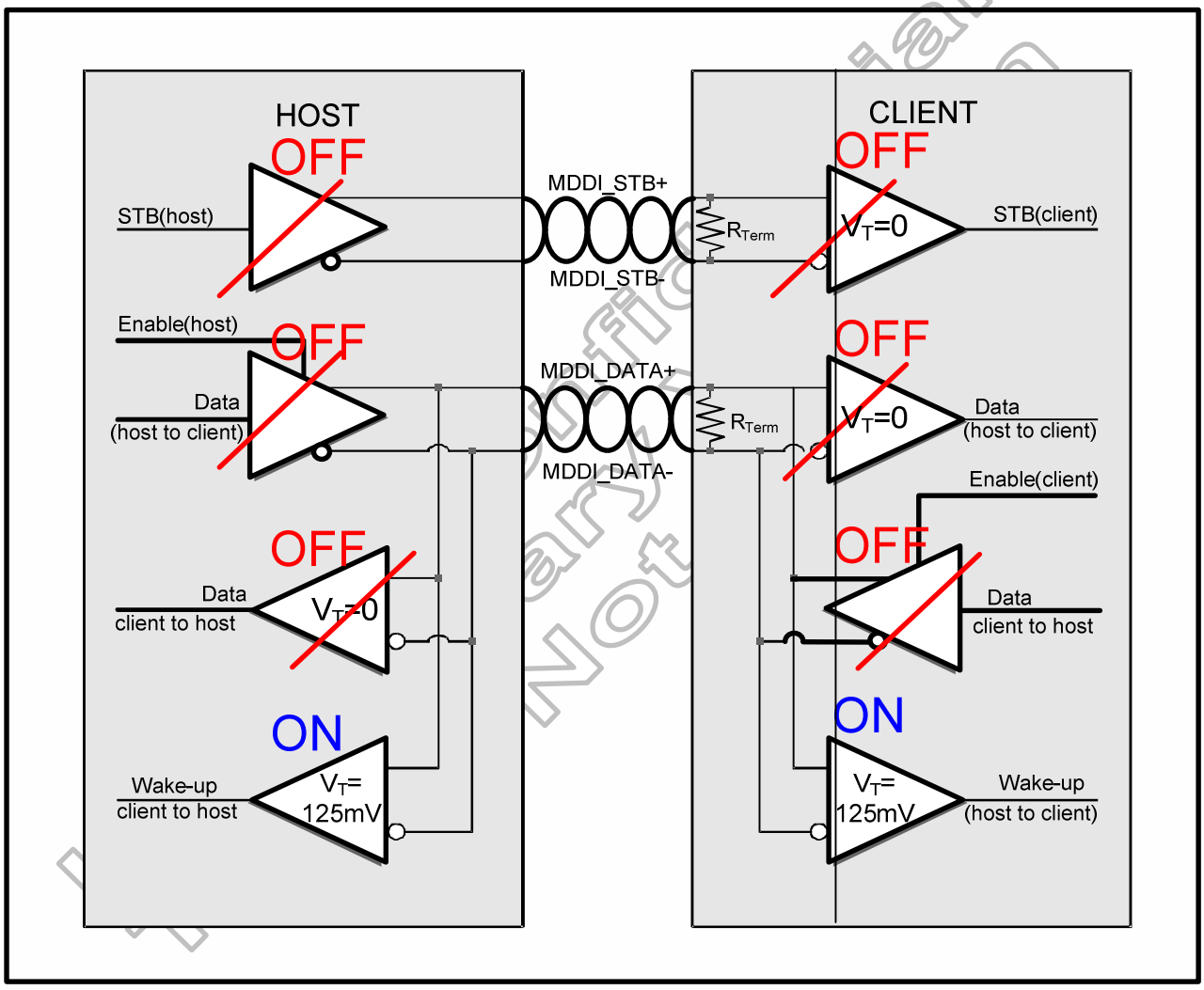


**Figure 4.43: MDDI Transceiver / Receiver State in Hibernation**

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detected using low-speed line receivers that consume only a fraction of the current as the differential receivers required to receive the signals at the maximum link operating speed.


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### 4.5.4.4 MDDI Link Wakeup Sequence

Figure below provide a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The labeled events are:

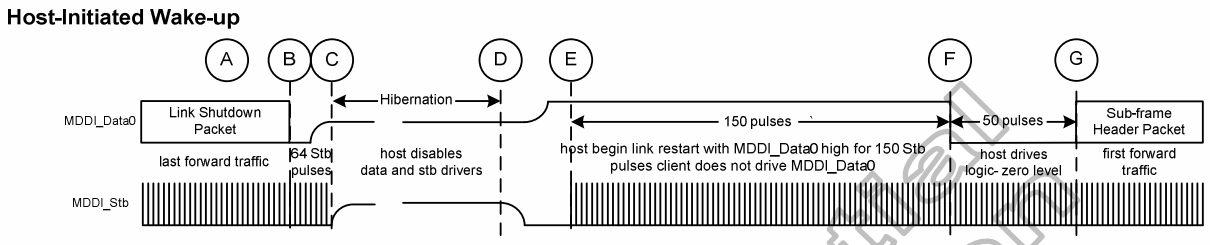


**Figure 4.44 Host-initiated Link Wakeup Sequence**

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

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An example of a typical client-initiated service request event with no contention is illustrated in below figure. The labeled events are:

### 4.5.4.5 MDDI Operation Mode

The MDDI Link provides six operation modes, the mode flow is illustrated as below.

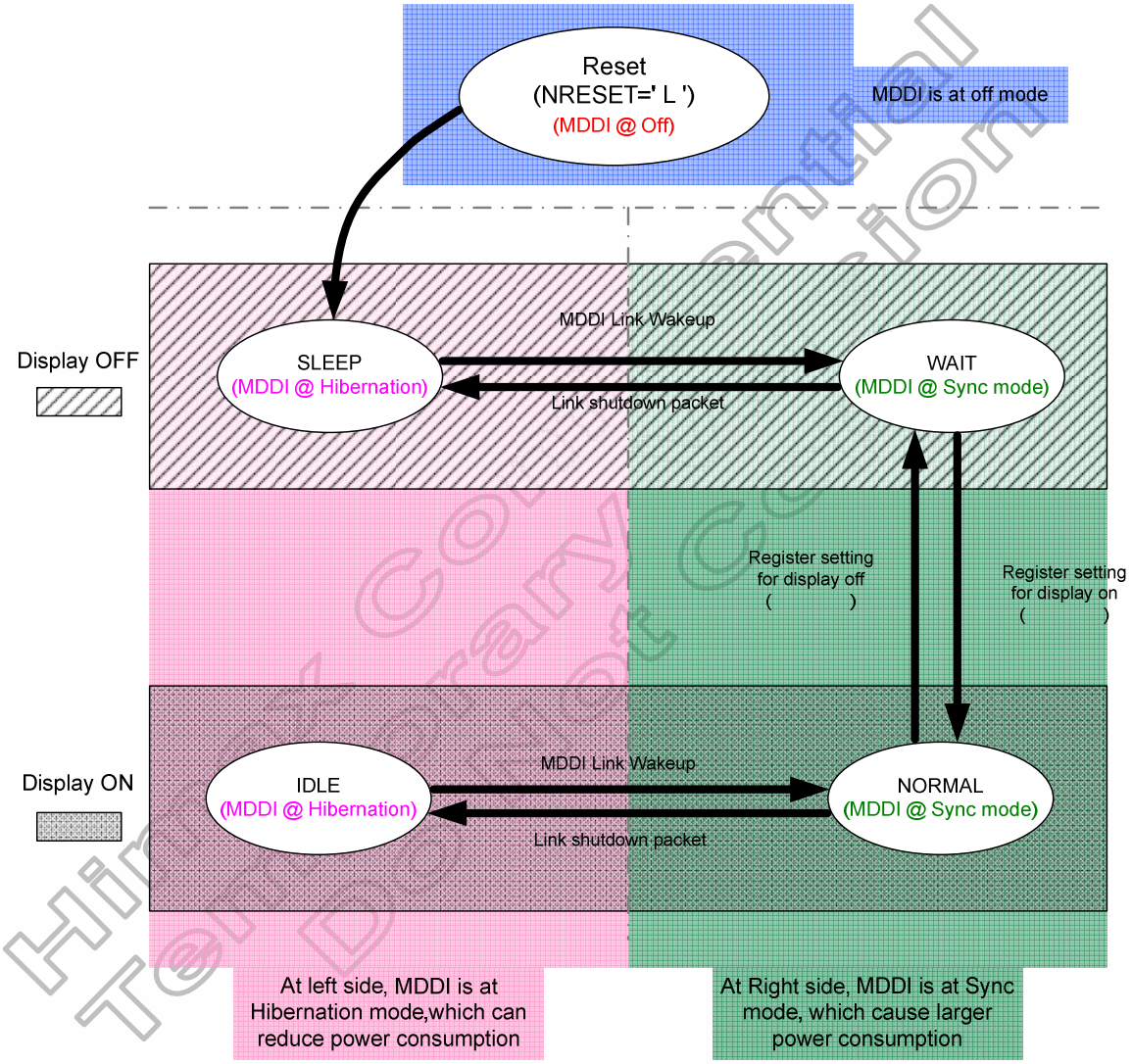


**Figure 4.45: MDDI Operation Mode**

The MDDI Link provides five operation modes that are listed in the Table 4.16.

| Function | RESET | SLEEP | WAIT | NORMAL | IDLE |
|---|---|---|---|---|---|
| MDDI hibernation receiver | OFF | ON | OFF | OFF | ON |
| MDDI normal receiver or normal driver | OFF | OFF | ON | ON | OFF |
| Register and RAM access | Disable | Disable | Enable | Enable | Disable |
| Internal oscillator(OSC) | OFF | OFF | ON/OFF(1) | ON(2) | ON(2) |
| Booster(VSP,VSN,VGH,VGL) | OFF | OFF | OFF | ON | ON |
| Regulator (VSPR,VSNR) | OFF | OFF | OFF | ON | ON |

**Note:** (1) While OSC_EN = 0 is defined the operation as OFF, and OSC_EN = 1 is ON.
(2) Do not set OSC_EN = 1 in Normal mode, If OSC stopped, indication also stops.

**Table 4.16: Operation Mode List**


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# 5. Functional Description

## 5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 2,764,800 bits (320x18x480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

### 5.1.1 Address counter (AC)

The HX8357-C contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

| MV | X range | Y range | Panel resolution |
|---|---|---|---|
| 0 | 0~319d. | 0~479d. | 320 RGBX480 dot |
| 1 | 0~479d. | 0~319d. | |

**Table 5.1: Addresses counter range**

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

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### 5.1.2 System interface to GRAM write direction

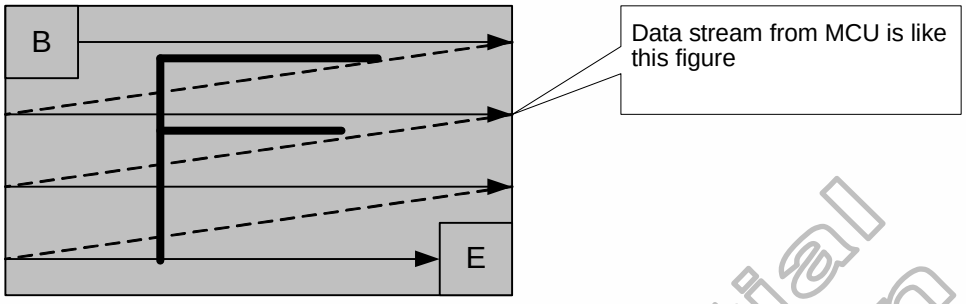


**Figure 5.1: Image data sending order from host**

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by MADTCL's MV(B5), MX(B6) and MY(B7) bits setting

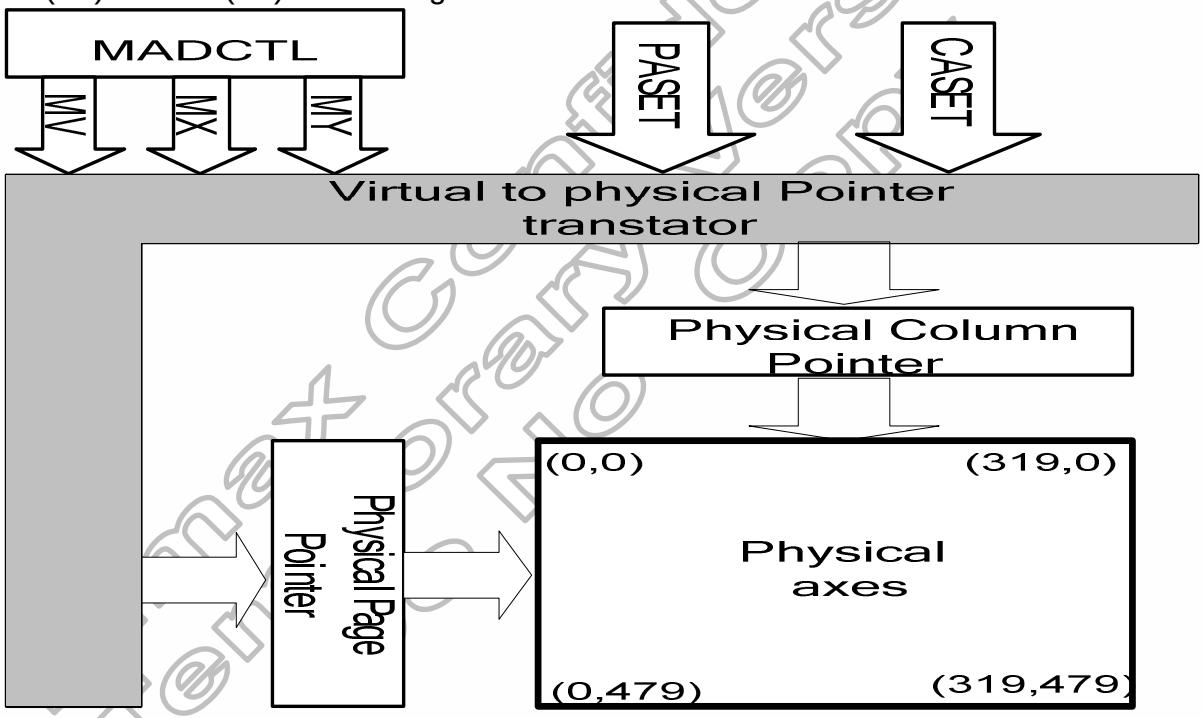


**Figure 5.2: MY,MX,MV Setting of GRAM control**

| MV | MX | MY | CASET | PASET |
|---|---|---|---|---|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Page Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (479-Physical Page Pointer) |
| 0 | 1 | 0 | Direct to (319-Physical Column Pointer) | Direct to Physical Page Pointer |
| 0 | 1 | 1 | Direct to (319-Physical Column Pointer) | Direct to (479-Physical Page Pointer) |
| 1 | 0 | 0 | Direct to Physical Page Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (479-Physical Page Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Page Pointer | Direct to (319-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (479-Physical Page Pointer) | Direct to (319-Physical Column Pointer) |

**Table 5.2: MY.MX.MV Setting of GRAM address mapping**

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The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

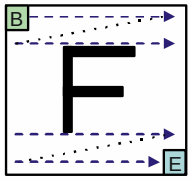
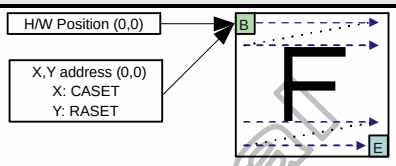
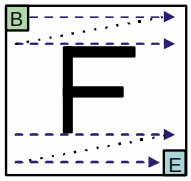
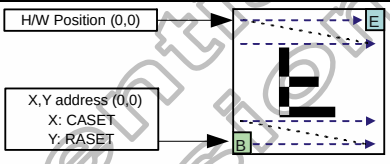
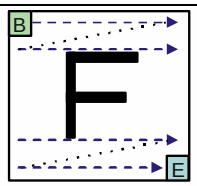
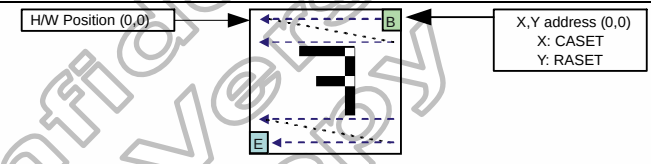
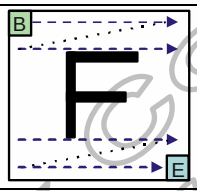
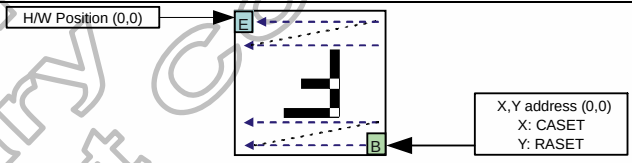
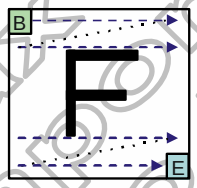
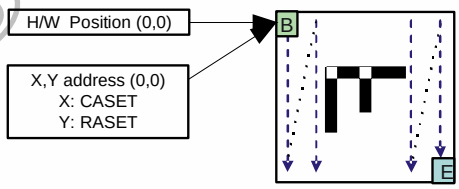
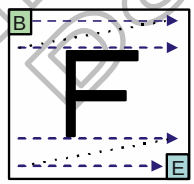
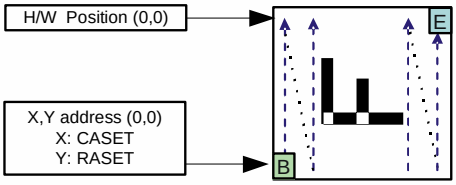
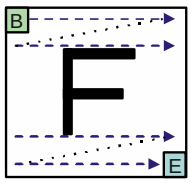
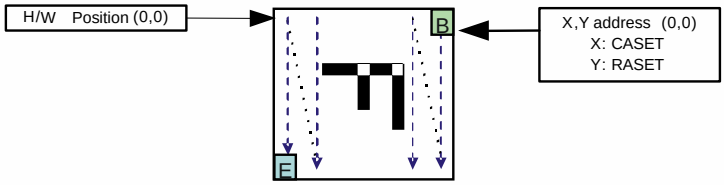
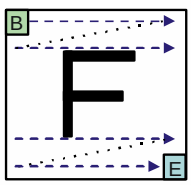
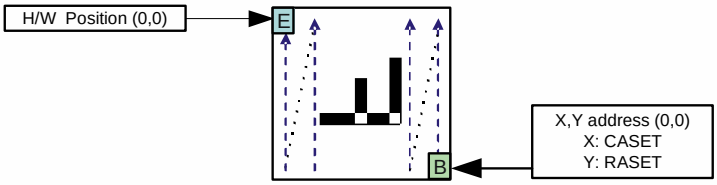
| Display Data Direction | MADCTR parameter MV | MX | MY | Image in the Host | Image in the Driver (GRAM) |
|---|---|---|---|---|---|
| Normal | 0 | 0 | 0 |  |  |
| Y-Invert | 0 | 0 | 1 |  |  |
| X-Invert | 0 | 1 | 0 |  |  |
| X-Invert Y-Invert | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange X-invert | 1 | 0 | 1 |  |  |
| X-Y Exchange Y-invert | 1 | 1 | 0 |  |  |
| X-Y Exchange X-invert Y-invert | 1 | 1 | 1 |  |  |

**Table 5.3: Address direction settings**

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### 5.1.3 Source, Gate and Memory Map


| Source Out | | S1 | S2 | S3 | S4 | S5 | S6 | | S955 | S956 | S957 | S958 | S959 | S960 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | RGB Order<br>—— :BGR=0<br>----- :BGR=1 | | | | | | | SA | |
| MY=0 | MY=1 | | | | | | | | | | | | | | ML=0 | ML=1 |
| 0 | 479 | R0 5-0 | G0 5-0 | B0 5-0 | R1 5-0 | G1 5-0 | B1 5-0 | – | R318 5-0 | G318 5-0 | B318 5-0 | R319 5-0 | G319 5-0 | B319 5-0 | 0 | 479 |
| 1 | 478 | | | | | | | – | | | | | | | 1 | 478 |
| 2 | 477 | | | | | | | – | | | | | | | 2 | 477 |
| 3 | 476 | | | | | | | – | | | | | | | 3 | 476 |
| 4 | 475 | | | | | | | – | | | | | | | 4 | 475 |
| 5 | 474 | | | | | | | – | | | | | | | 5 | 474 |
| 6 | 473 | | | | | | | – | | | | | | | 6 | 473 |
| 7 | 472 | | | | | | | – | | | | | | | 7 | 472 |
| 8 | 471 | | | | | | | – | | | | | | | 8 | 471 |
| 9 | 470 | | | | | | | – | | | | | | | 9 | 470 |
| 10 | 469 | | | | | | | – | | | | | | | 10 | 469 |
| 11 | 468 | | | | | | | – | | | | | | | 11 | 468 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : |
| 472 | 7 | | | | | | | – | | | | | | | 472 | 7 |
| 473 | 6 | | | | | | | – | | | | | | | 473 | 6 |
| 474 | 5 | | | | | | | – | | | | | | | 474 | 5 |
| 475 | 4 | | | | | | | – | | | | | | | 475 | 4 |
| 476 | 3 | | | | | | | – | | | | | | | 476 | 3 |
| 477 | 2 | | | | | | | – | | | | | | | 477 | 2 |
| 478 | 1 | | | | | | | – | | | | | | | 478 | 1 |
| 479 | 0 | | | | | | | – | | | | RN 5-0 | GN 5-0 | BN 5-0 | 479 | 0 |
| CA | MX=0 | 0 | | | 1 | | | | 318 | | | 319 | | | | |
| | MX=1 | 319 | | | 318 | | | | 1 | | | 0 | | | | |

Display Pattern Data
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**Note: RA** = Row Address.
**CA** = Column Address.
**SA** = Scan Address.
**MX** = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control (R36h) command
**MY** = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control (R36h) command
**ML** = Scan direction parameter, D4 parameter of Memory Access Control (R36h) command
**BGR** = Red, Green and Blue pixel position change, D3 parameter of Memory Access Control (R36h) command

**Figure 5.3: Memory Map 320RGBx480 dot**


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### 5.1.4 Fully Display, Partial Display, Vertical Scrolling Display

#### 5.1.4.1 Full Display

Example: (1) 320RGBx480 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x13Fh (R2Ah) and SP=0x000h, EP=0x1DFh (R2Bh), ML=0.

| GRAM | 00h<br>DB---DB<br>17 --- 0 | 01h<br>DB---DB<br>17 --- 0 | --------- | 13Eh<br>DB---DB<br>17 --- 0 | 13Fh<br>DB---DB<br>17 --- 0 |
|---|---|---|---|---|---|
| 000h | 000000H | 000001H | --------- | 00013EH | 00013FH |
| 001h | 001000H | 001001H | --------- | 00113EH | 00113FH |
| 002h | 002000H | 002001H | --------- | 00213EH | 00213FH |
| 003h | 003000H | 003001H | --------- | 00313EH | 00313FH |
| 004h | 004000H | 004001H | --------- | 00413EH | 00413FH |
| 005h | 005000H | 005001H | --------- | 00513EH | 00513FH |
| ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ |
| 1DAh | 1DA000H | 1DA001H | --------- | 1DA13EH | 1DA13FH |
| 1DBh | 1DB000H | 1DB001H | --------- | 1DB13EH | 1DB13FH |
| 1DCh | 1DC000H | 1DC001H | --------- | 1DC13EH | 1DC13FH |
| 1DDh | 1DD000H | 1DD001H | --------- | 1DD13EH | 1DD13FH |
| 1DEh | 1DE000H | 1DE001H | --------- | 1DE13EH | 1DE13FH |
| 1DFh | 1DF000H | 1DF001H | --------- | 1DF13EH | 1DF13FH |

**Table 5.4: Memory map of full display**

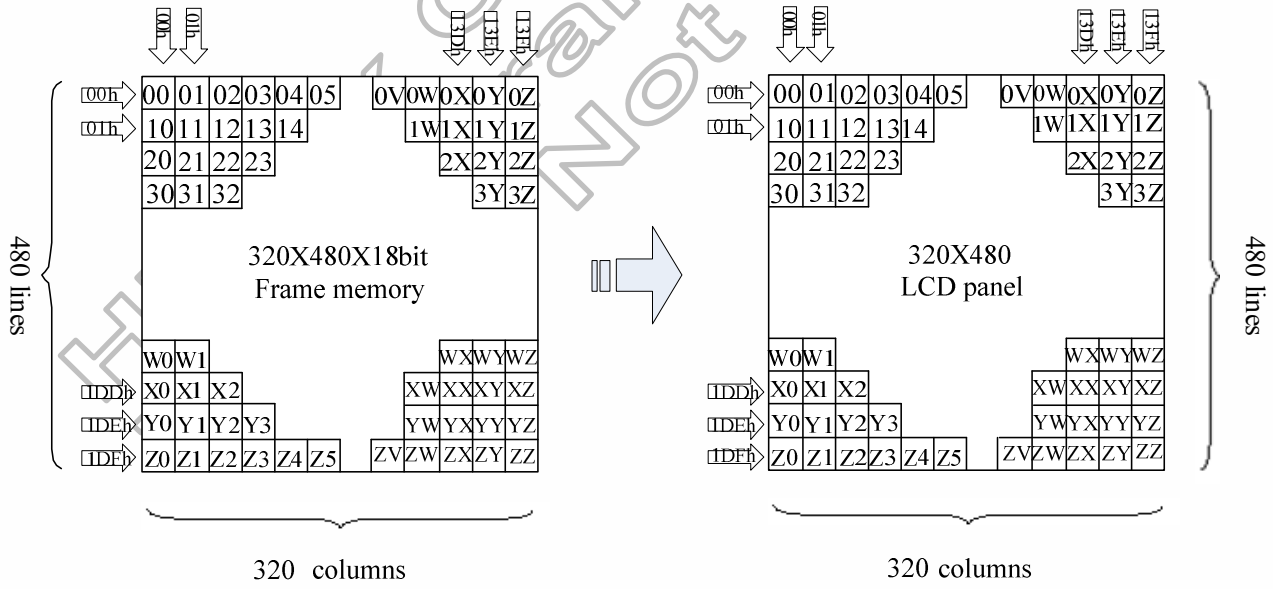


**Figure 5.4: Memory map of full display**

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### 5.1.4.2 Partial Display

Example: (1) 320RGBx480 dot display mode.
(2) PLTON instruction (R12h).
(3) SR[15:0]=0002h, ER[15:0]=01DBh, ML=0.

| LCD panel S/G pins | Pixel 1 | Pixel 2 | --------- | Pixel319 | Pixel320 |
|---|---|---|---|---|---|
| G1 | 00000 0H | 00000 1H | --------- | 00013 EH | 00013 FH |
| G2 | 00100 0H | 00100 1H | --------- | 00113 EH | 00113 FH |
| G3 | 00200 0H | 00200 1H | --------- | 00213 EH | 00213 FH |
| G4 | 00300 0H | 00300 1H | --------- | 00313 EH | 00313 FH |
| G5 | 00400 0H | 00400 1H | --------- | 00413 EH | 00413 FH |
| G6 | 00500 0H | 00500 1H | --------- | 00513 EH | 00513 FH |
| ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ |
| G475 | 1DA00 0H | 1DA00 1H | --------- | 1DA13 EH | 1DA13 FH |
| G476 | 1DB00 0H | 1DB00 1H | --------- | 1DB13 EH | 1DB13 FH |
| G477 | 1DC0 00H | 1DC0 01H | --------- | 1DC1 3EH | 1DC1 3FH |
| G478 | 1DD0 00H | 1DD0 01H | --------- | 1DD1 3EH | 1DD1 3FH |
| G479 | 1DE00 0H | 1DE00 1H | --------- | 1DE13 EH | 1DE13 FH |

**Table 5.5: Memory map of partial display**

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### 5.1.4.3 Vertical Scrolling Display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

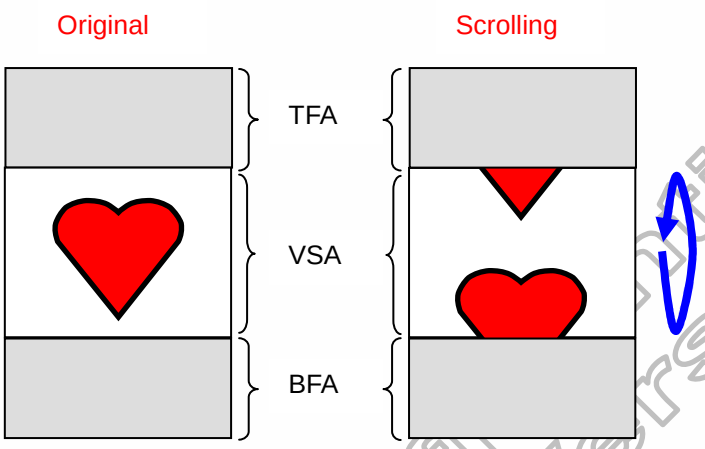


**Figure 5.5: Vertical scrolling**

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

Example 1 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=478,BFA=0 when MADCTL B4=0
(3) VSCRSADD=03h

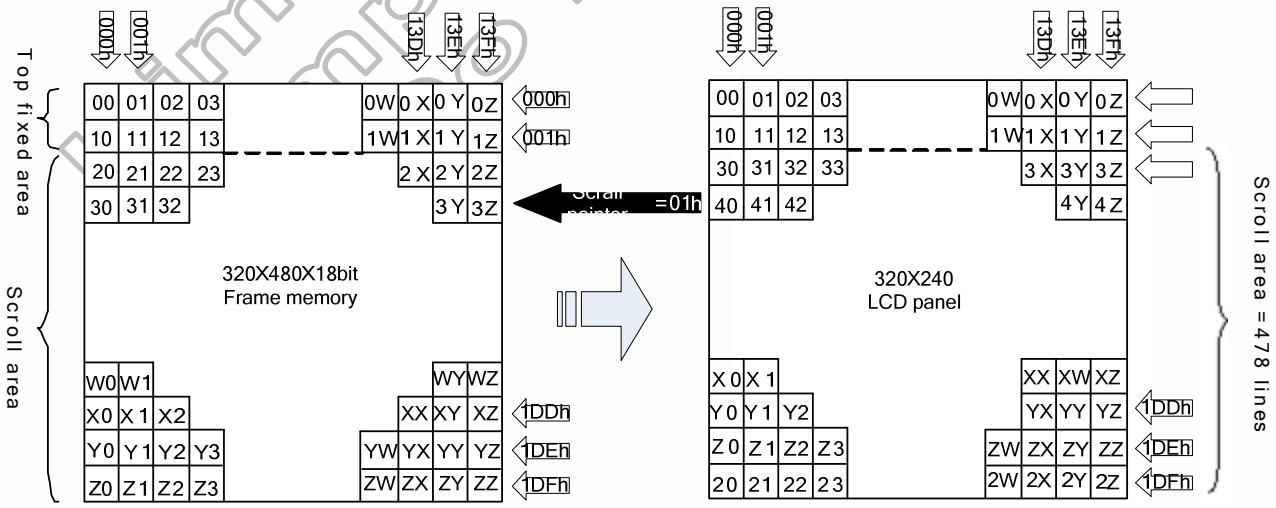


**Figure 5.6: Memory map of vertical scrolling example 1**

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Example 2 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=476,BFA=2 when MADCTL B4=0
(3) VSCRSADD=03h

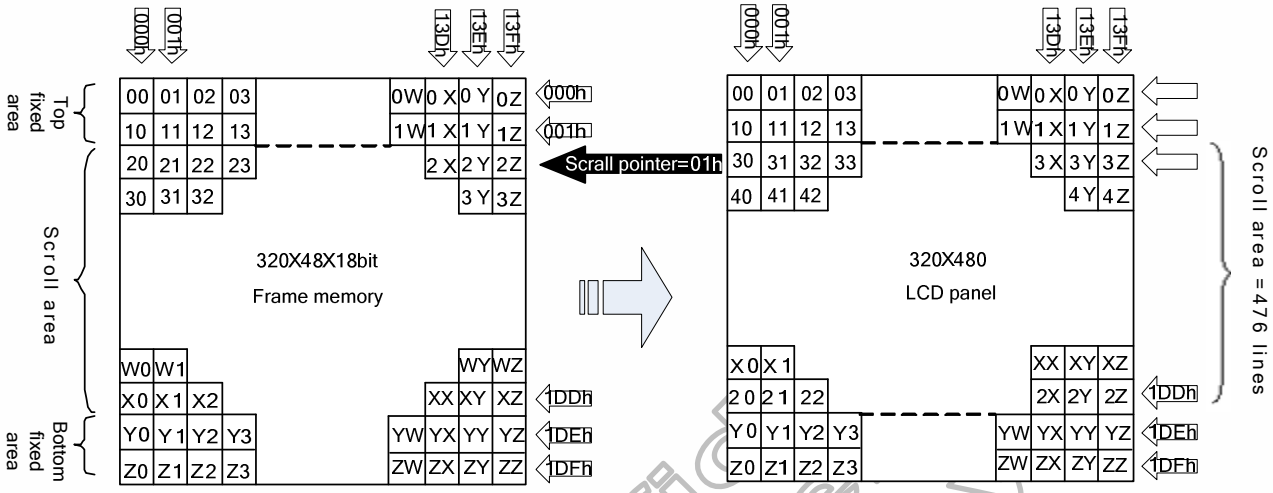


**Figure 5.7: Memory map of vertical scrolling example 2**

Example 3 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=476,BFA=2 when MADCTL B4=0
(3) VSCRSADD=04h

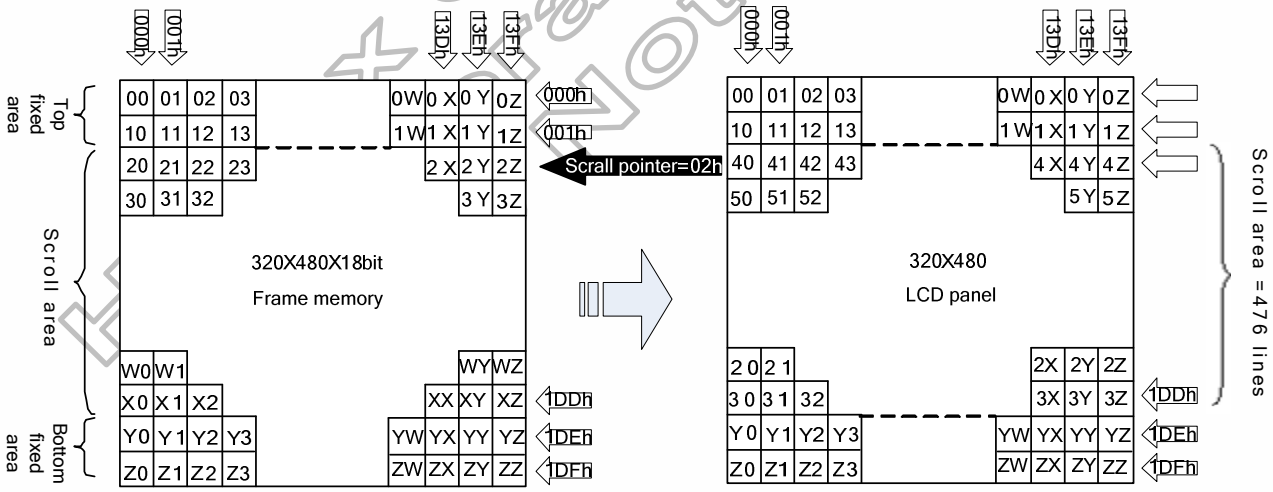


**Figure 5.8: Memory map of vertical scrolling example 3**

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**Vertical Scroll Example**

There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA ≠ Panel scan lines
N/A. Do not set TFA + VSA + BFA≠Panel scan lines. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA = Panel scan lines ( Scrolling)

Example 1 : (1) 320RGBx480 dot display mode.
(2) When TFA=0, VSA=480, BFA=0 and VSCRSADD=40. MADCTL parameter B4="0"

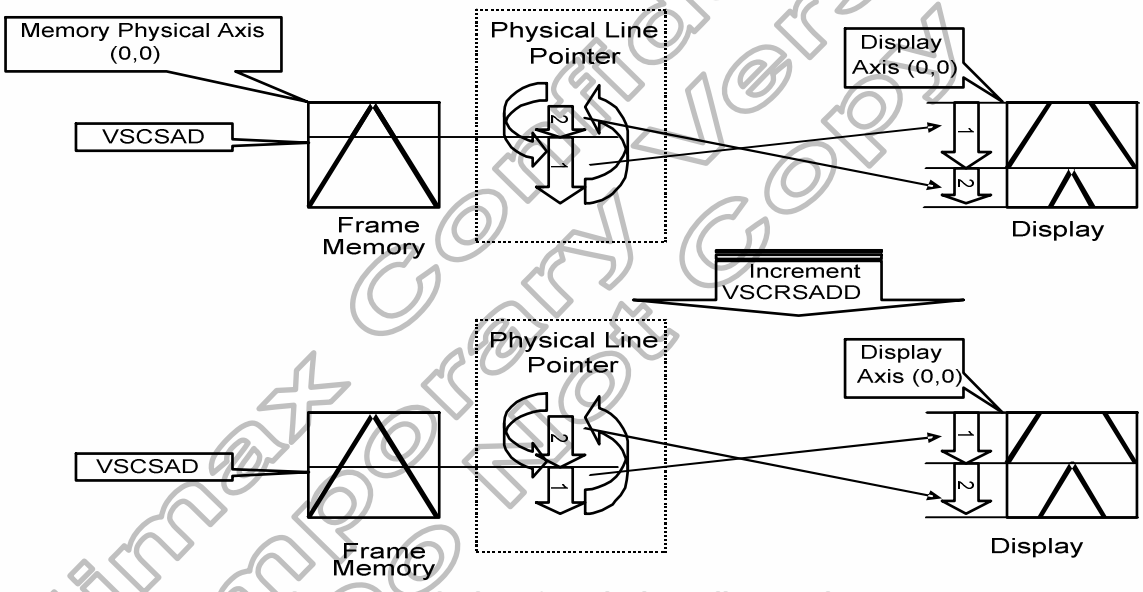


**Figure 5.9: Display of Vertical Scroll Example 1**

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Example 2 : (1) 320RGBx480 dot display mode.
(2) TFA=60, VSA=420, BFA=0 and VSCRSADD =160. MADCTRL parameter B4=”1”

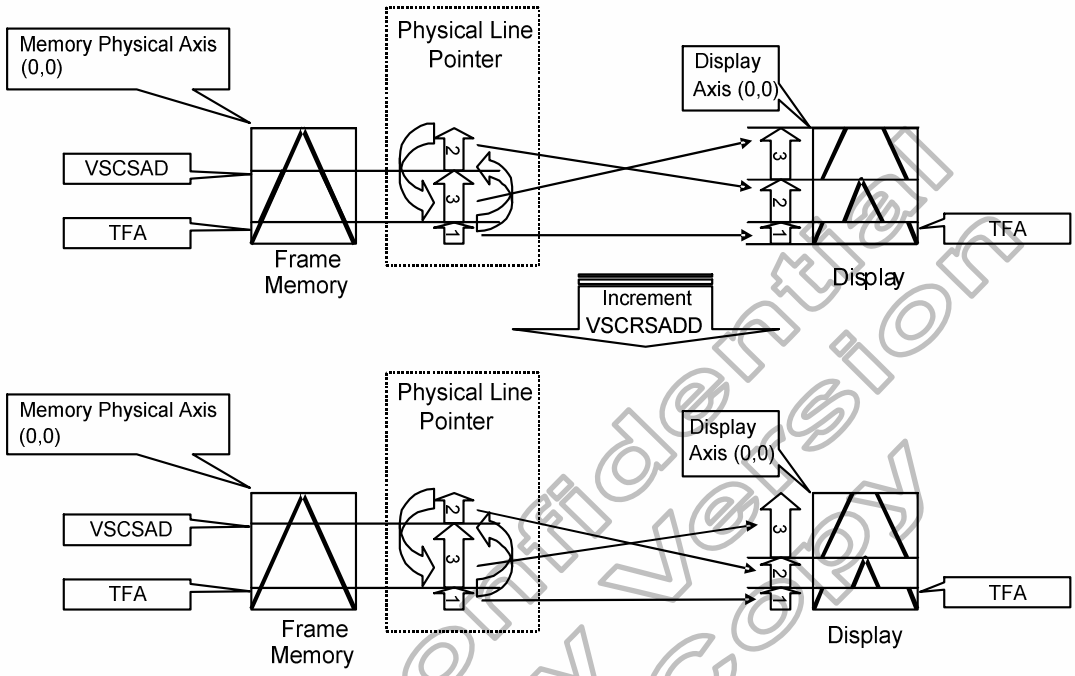


**Figure 5.10: Display of Vertical Scroll Example 2**

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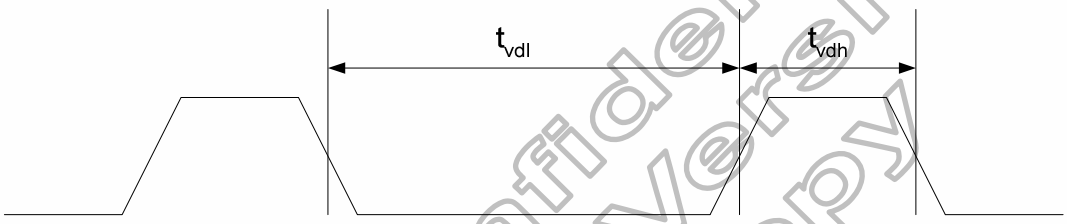
## 5.2 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

### 5.2.1 Tearing effect line modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:




$t_{vdh}$= The LCD display is not updated from the Frame Memory
$t_{vdl}$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Figure 5.11: TE mode 1 output**

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.
Ex:
1. TESL[15:0]=0, then TE signal will output after last Line finished.
2. TESL[15:0]=2, then TE signal will output at second Line start.

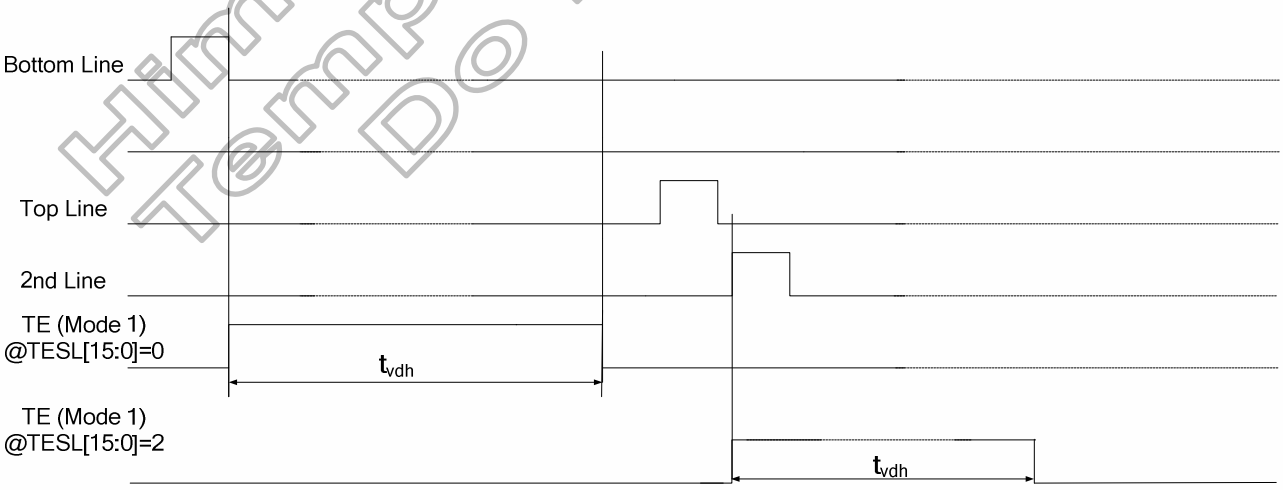



**Figure 5.12: TE delay output**

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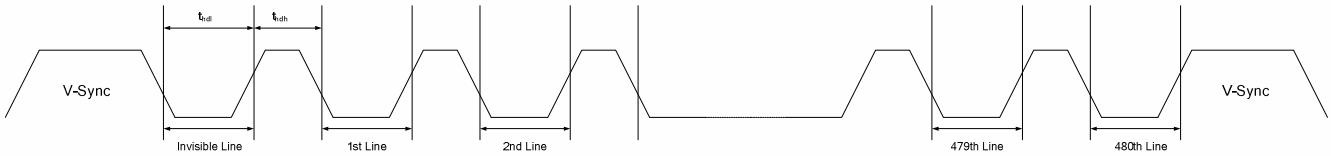
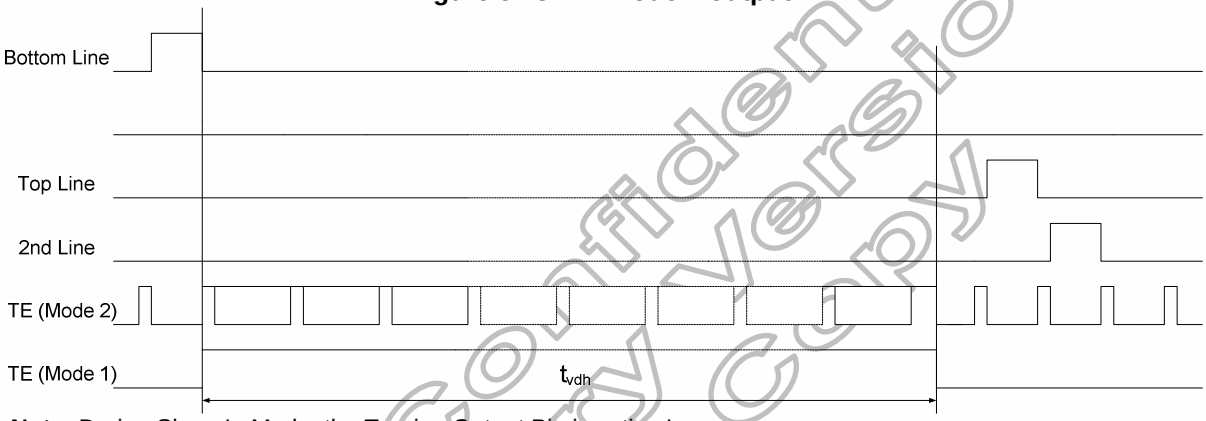
**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.




$t_{hdh}$= The LCD display is not updated from the Frame Memory
$t_{hdl}$= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

**Figure 5.13: TE mode 2 output**




**Note:** During Sleep In Mode, the Tearing Output Pin is active Low

**Figure 5.14: TE output waveform**

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### 5.2.2 Tearing effect line timing

The Tearing Effect signal is described below.

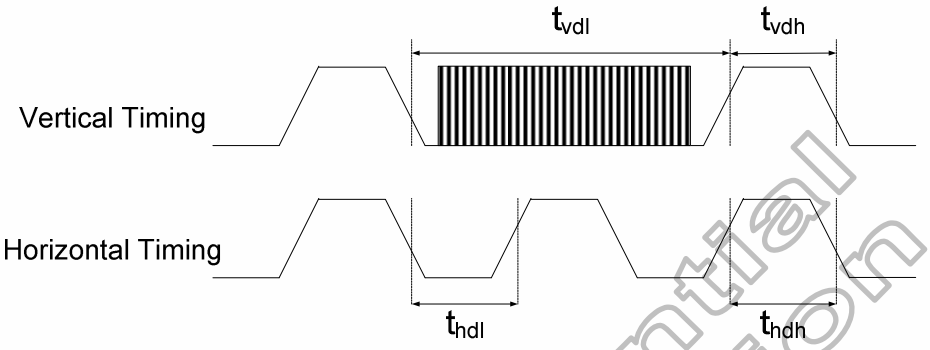


**Figure 5.15: Waveform of tearing effect signal**

Idle Mode Off (Frame Rate = 60 Hz)

| Symbol | Parameter | Spec. | | | Unit | Description |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| tvdl | Vertical Timing Low Duration | TBD | | - | ms | - |
| tvdh | Vertical Timing High Duration | 1000 | | - | µs | - |
| thdl | Horizontal Timing Low Duration | TBD | | - | µs | - |
| thdh | Horizontal Timing High Duration | TBD | | 500 | µs | - |

**Table 5.6: AC characteristics of tearing effect signal**

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

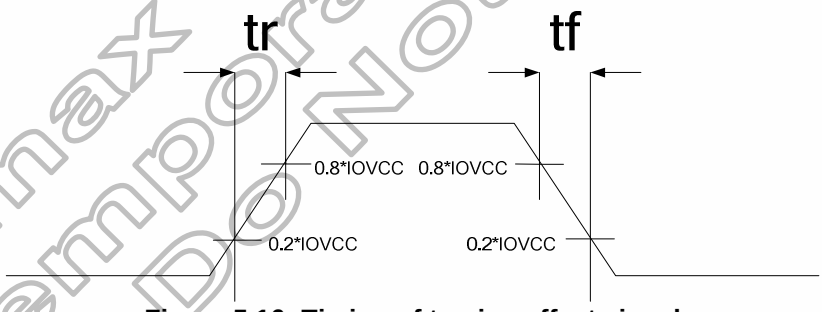


**Figure 5.16: Timing of tearing effect signal**

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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### 5.2.3 Example 1: MPU write is faster than panel read

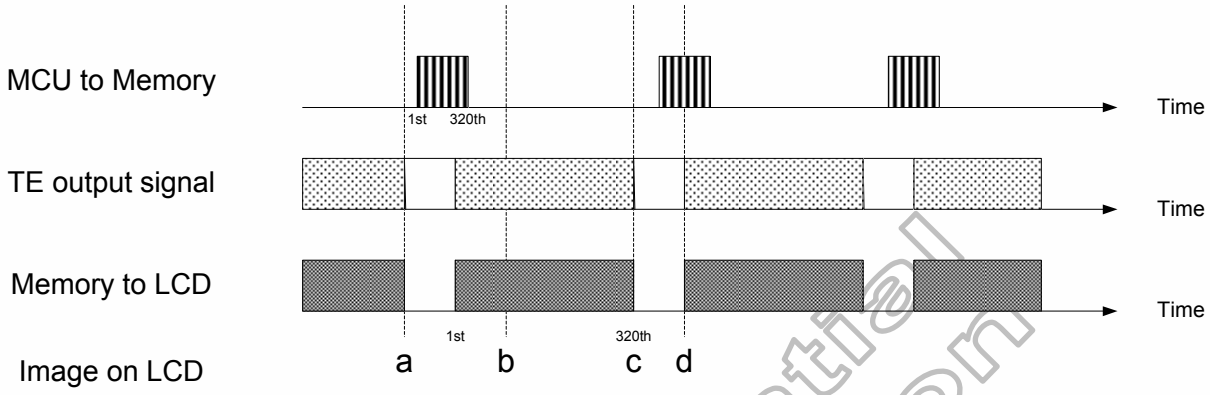


**Figure 5.17: Timing of MPU write is faster than panel read**

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

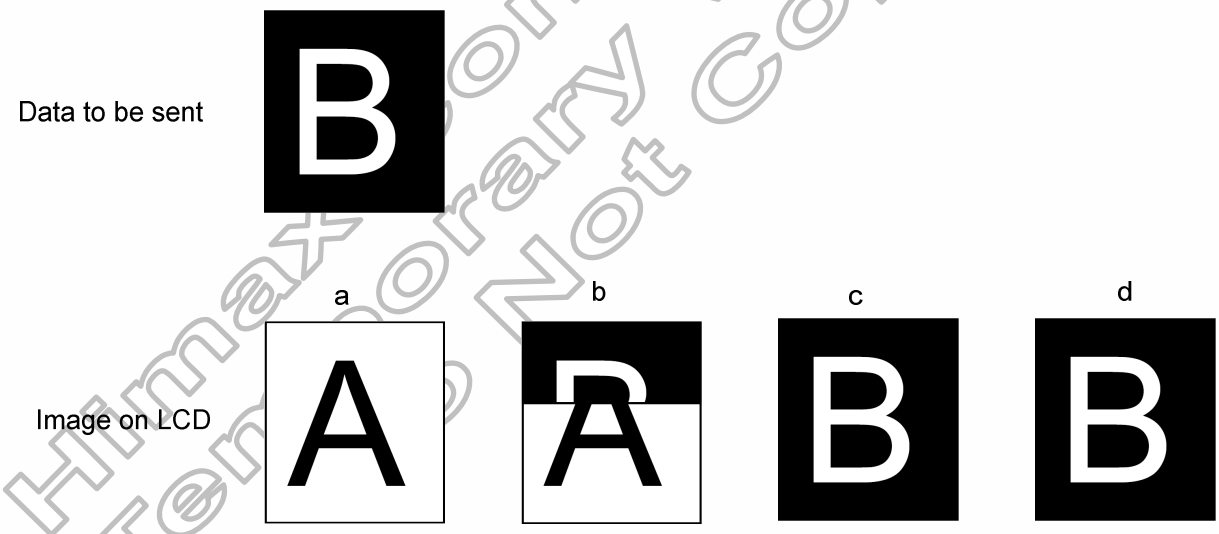


**Figure 5.18: Display of MPU write is faster than panel read**

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### 5.2.4 Example 2: MPU write is slower than panel read

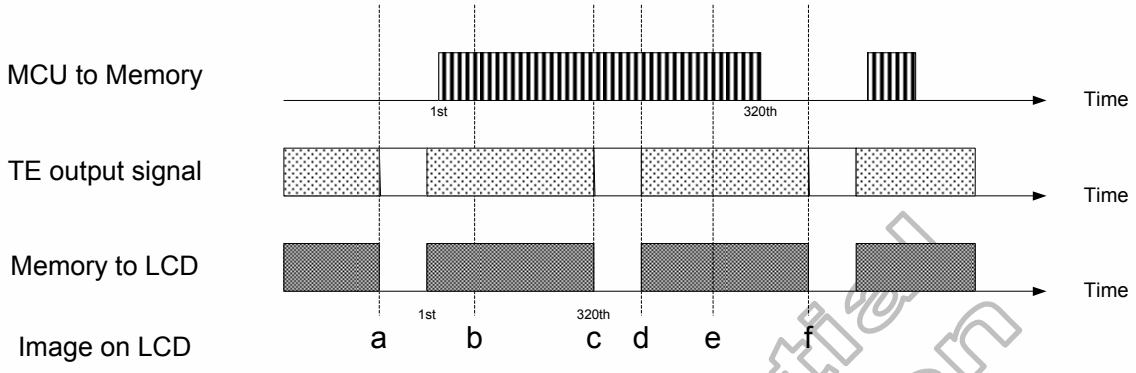


**Figure 5.19: Timing of MPU write is slower than panel read**

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

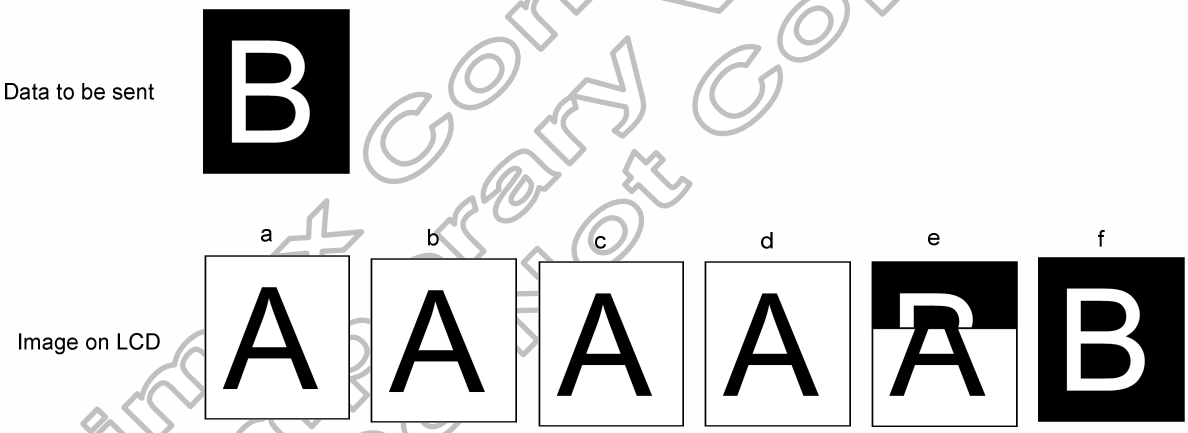


**Figure 5.20: Display of MPU write is slower than panel read**

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## 5.3Checksums

The display module consists of two 8-bit checksum registers, which are used checksum calculations for area registers (includes the frame memory), on the display module. Command area registers are registers which values users can change a command directly.

One of the checksum registers is “First Checksum” (FCS) and another is “Continue Checksum” (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on command area registers. This means that read commands are not used as a calculation starting trigger in this case.
The checksum calculation is always interrupted, when there is a new write access on command area registers.
The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on area registers and the new checksum value is calculated in the first time again.
The maximum time, when the FCS is readable, is 150ms after there is the last write access on area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last command area register has been calculated to the checksum.
The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on command area registers.

There is always updated a checksum comparison bit (See section: “Read Display Self-Diagnostic Result (0Fh)” and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

Users can read FCS, CCS and Comparison bit D0 values. See section: “Read First Checksum (AAh)”, “Read Continue Checksum (AFh)” and ”Read Display Self-Diagnostic Result (0Fh)”.
There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in “Sleep Out” mode and it is stopped in “Sleep In” mode.

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| Step Note 1 | Time Note 2 | Action | Temporary Register | First Checksum Register (FCS) | Continue Checksum Register (CCS) | Comment |
|---|---|---|---|---|---|---|
| 1 | 0 | Initialization | Set to 00h | Set to 00h | Set to 00h | The last write action on area registers => FCS and CCS registers are initialized. |
| 2 | 0 – 150ms | Counting Sum of command Area Registers | Counting | - | - | The first register counting is running |
| 3 | 150ms | Stores Sum of Registers on FCS Register | Set to 00h after Value is Moved to FCS Register | Stores Sum of Area Registers on FCS Register | - | The result of the first register counting is stored on the FCS register. The result of the FCS is available to the MCU. |
| 4 | 150 – 300ms | Counting Sum of command Area Registers | Counting | - | - | The second register counting is running |
| 5 | 300ms | 1) Stores Sum of Registers on CCS Register<br>2) Compares Stored FCS and CCS Values | Set to 00h after Value is Moved to CCS Register | - | Stores Sum of command Area Registers on CCS Register | The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MCU. |
| 6 | 300 – 450ms | Counting Sum of command Area Registers | Counting | - | - | The third register counting is running |
| 7 | 450ms | 1) Stores Sum of Registers on CCS Register<br>2) Compares Stored FCS and CCS Values | Set to 00h after Value is Moved to CCS Register | - | Stores Sum of command Area Registers on CCS Register | The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU. |
| 8 | 450 – 600ms | Counting Sum of command Area Registers | Counting | - | - | The fourth register counting is running |
| 9 | 600ms | 1) Stores Sum of Registers on CCS Register<br>2) Compares Stored FCS and CCS Values | Set to 00h after Value is Moved to CCS Register | - | Stores Sum of command Area Registers on CCS Register | The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU. |
| 10 | etc | - | - | - | - | Same Sequence Countinue e.g. steps 4 and 5 |

**Notes:**

1. This function is restarted at Step 1 if there is any write action on command area registers.
2. These time can be shorter on the display module.

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## 5.4 Oscillator

The HX8357-C can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, it can be adjusted by the **UADJ [3:0]** bits for initial 10MHz internal clock generation. With other dividers setting, the 10MHz internal clock can be used to generate clock for other part of the chip using.

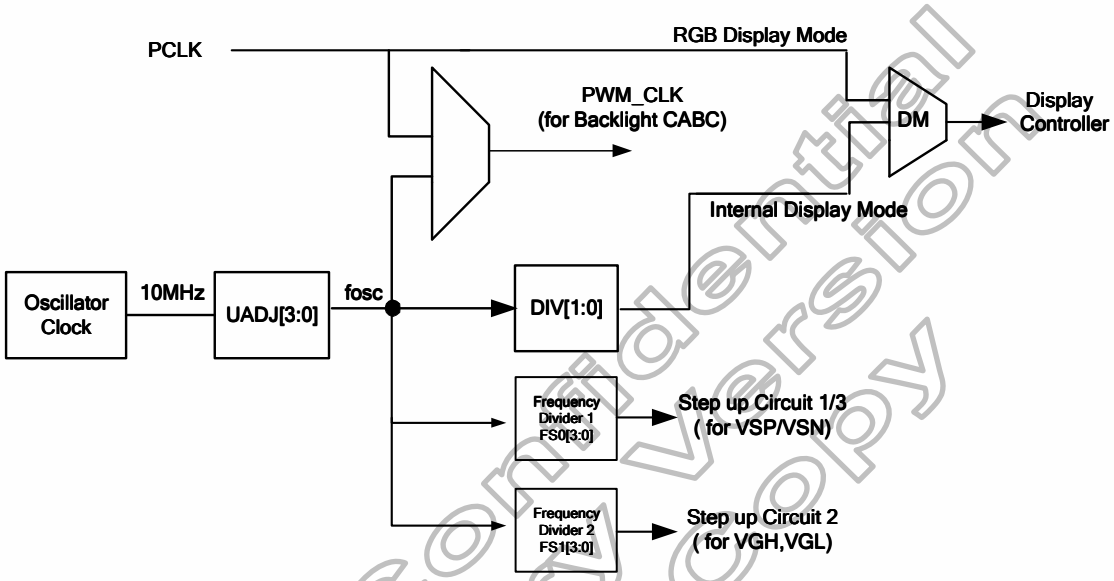


**Figure 5.21: HX8357-C internal clock circuit**

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## 5.5 Source driver

The HX8357-C contains a 481 channels of source driver (normal S1~S480; Zig-zag S1~S481) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 481 channels and generates corresponding gray scale voltage output, which can realize a 262k colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

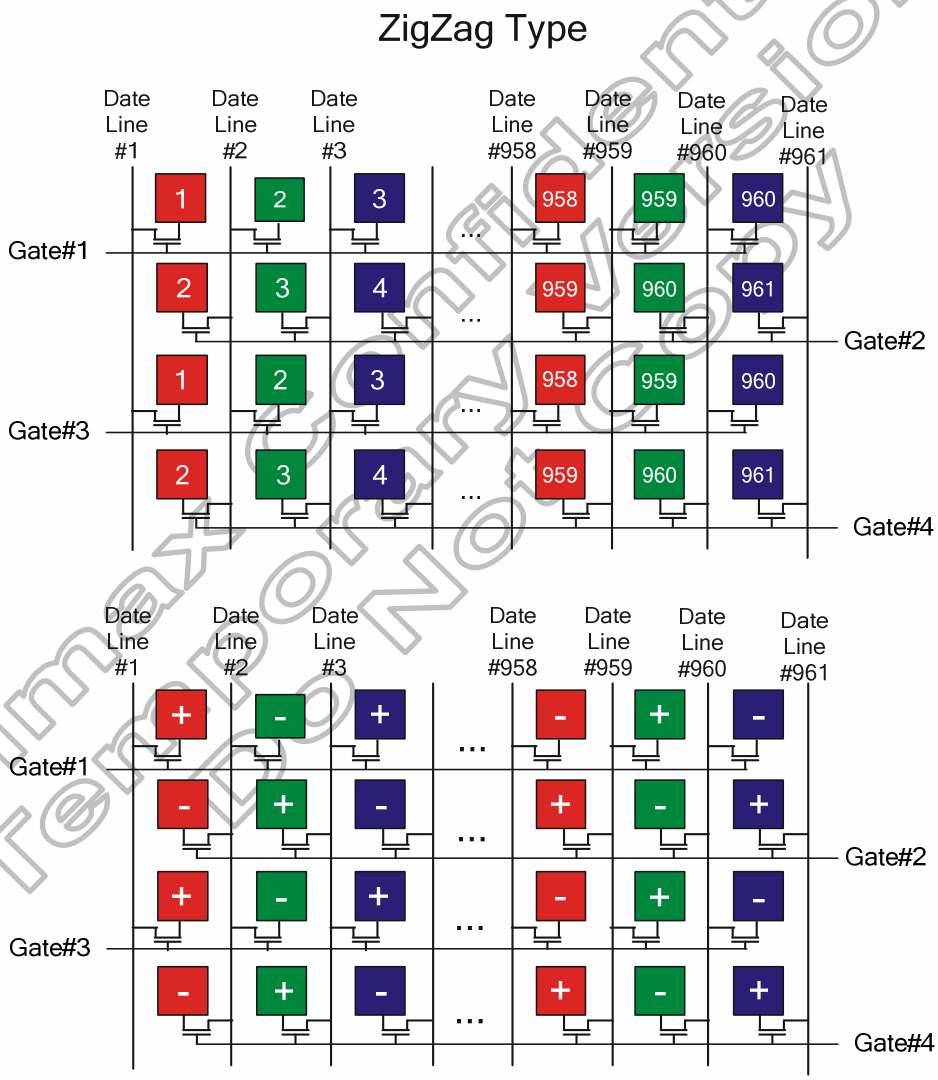


**Figure 5.22: Source channels of ZigZag inversion mode**

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## 5.6 Gate driver

The HX8357-C contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH in scan line, the other lines is VGL.

HX8357-C can set internal register SM_PANEL and GS_PANEL bit to determine the pin assignment of gate. The SM_PANEL and GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8357-C.

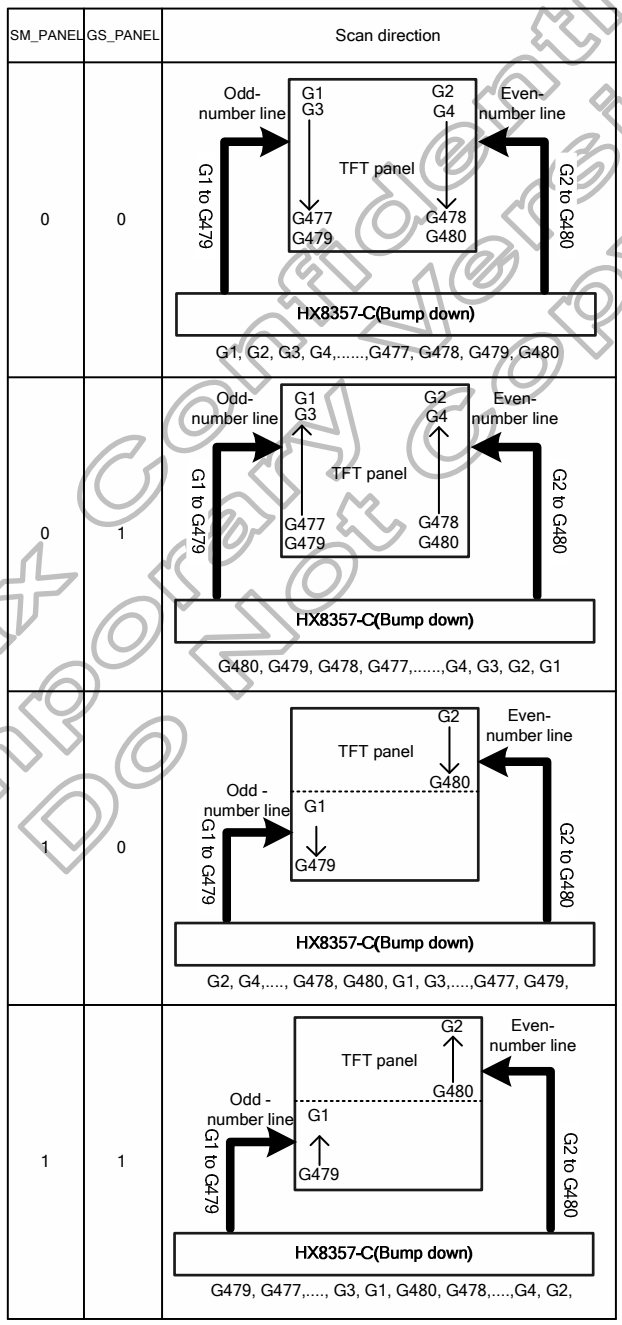


**Figure 5.23: Scan direction of Gate Driver**

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## 5.7 LCD power generation circuit

### 5.7.1 Power supply circuit

The power circuit of HX8357-C is used to generate supply voltages for LCD panel driving.

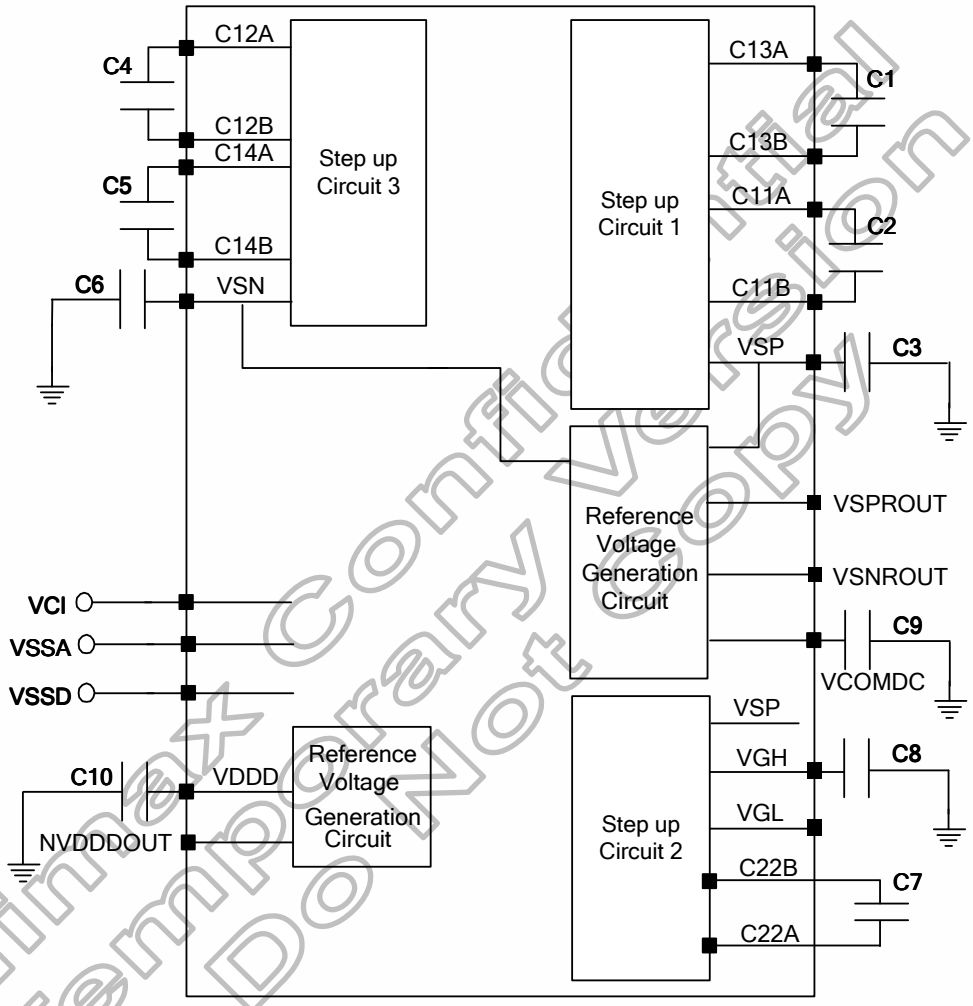


**Figure 5.24: Block diagram of HX8357-C power circuit**

### Specification of connected passive component

| Capacitor | Recommended voltage | Capacity |
|---|---|---|
| C1 (C13A/B) | 10V | 1 µF (B characteristics) |
| C2 (C11A/B) | 10V | 1 µF (B characteristics) |
| C3 (VSP) | 10V | 1 µF ~ 2.2uF (B characteristics) |
| C4 (C14A/B) | 10V | 1 µF (B characteristics) |
| C5 (C12A/B) | 10V | 1 µF (B characteristics) |
| C6 (VSN) | 10V | 1 µF~2.2uF (B characteristics) |
| C7 (C22A/B) | 16V | 1 µF (B characteristics) |
| C8 (VGH) | 25V | 1 µF (B characteristics) |
| C9 (VCOMDC) | 6V | 1 µF (B characteristics) |
| C10 (VDDD) | 6V | 1 µF (B characteristics) |

**Table 5.7 Adoptability of capacitor**

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### 5.7.2 LCD power generation scheme

The boost voltage generated is shown as below.

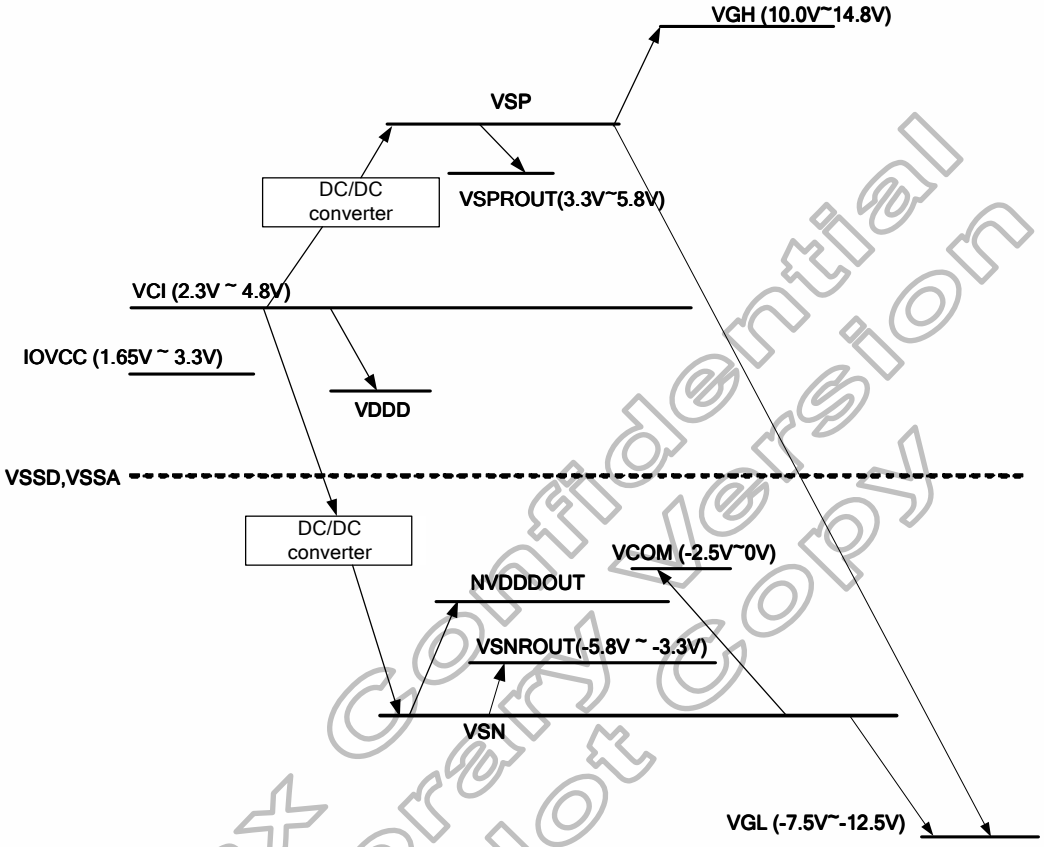


**Figure 5.25: LCD power generation scheme**

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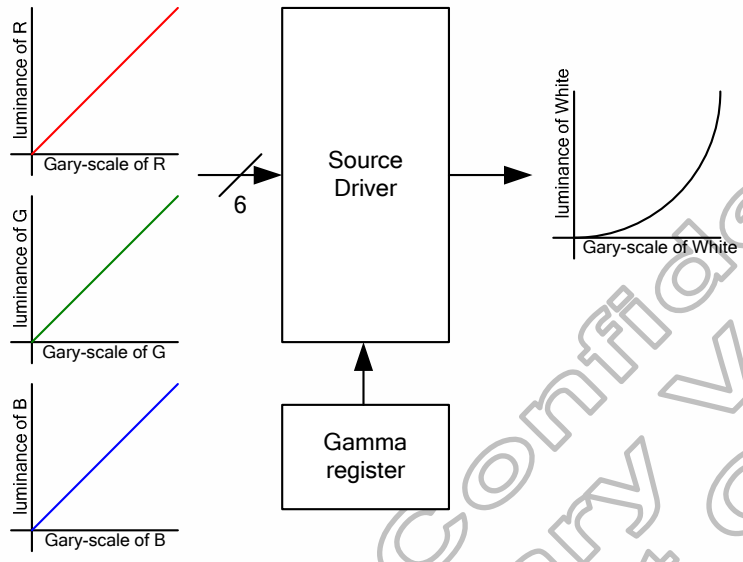
## 5.8 Gamma characteristic correction function

The HX8357-C offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver




B) Gamma adjustment of Digital Gamma Correction

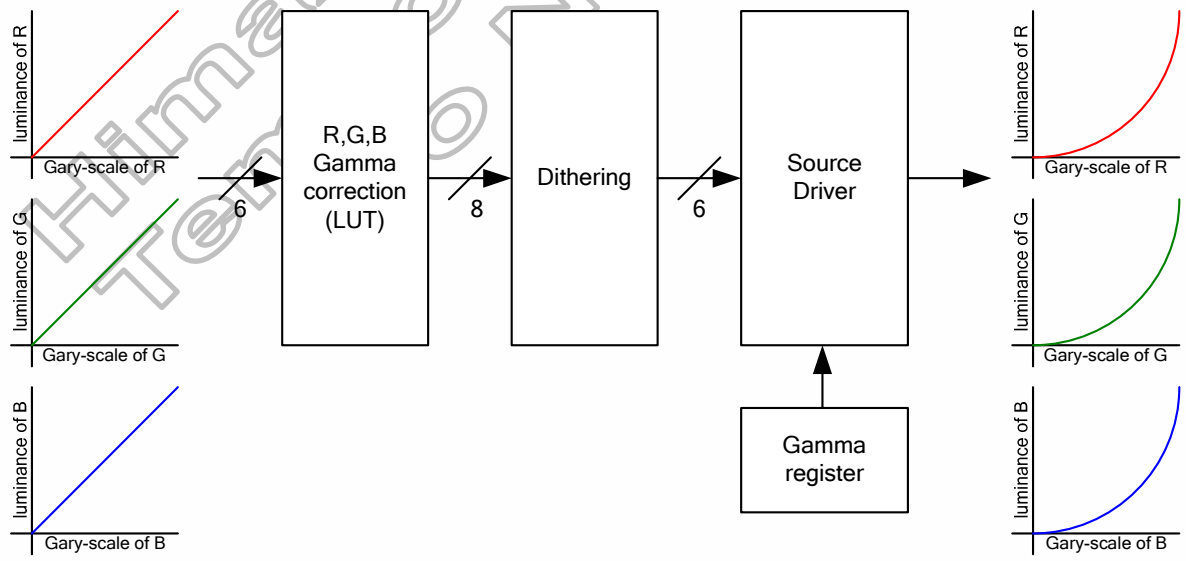



**Figure 5.26: Gamma adjustments different of source driver with digital gamma correction**

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### 5.8.1 Gamma characteristic correction function

The HX8357-C incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment operation is implemented by deciding the 16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

**Gamma resister stream**

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including 16 gamma reference voltages. VgP/N (0, 1, 2, 4, 6, 13, 20, 27, 36, 43, 50, 57, 59, 61, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

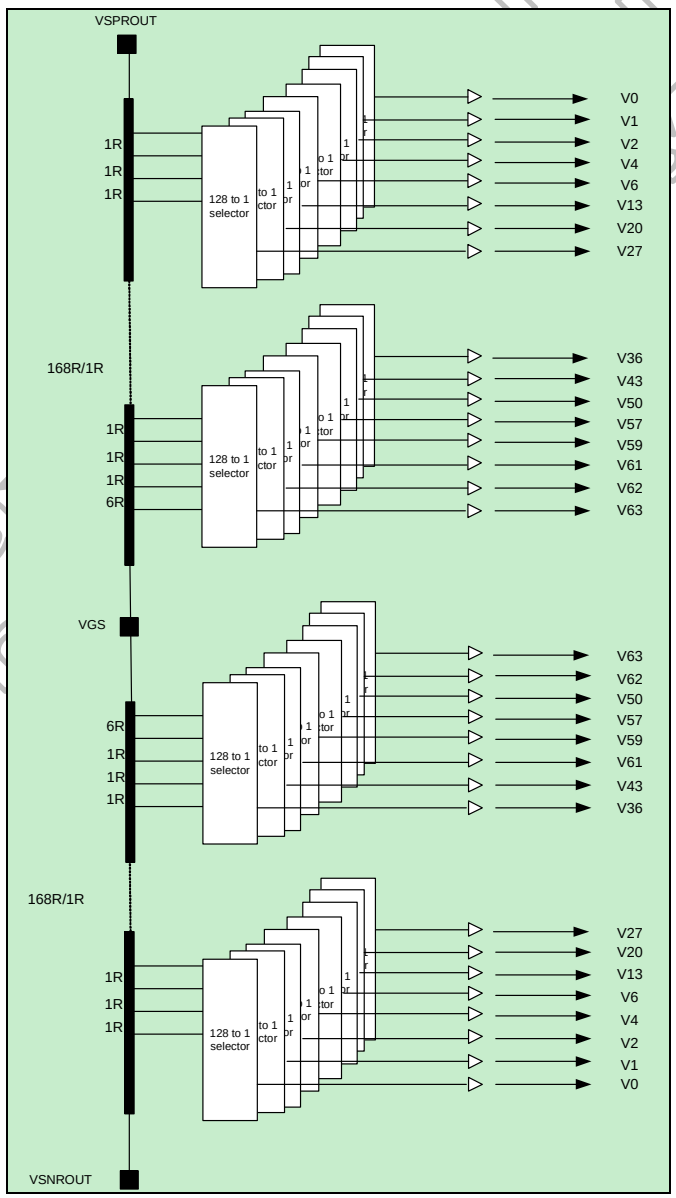


**Figure 5.27: Gamma resister stream and gamma reference voltage**


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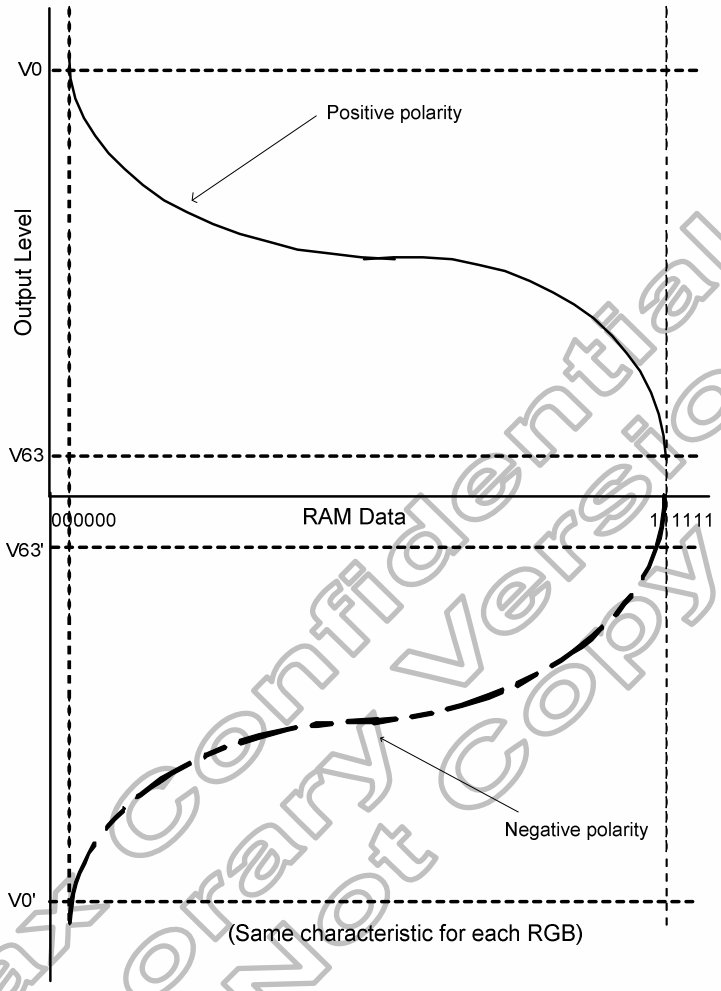


**Figure 5.28: Relationship between GRAM data and output level (normal white panel REV_Panel="0")**

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### Four-characteristic gamma curve selection

There are four kinds of Gamma Curve which can be selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

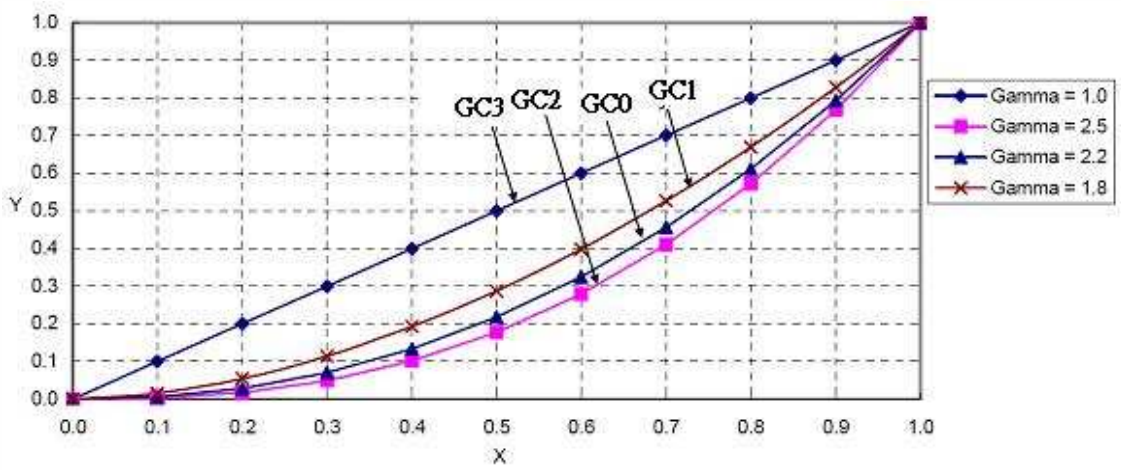


**Figure 5.29: Gamma curve according to GC0 to GC3 bit**

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### 5.8.2 Gray voltage generator for digital gamma correction

The HX8357-C digital gamma correction can reach the independent GAMMA curve of RGB. HX8357-C utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

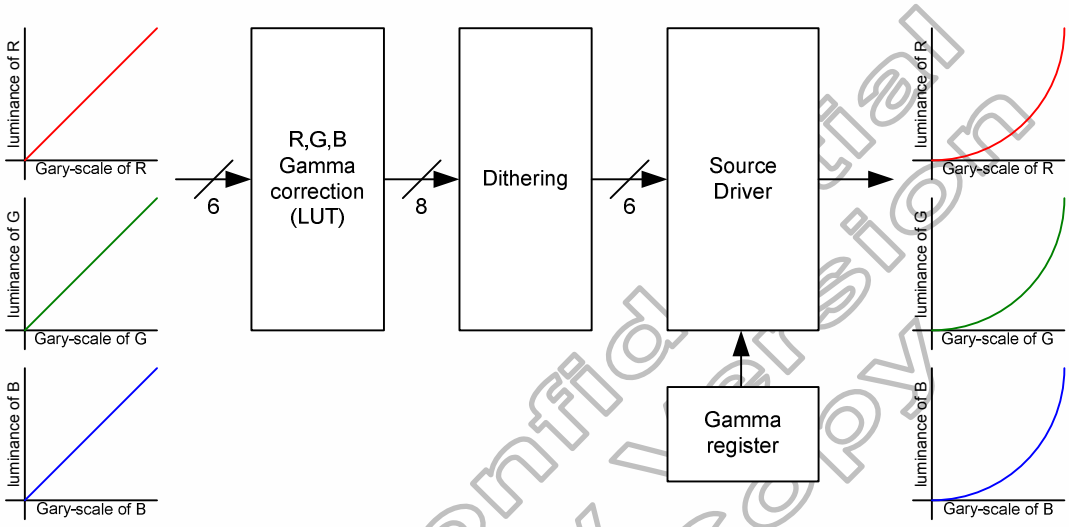


**Figure 5.30: Block diagram of digital gamma correction**

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V2, V4, ...., V60, V62, V63 voltage to the LUT register setting gray level voltage. V(2N+1) = (V(2N) + V(2N+2))/2 (N=0~30).

| Parameter | Input (6 bit) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Gray Mapping |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1st | R00h | R007 | R006 | R005 | R004 | R003 | R002 | R001 | R000 | 00h | R_V0 |
| 2nd | R02h | R017 | R016 | R015 | R014 | R013 | R012 | R011 | R010 | 08h | R_V2 |
| 3rd | R04h | R027 | R026 | R025 | R024 | R023 | R022 | R021 | R020 | 10h | R_V4 |
| : | : | : | : | : | : | : | : | : | : | : | : |
| 32nd | R62h | R317 | R316 | R315 | R314 | R313 | R312 | R311 | R310 | F8h | R_V62 |
| 33rd | R63h | R327 | R326 | R325 | R324 | R323 | R322 | R321 | R320 | FCh | R_V63 |
| 34th | G00h | G007 | G006 | G005 | G004 | G003 | G002 | G001 | G000 | 00h | G_V0 |
| 35th | G02h | G017 | G016 | G015 | G014 | G013 | G012 | G011 | G010 | 08h | G_V2 |
| 36th | G04h | G027 | G026 | G025 | G024 | G023 | G022 | G021 | G020 | 10h | G_V4 |
| : | : | : | : | : | : | : | : | : | : | : | : |
| 65th | G62h | G317 | G316 | G315 | G314 | G313 | G312 | G311 | G310 | F8h | G_V62 |
| 66th | G63h | G327 | R326 | G325 | G324 | G323 | G322 | G321 | G320 | FCh | G_V63 |
| 67th | B00h | B007 | B006 | B005 | B004 | B003 | B002 | B001 | B000 | 00h | B_V0 |
| 68th | B02h | B017 | B016 | B015 | B014 | B013 | B012 | B011 | B010 | 08h | B_V2 |
| 69th | B04h | B027 | B026 | B025 | B024 | B023 | B022 | B021 | B020 | 10h | B_V4 |
| : | : | : | : | : | : | : | : | : | : | : | : |
| 98th | B62h | B317 | B316 | B315 | B314 | B313 | B312 | B311 | B310 | F8h | B_V62 |
| 99th | B63h | B327 | B326 | B325 | B324 | B323 | B322 | B321 | B320 | FCh | B_V63 |

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## 5.9 Power function

### 5.9.1 Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order.
IOVCC, VCI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.
During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

**Note:** (1) There will be no damage to the display module if the power sequences are not met.
(2) There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
(3) There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
(4) If NRESET line is not held stable by host during Power on Sequence as defined in Sections 5.11.1.1 and 5.11.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence to ensure correct operation. Otherwise correct function is not guaranteed.

If NRESET line is not held stable by host during Power on Sequence as defined in Sections 5.9.1.1 and 5.9.1.2 then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence is complete to ensure correct operation, otherwise correct functionality is not guaranteed. The power on/off sequence is illustrated as below

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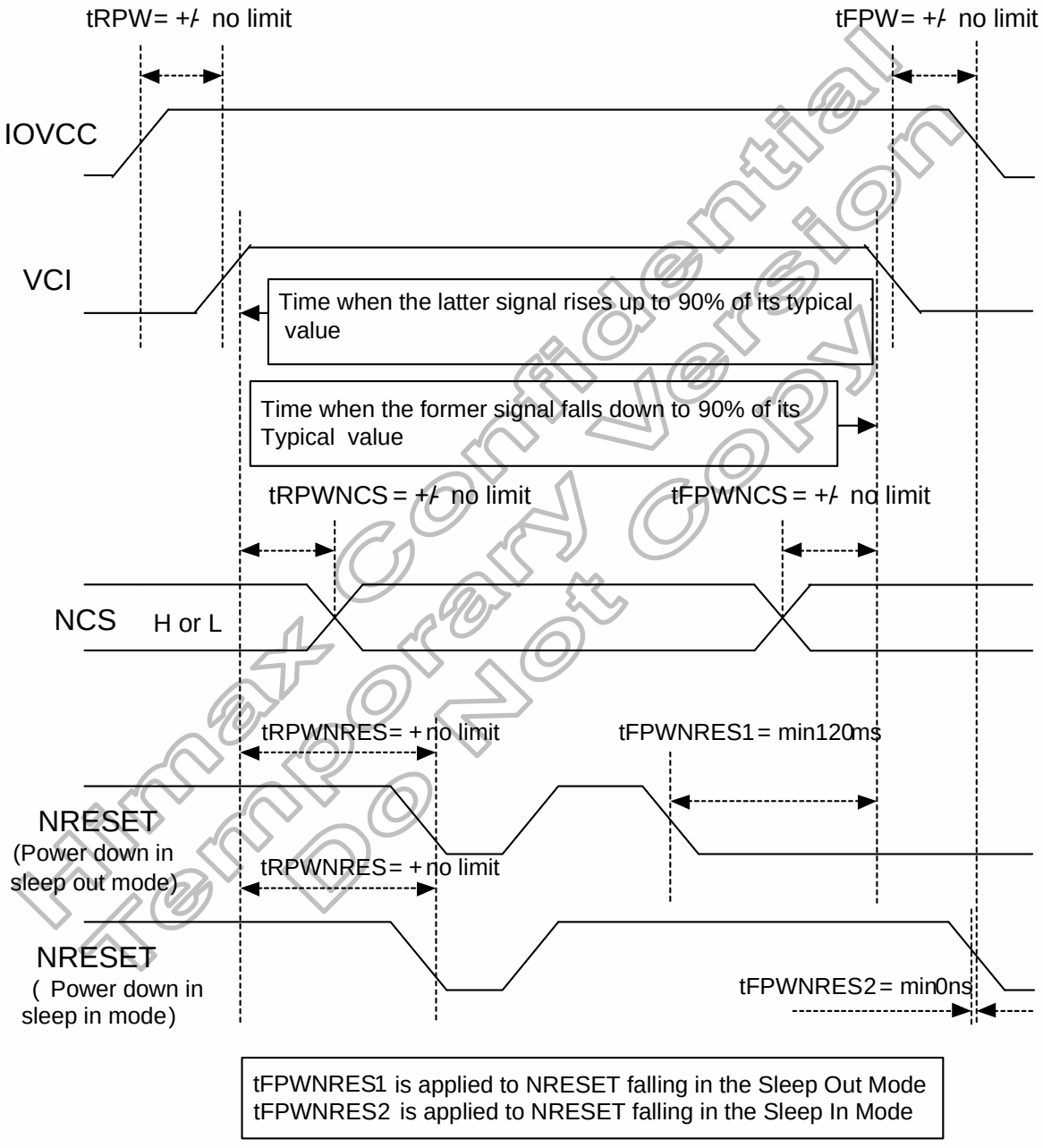
### 5.9.1.1 Case 1 – NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCI have been applied, otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.




Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

**Figure 5.31: Case 1 – NRESET line is held high or unstable by host at power on**

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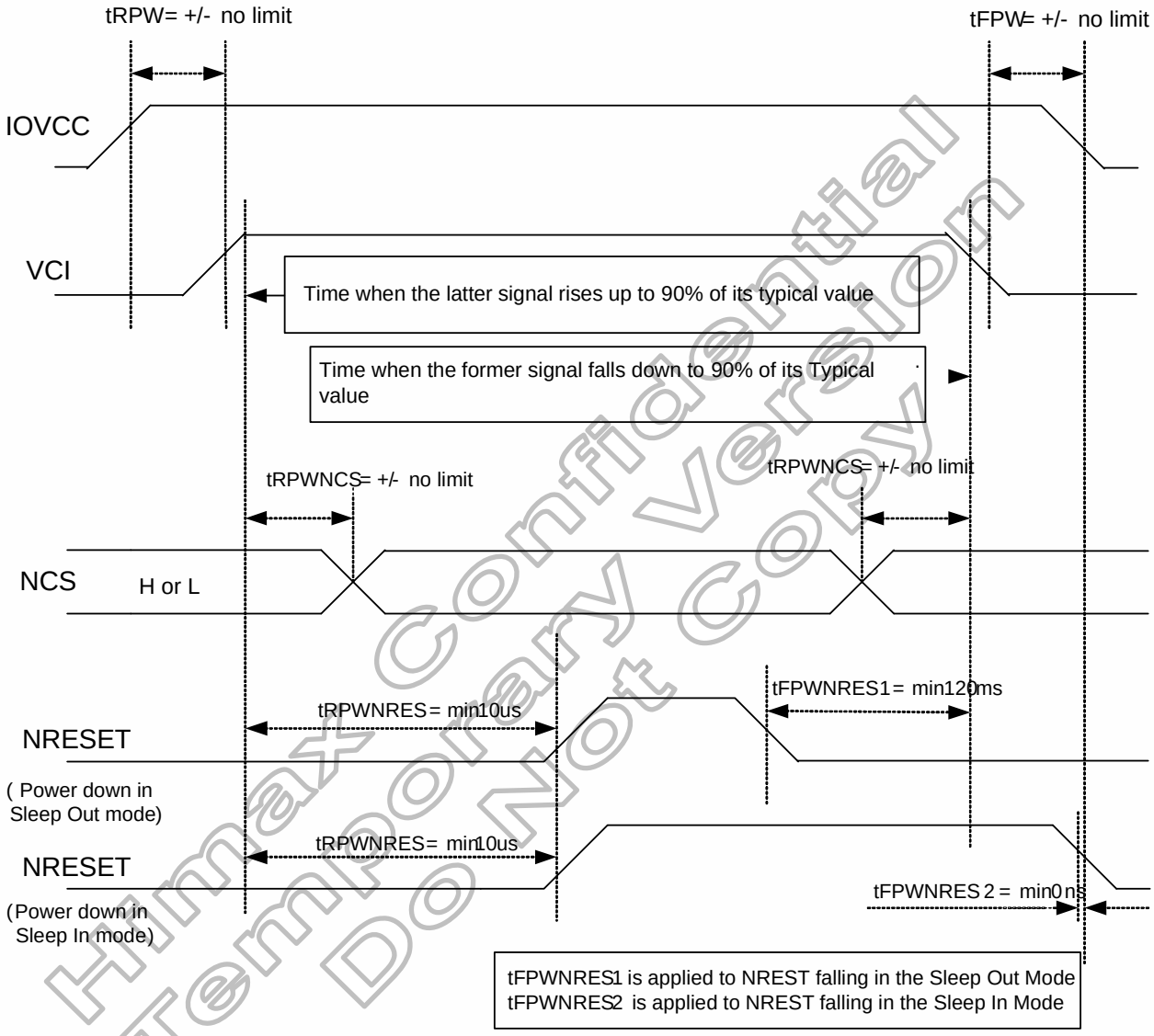
### 5.9.1.2 Case 2 – NRESET line is held low by host at power on

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after VCI have been applied.




Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

**Figure 5.32: NRESET line is held low by host at power on**

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### 5.9.2 Power levels definition

#### 5.9.2.1 General definition for power levels

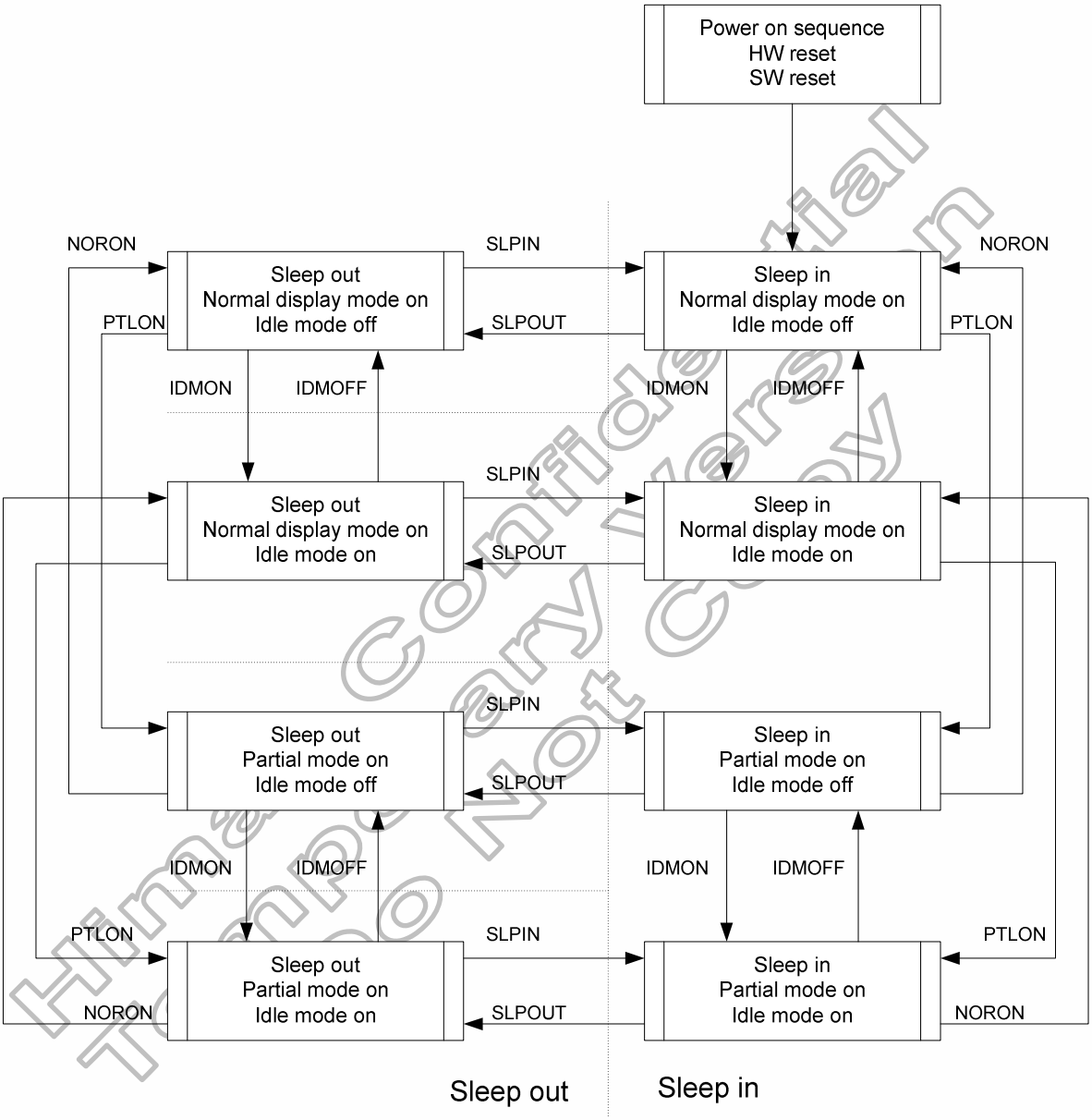


**Figure 5.33: Power flow chart for different power modes**

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### 5.9.3 Deep standby mode set up flow

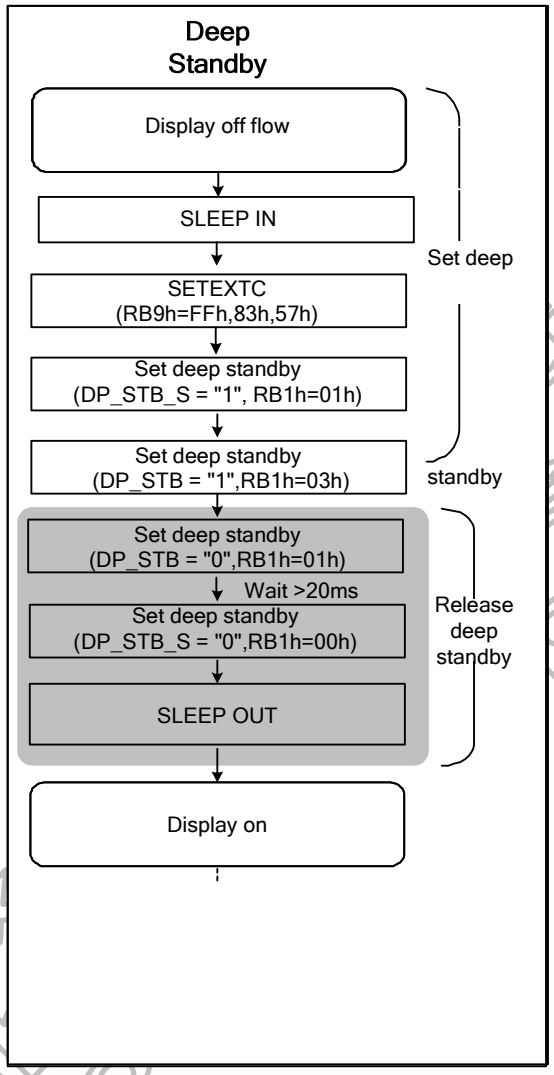


**Figure 5.34: Deep standby mode setting flow**

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## 5.10 Input / output pin state

### 5.10.1 Output pins

| Output or Bi-directional pins | After Power On | After Hardware Reset |
|---|---|---|
| DB23 to DB0 (Output driver) | High-Z (Inactive) | High-Z (Inactive) |
| SDO | High-Z (Inactive) | High-Z (Inactive) |
| CABC_ON | Low | Low |
| CABC_PWM | Low | Low |

**Table 5.8: Characteristics of output pins**

### 5.10.2 Input pins

| Input pins | During Power On Process | After Power On | After Hardware Reset | During Power Off Process |
|---|---|---|---|---|
| RESX | Input valid | Input valid | Input valid | Input valid |
| CSX | Input invalid | Input valid | Input valid | Input invalid |
| WRX_SCL | Input invalid | Input valid | Input valid | Input invalid |
| RDX | Input invalid | Input valid | Input valid | Input invalid |
| DCX | Input invalid | Input valid | Input valid | Input invalid |
| DIN_SDA | Input invalid | Input valid | Input valid | Input invalid |
| VSYNC | Input invalid | Input valid | Input valid | Input invalid |
| HSYNC | Input invalid | Input valid | Input valid | Input invalid |
| DE | Input invalid | Input valid | Input valid | Input invalid |
| PCLK | Input invalid | Input valid | Input valid | Input invalid |
| D[23:0] | Input invalid | Input valid | Input valid | Input invalid |
| OSC, IM2, IM1,IM0 | Input invalid | Input valid | Input valid | Input invalid |
| TEST3-1 | Input invalid | Input valid | Input valid | Input invalid |

**Table 5.9: Characteristics of input pins**

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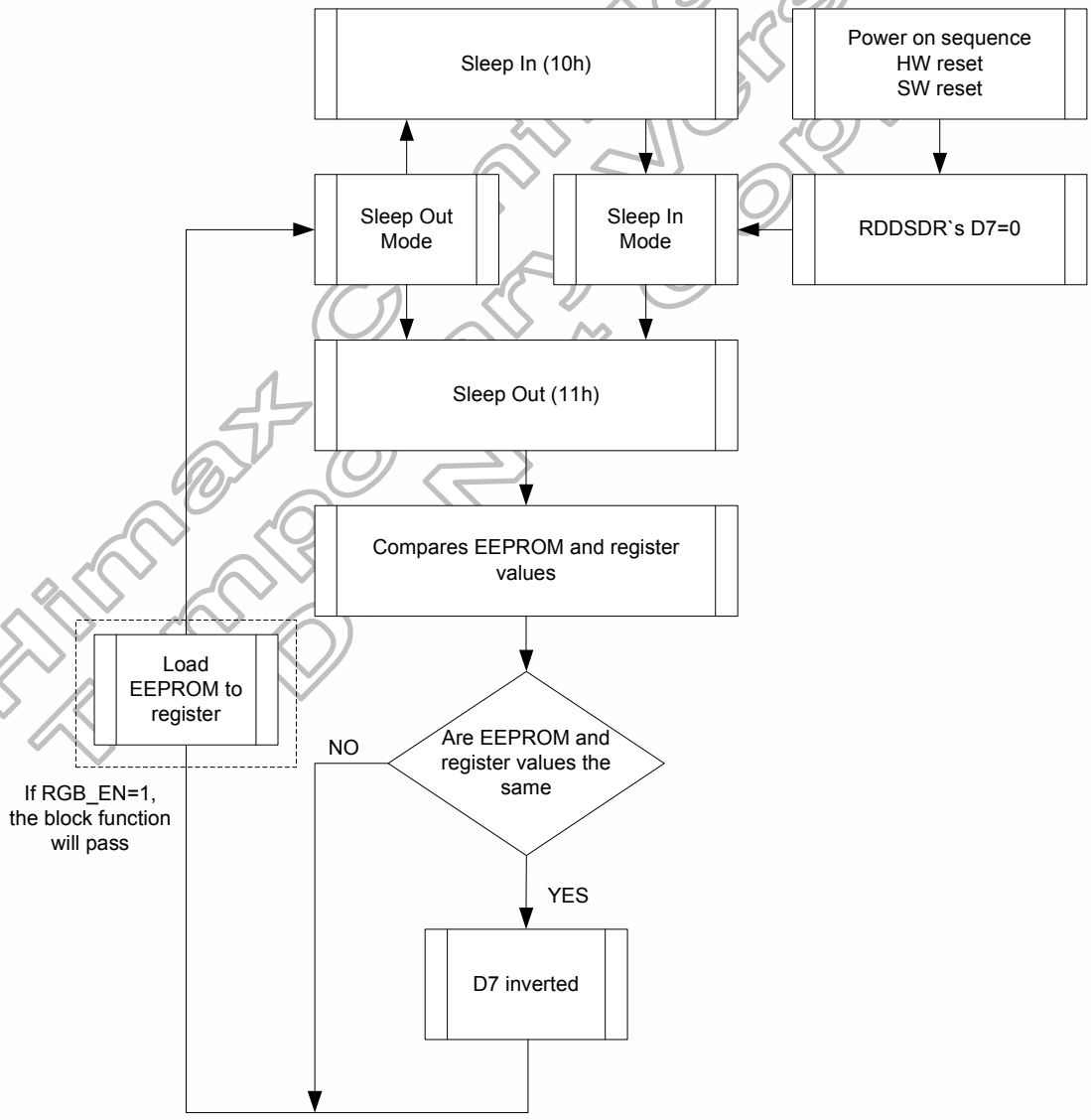
## 5.11 Sleep out – command and self-diagnostic functions of display module

### 5.11.1 Register loading detection

Sleep Out-command (See section 6.2.15“Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in section 6.2.13 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The bit used for this command is D7). If those both values are not the same, this bit (D7) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.




**Note:** There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

**Figure 5.35: RDDSDR register loading detection flow**

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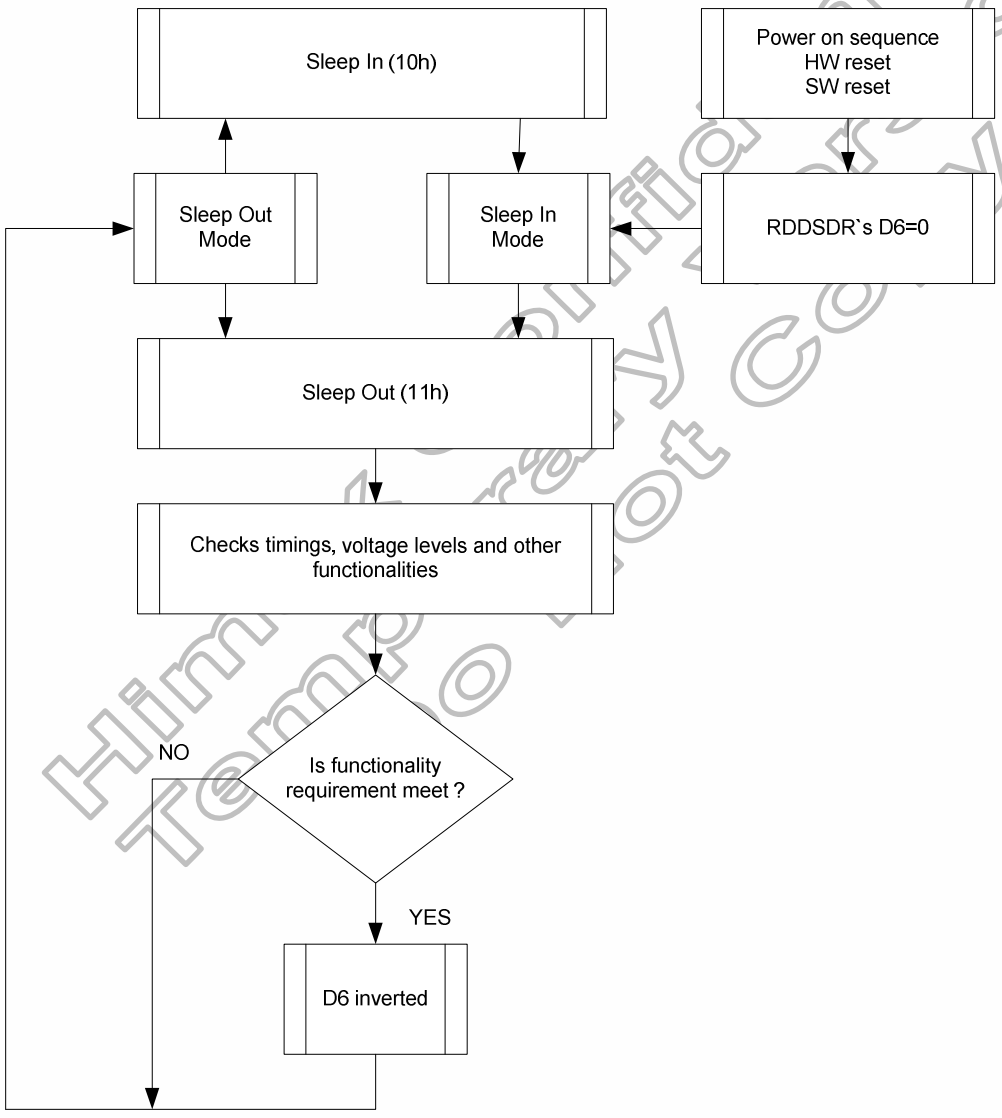
### 5.11.2 Functionality detection

Sleep Out-command (See section 6.2.15 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in section 6.2.13 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.




**Note:** There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

**Figure 5.36: Functionality detection flow**

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## 5.12 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

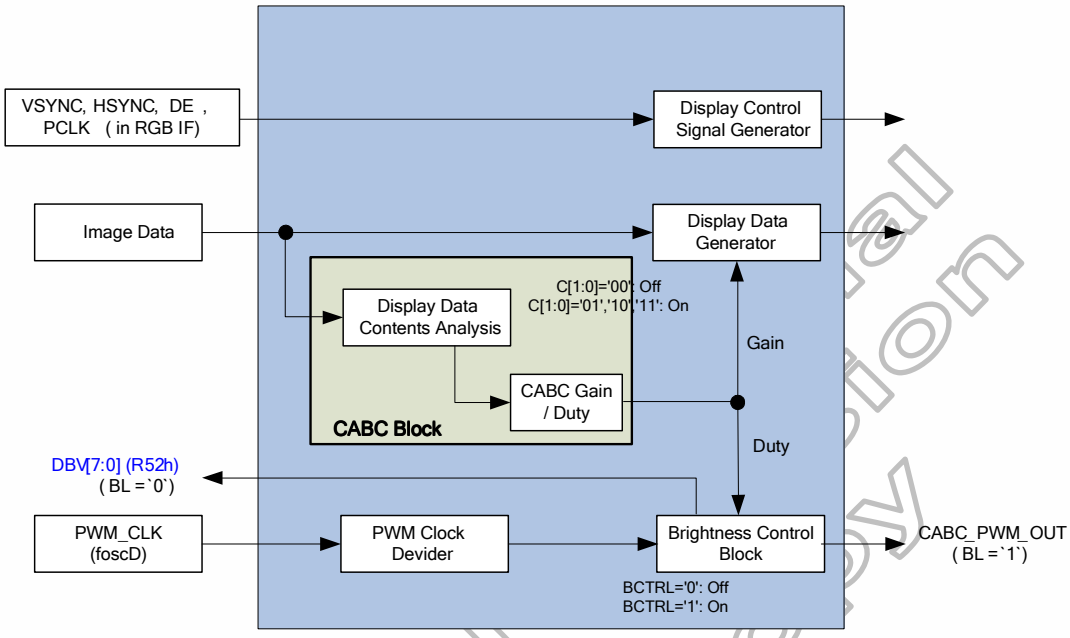


**Figure 5.37:CABC block diagram**

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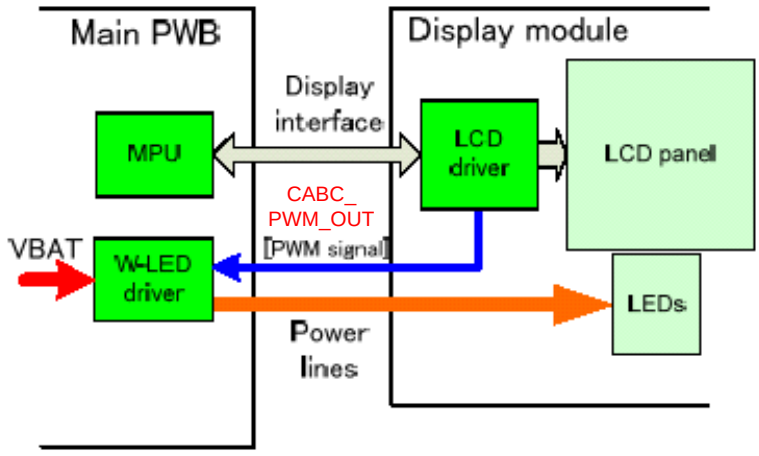
### 5.12.1 Module architectures

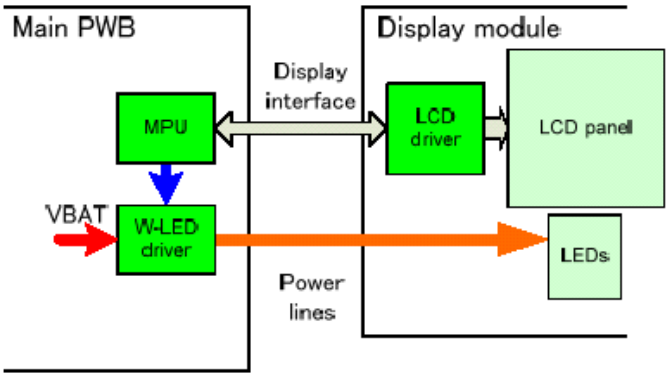
The HX8357-C can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- **Architecture I**




1. **BL** =`1` of R53h
2. LED backlight brightness for the display is controlled by external output "CABC_PWM_OUT".

- **Architecture II**




1. **BL** =`0` of R53h
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R52h.
3. Read commands R52h should be synchronized with V-sync.

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### 5.12.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness. The CABC_PWM_OUT output active polarity is defined by **INVPULS** bit of RC9h.

The CABC_PWM_OUT output period is controlled by **PWMDIV[2:0]** and **PWM_PERIOD[7:0]** bits of RC9h setting.

Ex: PWM CLK is 5.5MHz (period 180ns), PWMDIV=110(divide by 64),
and PWM_PERIOD=00h (the value is 0+1).
➔ CABC_PWM_OUT period = 180ns x 64 x (1x256) = 2.95 ms

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as DBV[7:0]/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R51h) = '$228_{DEC}$' and CABC duty is 74%. Then CABC_PWM_OUT duty = 228 / 255 x 74% ≡ 66.16%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.95ms, and the low-level of CABC_PWM_OUT = 1.00ms.

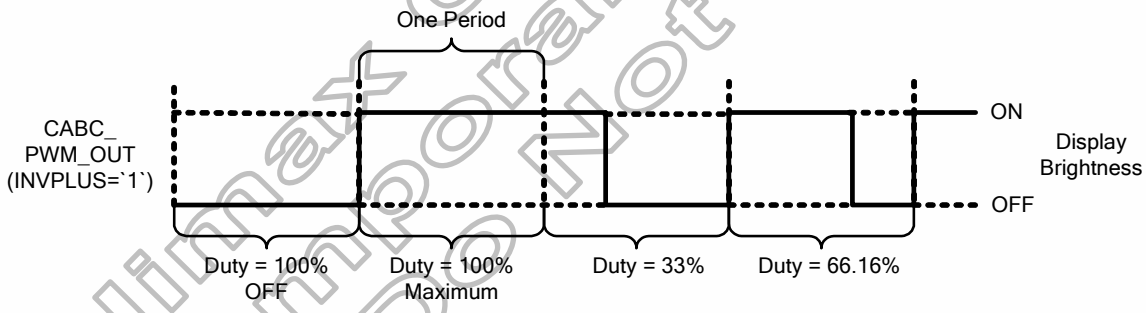


**Figure 5.38: CABC_PWM_OUT output duty**

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low (**INVPULS='1'**) and the DBV[7:0](R52h) will be read a value as $169_{DEC}$ (169/255≡ 66.27%).

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### 5.12.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. "**CMB[7:0],** Read CABC minimum brightness (R5Fh) "always read the setting value of "**CMB[7:0],** Write CABC minimum brightness (R5Eh)".

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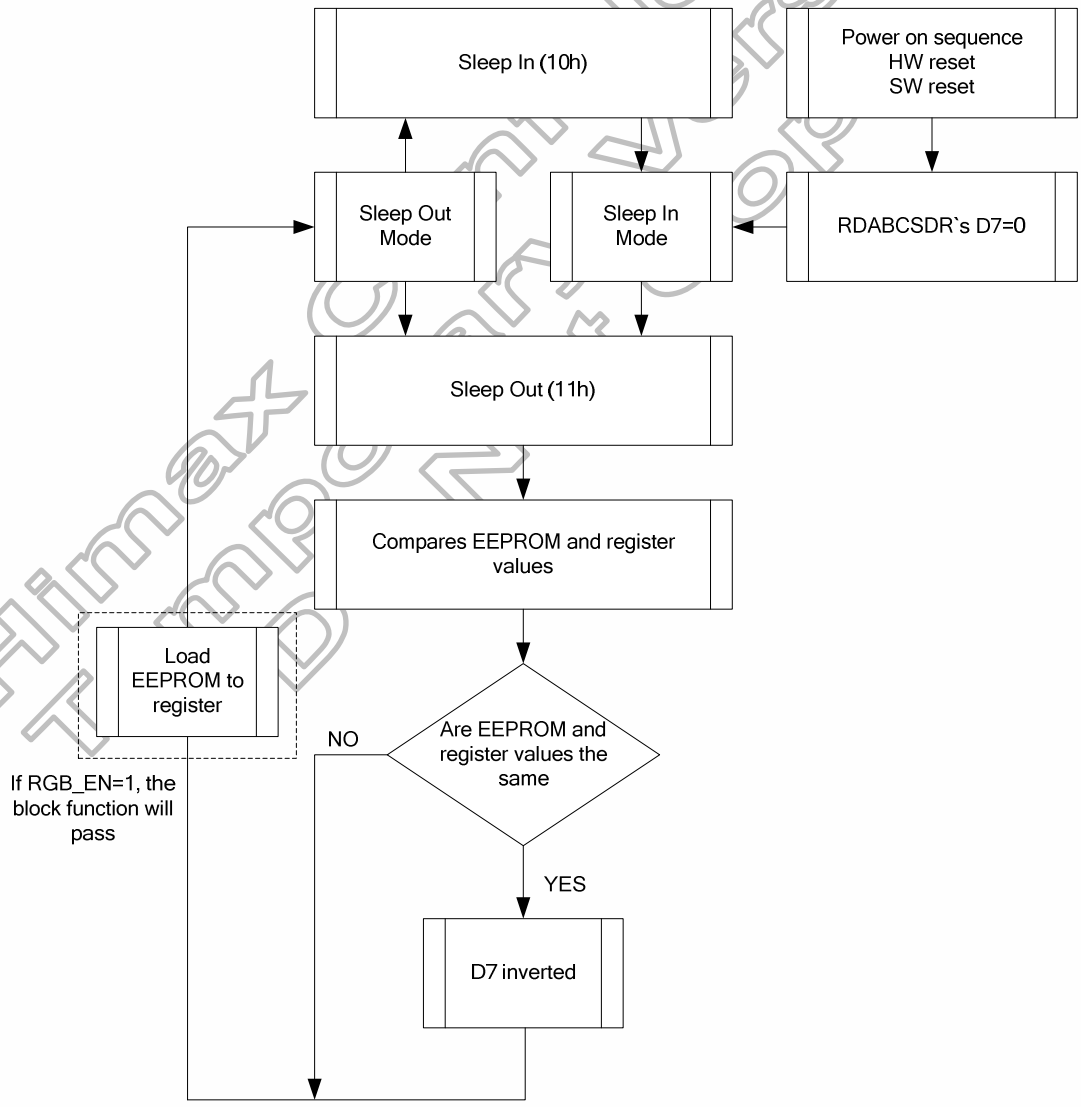
### 5.12.3.1Register loading detection

Sleep Out command (See section 6.2.15, Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: compares register and EEPROM values, 2nd step: loads EEPROM values to registers). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.2.50 “Read Automatic Brightness Control Self-Diagnostic Result (68h)” (=RDABCSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).
The flow chart for this internal function is following:




**Note:** There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module

**Figure 5.39: RDABCSDR register loading detection flow**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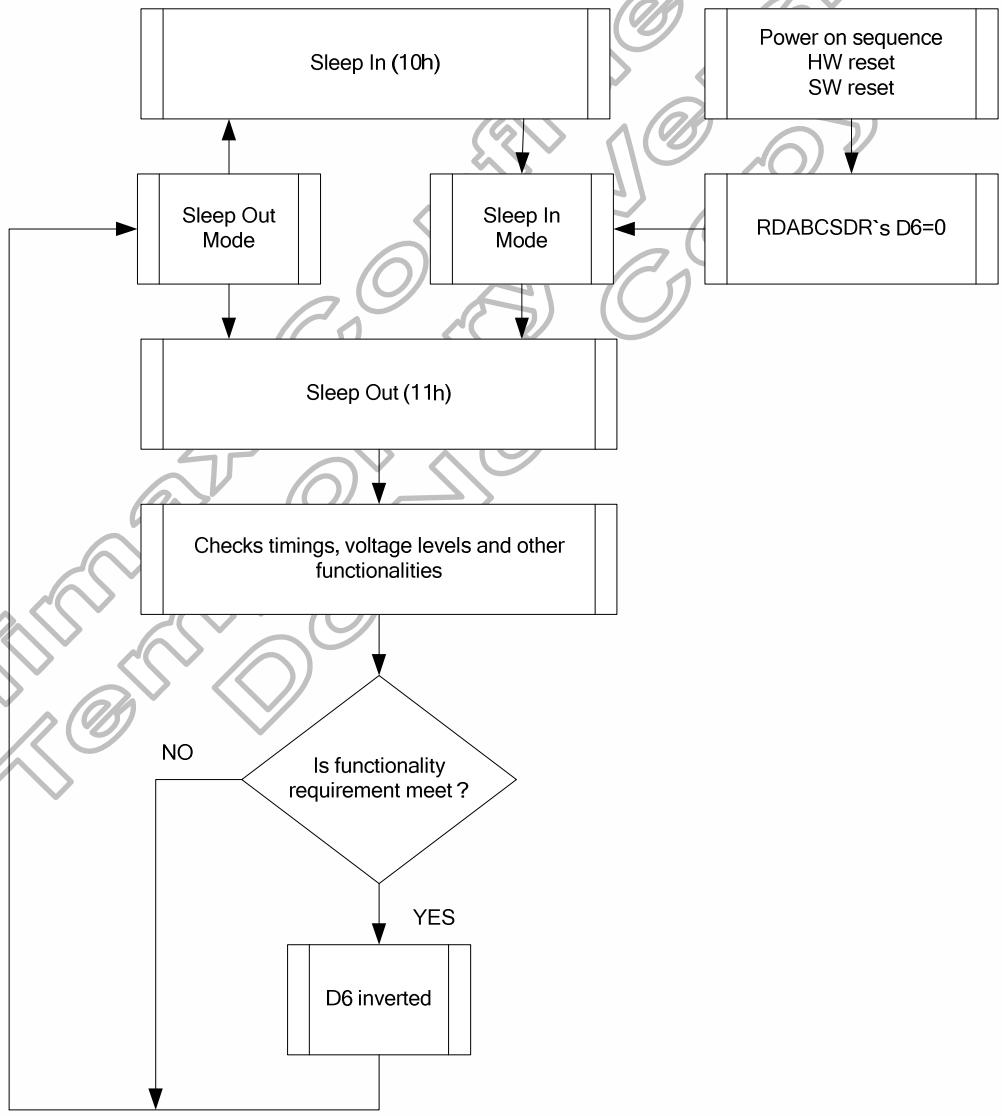
### 5.12.3.2Functionality detection

Sleep Out command (See section 6.2.15, Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If the functionality requirement is met, there is inverted (increased by 1) a bit, which defined in command 6.2.50 “Read Automatic Brightness Control Self-Diagnostic Result (68h)” (=RDABCSDR) (The used bit of this command is D6). If the functionality requirement is not same, this bit (D6) is not inverted (=not increased by 1).

The flow chart for this internal function is following:




**Note:** There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDABCSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

**Figure 5.40: RDABCSDR functionality detection flow**

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### 5.12.4 Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

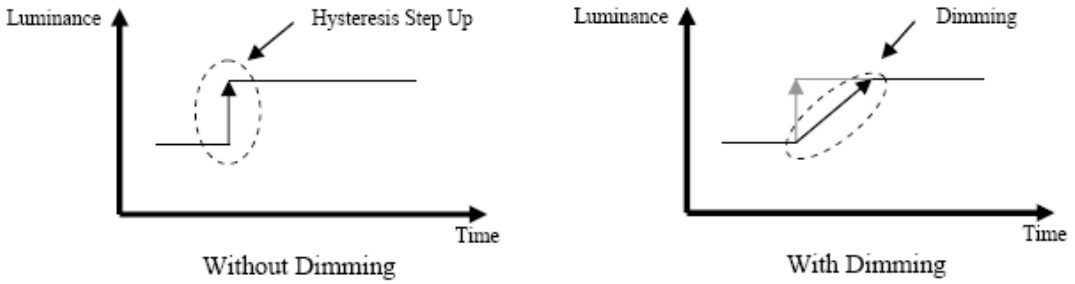


**Figure 5.41: Dimming function**

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## 5.13 OTP programing

### 5.13.1 OTP Table

| OTP_Index | Table_ Index | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01 | 01 | ID1[7:0] | | | | | | | |
| | 02 | ID2[7:0] | | | | | | | |
| | 03 | ID3[7:0] | | | | | | | |
| | 04 | ID1[7:0] | | | | | | | |
| | 05 | ID2[7:0] | | | | | | | |
| | 06 | ID3[7:0] | | | | | | | |
| | 07 | ID1[7:0] | | | | | | | |
| | 08 | ID2[7:0] | | | | | | | |
| | 09 | ID3[7:0] | | | | | | | |
| | 0A | ID1[7:0] | | | | | | | |
| | 0B | ID2[7:0] | | | | | | | |
| | 0C | ID3[7:0] | | | | | | | |
| 0D | 0D | * | VCOM[6:0] | | | | | | |
| | 0E | * | VCOM[6:0] | | | | | | |
| | 0F | * | VCOM[6:0] | | | | | | |
| | 10 | * | VCOM[6:0] | | | | | | |
| 12 | 12 | * | * | * | SM_PANEL | SS_PANEL | GS_PANEL | REV_PANEL | BGR_PANEL |
| 13 | 13 | * | * | TRI | XDK | | BT[2:0] | | |
| | 14 | * | * | VRH[5:0] | | | | | |
| | 15 | * | * | NVRH[5:0] | | | | | |
| 16 | 16 | FS1[3:0] | | | | FS0[3:0] | | | |
| 18 | 18 | SDO_EN | BYPASS | EPF[1:0] | * | * | RM | DM | |
| | 19 | * | * | * | * | DPL | HSPL | VSPL | EPL |
| 1A | 1A | ZINV | | I_NW[1:0] | | * | * | N_NW[1:0] | |
| 1B | 1B | * | * | * | * | * | * | * | DGC_EN |
| | 1C | DGC_LUT_R00 | | | | | | | |
| | 1D | DGC_LUT_R01 | | | | | | | |
| | 1E | DGC_LUT_R02 | | | | | | | |
| | | : | | | | | | | |
| | 7C | DGC_LUT_B30 | | | | | | | |
| | 7D | DGC_LUT_B31 | | | | | | | |
| | 7E | DGC_LUT_B32 | | | | | | | |
| 7F | 7F | DDB1[7:0] | | | | | | | |
| | 80 | DDB2[7:0] | | | | | | | |
| | 81 | DDB3[7:0] | | | | | | | |
| | 82 | DDB4[7:0] | | | | | | | |
| 83 | 83 | | VRP0[6:0] | | | | | | |
| | 84 | | VRP1[6:0] | | | | | | |
| | 85 | | VRP2[6:0] | | | | | | |
| | | : | | | | | | | |
| | A1 | | VRN14[6:0] | | | | | | |
| | A2 | | VRN15[6:0] | | | | | | |
| | A3 | CGN[1:0] | | CGN[1:0] | | CGP[1:0] | | CGP[1:0] | |
| A4 | A4 | PWM2_OE | | | | | | | |
| A5 | A5 | | | | | | | | MESSI_EN |

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| OTP_Index | Table_ Index | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| A6 | A6 | Bkx[1:0] | | Bky[1:0] | | Wx[1:0] | | Wy[1:0] | |
| | A7 | Bkx[9:2] | | | | | | | |
| | A8 | Bky[9:2] | | | | | | | |
| | A9 | Wx[9:2] | | | | | | | |
| | AA | Wy[9:2] | | | | | | | |
| | AB | Rkx[1:0] | | Rky[1:0] | | Gx[1:0] | | Gy[1:0] | |
| | AC | Rx[9:2] | | | | | | | |
| | AD | Ry[9:2] | | | | | | | |
| | AE | Gx[9:2] | | | | | | | |
| | AF | Gy[9:2] | | | | | | | |
| | B0 | Bx[1:0] | | By[1:0] | | Ax[1:0] | | Ay[1:0] | |
| | B1 | Bx[9:2] | | | | | | | |
| | B2 | By[9:2] | | | | | | | |
| | B3 | Ax[9:2] | | | | | | | |
| | B4 | Ay[9:2] | | | | | | | |

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### 5.13.2 OTP programming flow

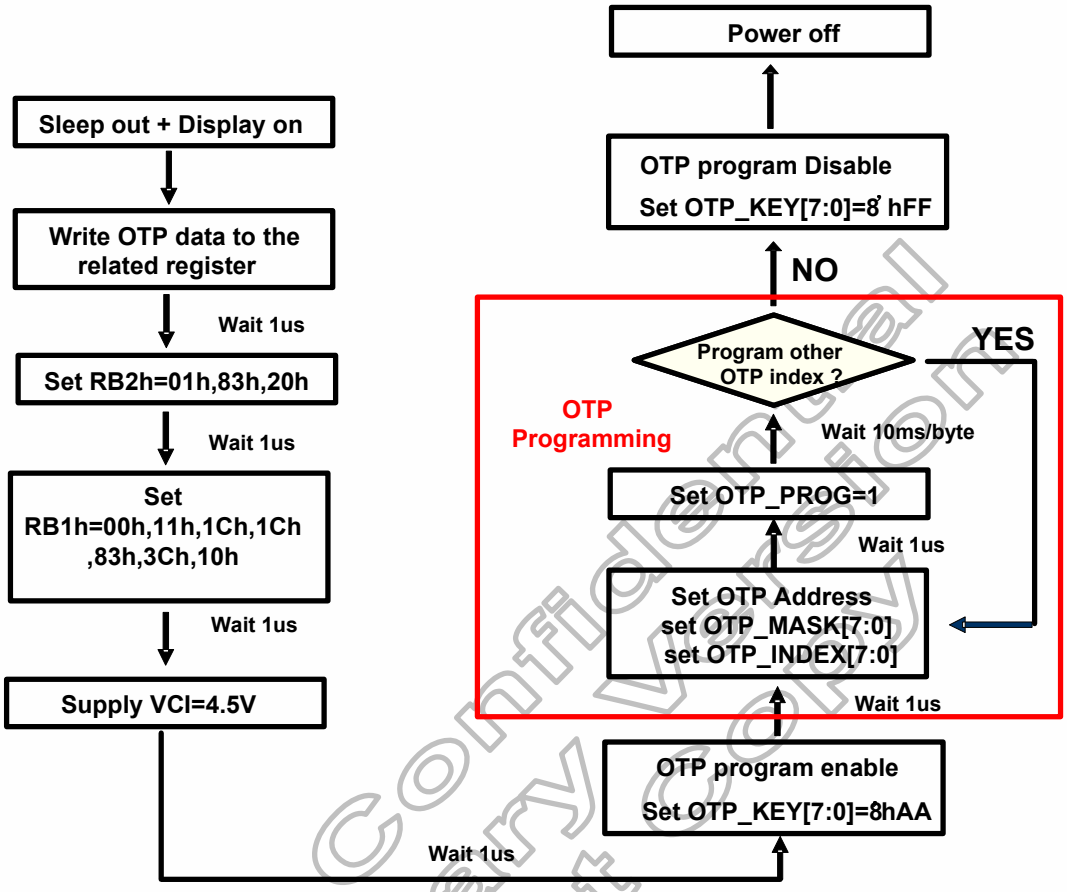


Figure 5.42: OTP programming sequence

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# 6. Command Set

## 6.1 Command set list

### 6.1.1 Standard command

| (Hex) | Operation code | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Default (Hex) | MESSI_ENB '0' | MESSI_ENB '1' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | NOP | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No Operation | - | Yes | |
| 01 | SWRESET | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software Reset | - | Yes | |
| 04 | RDDIDIF | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Read Display Identification Information | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | ID1[7:0] | | | | | | | | ID1 | 00h | | |
| | | 1 | ↑ | 1 | ID2[7:0] | | | | | | | | ID2 | 00h | | |
| | | 1 | ↑ | 1 | ID3[7:0] | | | | | | | | ID3 | 00h | | |
| 05 | RDNUMPE | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Read Number of the Errors on DSI | - | Yes | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | P[7:0] | | | | | | | | - | 00h | | |
| 06 | RDRED | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Read Red Colour | - | Yes | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | xx | 00h | | |
| 07 | RDGREEN | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Read Green Colour | - | Yes | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | xx | 00h | | |
| 08 | RDBLUE | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Read Blue Colour | - | Yes | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | xx | 00h | | |
| 0A | RDDPM | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Read display power mode | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | - | 08h | | |
| 0B | RDDMADCTL | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Read display MADCTL | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | - | 00h | | |
| 0C | RDDCOLMOD | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Read display pixel format | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | - | D6 | D5 | D4 | - | D2 | D1 | D0 | - | 07h | | |
| 0D | RDDIM | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | Read display image mode | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D7 | D6 | D5 | 0 | 0 | D2 | D1 | D0 | - | 00h | | |
| 0E | RDDSM | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Read display signal mode | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D7 | D6 | 0 | 0 | 0 | 0 | 0 | D0 | - | 00h | | |
| 0F | RDDSDR | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Read display self-diagnostic result | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | X | Dummy read | - | | |
| | | 1 | ↑ | 1 | D7 | D6 | 0 | 0 | 0 | 0 | 0 | D0 | - | 00h | | |
| 10 | SLPIN | 0 | 1 | ↑ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Sleep In | - | Yes | |
| 11 | SLPOUT | 0 | 1 | ↑ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Sleep Out | - | Yes | |

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| (Hex) | Operation code | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Default (Hex) | MESSI_ENB '0' | MESSI_ENB '1' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 | PTLON | 0 | 1 | ↑ | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Partial Mode On | - | Yes | |
| 13 | NORON | 0 | 1 | ↑ | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Normal display mode on | - | Yes | |
| 20 | INVOFF | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Display inversion off | - | Yes | |
| 21 | INVON | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Display inversion on | - | Yes | |
| 22 | ALLPOFF | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | All Pixel Off | - | Yes | |
| 23 | ALLPON | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | All Pixel On | - | Yes | |
| 26 | GAMSET | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Gamma Set | - | Yes | |
| | | 0 | 1 | ↑ | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 | Gamma Curve | 01h | | |
| 28 | DISPOFF | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Display off | - | Yes | |
| 29 | DISPON | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Display on | - | Yes | |
| 2A | CASET | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Column Address Set | - | Yes | |
| | | 1 | 1 | ↑ | SC15 | SC14 | SC13 | SC12 | SC11 | SC10 | SC9 | SC8 | Column address start | 00h | | |
| | | 1 | 1 | ↑ | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | Column address start | 00h | | |
| | | 1 | 1 | ↑ | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 | Column address end | 01h | | |
| | | 1 | 1 | ↑ | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | Column address end | 67h | | |
| 2B | PASET | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Row address set | - | Yes | |
| | | 1 | 1 | ↑ | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | Row address start | 00h | | |
| | | 1 | 1 | ↑ | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | Row address start | 00h | | |
| | | 1 | 1 | ↑ | EP15 | EP14 | EP13 | EP12 | EP11 | EP10 | EP9 | EP8 | Row address end | 02h | | |
| | | 1 | 1 | ↑ | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | Row address end | 7Fh | | |
| 2C | RAMWR | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Memory Write | - | Yes | |
| | | 1 | 1 | ↑ | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | Write data | - | | |
| | | 1 | 1 | ↑ | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | Write data | - | | |
| | | 1 | 1 | ↑ | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | Write data | - | | |
| 2E | RAMRD | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Memory read | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | Read data | - | | |
| | | 1 | ↑ | 1 | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | Read data | - | | |
| | | 1 | ↑ | 1 | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | - | - | | |
| 30 | PLTAR | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Partial Area | - | Yes | |
| | | 1 | 1 | ↑ | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | Start row | 00h | | |
| | | 1 | 1 | ↑ | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | Start row | 00h | | |
| | | 1 | 1 | ↑ | ER15 | ER14 | ER13 | ER12 | ER11 | ER10 | ER9 | ER8 | End row | 02h | | |
| | | 1 | 1 | ↑ | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | End row | 7Fh | | |

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| (Hex) | Operation Code | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Default (Hex) | MESSI_ENB '0' | MESSI_ENB '1' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 33 | VSCRDEF | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Vertical scrolling definition | - | Yes | |
| | | 1 | 1 | ↑ | TFA[15:8] | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | TFA[7:0] | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | VSA[15:8] | | | | | | | | - | 02h | | |
| | | 1 | 1 | ↑ | VSA[7:0] | | | | | | | | - | 80h | | |
| | | 1 | 1 | ↑ | BFA[15:8] | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | BFA[7:0] | | | | | | | | - | 00h | | |
| 34 | TEOFF | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Tearing Effect Line OFF | - | Yes | |
| 35 | TEON | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Tearing Effect Line ON | - | Yes | |
| 36 | MADCTL | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Memory Access Control | - | Yes | |
| | | 1 | 1 | ↑ | B7 | B6 | B5 | B4 | B3 | B2 | 0 | 0 | - | 00h | | |
| 37 | VSCRSADD | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Vertical scrolling start address | - | Yes | |
| | | 1 | 1 | ↑ | VSP[15:8] | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | VSP[7:0] | | | | | | | | - | 00h | | |
| 38 | IDMOFF | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Idle mode off | - | Yes | |
| 39 | IDMON | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Idle mode on | - | Yes | |
| 3A | COLMOD | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | | - | Yes | |
| | | 1 | 1 | ↑ | 0 | D6 | D5 | D4 | 0 | D2 | D1 | D0 | - | 07h | | |
| 3C | RAMWRCON | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | Memory write | - | Yes | |
| | | 1 | 1 | ↑ | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | - | - | | |
| | | 1 | 1 | ↑ | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | - | - | | |
| | | 1 | 1 | ↑ | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | - | - | | |
| 3E | RAMRDCON | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | Memory read | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | - | - | | |
| | | 1 | ↑ | 1 | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | - | - | | |
| | | 1 | ↑ | 1 | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | - | - | | |
| 44 | TESL | 0 | 1 | ↑ | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | TESL | - | No | Yes |
| | | 1 | 1 | ↑ | TELINE[15:8](8'b0) | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | TELINE[7:0](8'b0) | | | | | | | | - | 00h | | |
| 45 | GETSCAN | 0 | 1 | ↑ | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Reture the current scanline SLN[15:0] | - | No | Yes |
| | | 1 | 1 | ↑ | SLN[15:8] | | | | | | | | - | 00h | | |
| | | 1 | 1 | ↑ | SLN[7:0] | | | | | | | | - | 00h | | |
| 51 | WRDISBV | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Write Display Brightness | - | Yes | |
| | | 1 | 1 | ↑ | DBV[7:0] | | | | | | | | - | 00h | | |
| 52 | RDDISBV | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | Read Display Brightness Value | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | DBV[7:0] | | | | | | | | - | 00h | | |
| 53 | WRCTRLD | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | Write CTRL Display | - | Yes | |
| | | 1 | 1 | ↑ | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | | 00h | | |
| 54 | RDCTRLD | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | Read Control Value Display | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | - | 00h | | |
| 55 | WRCABC | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | Write Adaptive Brightness Control | - | Yes | |
| | | 1 | 1 | ↑ | 0 | 0 | 0 | 0 | 0 | 0 | CABC[1:0] | | - | 00h | | |

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| (Hex) | Operation Code | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Default (Hex) | MESSI_ENB '0' | MESSI_ENB '1' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 56 | RDCABC | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | Read Adaptive Brightness Control Content | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C1 | C0 | - | 00h | | |
| 5E | WRCABCMB | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | Write CABC minimum brightness | - | | Yes |
| | | 1 | 1 | ↑ | CMB[7:0] | | | | | | | | - | 00h | | |
| 5F | RDCABCMB | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | Read CABC minimum brightness | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | CMB[7:0] | | | | | | | | - | 00h | | |
| 68 | RDABCSDR | 0 | 1 | ↑ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Read Automatic Brightness Control Self-Diagnostic Result | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | - | | |
| | | 1 | ↑ | 1 | D[7:6] | | 0 | 0 | 0 | 0 | 0 | 0 | - | 00h | | |
| 70 | RDBWLB | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Read Black/White Low Bits | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Bkx1 | Bkx0 | Bky1 | Bky0 | Wx1 | Wx0 | Wy1 | Wy0 | - | - | | |
| 71 | RDBkx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Read Bkx | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Bkx9 | Bkx8 | Bkx7 | Bkx6 | Bkx5 | Bkx4 | Bkx3 | Bkx2 | - | - | | |
| 72 | RDBky | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Read Bky | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Bky9 | Bky8 | Bky7 | Bky6 | Bky5 | Bky4 | Bky3 | Bky2 | - | - | | |
| 73 | RDWx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | Read Wx | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Wx9 | Wx8 | Wx7 | Wx6 | Wx5 | Wx4 | Wx3 | Wx2 | - | - | | |
| 74 | RDWy | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | Read Wy | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | - | - | | |
| 75 | RDRGLB | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Read Red/Green Low Bits | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Rx1 | Rx0 | Ry1 | Rx0 | Gx1 | Gx0 | Gy1 | Gy0 | - | - | | |
| 76 | RDRx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | Read Rx | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | Rx3 | Rx2 | - | - | | |
| 77 | RDRy | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | Read Ry | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Ry9 | Ry8 | Ry7 | Ry6 | Ry5 | Ry4 | Ry3 | Ry2 | - | - | | |
| 78 | RDGx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Read Gx | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Gx9 | Gx8 | Gx7 | Gx6 | Gx5 | Gx4 | Gx3 | Gx2 | - | - | | |
| 79 | RDRy | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | Read Gy | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Gy9 | Gy8 | Gy7 | Gy6 | Gy5 | Gy4 | Gy3 | Gy2 | - | - | | |
| 7A | RDBALB | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | Read Biue/AColour Low Bits | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Bx1 | Bx0 | By1 | Bx0 | Ax1 | Ax0 | Ay1 | Ay0 | - | - | | |
| 7B | RDBx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | Read Bx | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Bx9 | Bx8 | Bx7 | Bx6 | Bx5 | Bx4 | Bx3 | Bx2 | - | - | | |
| 7C | RDBy | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Read By | - | | Yes |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | By9 | By8 | By7 | By6 | By5 | By4 | By3 | By2 | - | - | | |

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| (Hex) | Operation Code | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Default (Hex) | MESSI_ENB '0' | MESSI_ENB '1' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7D | RDAx | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Read Ax | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Ax9 | Ax8 | Ax7 | Ax6 | Ax5 | Ax4 | Ax3 | Ax2 | - | - | | |
| 7E | RDAy | 0 | 1 | ↑ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Read Ay | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | Ay9 | Ay8 | Ay7 | Ay6 | Ay5 | Ay4 | Ay3 | Ay2 | - | - | | |
| A1 | Read_DDB_start | 0 | 1 | ↑ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Read the DDB from the provided location. | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| | | 1 | ↑ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0xFF | FFh | | |
| A8 | Read_DDB_continue | 0 | 1 | ↑ | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Continue reading the DDB from the last read location. | - | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | - | 00h | | |
| AA | RDFCS | 0 | 1 | ↑ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Read First Checksum | | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | 00h | | |
| | | 1 | ↑ | 1 | FCS[7:0] | | | | | | | | | 00h | | |
| AF | RDCCS | 0 | 1 | ↑ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Read Continue Checksum | | Yes | |
| | | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | Dummy read | 00h | | |
| | | 1 | ↑ | 1 | CCS[7:0] | | | | | | | | | 00h | | |
| DA | RDID1 | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Read ID1 | - | Yes | |
| | | 1 | 1 | ↑ | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | 1 | ↑ | module's manufacturer[7:0] | | | | | | | | - | 00h | | |
| DB | RDID2 | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | Read ID2 | - | Yes | |
| | | 1 | 1 | ↑ | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | 1 | ↑ | LCD module/driver version [7:0] | | | | | | | | - | 00h | | |
| DC | RDID3 | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Read ID3 | - | Yes | |
| | | 1 | 1 | ↑ | x | x | x | x | x | x | x | x | Dummy read | - | | |
| | | 1 | 1 | ↑ | LCD module/driver ID[7:0] | | | | | | | | - | 00h | | |

**Note:** (1) Undefined commands are treated as NOP (00h) command.

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### 6.1.2 User define command list table(T.B.D)

| (Hex) | Operation Code | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B0 | SETOSC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Set Internal Oscillator |
| | | 1 | ↑ | 1 | - | I_UADJ[3:0] | | | | N_UADJ[3:0] | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | OSC_EN | |
| B1 | SETPOWER | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Set power control |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | DP_STB | |
| | | 1 | ↑ | 1 | - | - | - | TRI | XDK | - | BT[2:0] | | | |
| | | 1 | ↑ | 1 | - | - | - | VRH[5:0] | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | NVRH[5:0] | | | | | | |
| | | 1 | ↑ | 1 | - | GASEN | - | - | - | - | AP[2:0] | | | |
| | | 1 | ↑ | 1 | - | FS1[3:0] | | | | FS0[3:0] | | | | |
| | | 1 | ↑ | 1 | - | - | VCOMG | 1 | PON | DK | 0 | 0 | STB | |
| B2 | SETDISPLAY | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Set Display control |
| | | 1 | ↑ | 1 | - | - | - | - | - | ISC[3:0] | | | | |
| | | 1 | ↑ | 1 | - | PT[1:0] | | - | - | - | - | PTG | REF | |
| | | 1 | ↑ | 1 | - | - | - | NL[5:0] | | | | | | |
| | | 1 | ↑ | 1 | - | - | SCN[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | GON | DTE | D[1:0] | | - | - | |
| B3 | SETRGB | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Set RGB I/F |
| | | 1 | ↑ | 1 | - | SDO_ENB | BYPASS | EPF[1:0] | | - | - | RM | DM | |
| | | 1 | ↑ | 1 | - | - | - | - | - | DPL | HSPL | VSPL | EPL | |
| | | 1 | ↑ | 1 | - | RCM | HBP[5:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VBP[5:0] | | | | | | | |
| B4 | SETCYC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Set Display cycle |
| | | 1 | ↑ | 1 | - | ZINV | - | I_NW[1:0] | | - | - | N_NW[1:0] | | |
| | | 1 | ↑ | 1 | - | - | RTN[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | OSC_DIV2 | - | DIV[1:0] | | |
| | | 1 | ↑ | 1 | - | N_DUM[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | I_DUM[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | GDON[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | GDOF[7:0] | | | | | | | | |
| B6 | SETVCOM | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Set VCOM voltage |
| | | 1 | ↑ | 1 | - | - | VCOM[6:0] | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | VCOM_OTP_TIMES[2:0] | | | |
| B7 | SETOTP | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Set OTP |
| | | 1 | ↑ | 1 | - | OTP_KEY[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | OTP_MASK[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | OTP_INDEX[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | LOAD_DIS | VPP_EN | OTP_POR | OTP_PWE | OTP_PTM[1:0] | | VPP_SEL | OTP_PROG | |
| | | 1 | 1 | ↑ | - | OTP_DOUT[7:0](8'hFF) | | | | | | | | |
| B9 | SETEXTC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Enter extention command |
| | | 1 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | 1 | ↑ | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | | 1 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | |

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| (Hex) | Operation Code | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1 | SETDGC | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Set Digital Gamma Correction |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | DGC_EN | |
| | | 1 | ↑ | 1 | - | DGC_LUT_R00[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | : | | | | | | | | |
| | | 1 | ↑ | 1 | - | DGC_LUT_R32[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | DGC_LUT_G00[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | : | | | | | | | | |
| | | 1 | ↑ | 1 | - | DGC_LUT_G32[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | DGC_LUT_B00[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | : | | | | | | | | |
| | | 1 | ↑ | 1 | - | DGC_LUT_B32[7:0] | | | | | | | | |
| C3 | SETID | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Set ID |
| | | 1 | ↑ | 1 | - | ID1[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | ID2[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | ID3[7:0] | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | ID_OTP_TIMES[2:0] | | | |
| C4 | SET DDB | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | SET DDB |
| | | 1 | ↑ | 1 | - | DDB1[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | DDB2[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | DDB3[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | DDB4[7:0] | | | | | | | | |
| C9 | SETCABC | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SET CABC |
| | | 1 | ↑ | 1 | - | BC_CTL | PWMDIV[2:0] | | | 1 | 1 | INVPLUS | 1 | |
| | | 1 | ↑ | 1 | - | PWM_PERIOD[7:0] | | | | | | | | |
| CC | SETPANEL | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Set Panel characteristics |
| | | 1 | ↑ | 1 | - | - | - | - | SM_PANEL | SS_PANEL | GS_PANEL | REV_PANEL | BGR_PANEL | |

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| (Hex) | Operation Code | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E0 | SETGAMMA | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Set Gamma |
| | | 1 | ↑ | 1 | - | - | VRP0[6:0] | | | | | | | Set Gamma |
| | | 1 | ↑ | 1 | - | - | VRP1[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP2[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP3[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP4[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP5[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP6[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP7[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP8[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP9[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP10[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP11[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP12[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP13[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP14[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRP15[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN0[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN1[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN2[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN3[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN4[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN5[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN6[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN7[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN8[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN9[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN10[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN11[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN12[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN13[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN14[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | - | VRN15[6:0] | | | | | | | |
| | | 1 | ↑ | 1 | - | CGN1[1:0] | | CGN0[1:0] | | CGP1[1:0] | | CGP0[1:0] | | |
| | | 1 | ↑ | 1 | - | | | | | | | | GMA_RELOAD | |
| EA | SETMESSI | 0 | 1 | ↑ | - | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Set command type |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | SPI_DCX_SEL | MESSI_ENB | |
| EB | SETCOLOR | 0 | 1 | ↑ | - | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Set Color |
| | | 1 | 1 | ↑ | - | Bkx1 | Bkx0 | Bky1 | Bky0 | Wx1 | Wx0 | Wy1 | Wy0 | |
| | | 1 | 1 | ↑ | - | Bkx9 | Bkx8 | Bkx7 | Bkx6 | Bkx5 | Bkx4 | Bkx3 | Bkx2 | |
| | | 1 | 1 | ↑ | - | Bky9 | Bky8 | Bky7 | Bky6 | Bky5 | Bky4 | Bky3 | Bky2 | |
| | | 1 | 1 | ↑ | - | Wx9 | Wx8 | Wx7 | Wx6 | Wx5 | Wx4 | Wx3 | Wx2 | |
| | | 1 | 1 | ↑ | - | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | |
| | | 1 | 1 | ↑ | - | Rx1 | Rx0 | Ry1 | Ry0 | Gx1 | Gx0 | Gy1 | Gy0 | |
| | | 1 | 1 | ↑ | - | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | Rx3 | Rx2 | |
| | | 1 | 1 | ↑ | - | Ry9 | Ry8 | Ry7 | Ry6 | Ry5 | Ry4 | Ry3 | Ry2 | |
| | | 1 | 1 | ↑ | - | Gx9 | Gx8 | Gx7 | Gx6 | Gx5 | Gx4 | Gx3 | Gx2 | |
| | | 1 | 1 | ↑ | - | Gy9 | Gy8 | Gy7 | Gy6 | Gy5 | Gy4 | Gy3 | Gy2 | |
| | | 1 | 1 | ↑ | - | Bx1 | Bx0 | By1 | By0 | Ax1 | Ax0 | Ay1 | Ay0 | |
| | | 1 | 1 | ↑ | - | Bx9 | Bx8 | Bx7 | Bx6 | Bx5 | Bx4 | Bx3 | Bx2 | |
| | | 1 | 1 | ↑ | - | By9 | By8 | By7 | By6 | By5 | By4 | By3 | By2 | |
| | | 1 | 1 | ↑ | - | Ax9 | Ax8 | Ax7 | Ax6 | Ax5 | Ax4 | Ax3 | Ax2 | |
| | | 1 | 1 | ↑ | - | Ay9 | Ay8 | Ay7 | Ay6 | Ay5 | Ay4 | Ay3 | Ay2 | |
| FE | SETREADINDEX | 0 | 1 | ↑ | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | SET SPI READ Command Address |
| | | 1 | 1 | ↑ | - | CMD_ADD[7:0] | | | | | | | | |
| FF | GETSPIREAD | 0 | 1 | ↑ | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Read SPI Command Data |
| | | 1 | ↑ | 1 | - | CMD_DATA1[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | : | | | | | | | | |
| | | 1 | ↑ | 1 | - | CMD_DATAn[7:0] | | | | | | | | |

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## 6.2 Command description

### 6.2.1 NOP

<table>
<tr><td>00 H</td><td colspan="13">NOP (No Operation)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR (Memory Write) or RAMRD (Memory Read) command.</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">-</td></tr>
</table>

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### 6.2.2 Software reset (01h)

| 01 H | SWRESET (Software Reset) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)<br>The display is blank immediately.<br>Note: The GRAM contents are unaffected by this command. | | | | | | | | | | | | |
| Restriction | It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this 5m sec.<br>If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command.<br>SW Reset command cannot be sent during Sleep Out sequence. | | | | | | | | | | | | |

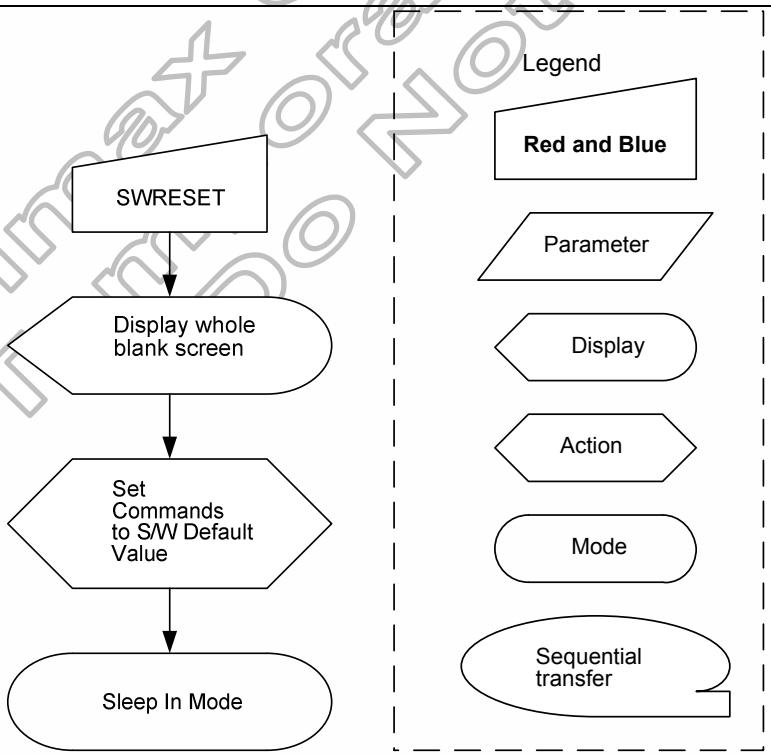
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | N/A |
| S/W Reset | N/A |
| H/W Reset | N/A |

Flow Chart

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### 6.2.3 Read display identification information (04h)

| 04 H | RDDIDIF (Read Display Identification Information) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | - |
| 3rd parameter | 1 | 1 | ↑ | - | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | - |
| 4th parameter | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | - |
| Description | This read byte returns 24-bit display identification information.<br>The 1st parameter is dummy data.<br>The 2nd parameter: LCD module's manufacturer ID.<br>The 3rd parameter: LCD module/driver version ID.<br>The 4th parameter: LCD module/driver ID.<br>**Note:** Commands RDID1/2/3(DAh, DBh and DCh) read data correspond to the parameters 2, 3, 4 of the command 04h, respectively. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

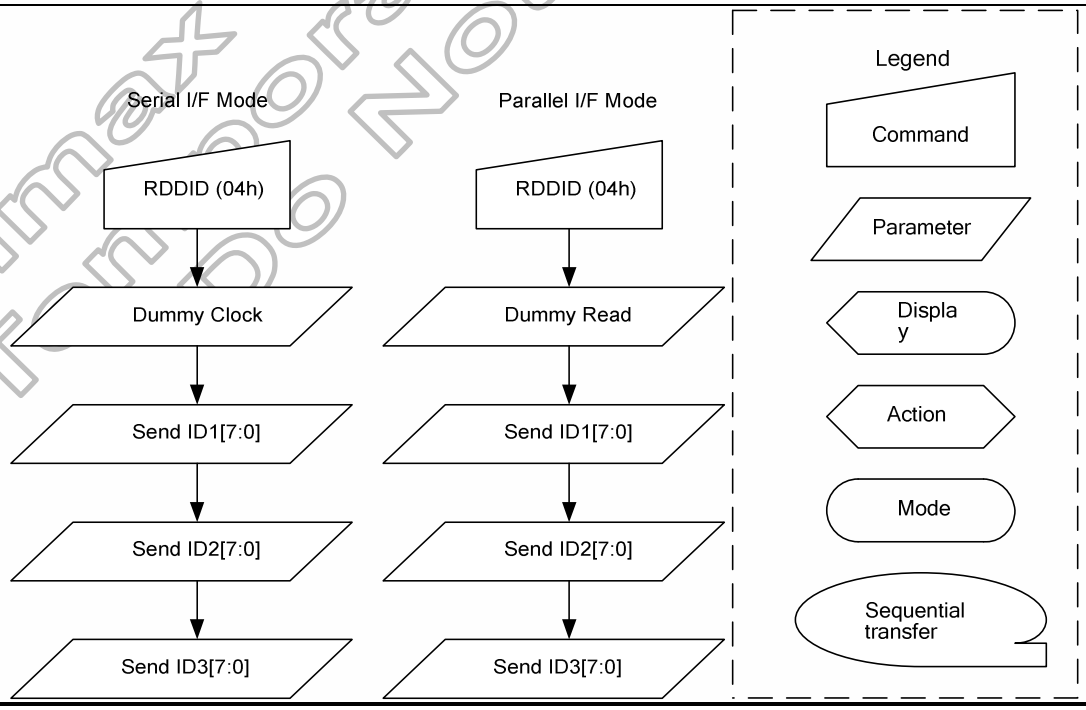
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.4 RDNUMPE: Read Number of the Errors on DSI (05h)

| 05h | RDNUMPE (Read Number of the Errors on DSI) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | Dummy read |
| 1st parameter | 1 | ↑ | 1 | - | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | xx |
| Description | The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below.<br>P[6..0] bits are telling a number of the errors.<br>P[7] is set to '1' if there is overflow with P[6..0] bits.<br>P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed). | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

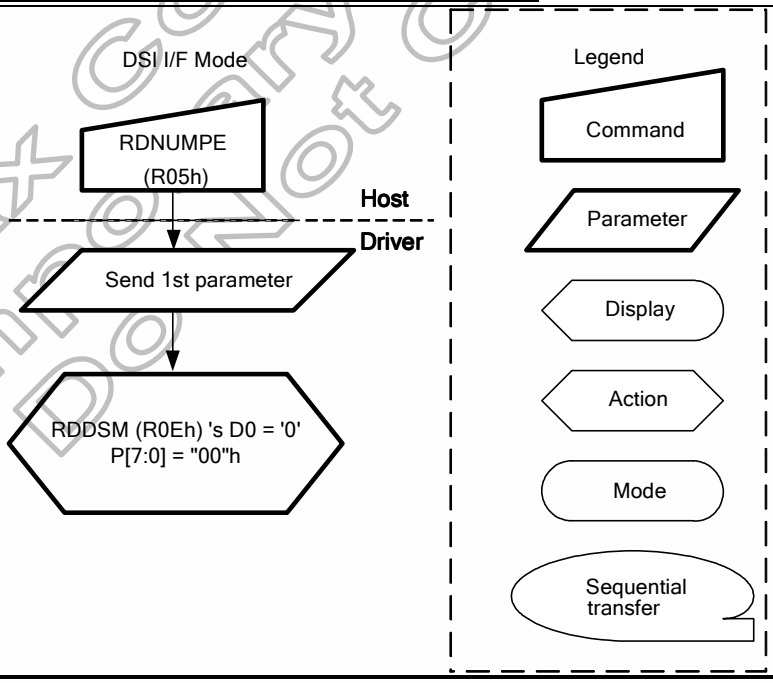
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.5Read red color (06h)

| 06 H | RDRED (Read Red Color) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | R5 | R4 | R3 | R2 | R1 | R0 | - |
| Description | The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F.<br>16 bit format: R5 is MSB and R1 is LSB. R0 is set to '0'.<br>18 bit format: R5 is MSB and R0 is LSB. | | | | | | | | | | | | |
| Restriction | When BYPASS='0', this command is working as a NOP (00h) command. | | | | | | | | | | | | |

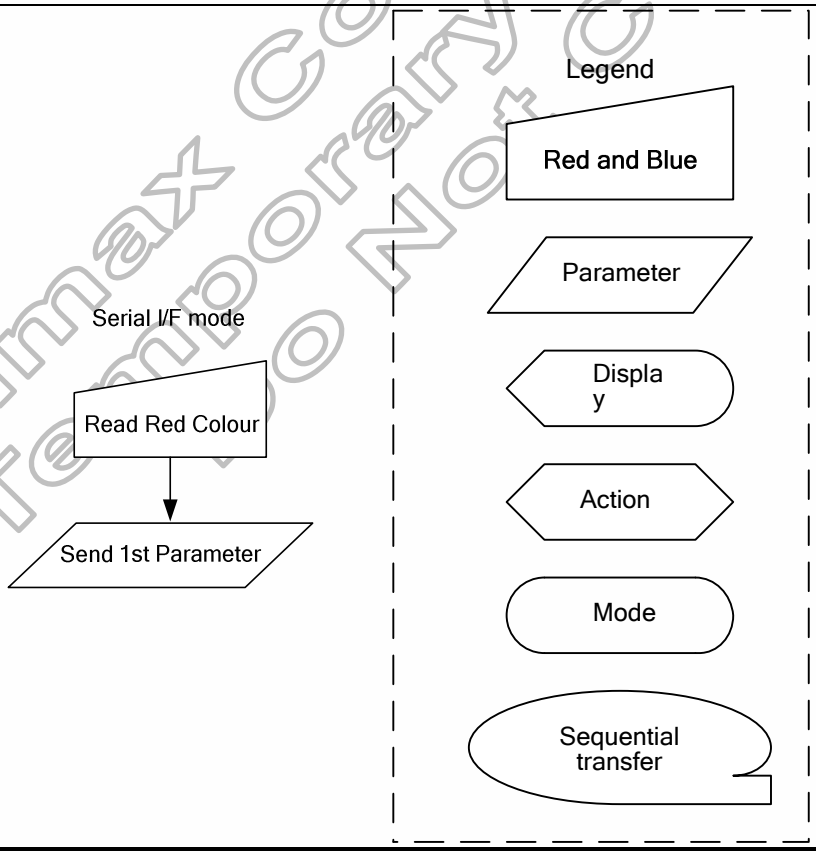
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.6 Read green color (07h)

| 07 H | RDGREEN (Read Green Color) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | G5 | G4 | G3 | G2 | G1 | G0 | - |
| Description | The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F.<br>16, 18 bit formats: G5 is MSB and G0 is LSB. | | | | | | | | | | | | |
| Restriction | When BYPASS='0' is disabled, this command is working as a NOP (00h) command. | | | | | | | | | | | | |

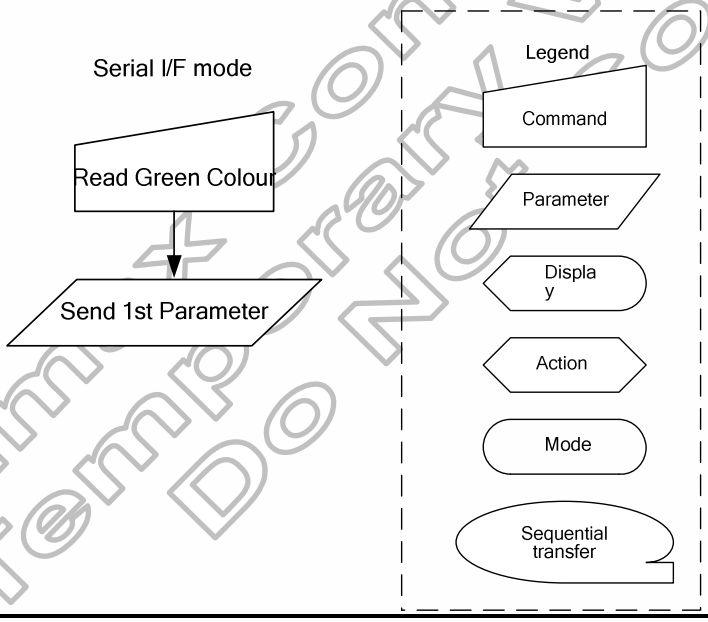
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.7 Read blue color (08h)

| 08 H | RDBLUE (Read Blue Color) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | B5 | B4 | B3 | B2 | B1 | B0 | - |
| Description | The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F.<br>16 bit format: B5 is MSB and B1 is LSB. B0 is set to '0'.<br>18 bit format: B5 is MSB and B0 is LSB. | | | | | | | | | | | | |
| Restriction | When BYPASS='0' is disabled, this command is working as a NOP (00h) command. | | | | | | | | | | | | |

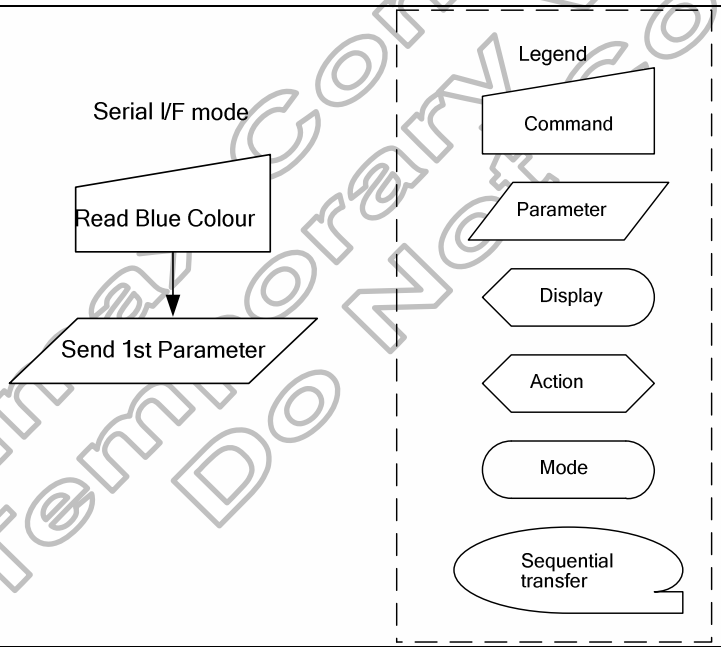
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.8 Read display power mode (0Ah)

| 0A H | RDDPM (Read Display Power Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | xx |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| D7 | Booster Voltage Status | - |
| D6 | Idle Mode On/Off | - |
| D5 | Partial Mode On/Off | - |
| D4 | Sleep In/Out | - |
| D3 | Display Normal Mode On/Off | - |
| D2 | Display On/Off | - |
| D1 | Not Defined | Set to '0' |
| D0 | Not Defined | Set to '0' |

**Bit D7 – Booster Voltage Status**
'0' = Booster Off or has a fault.
'1' = Booster On and working OK (Meets display supplier's optical requirements).
**Bit D6 – Idle Mode On/Off**
'0' = Idle Mode Off.
'1' = Idle Mode On.
**Bit D5 – Partial Display Mode On/Off**
'0' = Partial Mode Off.
'1' = Partial Mode On.
**Bit D4 – Sleep In/Out**
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
**Bit D3 – Normal Display Mode On/Off**
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
**Bit D2 – Display On/Off**
'0' = Display is Off.
'1' = Display is On.
**Bit D1 – Not Defined**
This bit is not applicable for this project, so it is set to '0'.
**Bit D0 – Not Defined**
This bit is not applicable for this project, so it is set to '0'.

**Restrictions**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 08h |
| S/W Reset | 08h |
| H/W Reset | 08h |

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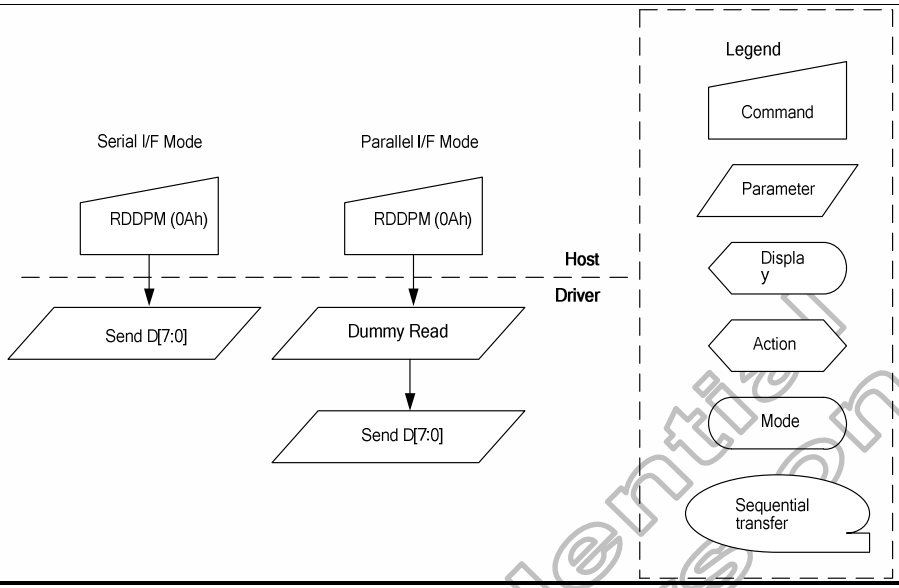
Flow Chart

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### 6.2.9 Read display MADCTL (0Bh)

| 0B H | RDDMADCTL (Read Display MADCTL) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | D6 | D5 | D4 | D3 | D2 | 0 | 0 | xx |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| D7 | Page Address Order | - |
| D6 | Column Address Order | - |
| D5 | Page/Column Order | - |
| D4 | Line Address Order | - |
| D3 | RGB/BGR Order | - |
| D2 | Display Data Latch Order | - |
| D1 | Switching between Segment outputs and RAM | Set to '0' |
| D0 | Switching between Common outputs and RAM | Set to '0' |

**Bit D7 – Page Address Order**
'0' = Top to Bottom (When MADCTL B7(MY) = '0').
'1' = Bottom to Top (When MADCTL B7(MY) ='1').
**Bit D6 – Column Address Order**
'0' = Left to Right (When MADCTL B6(MX) = '0').
'1' = Right to Left (When MADCTL B6(MX) = '1').
**Bit D5 –Page / Column Order**
'0' = Normal Mode (When MADCTL B5(MV) = '0').
'1' = Reverse Mode (When MADCTL B5(MV) = '1').
**Bit D4 – Line Address Order**
'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').
**Bit D3 – RGB/BGR Order**
'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').
**Note:** For bits D4, D3 and D2 also refer to 6.2.32 Memory Access Control (R36h)
**Bit D2 – Display Data Latch Order**
'0' = LCD Refresh Left to Right (When MADCTL B2 = '0').
'1' = LCD Refresh Right to Left (When MADCTL B2 = '1').
**Bit D1 – Switching Between Segment Outputs and RAM**
This bit is not applicable for this project, so it is set to '0'.
**Bit D0 – Switching Between Common Outputs and RAM**
This bit is not applicable for this project, so it is set to '0'.

**Restrictions**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | No Change |
| H/W Reset | 00h |

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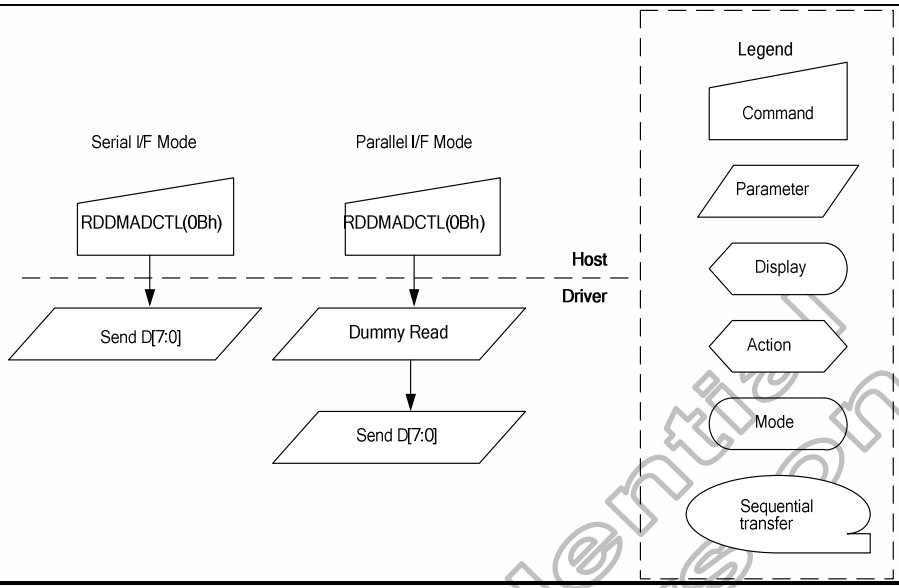
Flow Chart

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### 6.2.10 Read display pixel format (0Ch)

| 0C H | RDDCOLMOD (Read Display COLMOD) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | 0 | D6 | D5 | D4 | 0 | D2 | D1 | D0 | xx |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| D7 | Reserved | Set to '0' |
| D6 | DPI Interface Pixel format | - |
| D5 | | - |
| D4 | | - |
| D3 | Reserved | Set to '0' |
| D2 | DBI Interface Pixel format | - |
| D1 | | - |
| D0 | | - |

Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
Bits D2, D1, D0 – DSI, DBI Interface Colour Pixel Format Definition.

| Interface Colour Format | D6/D2 | D5/D1 | D4/D0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| 12 bit/pixel | 0 | 1 | 1 |
| Not Defined | 1 | 0 | 0 |
| 16 bit/pixel | 1 | 0 | 1 |
| 18 bit/pixel | 1 | 1 | 0 |
| 24 bit/pixel | 1 | 1 | 1 |

If a particular interface, either DSI, DBI or DPI, is not used then the corresponding bits in the

**Restrictions**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 18-bit/pixel |
| S/W Reset | 18-bit/pixel |
| H/W Reset | 18-bit/pixel |

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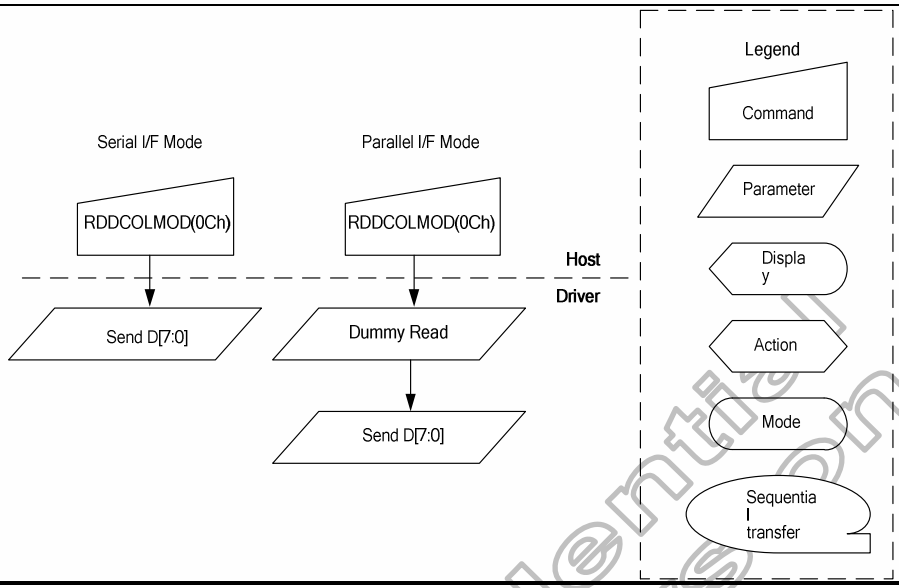
Flow Chart

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### 6.2.11 Read display image mode (0Dh)

| 0D H | RDDIM (Read Display Image Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | 0 | D5 | 0 | 0 | D2 | D1 | D0 | xx |

Description

This command indicates the current status of the display as described in the table below:

**Bit D7 – Vertical Scrolling On/Off**

'0' = Vertical Scrolling is Off.

'1' = Vertical Scrolling is On.

**Bit D6 – Horizontal Scrolling Status**

This bit is not applicable for this project, so it is set to '0'

**Bit D5 – Inversion On/Off**

'0' = Inversion is Off.

'1' = Inversion is On.

This bit is not applicable for this project, so it is set to '0'

**Bit D4 – All Pixels On**

This bit is not applicable for this project, so it is set to '0'

**Bit D3 – All Pixels Off**

This bit is not applicable for this project, so it is set to '0'

**Bits D2, D1, D0 – Gamma Curve Selection**

| Gamma Curve Selected | D2 | D1 | D0 | Gamma Set (R26h) Parameter |
|---|---|---|---|---|
| Gamma Curve 1 | 0 | 0 | 0 | GC0 |
| Gamma Curve 2 | 0 | 0 | 1 | GC1 |
| Gamma Curve 3 | 0 | 1 | 0 | GC2 |
| Gamma Curve 4 | 0 | 1 | 1 | GC3 |
| Not Defined | 1 | 0 | 0 | Not Defined |
| Not Defined | 1 | 0 | 1 | Not Defined |
| Not Defined | 1 | 1 | 0 | Not Defined |
| Not Defined | 1 | 1 | 1 | Not Defined |

Restrictions

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | No change |
| H/W Reset | 00h |

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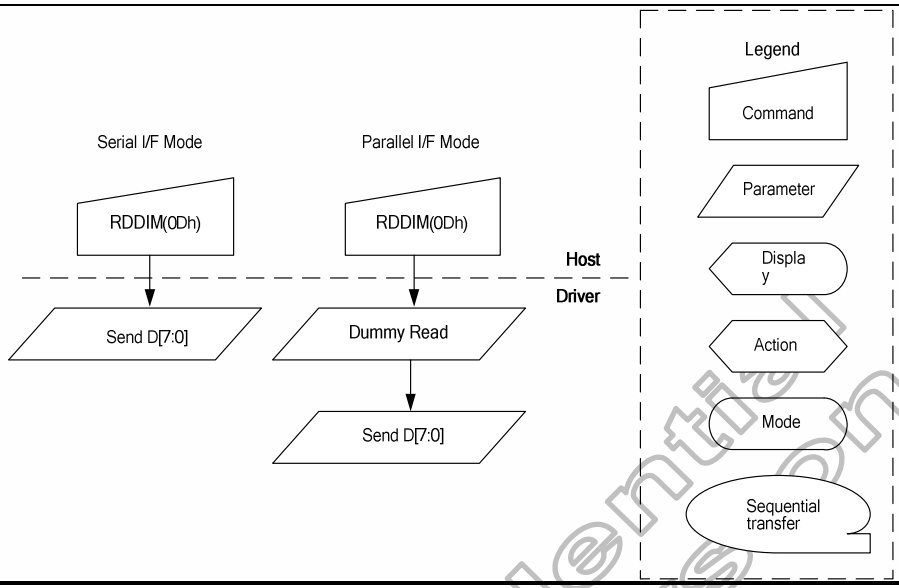
Flow Chart

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### 6.2.12 Read display signal mode (0Eh)

| 0E H | RDDSM (Read Display Signal Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | D6 | D5 | D4 | D3 | D2 | 0 | D0 | xx |

**Description**

This command indicates the current status of the display as described in the table below:
Bit D7 – Tearing Effect Line On/Off
'0' = Tearing Effect Line Off.
'1' = Tearing Effect On.
Bit D6 – Tearing Effect Line Output Mode, see section 5.2 for mode definitions.
'0' = Mode 1.
'1' = Mode 2.
Bit [D5:D1] – are for future use and are set to '0'.
Bit D0 – Error on DSI, see section **"6.2.4RDNUMPE: Read Number of the Errors on DSI (05h)"**
'0' = No Error.
'1' = Error.

**Restrictions**

-

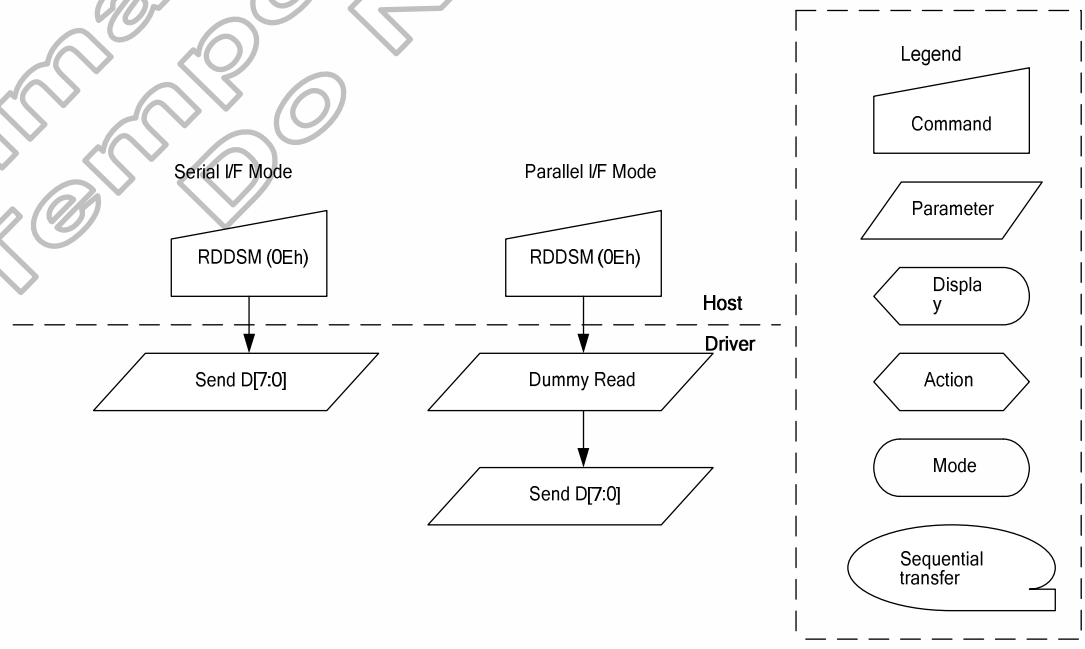
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.13 Read display self-diagnostic result (0Fh)

| 0F H | RDDSDR (Read Display Self-Diagnostic Result) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | D6 | 0 | 0 | 0 | 0 | 0 | D0 | - |

**Description**

The display module returns the self-diagnostic results following a Sleep Out command.
Bit D7 – Register Loading Detection
Bit D6 – Functionality Detection
Bits D[5:1] – Reserved, Set to '0'.
Bit D0 – Checksums comparison
'0' = Checksums are same
'1' = Checksums are not same

**Restrictions**

-

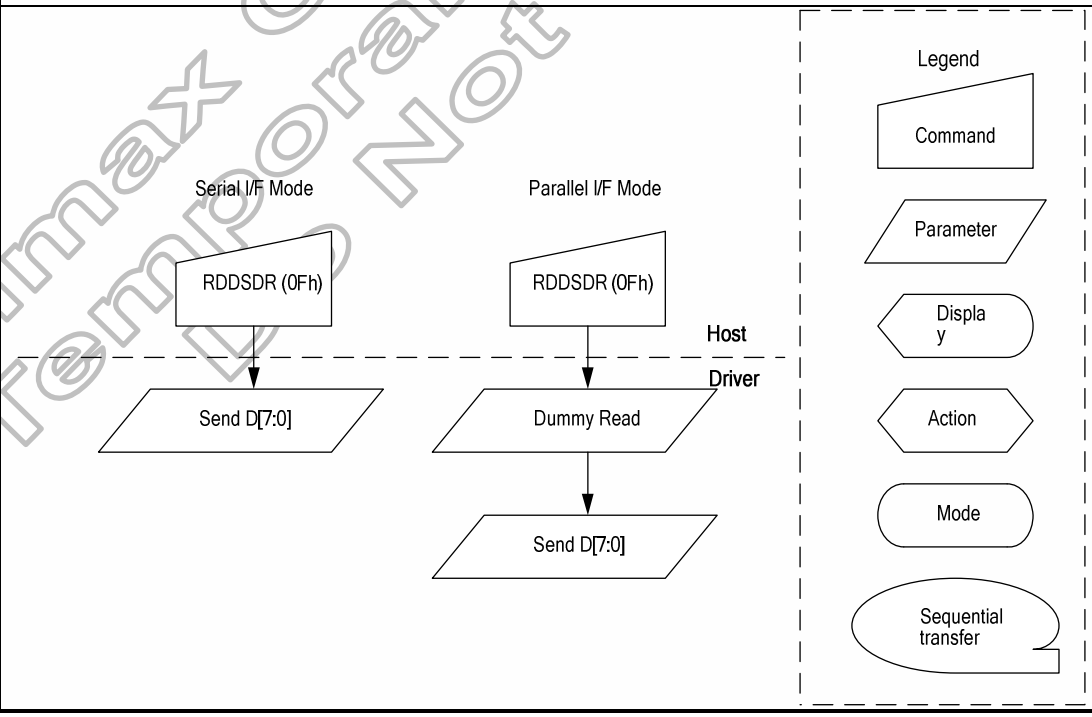
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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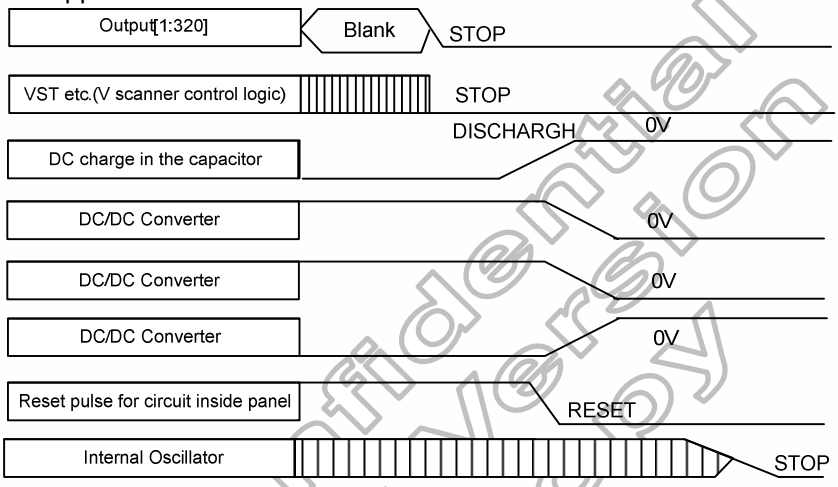
### 6.2.14 Sleep in (10h)

| 10 H | SLPIN (Sleep In) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.<br>  <br><br>MCU interface and memory are still working and the memory keeps its contents. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).<br>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.<br>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. | | | | | | | | | | | | |
| Register Availability | Status \| Availability<br>Normal Mode On, Idle Mode Off, Sleep Out \| Yes<br>Normal Mode On, Idle Mode On, Sleep Out \| Yes<br>Partial Mode On, Idle Mode Off, Sleep Out \| Yes<br>Partial Mode On, Idle Mode On, Sleep Out \| Yes<br>Sleep In or Booster Off \| Yes | | | | | | | | | | | | |
| Default | Status \| Default Value<br>Power On Sequence \| Sleep In Mode<br>S/W Reset \| Sleep In Mode<br>H/W Reset \| Sleep In Mode | | | | | | | | | | | | |

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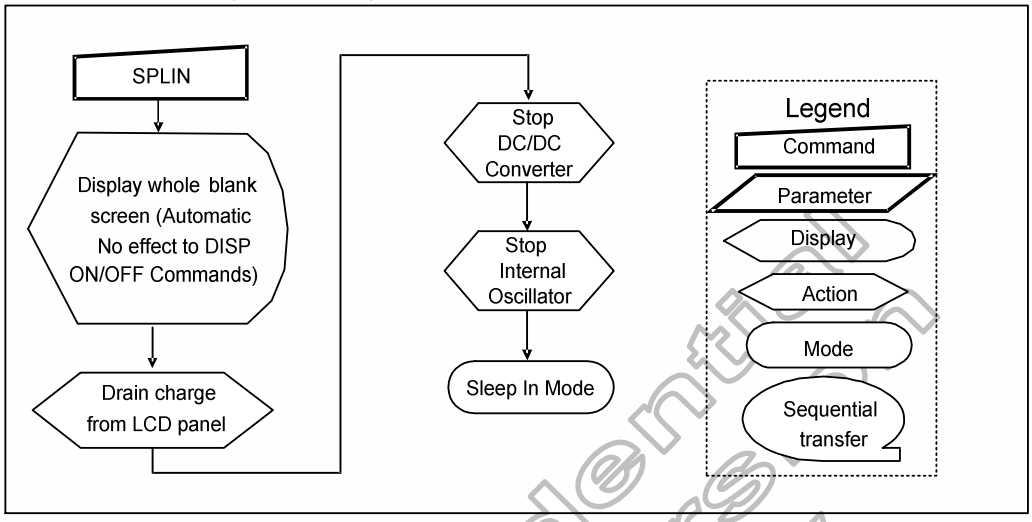
Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.

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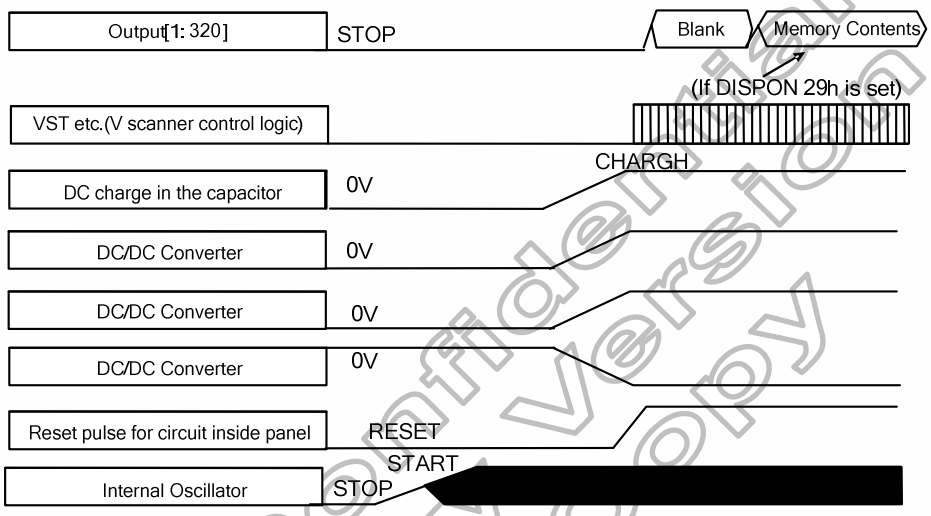
### 6.2.15 Sleep out (11h)

| 11 H | SLPOUT (Sleep Out) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command turns off sleep mode.<br>In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.<br>  <br> | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).<br>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.<br>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.<br>The display module is doing self-diagnostic functions during this 5msec.<br>It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep In Mode |
| S/W Reset | Sleep In Mode |
| H/W Reset | Sleep In Mode |

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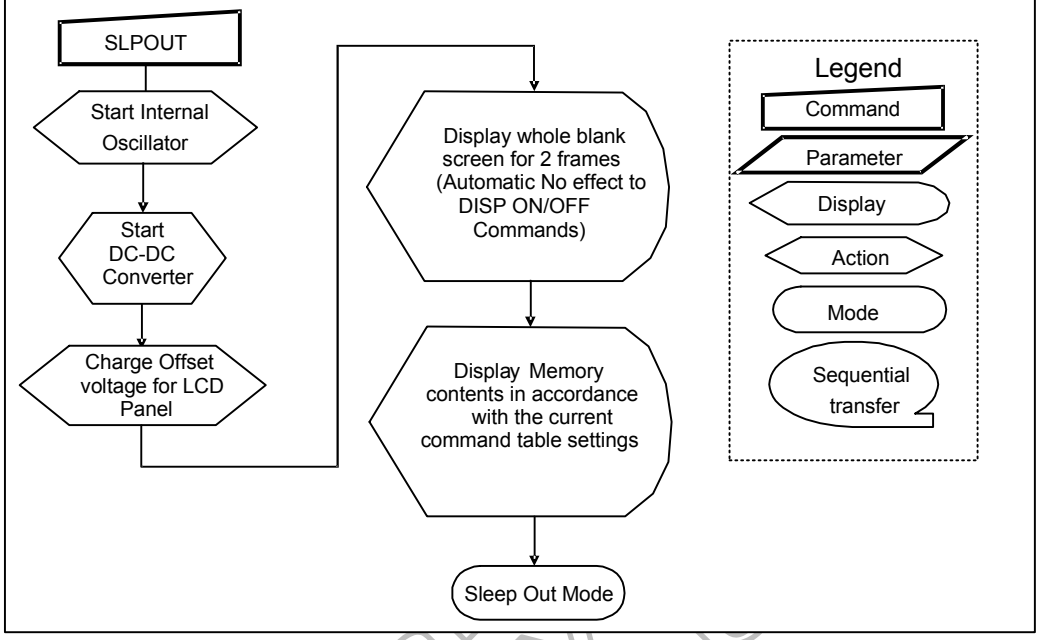
Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.

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### 6.2.16 Partial mode on (12h)

| 12 H | PTLON (Partial Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. | | | | | | | | | | | | |
| Restrictions | This command has no effect when Partial mode is active. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Normal Display Mode On |
| S/W Reset | Normal Display Mode On |
| H/W Reset | Normal Display Mode On |

| Flow Chart | See Partial Area (30h) |
|---|---|

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### 6.2.17 Normal display mode on (13h)

| 13 H | NORON (Normal Display Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. | | | | | | | | | | | | |
| Restriction | This command has no effect when Normal mode is active. | | | | | | | | | | | | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In or Booster Off / Yes | | | | | | | | | | | | |
| Default | Status / Default Value<br>Power On Sequence / Normal Display Mode On<br>S/W Reset / Normal Display Mode On<br>H/W Reset / Normal Display Mode On | | | | | | | | | | | | |
| Flow Chart | See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command. | | | | | | | | | | | | |

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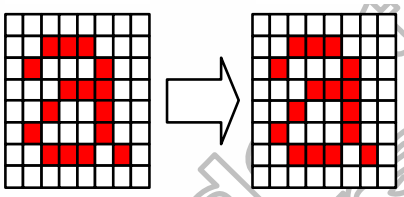
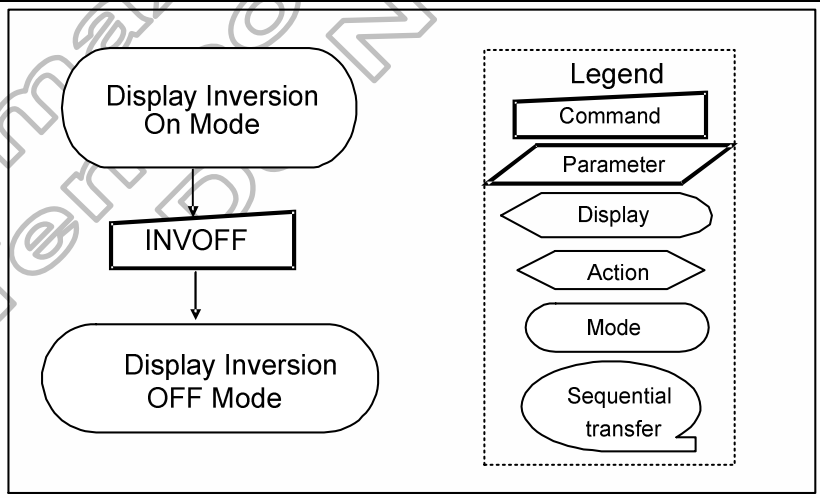
### 6.2.18 Display inversion off (20h)

| 20 H | INVOFF (Display Inversion Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is used to recover from display inversion mode.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>(Example)<br>memory display<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in inversion off mode. | | | | | | | | | | | | |

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In or Booster Off | Yes |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display Inversion Off |
| | S/W Reset | Display Inversion Off |
| | H/W Reset | Display Inversion Off |

Flow Chart

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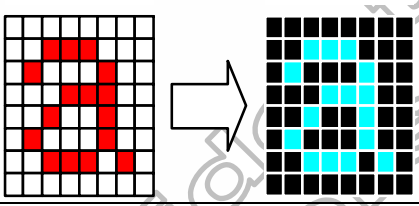
### 6.2.19 Display inversion on (21h)

| 21 H | INVON (Display Inversion On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is used to enter into display inversion mode.<br>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.<br>This command does not change any other status.<br>(Example)<br>memory display<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in inversion on mode. | | | | | | | | | | | | |

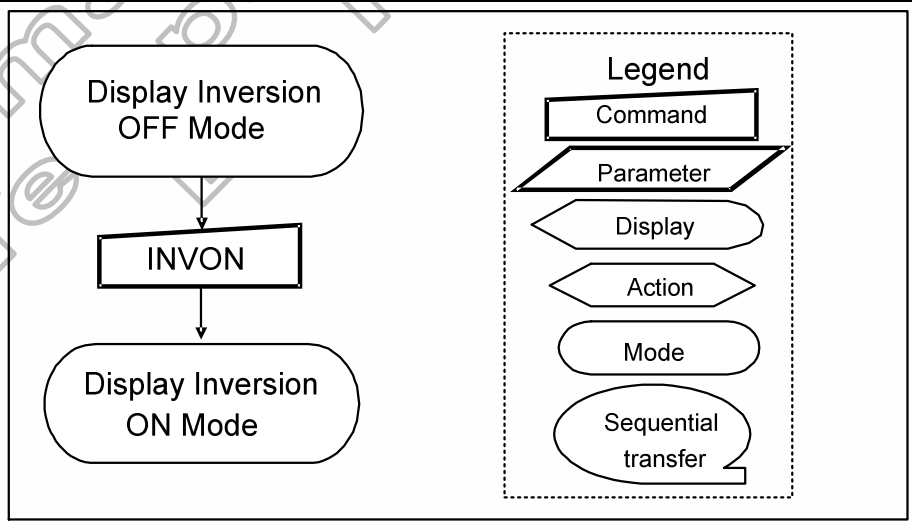
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion Off |
| S/W Reset | Display Inversion Off |
| H/W Reset | Display Inversion Off |

Flow Chart

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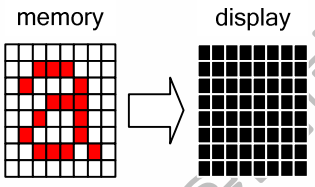
### 6.2.20 All pixel off (22h)

| 22h | ALLPOFF (All Pixel Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status<br>(Example)<br>  <br><br>'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in all pixels off mode. | | | | | | | | | | | | |

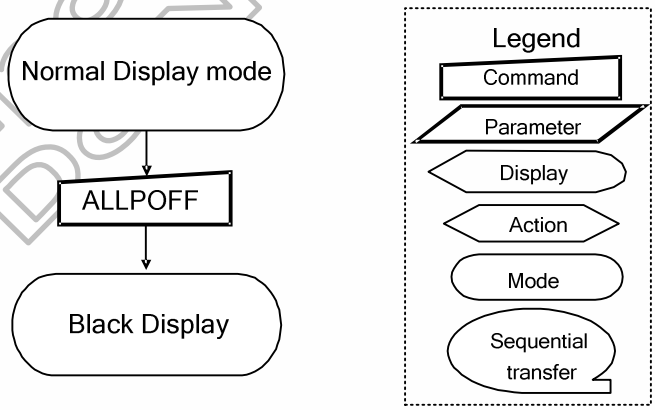
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | off |
| S/W Reset | off |
| H/W Reset | off |

Flow Chart

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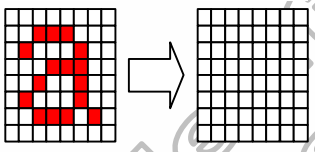
### 6.2.21 All pixel on (23h)

| 23h | ALLPON(All Pixel On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command turns the display panel white in 'Sleep out ' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>(Example)<br>memory display<br>  <br>'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in all pixels on mode. | | | | | | | | | | | | |

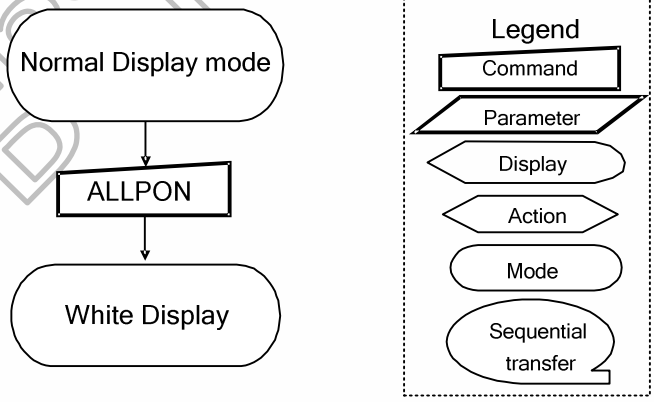
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | off |
| S/W Reset | off |
| H/W Reset | off |

Flow Chart

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### 6.2.22 Gamma set (26h)

| 26 H | GAMSET (Gamma Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 |
| Parameter | 1 | ↑ | 1 | - | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 | - |

**Description**

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:

| GC[7..0] | Parameter | Curve Selected |
|---|---|---|
| 01h | GC0 | Gamma Curve 1 |
| 02h | GC1 | Gamma Curve 2 |
| 04h | GC2 | Gamma Curve 3 |
| 08h | GC3 | Gamma Curve 4 |

**Note:** All other values are undefined.

**Restriction**

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

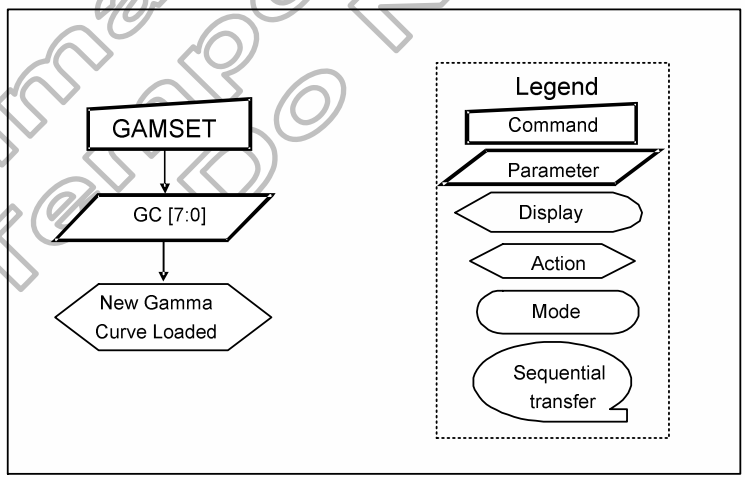
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 01h |
| S/W Reset | 01h |
| H/W Reset | 01h |

**Flow Chart**

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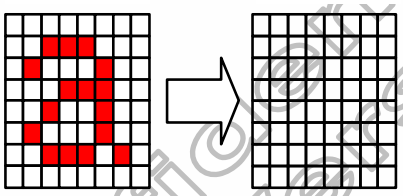
### 6.2.23 Display off (28h)

| 28 H | DISPOFF (Display Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>There will be no abnormal visible effect on the display.<br>(Example)<br>memory display<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display off mode. | | | | | | | | | | | | |

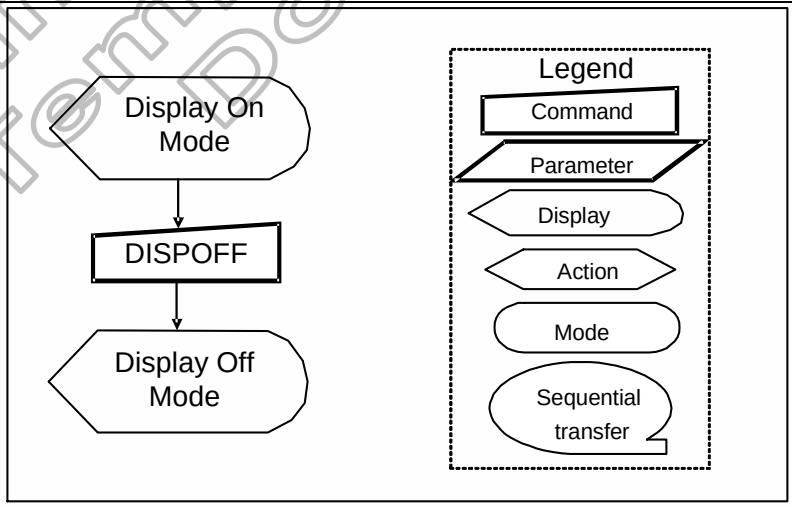
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Off |
| S/W Reset | Display Off |
| H/W Reset | Display Off |

Flow Chart

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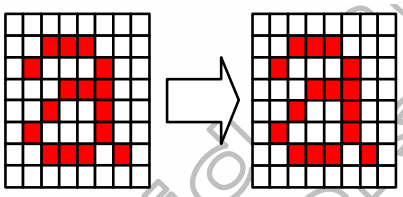
### 6.2.24 Display on (29h)

| 29 H | DISPON (Display On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>(Example)<br>memory display<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display on mode. | | | | | | | | | | | | |

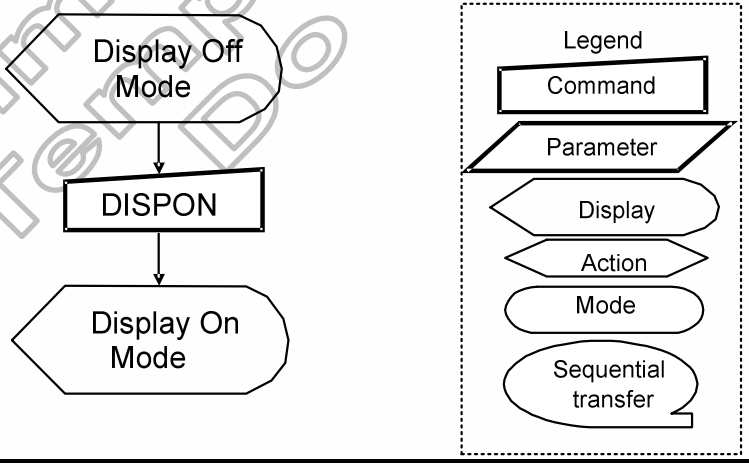
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Off |
| S/W Reset | Display Off |
| H/W Reset | Display Off |

Flow Chart

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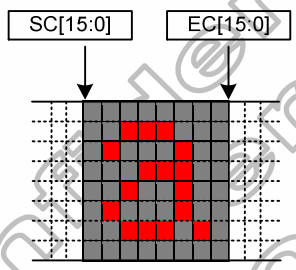
### 6.2.25 Column address set (2Ah)

| 2A H | CASET (Column Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A |
| 1st parameter | 1 | ↑ | 1 | - | SC15 | SC14 | SC13 | SC12 | SC11 | SC10 | SC9 | SC8 | Note 1 |
| 2nd parameter | 1 | ↑ | 1 | - | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | |
| 3rd parameter | 1 | ↑ | 1 | - | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 | Note 1 |
| 4th parameter | 1 | ↑ | 1 | - | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | |

**Description**

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)




**Restriction**

SC[15:0] always must be equal to or less than EC[15:0]
**Note:** When SC[15:0] or EC[15:0] is greater than maximum address like below, data out of range will be ignored
0000h<=SC[15:0]<=EC[15:0] <=013Fh ,when MADCTL's B5=0
0000h<=SC[15:0]<=EC[15:0] <=01DFh ,when MADCTL's B5=1

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SC[15:0]=0000h | EC[15:0]=013Fh |
| SW Reset | SC[15:0]=0000h | EC[15:0]=013Fh |
| HW Reset | SC[15:0]=0000h | EC[15:0]=013Fh |

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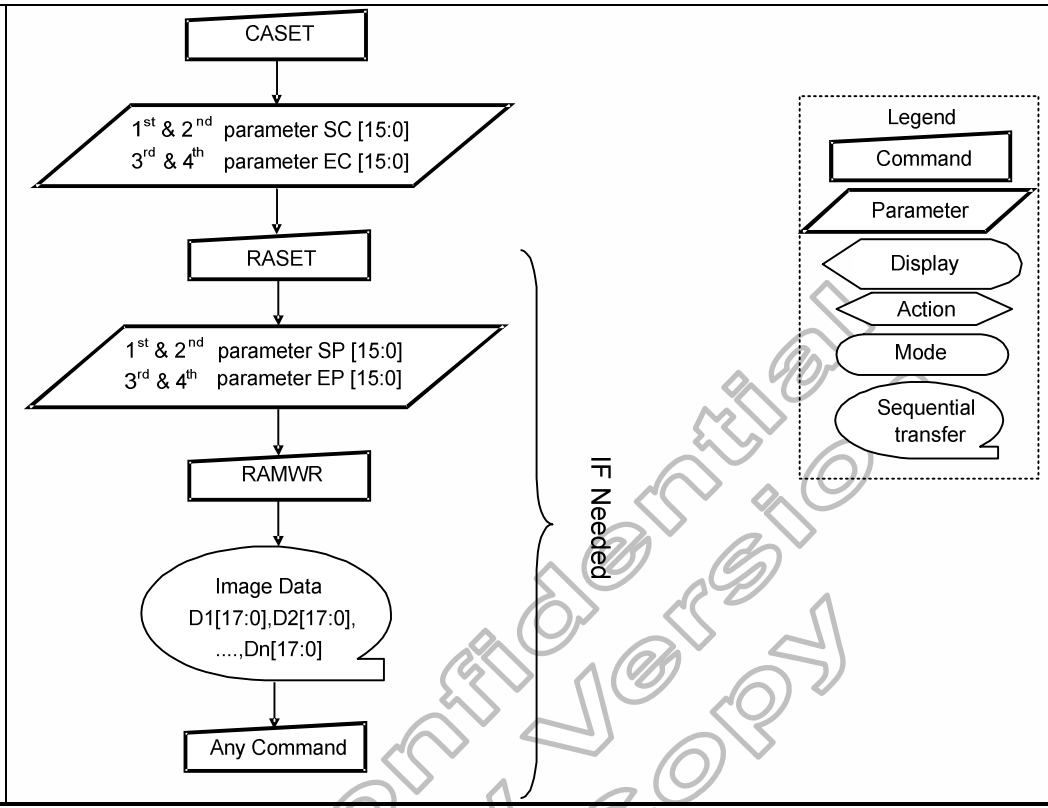
Flow Chart

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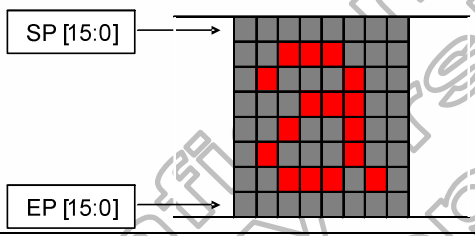
### 6.2.26 Page address set (2Bh)

| 2B H | PASET (Page Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B |
| 1st parameter | 1 | ↑ | 1 | - | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | Note 1 |
| 2nd parameter | 1 | ↑ | 1 | - | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | |
| 3rd parameter | 1 | ↑ | 1 | - | EP15 | EP14 | EP13 | EP12 | EP11 | EP10 | EP9 | EP8 | Note 1 |
| 4th parameter | 1 | ↑ | 1 | - | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | |

**Description**

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)




**Restriction**

SP[15:0] always must be equal to or less than EP[15:0]
**Note:** When SP[15:0] or EP[15:0] is greater than maximum row address like below, data of out of range will be ignored
0000h<=SP[15:0]<=EP[15:0]<=01DFh (When MADCTL's B5=0)
0000h<=SP[15:0]<=EP[15:0]<=013Fh (When MADCTL's B5=1)

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SP[15:0]=0000h | EP[15:0]=01DFh |
| SW Reset | SP[15:0]=0000h | EP[15:0]=01DFh |
| HW Reset | SP[15:0]=0000h | EP[15:0]=01DFh |

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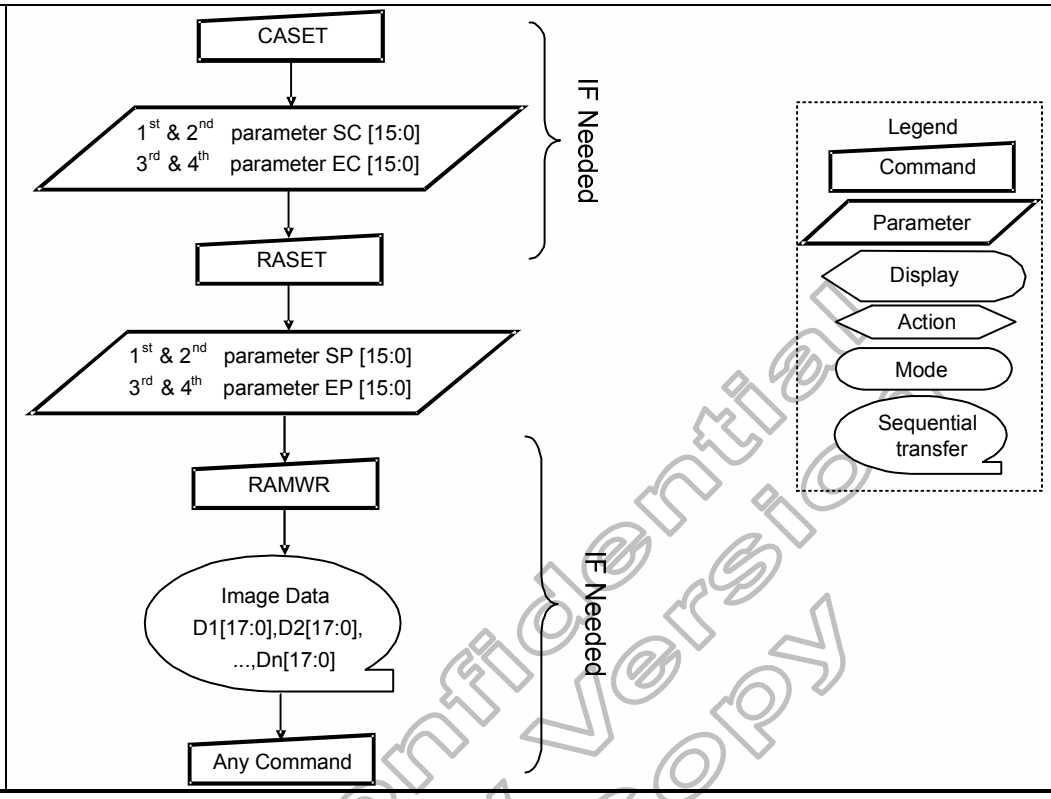
Flow Chart

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### 6.2.27 Memory write (2Ch)

| 2C H | RAMWR (Memory Write) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C |
| 1st parameter | 1 | ↑ | 1 | D1[15:0] | | | | | | | | | 00..FF |
| : | 1 | ↑ | 1 | Dx[15:0] | | | | | | | | | 00..FF |
| nth parameter | 1 | ↑ | 1 | Dn[15:0] | | | | | | | | | 00..FF |

**Description**

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting.
Then D[7:0] is stored in frame memory and the column register and the page register incremented.
Sending any other command can stop frame Write.

**Restriction**

In all color modes, there is no restriction on length of parameters.

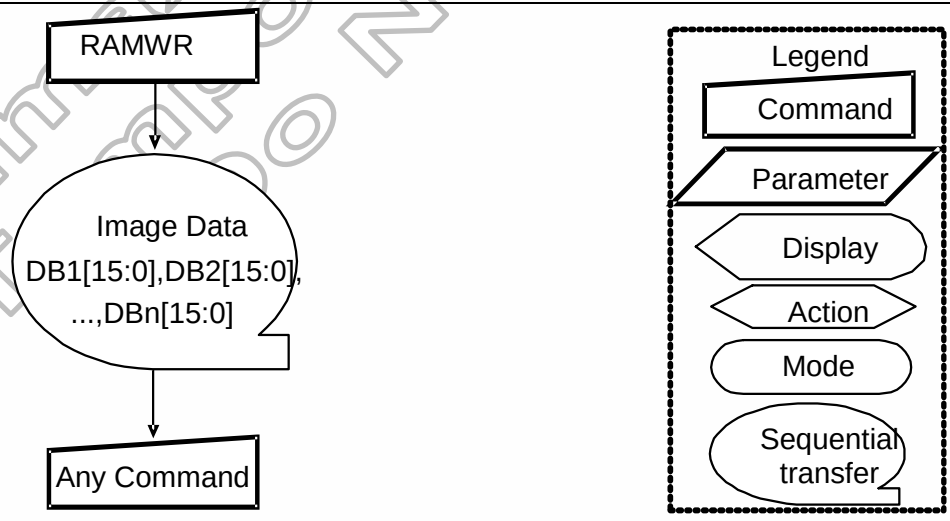
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | No |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |
| H/W Reset | Contents of memory is not cleared |

**Flow Chart**

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### 6.2.28 Memory read (2Eh)

| 2E H | RAMRD (Memory Read) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | ↑ | 1 | D1[15:0] | | | | | | | | | 00..FF |
| : | 1 | ↑ | 1 | Dx[15:0] | | | | | | | | | 00..FF |
| (n+1)th parameter | 1 | ↑ | 1 | Dn[15:0] | | | | | | | | | 00..FF |
| Description | This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status.<br>When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.<br>The Start Column/Start Page positions are different in accordance with MADCTL setting.<br>Then D[7:0] is read back from the frame memory and the column register and the page register incremented<br>Frame Read can be stopped by sending any other command. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

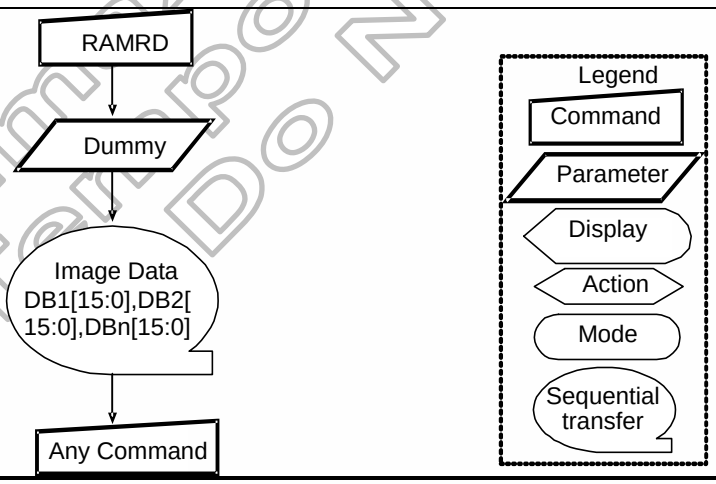
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | No |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |
| H/W Reset | Contents of memory is not cleared |

Flow Chart

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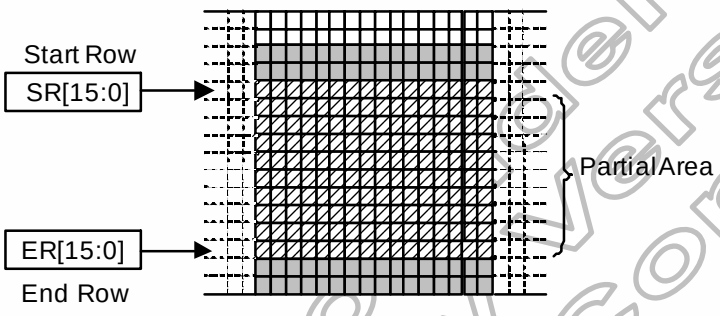
### 6.2.29 Partial area (30h)

| 30 H | PLTAR (Partial Area) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 |
| 1st parameter | 1 | ↑ | 1 | - | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | 0000: 01DF |
| 2nd parameter | 1 | ↑ | 1 | - | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | |
| 3rd parameter | 1 | ↑ | 1 | - | ER15 | ER14 | ER13 | ER12 | ER11 | ER10 | ER9 | ER8 | 0000: 01DF |
| 4th parameter | 1 | ↑ | 1 | - | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | |

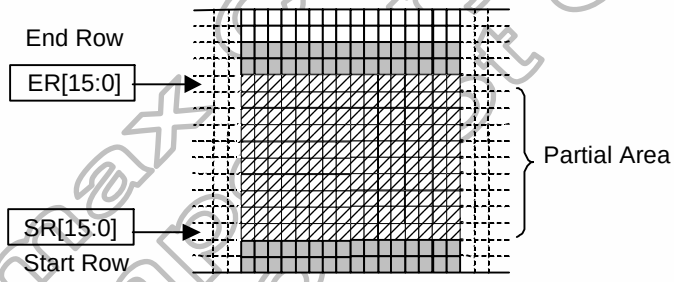
**Description**

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

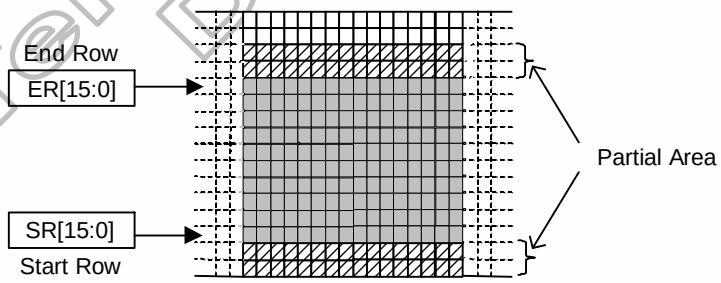
If End Row > Start Row when MADCTL B4(ML) = 0:




If End Row > Start Row when MADCTL B4(ML) = 1:




If End Row<Start Row when MADCTL's B4(ML) = 0:




If End Row = Start Row then the Partial Area will be one row deep.

**Restriction**

SR[15:0] and ER[15:0] cannot be exceeding than 01DFh.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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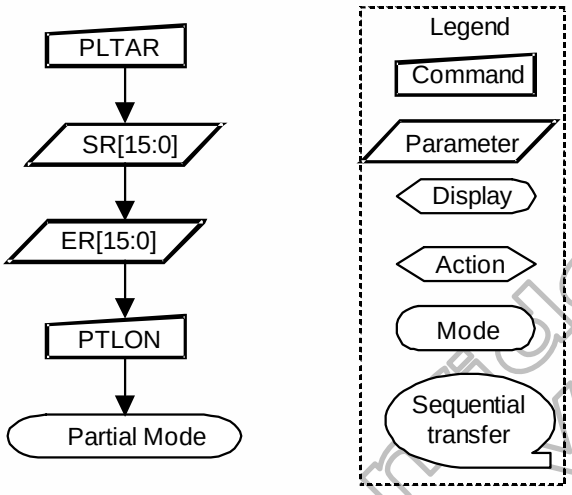
**Default**

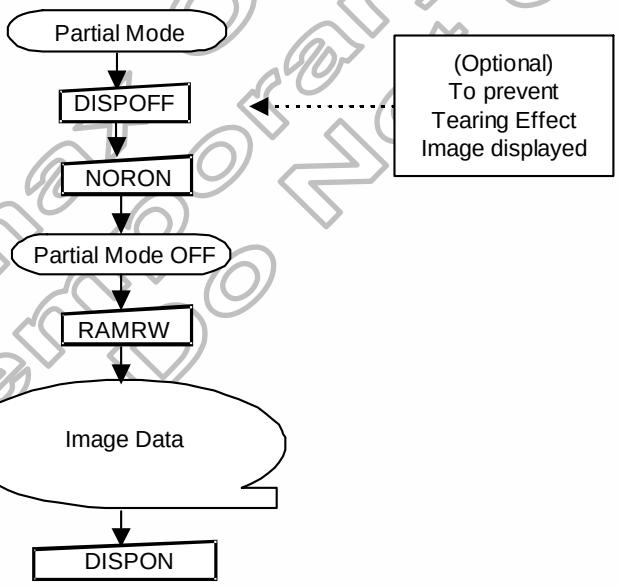
| Status | Default Value | |
|---|---|---|
| Power On Sequence | SR[15:0]=0000h | ER[15:0]=01DFh |
| S/W Reset | SR[15:0]=0000h | ER[15:0]=01DFh |
| H/W Reset | SR[15:0]=0000h | ER[15:0]=01DFh |

**Flow Chart**

1. To Enter Partial Display Mode:




2. To Leave Partial Display Mode

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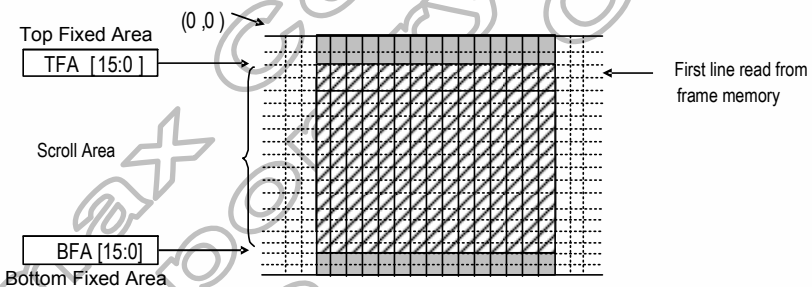
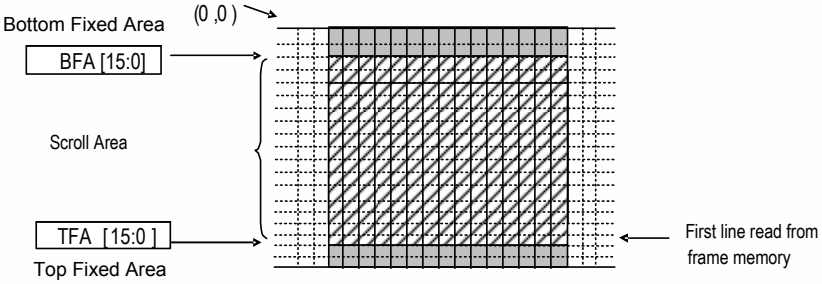
### 6.2.30 Vertical scrolling definition (33h)

| 33 H | VSCRDEF (Vertical Scrolling Definition) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 |
| 1st parameter | 1 | ↑ | 1 | - | TFA 15 | TFA 14 | TFA 13 | TFA 12 | TFA 11 | TFA 10 | TFA 9 | TFA 8 | 0000: 01E0 |
| 2nd parameter | 1 | ↑ | 1 | - | TFA 7 | TFA 6 | TFA 5 | TFA 4 | TFA 3 | TFA 2 | TFA 1 | TFA 0 | |
| 3rd parameter | 1 | ↑ | 1 | - | VSA 15 | VSA 14 | VSA 13 | VSA 12 | VSA 11 | VSA 10 | VSA 9 | VSA 8 | 0000: 01E0 |
| 4th parameter | 1 | ↑ | 1 | - | VSA 7 | VSA 6 | VSA 5 | VSA 4 | VSA 3 | VSA 2 | VSA 1 | VSA 0 | |
| 5th parameter | 1 | ↑ | 1 | - | BFA 15 | BFA 14 | BFA 13 | BFA 12 | BFA 11 | BFA 10 | BFA 9 | BFA 8 | 0000: 01E0 |
| 6th parameter | 1 | ↑ | 1 | - | BFA 7 | BFA 6 | BFA 5 | BFA 4 | BFA 3 | BFA 2 | BFA 1 | BFA 0 | |
| Description | This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer. | | | | | | | | | | | | |
| |  | | | | | | | | | | | | |
| | When MADCTL B4=1<br>The 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display). | | | | | | | | | | | | |
| |  | | | | | | | | | | | | |
| Restriction | The condition is (TFA+VSA+BFA)=480, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write. | | | | | | | | | | | | |

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**Register Availability**

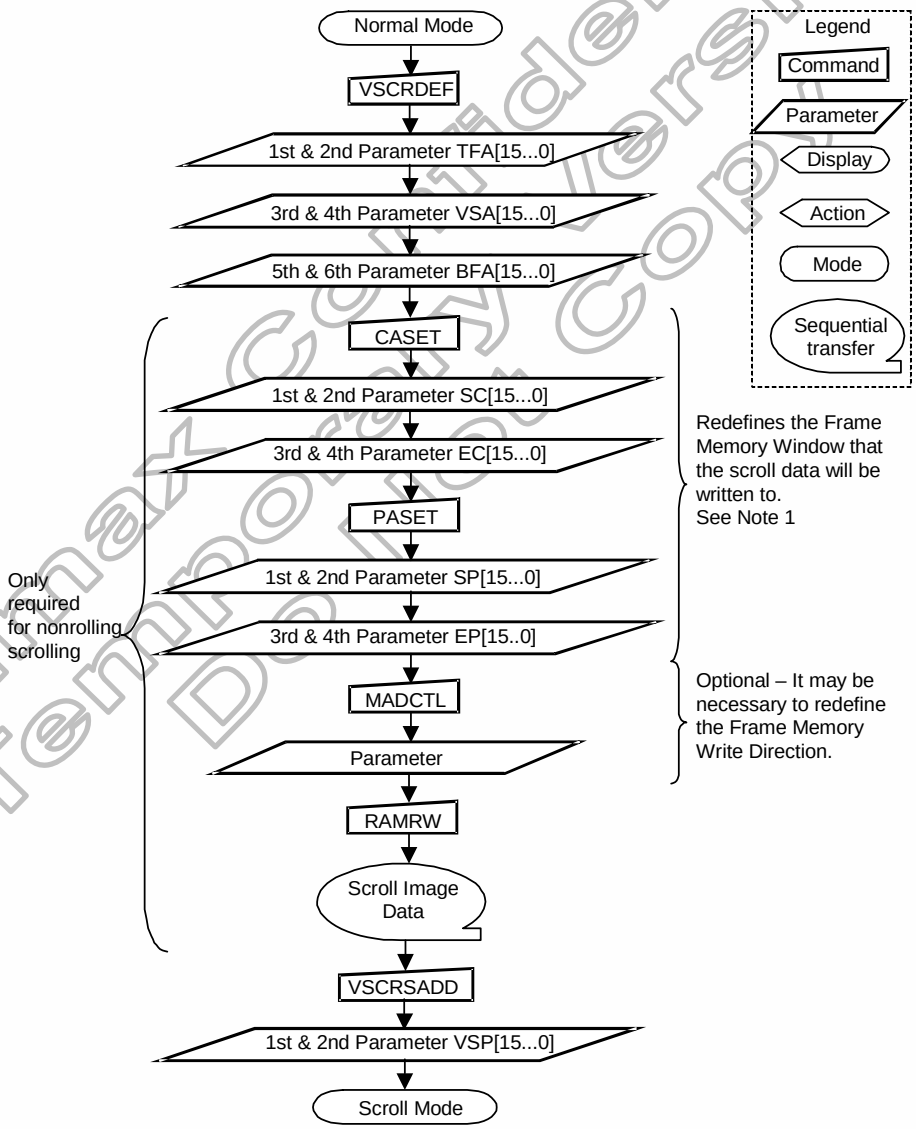
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| Power On Sequence | TFA[15:0]=0000 | VSA[15:0]=01E0h | BFA[15:0]=0000 |
| S/W Reset | TFA[15:0]=0000 | VSA[15:0]=01E0h | BFA[15:0]=0000 |
| H/W Reset | TFA[15:0]=0000 | VSA[15:0]=01E0h | BFA[15:0]=0000 |

**Flow Charts**

1. To enter Vertical Scroll Mode:




**Note:** The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

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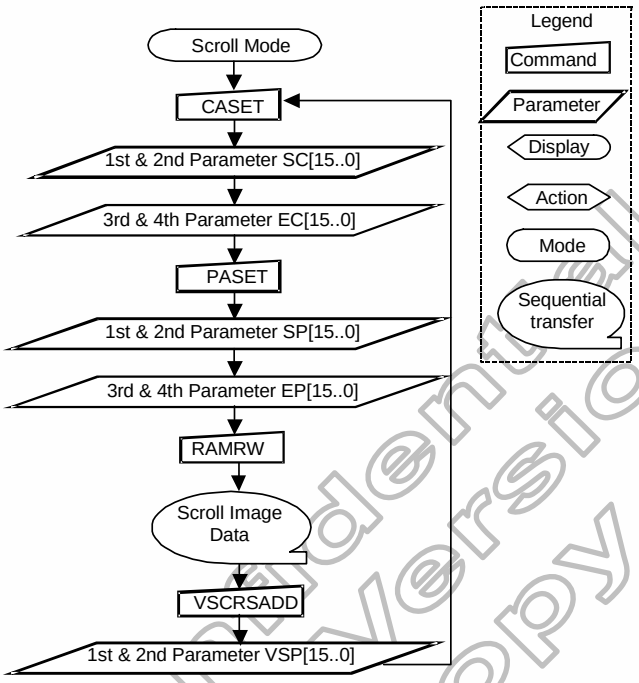
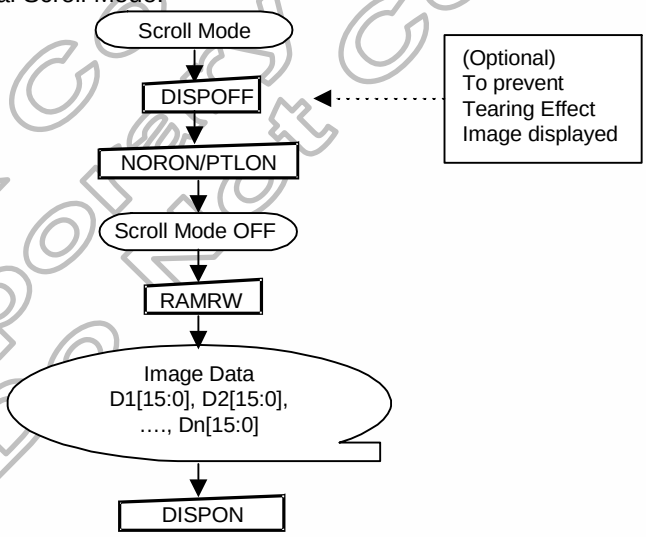
2. Continuous Scroll:




3. To Leave Vertical Scroll Mode:




**Note**: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

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### 6.2.31 Tearing effect line off (34h)

| 34 H | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command is used to turn OFF the Tearing Effect output signal from the TE signal line. | | | | | | | | | | | | |
| Restriction | This command has no effect when Tearing Effect output is already OFF. | | | | | | | | | | | | |

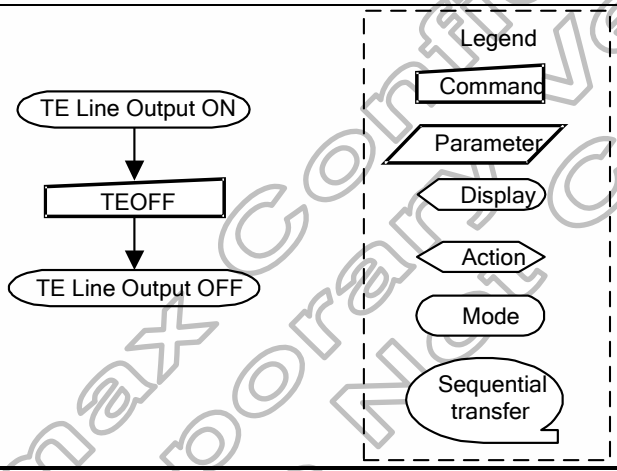
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Tearing Effect Off |
| S/W Reset | Tearing Effect Off |
| H/W Reset | Tearing Effect Off |

Flow Chart

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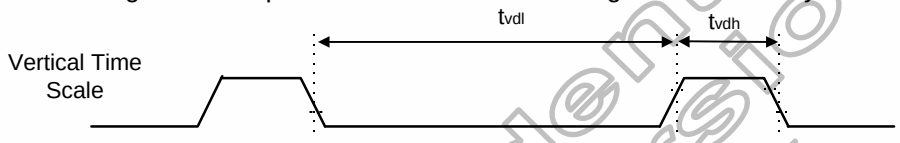
### 6.2.32 Tearing effect line on (35h)

| 35 H | TEON (Tearing Effect Line ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 |
| 1stparameter | 0 | ↑ | 1 | - | - | - | - | - | - | - | - | TEMODE | - |

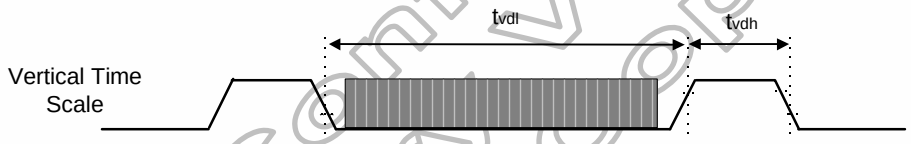
**Description**

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only:




When TEMODE=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:




**Note:** During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

**Restriction**

This command has no effect when Tearing Effect output is already ON.

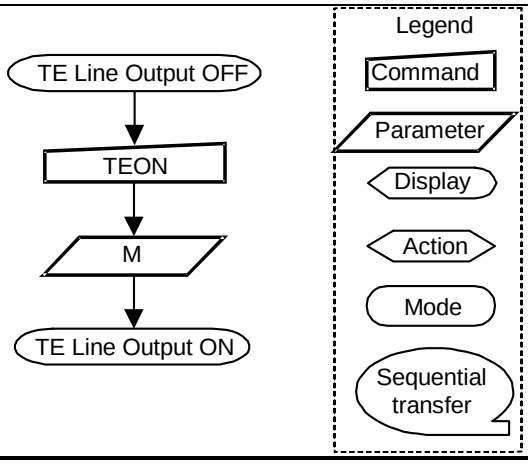
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Tearing Effect Off |
| S/W Reset | Tearing Effect Off |
| H/W Reset | Tearing Effect Off |

**Flow Chart**

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## 6.2.33 Memory access control (36h)

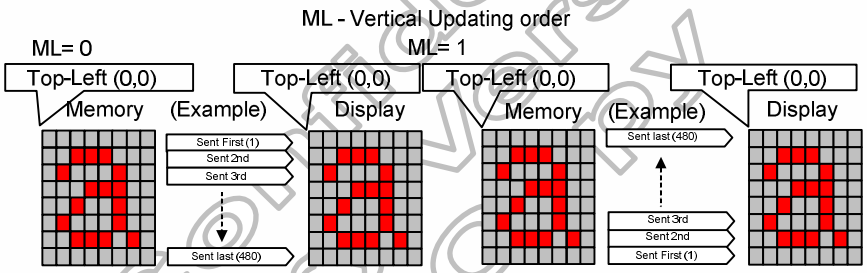
| 36 H | MADCTL (Memory Access Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 |
| 1st parameter | 1 | ↑ | 1 | - | MY | MX | MV | ML | BGR | SS | - | - | - |

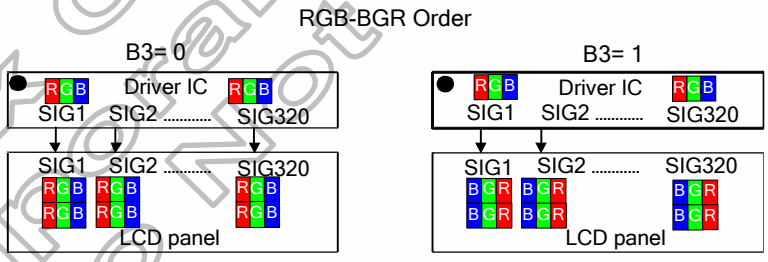
Description

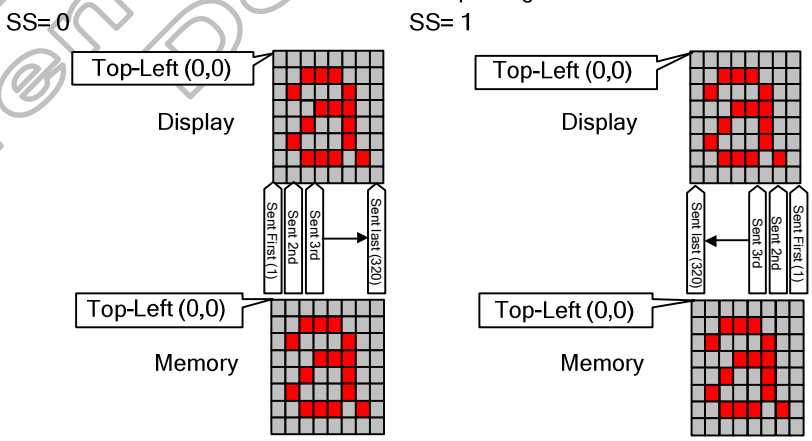
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

| BIT | NAME | DESCRIPTION |
|---|---|---|
| B7 | PAGE ADDRESS ORDER (MY) | These 3 bits controls MCU to memory write/read direction. |
| B6 | COLUMN ADDRESS ORDER (MX) | |
| B5 | PAGE/COLUMN SELECTION (MV) | |
| B4 | Vertical ORDER (ML) | LCD vertical refresh direction control |
| B3 | RGB-BGR ORDER (BGR) | Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel) |
| B2 | Horizontal ORDER (SS) | LCD horizontal refresh direction control |




Note: Top-Left (0,0) means a physical memory location.
Bit D1 – Switching Between Segment Output and RAM
This bit is not applicable for this project, so it is set to '0'
Bit D0 – Switching Between Common Output and RAM
This bit is not applicable for this project, so it is set to '0'

Restriction

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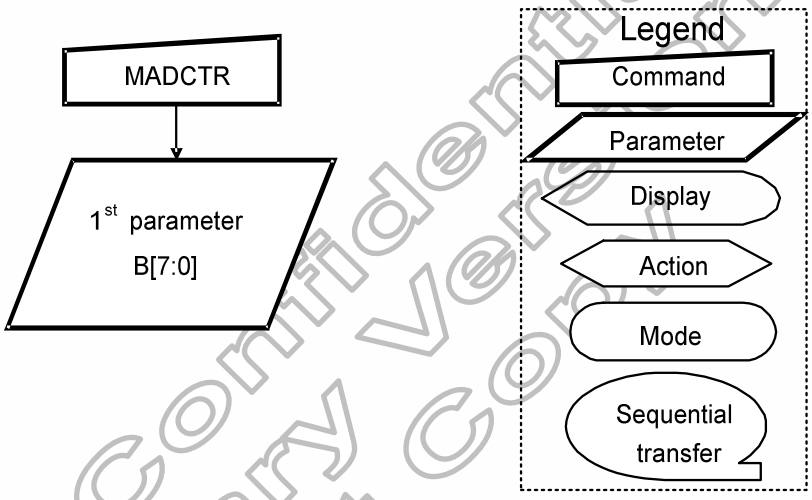
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | No change |
| H/W Reset | 00h |

**Flow Chart**

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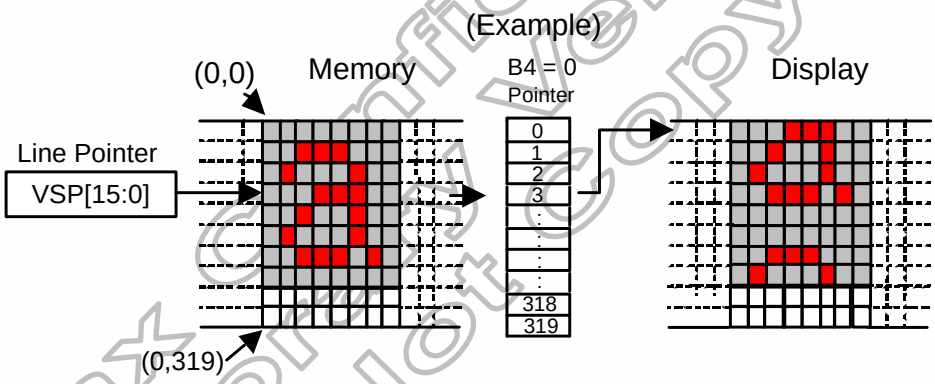
### 6.2.34 Vertical scrolling start address (37h)

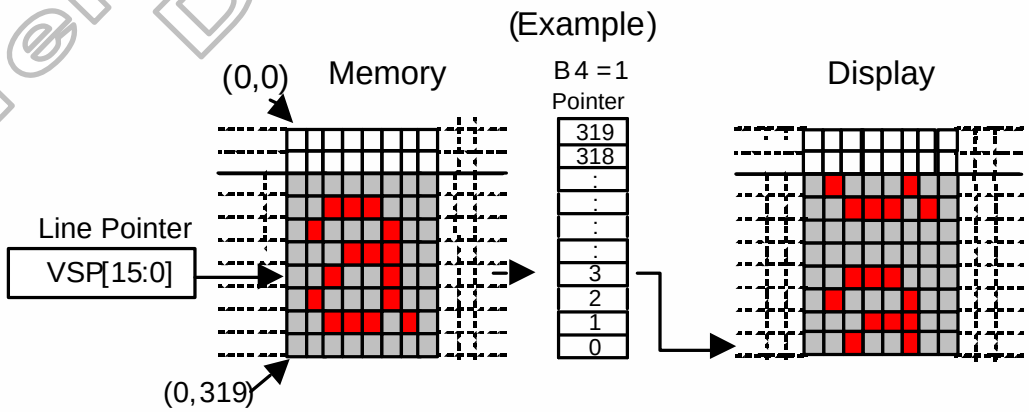
| 37 H | VSCRSADD (Vertical Scrolling Start Address) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37 |
| 1st parameter | 1 | 1 | ↑ | - | VSP 15 | VSP 14 | VSP 13 | VSP 12 | VSP 11 | VSP 10 | VSP 9 | VSP 8 | 01. DF |
| 2nd parameter | 1 | 1 | ↑ | - | VSP 7 | VSP 6 | VSP 5 | VSP 4 | VSP 3 | VSP 2 | VSP 1 | VSP 0 | |

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When MADCTL B4='0'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '318'd' and VSP = '3d'




When MADCTL B4='1'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02d, Vertical Scrolling Area VSA = '318d' and VSP = '3d'




When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

| Restriction | Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel. |
|---|---|

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

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### 6.2.35 Idle mode off (38h)

| 38 H | IDMOFF (Idle Mode Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is used to recover from Idle mode on.<br>In the idle off mode, LCD can display maximum 262,144 colors. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in idle off mode. | | | | | | | | | | | | |

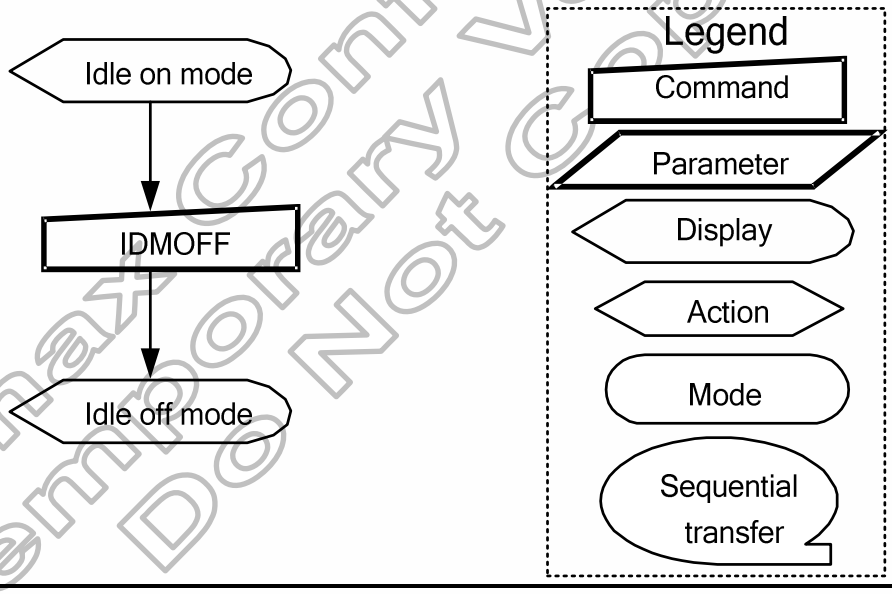
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Idle Mode Off |
| S/W Reset | Idle Mode Off |
| H/W Reset | Idle Mode Off |

Flow Chart

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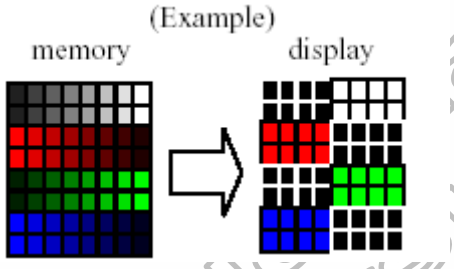
### 6.2.36 Idle mode on (39h)

| 39 H | IDMON (Idle Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |

**Description**

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.




| Memory contents vs. Display Color | | | |
|---|---|---|---|
| | $R_5 R_4 R_3 R_2 R_1 R_0$ | $G_5 G_4 G_3 G_2 G_1 G_0$ | $B_5 B_4 B_3 B_2 B_1 B_0$ |
| Black | 0XXXXX | 0XXXXX | 0XXXXX |
| Blue | 0XXXXX | 0XXXXX | 1XXXXX |
| Red | 1XXXXX | 0XXXXX | 0XXXXX |
| Magenta | 1XXXXX | 0XXXXX | 1XXXXX |
| Green | 0XXXXX | 1XXXXX | 0XXXXX |
| Cyan | 0XXXXX | 1XXXXX | 1XXXXX |
| Yellow | 1XXXXX | 1XXXXX | 0XXXXX |
| White | 1XXXXX | 1XXXXX | 1XXXXX |

**Restriction**

This command has no effect when module is already in idle off mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Idle Mode Off |
| S/W Reset | Idle Mode Off |
| H/W Reset | Idle Mode Off |

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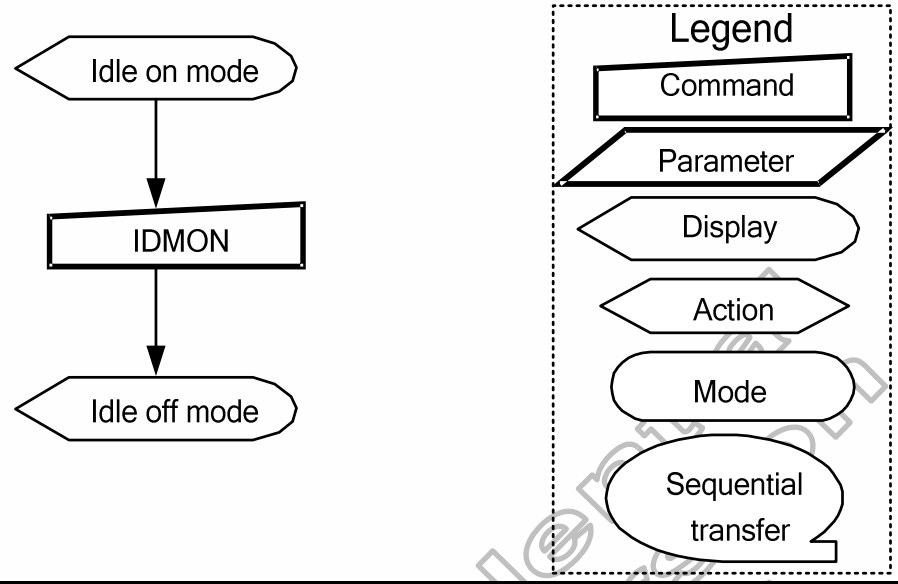
Flow Chart

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### 6.2.37 Interface pixel format (3Ah)

| 3A H | COLMOD (Interface Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A |
| 1st parameter | 1 | ↑ | 1 | - | - | CS EL2 | CS EL1 | CS EL0 | - | D2 | D1 | D0 | |

**Description**

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

DBI interface (RM='0')

| Interface Format | D2 | D1 | D0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| 12 Bit/Pixel | 0 | 1 | 1 |
| Not Defined | 1 | 0 | 0 |
| 16 Bit/Pixel | 1 | 0 | 1 |
| 18 Bit/Pixel | 1 | 1 | 0 |

DPI interface (RM='1')

| Interface Format | CSEL2 | CSEL1 | CSEL0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| Not Defined | 0 | 1 | 1 |
| Not Defined | 1 | 0 | 0 |
| 16 Bit/Pixel | 1 | 0 | 1 |
| 18 Bit/Pixel | 1 | 1 | 0 |
| Not Defined | 1 | 1 | 1 |

**Restriction**

There is no visible effect until the Frame Memory is written to.

**Register Availability**

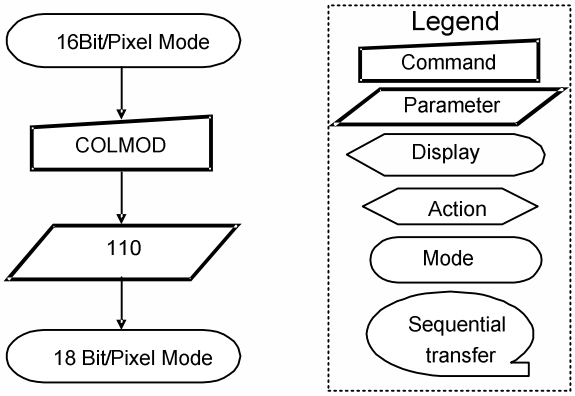
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 18-bit/pixel |
| S/W Reset | No Change |
| H/W Reset | 18-bit/pixel |

**Flow Chart**

Example:

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### 6.2.38 Write_memory_contiune (3Ch)

| 3Ch | Write_memory_contiune | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C |
| 1st parameter | 1 | 1 | ↑ | - | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00..FF |
| : | 1 | 1 | ↑ | - | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | 00..FF |
| Nth parameter | 1 | 1 | ↑ | - | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | 00..FF |

**Description**

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Sending any other command can stop frame Write.
If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

**Restriction**

In all colour modes, there is no restriction on length of parameters.

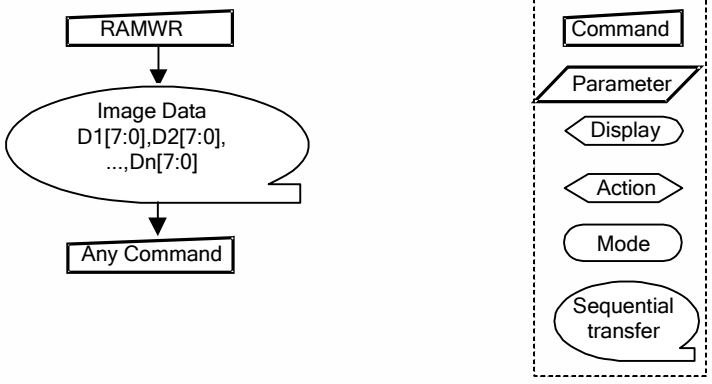
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is set randomly |
| H/W Reset | Contents of memory is set randomly |

**Flow Chart**

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### 6.2.39 Raed_memory_continue (3Eh)

| 3Eh | Raed_memory_continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00..FF |
| : | 1 | ↑ | 1 | - | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | 00..FF |
| (n+1)th parameter | 1 | ↑ | 1 | - | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | 00..FF |
| Description | This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.<br>If set_address_mode B5=0:<br>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.<br>If set_address_mode B5=1:<br>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command. | | | | | | | | | | | | |
| Restriction | Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.<br>A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined. | | | | | | | | | | | | |

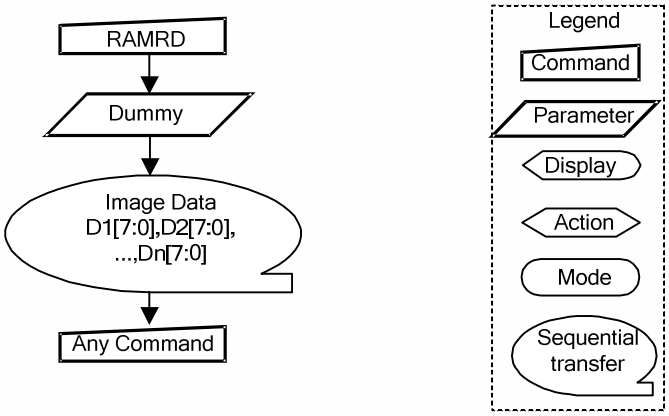
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is set randomly |
| H/W Reset | Contents of memory is set randomly |

Flow Chart

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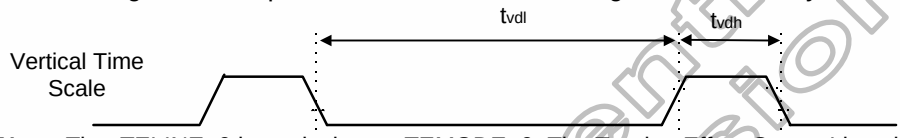
### 6.2.40 Set tear scan line (44h)

| 44 H | TESL(Tear Effect Scan Lines) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 |
| 1st parameter | 1 | 1 | ↑ | - | TELINE[15:8](8'b0) | | | | | | | | 00..FF |
| 2nd parameter | 1 | 1 | ↑ | - | TELINE[7:0](8'b0) | | | | | | | | 00..FF |
| Description | This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line TELINE. The TE signal is not affected by changing MADCTL bit B4.<br>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.<br>The Tearing Effect Output line consists of V-Blanking information only:<br>  <br><br>**Note:** That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode. | | | | | | | | | | | | |
| Restriction | The command has no effect when Tearing Effect output is already ON. | | | | | | | | | | | | |

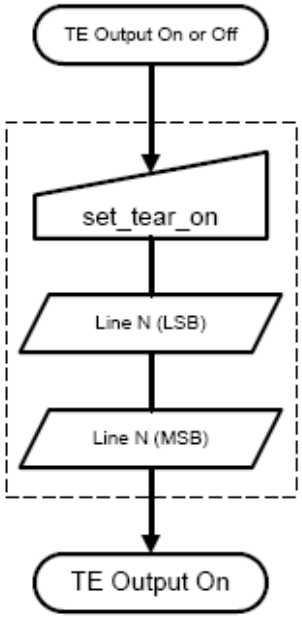
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | TELINE[15:8]=0000h |
| S/W Reset | TELINE[15:8]=0000h |
| H/W Reset | TELINE[15:8]=0000h |

Flow Chart

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### 6.2.41 Get Scan Lines (45h)

| 45 H | GETSL(Mipi new Get Scan Lines) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15~D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 |
| 1st parameter | 1 | ↑ | 1 | - | X | X | X | X | X | X | X | X | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | SL[15:8] | | | | | | | | - |
| 3th parameter | 1 | ↑ | 1 | - | SL[7:0] | | | | | | | | - |
| Description | The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

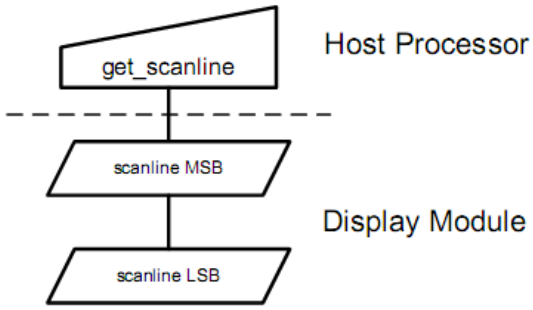
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.42 Write display brightness value (51h)

| 51 H | WRDISBV (Write Display Brightness Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 |
| 1st parameter | 1 | ↑ | 1 | - | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | 00..FF |
| Description | This command is used to adjust the brightness value of the display.<br>The backlight PWM pulse output duty is equal to DBV[7:0]/255 x CABC_duty.<br>For details, please refer to chapter “5.12.2 Brightness control block” | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

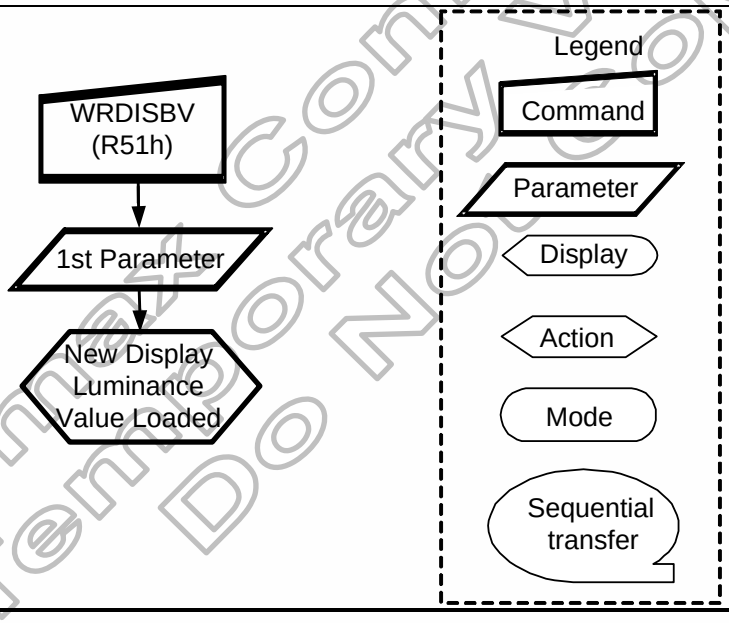
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.43 Read display brightness value (52h)

| 52H | RDDISBV (Read Display Brightness Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | xx |
| 2nd parameter | 1 | 1 | ↑ | - | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | xx |
| Description | This command returns the brightness value of the display.<br><br>DBV[7:0] is reset when display is in sleep-in mode.<br>DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (R53h)" command is '0'.<br>DBV[7:0] is manual set brightness specified with "Write CTRL Display (R53h)" command when bit BCTRL is '1'.<br>When bit BCTRL of "Write CTRL Display (R53h)" command is '1' and bit C1/C0 of "Write Content Adaptive Brightness Control (R55h)" are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (R51h)" command.<br>For details, please refer to chapter "5.12.2 Brightness control block". | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

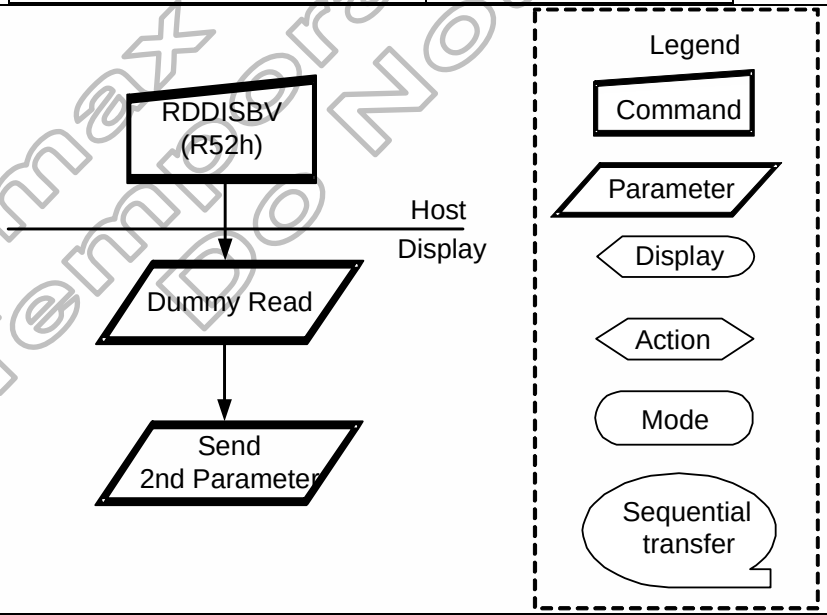
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.44 Write control display (53h)

| 53H | WRCTRLD (Write Control Display) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 |
| 1st parameter | 1 | ↑ | 1 | - | - | - | BCTRL | - | DD | BL | - | - | 00..FF |

**Description**

This command is used to control display brightness.

**BCTRL:** Backlight Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off (Brightness registers are 00h, DBV[7:0] of R52h)
1 = On (Brightness registers are active, according to the other parameters.)

Display Dimming **(DD):** (Only for manual brightness setting)
**DD** = **0**: Display Dimming is off
**DD = 1**: Display Dimming is on

**BL:** Backlight Control On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low. )
1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

**Restriction**

-

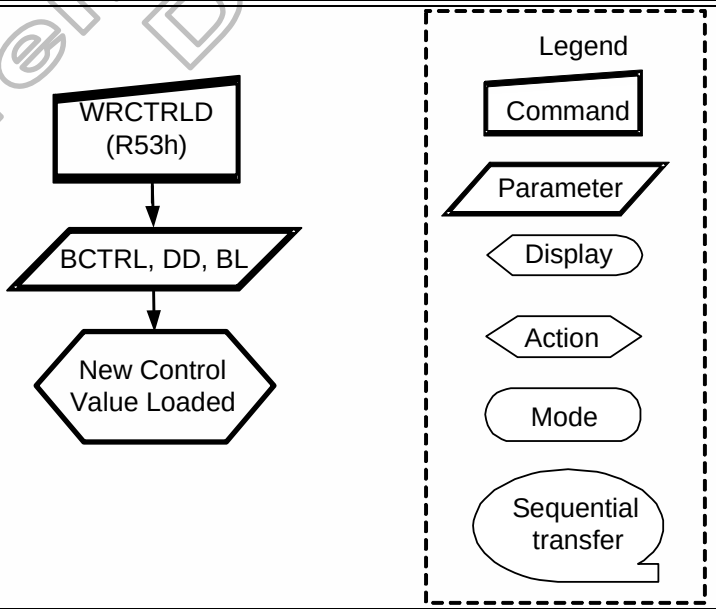
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.45 Read control value display (54h)

| 54H | RDCTRLD (Read Control Value Display) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | xx |
| 2nd parameter | 1 | 1 | ↑ | - | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | xx |

**Description**

This command returns ambient light and brightness control values, see chapter: "Write CTRL Display (R53h)".

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off
1 = On

Display Dimming (DD):
DD = 0: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off
1 = On

**Restriction**

-

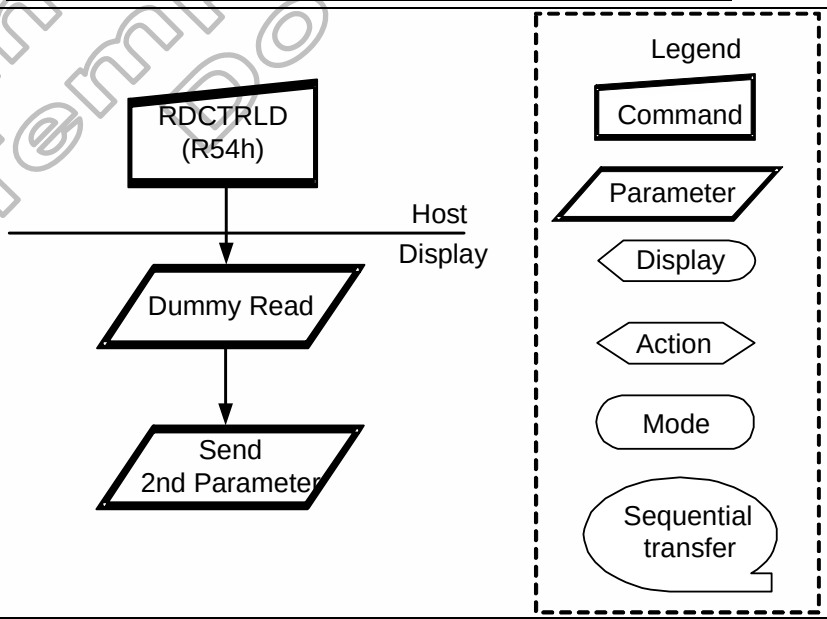
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.46 Write content adaptive brightness control (55h)

| 55H | WRCABC (Write Content Adaptive Brightness Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | C1 | C0 | 00..03 |

**Description**

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function | Note |
|---|---|---|---|
| 0 | 0 | Off | - |
| 0 | 1 | User Interface Image | - |
| 1 | 0 | Still Picture | - |
| 1 | 1 | Moving Image | - |

**Restriction**

-

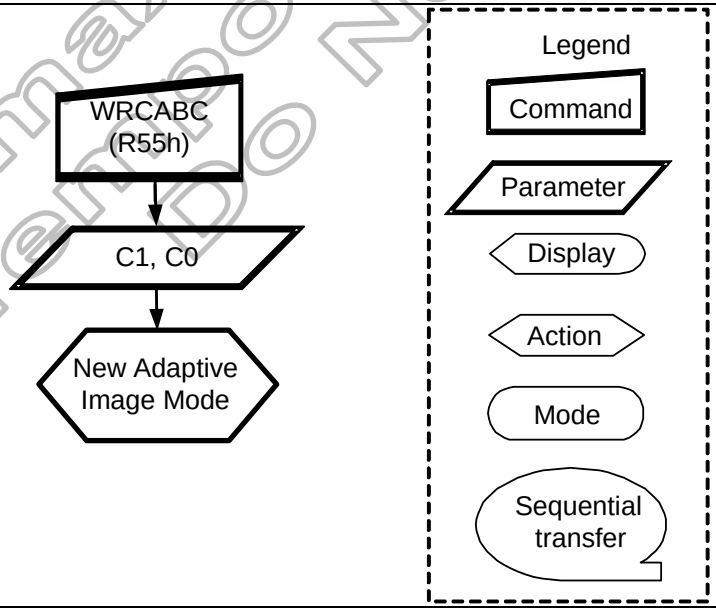
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.47 Read content adaptive brightness control (56h)

| 56H | RDCABC (Read Content Adaptive Brightness Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | xx |
| 2nd parameter | 1 | 1 | ↑ | - | 0 | 0 | 0 | 0 | 0 | 0 | C1 | C0 | xx |

**Description**

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function | Note |
|---|---|---|---|
| 0 | 0 | Off | - |
| 0 | 1 | User Interface Image | - |
| 1 | 0 | Still Picture | - |
| 1 | 1 | Moving Image | - |

**Restriction**

-

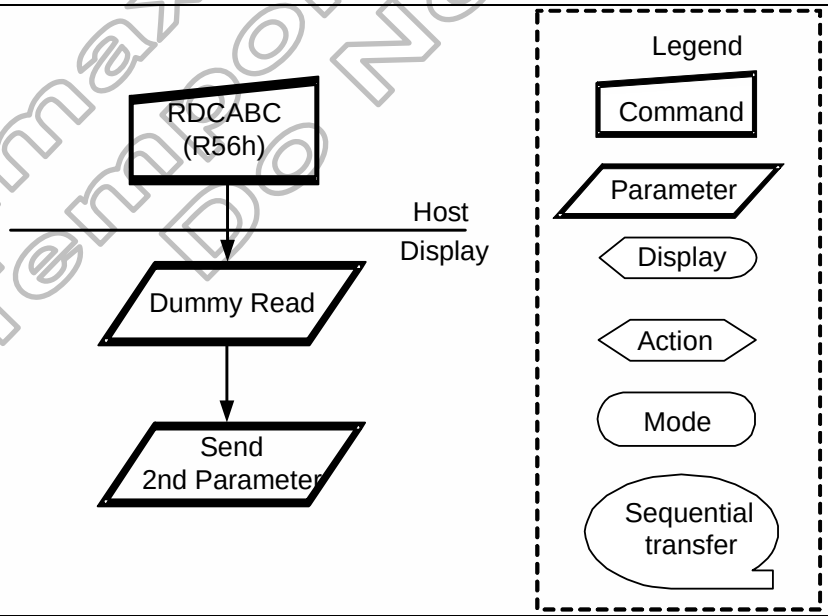
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.48 Write CABC minimum brightness (5Eh)

| 5EH | WRCABCMB (Write CABC Minimum Brightness) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E |
| 1st parameter | 1 | ↑ | 1 | - | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | 00..FF |
| Description | This command is used to set the minimum brightness value of the display for CABC function.<br><br>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.<br>For details, please refer to chapter “5.12.3 Minimum brightness setting of CABC function”. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

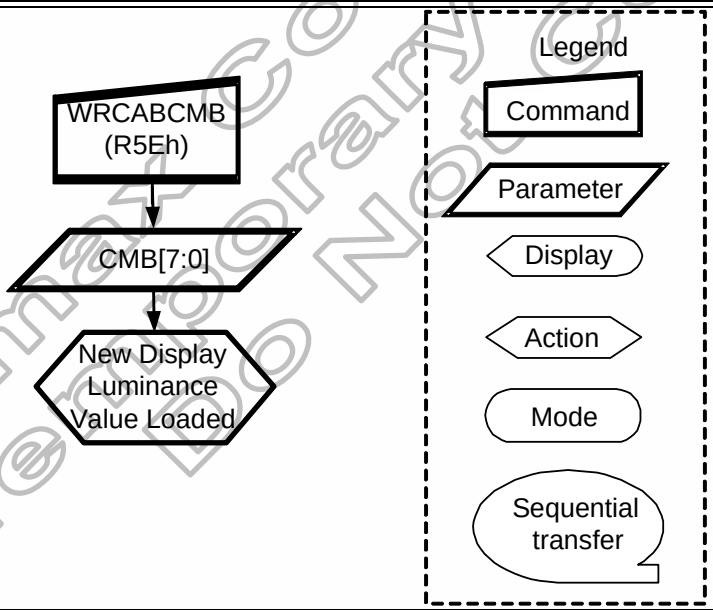
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.49 Read CABC minimum brightness (5Fh)

| 5FH | RDCABCMB (Read CABC Minimum Brightness) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | xx |
| 2nd parameter | 1 | 1 | ↑ | - | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | xx |

**Description**

This command is used to return the minimum brightness value of CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (R5Eh)" command.

**Restriction**

-

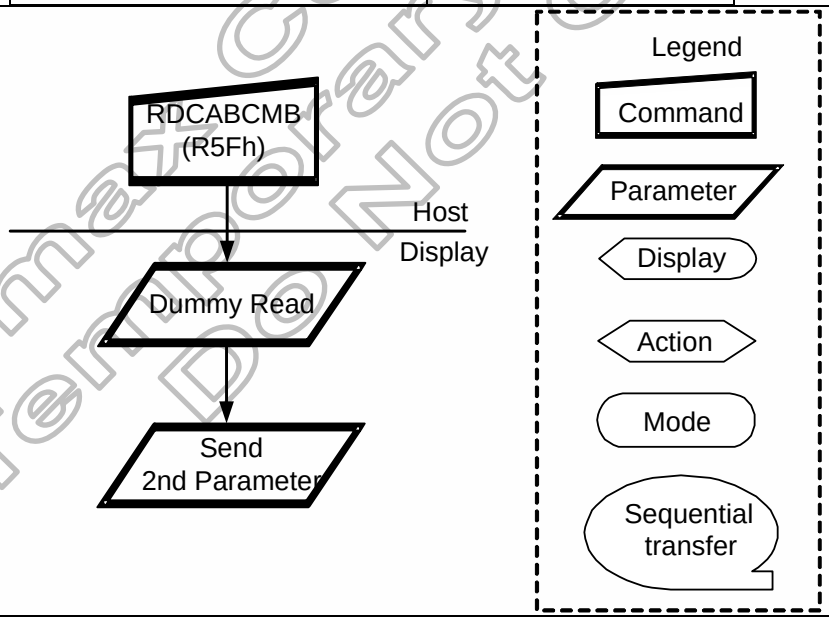
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**

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### 6.2.50 Read automatic brightness control self-diagnostic result (68h)

| 68H | RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | xx |
| 2nd parameter | 1 | 1 | ↑ | - | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | xx |
| Description | This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out command as described in the table below.<br>**Bit D7:** Register Loading Detection.<br>**Bit D6:** Functionality Detection.<br>Bit D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

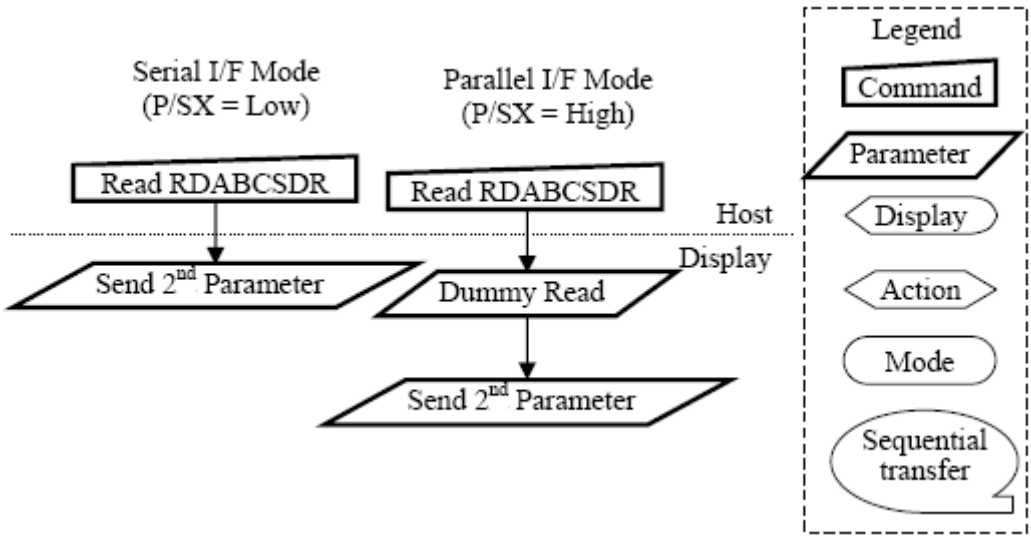
Register Availability

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart

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### 6.2.51 Read Black/White Low Bits (70h)

| 70h | RDBWLK (Read Black/White Low Bits) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Bkx1 | Bkx0 | Bky1 | Bky0 | Wx1 | Wx0 | Wy1 | Wy0 | xx |
| Description | This command returns the lowest bits of black and white color characteristics.<br>Black: Bkx and Bky<br>White: Wx and Wy | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

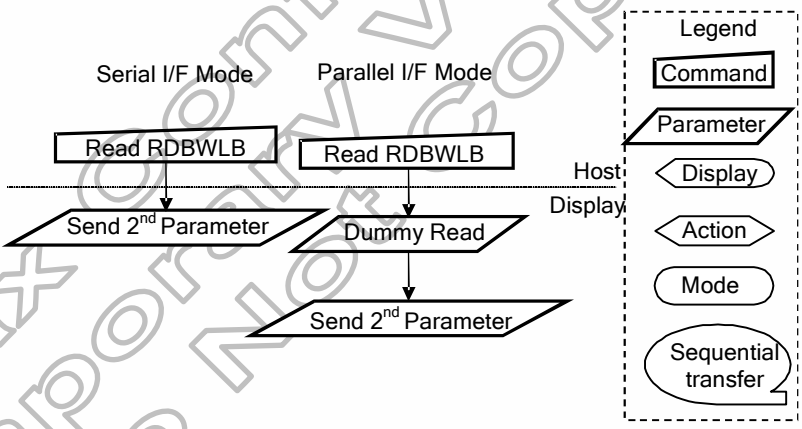
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.52 Read Bkx (71h)

| 71h | RDBkx (Read Bkx) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Bkx9 | Bkx8 | Bkx7 | Bkx6 | Bkx5 | Bkx4 | Bkx3 | Bkx2 | xx |
| Description | This command returns the Bkx bits (Bkx[9:2]) of black color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

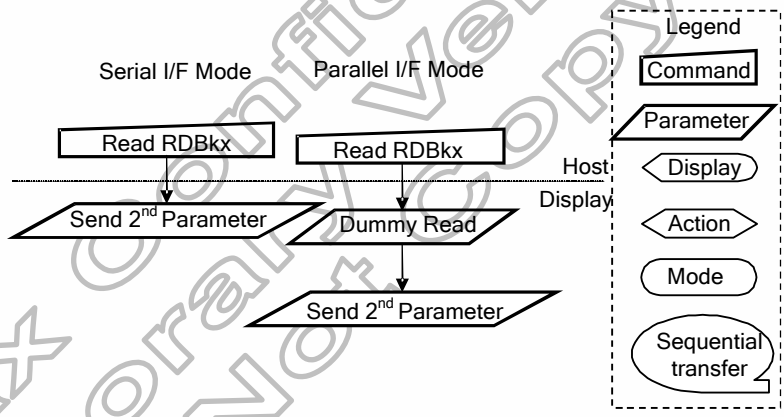
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.53 Read Bky (72h)

| 72h | RDBky (Read Bky) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 72 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Bky9 | Bky8 | Bky7 | Bky6 | Bky5 | Bky4 | Bky3 | Bky2 | xx |
| Description | This command returns the Bky bits (Bky[9:2]) of black color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

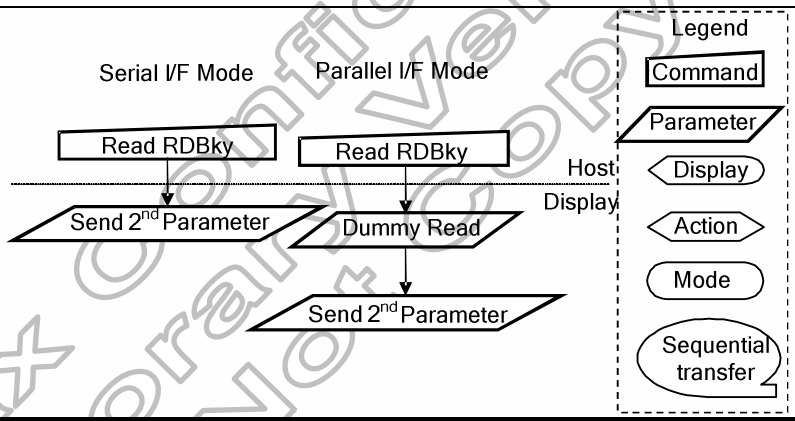
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.54 Read Wx (73h)

| 73h | RDWx (Read Wx) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Wx9 | Wx8 | Wx7 | Wx6 | Wx5 | Wx4 | Wx3 | Wx2 | xx |
| Description | This command returns the Wx bits (Wx[9:2]) of white color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

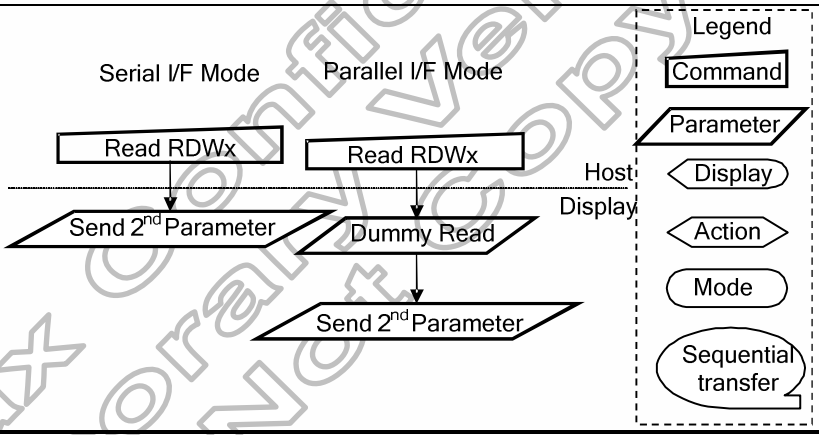
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.55 Read Wy (74h)

| 74h | RDWy (Read Wy) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | xx |
| Description | This command returns the Wy bits (Wy[9:2]) of white color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

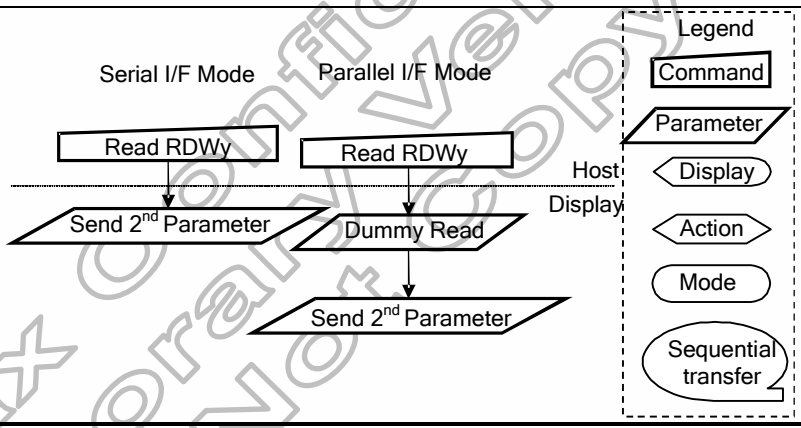
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.56 Read Red/Green Low Bits (75h)

| 75h | RDRGLB (Read Red/Green Low Bits) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 75 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Rx1 | Rx0 | Ry1 | Ry0 | Gx1 | Gx0 | Gy1 | Gy0 | xx |
| Description | This command returns the lowest bits of red and green color characteristics.<br>Red: Rx and Ry<br>Green: Gx and Gy | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

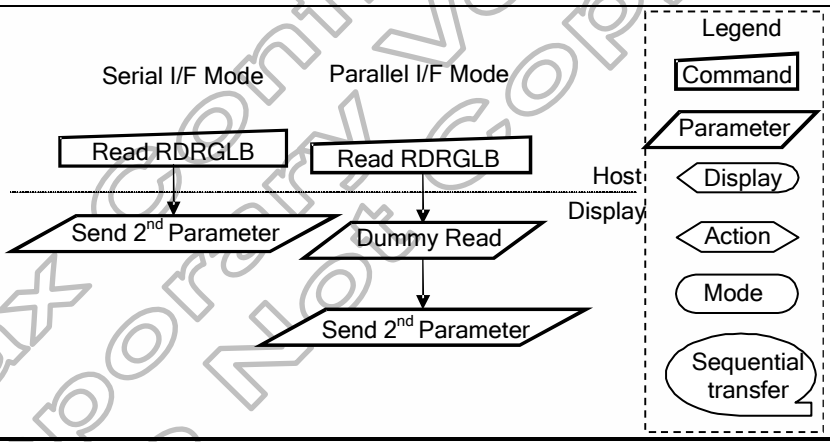
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.57 Read Rx (76h)

| 76h | RDRx (Read Rx) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | Rx3 | Rx2 | xx |
| Description | This command returns the Rx bits (Rx[9:2]) of red color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

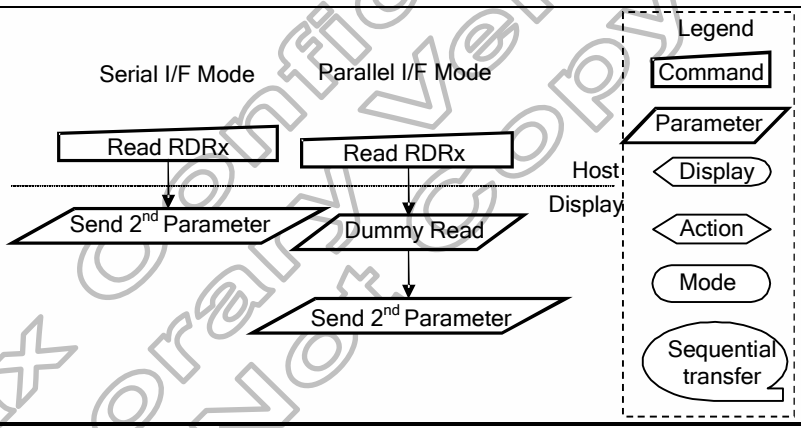
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.58 Read Ry (77h)

| 77h | RDRy (Read Ry) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 77 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Ry9 | Ry8 | Ry7 | Ry6 | Ry5 | Ry4 | Ry3 | Ry2 | xx |
| Description | This command returns the Ry bits (Ry[9:2]) of red color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

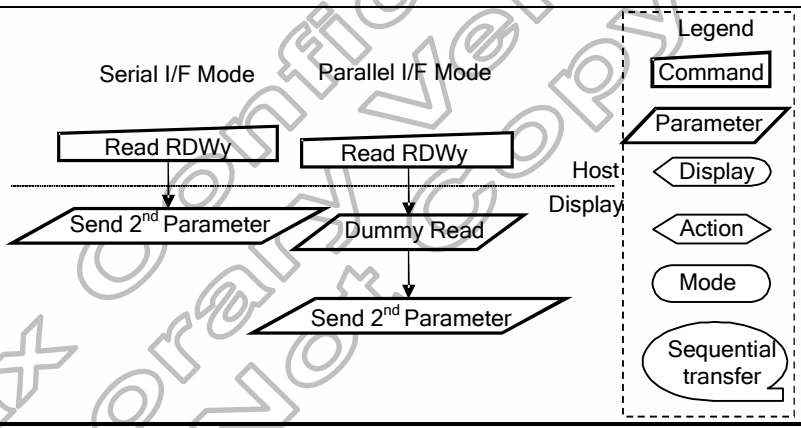
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.59 Read Gx (78h)

| 78h | RDGx (Read Gx) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Gx9 | Gx8 | Gx7 | Gx6 | Gx5 | Gx4 | Gx3 | Gx2 | xx |
| Description | This command returns the Gx bits (Gx[9:2]) of green color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

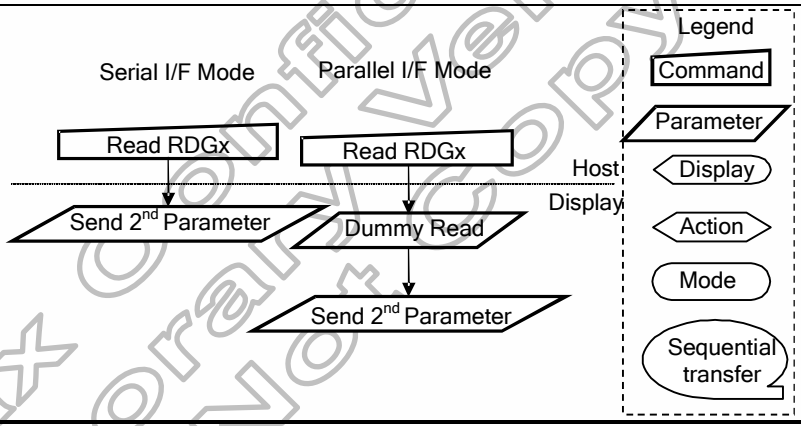
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.60 Read Gy (79h)

| 79h | RDGy (Read Gy) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 79 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Gy9 | Gy8 | Gy7 | Gy6 | Gy5 | Gy4 | Gy3 | Gy2 | xx |
| Description | This command returns the Gy bits (Gy[9:2]) of green color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

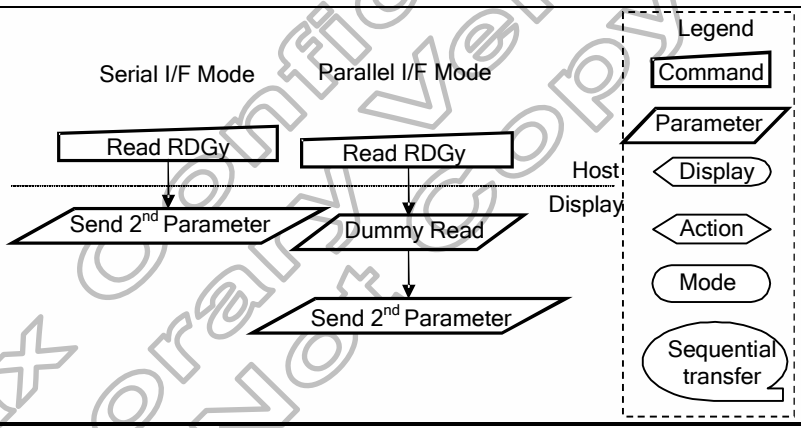
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.61 Read Blue/AColur Low Bits (7Ah)

| 7Ah | RDBALB (Read Blue/AColour Low Bits) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Bx1 | Bx0 | By1 | By0 | Ax1 | Ax0 | Ay1 | Ay0 | xx |
| Description | This command returns the lowest bits of blue and A color characteristics.<br>Blue: Bx and By<br>A: Ax and Ay<br>If A is not used Ax[1:0] and Ay[1:0] bits are set to '0's. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

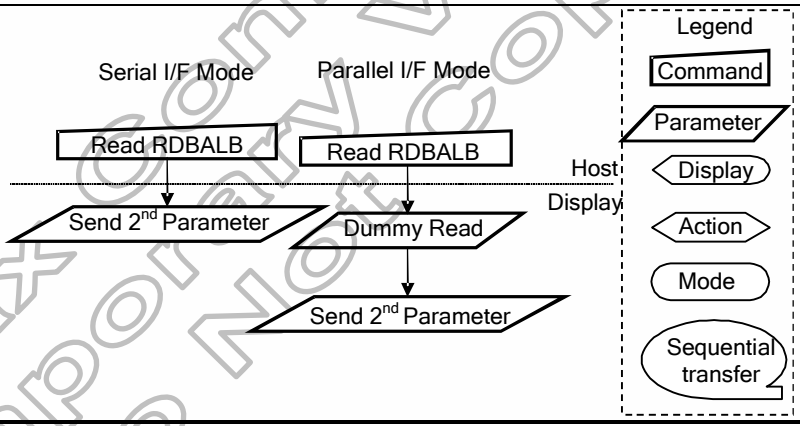
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.62 Read Bx (7Bh)

| 7Bh | RDBx (Read Bx) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Bx9 | Bx8 | Bx7 | Bx6 | Bx5 | Bx4 | Bx3 | Bx2 | xx |
| Description | This command returns the Bx bits (Bx[9:2]) of blue color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

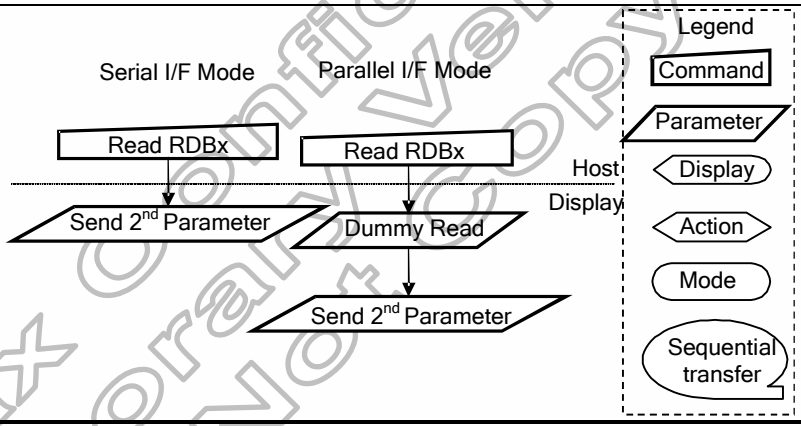
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.63 Read By (7Ch)

| 7Ch | RDBy (Read By) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | By9 | By8 | By7 | By6 | By5 | By4 | By3 | By2 | xx |
| Description | This command returns the Gy bits (Gy[9:2]) of Blue color characteristics. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

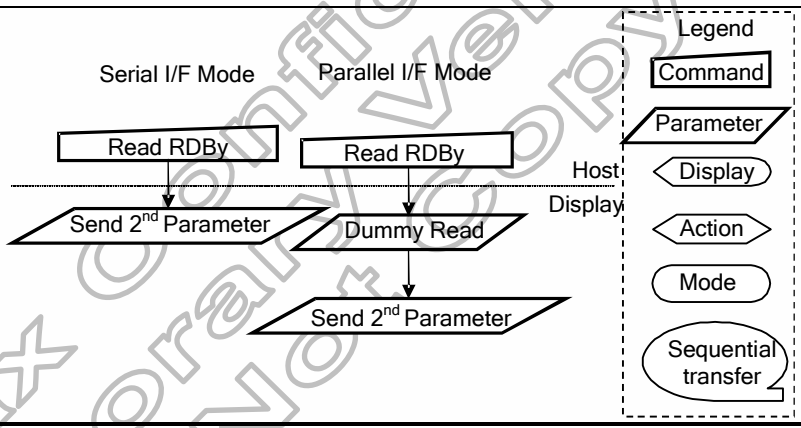
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.64 Read Ax (7Dh)

| 7Dh | RDAx (Read Ax) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Ax9 | Ax8 | Ax7 | Ax6 | Ax5 | Ax4 | Ax3 | Ax2 | xx |
| Description | This command returns the Ax bits (Ax[9:2]) of A color characteristics.<br>Ax[9:2] are set to '0's if they are not used. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

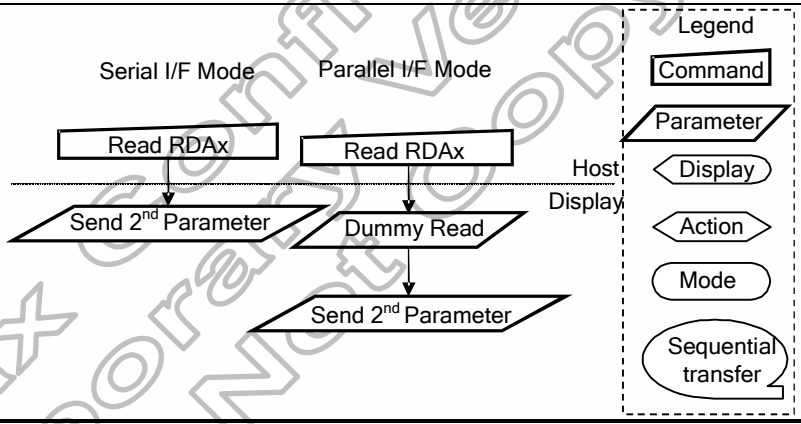
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.65 Read Ay (7Eh)

| 7Eh | RDAy (Read Ay) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 2nd parameter | 1 | ↑ | 1 | - | Ay9 | Ay8 | Ay7 | Ay6 | Ay5 | Ay4 | Ay3 | Ay2 | xx |
| Description | This command returns the Ay bits (Ay[9:2]) of A color characteristics.<br>Ay[9:2] are set to '0's if they are not used. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

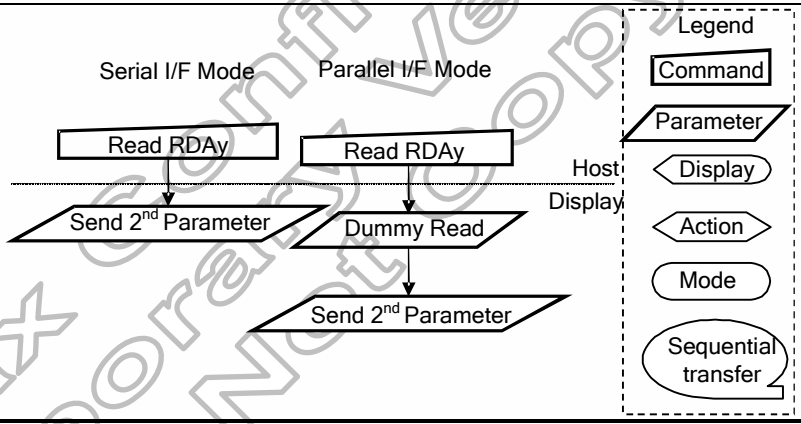
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | XXh |
| S/W Reset | XXh |
| H/W Reset | XXh |

Flow Chart

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### 6.2.66 Read_DDB_start (A1h)

| A1h | Read_DDB_start | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | X | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 3rd parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| 4th parameter | 1 | ↑ | 1 | | x | x | x | x | x | x | x | x | xx |
| 5th parameter | 1 | ↑ | 1 | | x | x | x | x | x | x | x | x | xx |
| 6th parameter | 1 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

**Description**

The format of returned data is as follows:
Parameter 2: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.
Parameter 3: MS (most significant) byte of Supplier ID.
Parameter 4: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.
Parameter 5: MS (most significant) byte of Supplier Elective Data
Parameter 6: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)

**Restrictions**

-

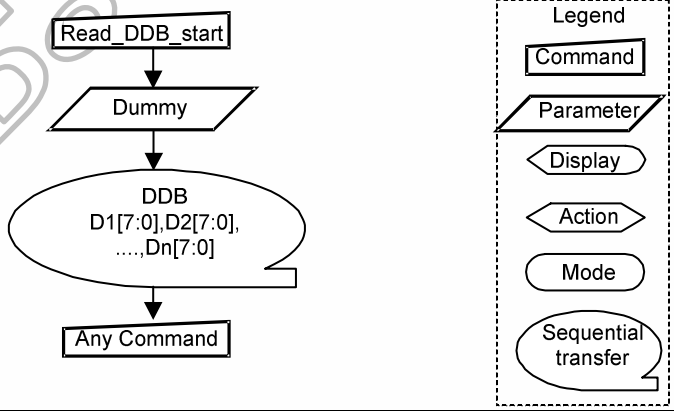
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default value |
|---|---|
| Power On Sequence | PA 2nd~5th =OTP Value, PA 6th =FFh |
| S/W Reset | PA 2nd~5th =OTP Value, PA 6th =FFh |
| H/W Reset | PA 2nd~5th =OTP Value, PA 6th =FFh |

**Flow Chart**

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### 6.2.67 Read_DDB_continue (A8h)

| A8h | Read_DDB_continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 |
| 1st parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| : | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| Nth parameter | 1 | ↑ | 1 | - | x | x | x | x | x | x | x | x | xx |
| Description | A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined. | | | | | | | | | | | | |
| Restrictions | - | | | | | | | | | | | | |

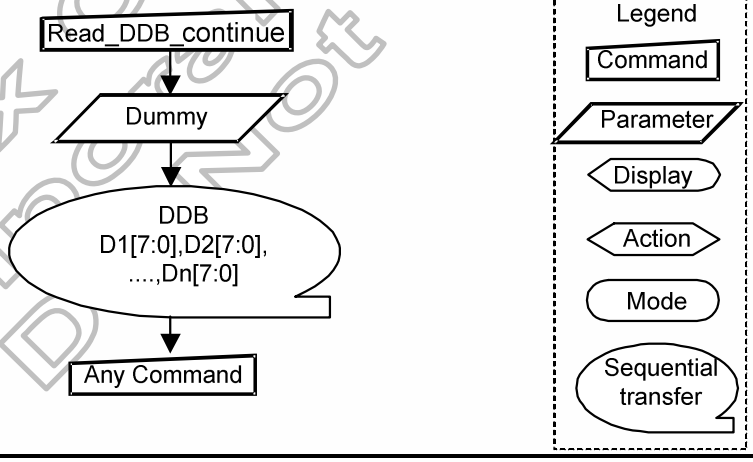
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default value |
|---|---|
| Power On Sequence | Without reading A1h, read PA 2nd~5th is the same as A1h 2nd~5th OTP value, and the 6th read is FFh. |
| S/W Reset | Without reading A1h, read PA 2nd~5th is the same as A1h 2nd~5th OTP value, and the 6th read is FFh. |
| H/W Reset | Without reading A1h, read PA 2nd~5th is the same as A1h |

Flow Chart

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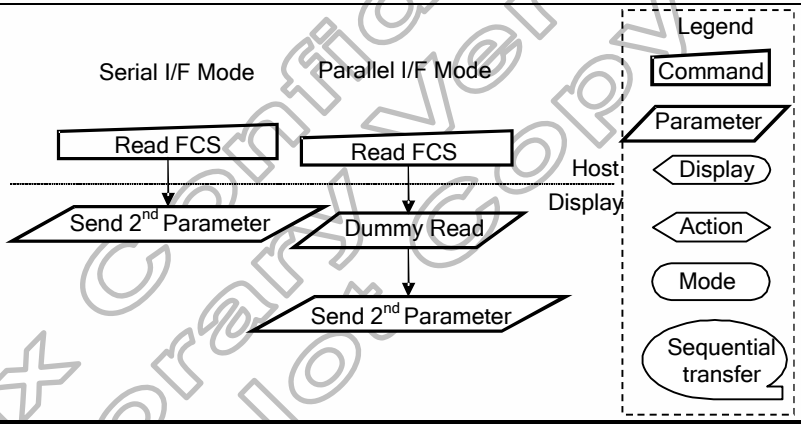
### 6.2.68 Read First Checksum (AAh)

| AAH | RDFCS (Read First Checksum) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | AA |
| 1st parameter | 1 | ↑ | 1 | - | XX | XX | XX | XX | XX | XX | XX | XX | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | FCS[7:0] | | | | | | | | xx |
| Description | This command returns the first checksum what has been calculated from<br>The area registers and the frame memory after the write access to those registers and/or frame memory has been done. | | | | | | | | | | | | |
| Restrictions | It will be necessary to wait 150ms after there is the last write access on command area registers before there can read this checksum value. | | | | | | | | | | | | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes | | | | | | | | | | | | |
| Default | FCS[7:0] = 0x00h | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |



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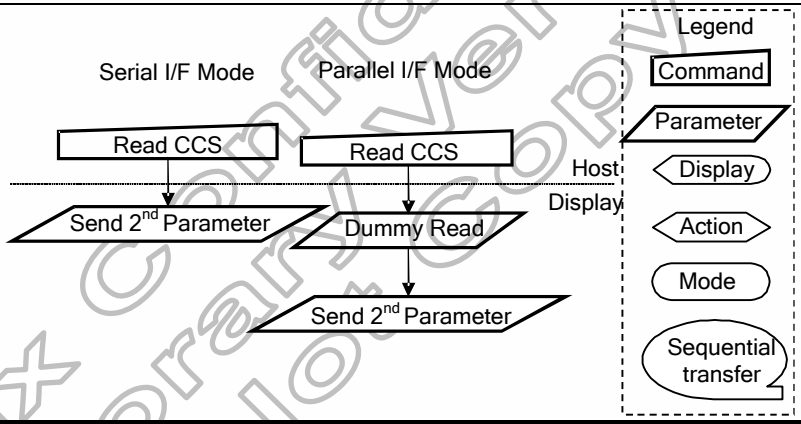
### 6.2.69 Read Continue Checksum (AFh)

| AFH | RDCCS (Read Continue Checksum) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | AA |
| 1st parameter | 1 | ↑ | 1 | - | XX | XX | XX | XX | XX | XX | XX | XX | Dummy read |
| 2nd parameter | 1 | ↑ | 1 | - | CCS[7:0] | | | | | | | | xx |
| Description | This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from command area registers and the frame memory after the write access to those registers and/or frame memory has been done. | | | | | | | | | | | | |
| Restrictions | It will be necessary to wait 300ms after there is the last write access on command area registers before there can read this checksum value in the first time. | | | | | | | | | | | | |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes | | | | | | | | | | | | |
| Default | CCS[7:0] = 0x00h | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |



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### 6.2.70 Read ID1 (DAh)

| DA H | RDID1 (Read ID1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | module's manufacturer m[7:0] | | | | | | | | - |
| Description | This read byte identifies the LCD module's manufacturer. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

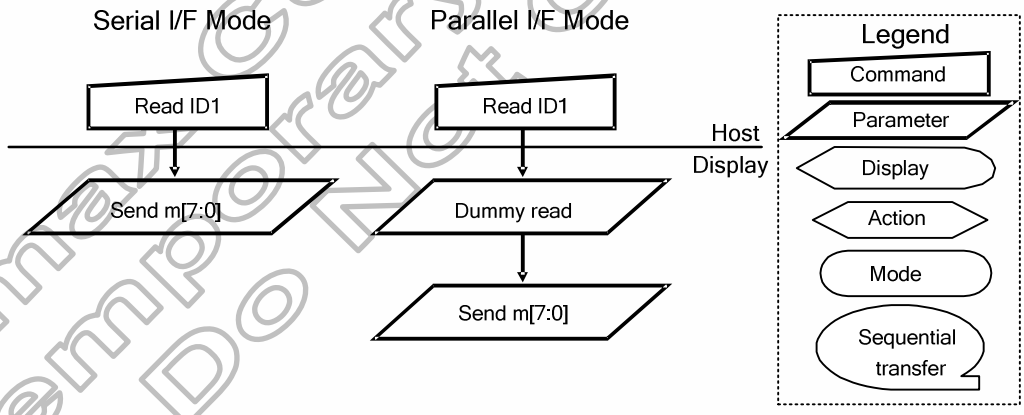
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | xxHEX |
| S/W Reset | xxHEX |
| H/W Reset | xxHEX |

Flow Chart

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### 6.2.71 Read ID2 (DBh)

| DB H | RDID2 (Read ID2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | - |
| Description | This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. | | | | | | | | | | | | |
| Restrictions | - | | | | | | | | | | | | |

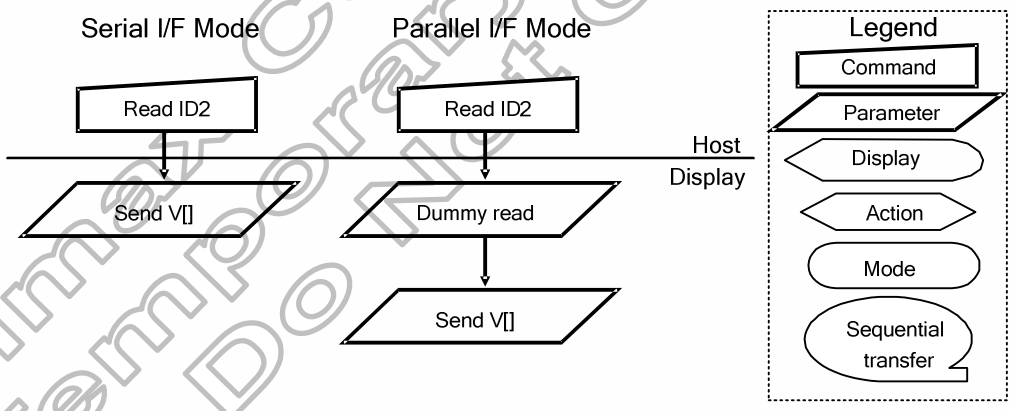
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | xxHEX |
| S/W Reset | xxHEX |
| H/W Reset | xxHEX |

Flow Chart

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### 6.2.72 Read ID3 (DCh)

| DC H | RDID3 (Read ID3) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | - |
| Description | This read byte identifies the LCD module/driver. | | | | | | | | | | | | |
| Restrictions | - | | | | | | | | | | | | |

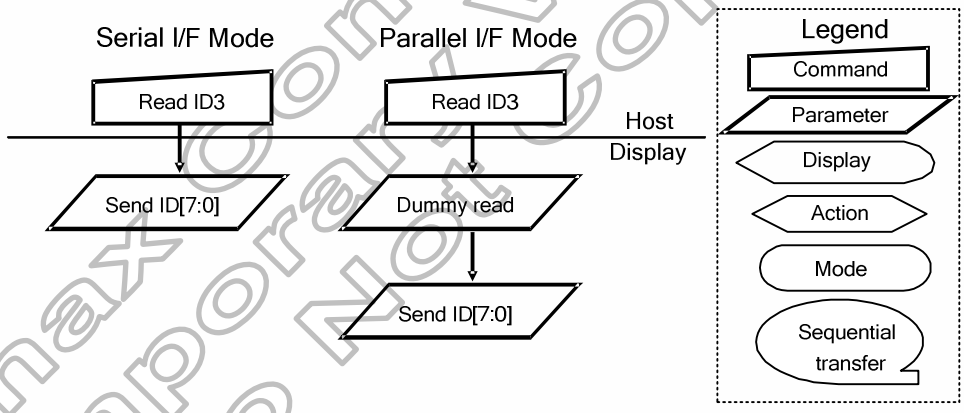
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | xxHEX |
| S/W Reset | xxHEX |
| H/W Reset | xxHEX |

Flow Chart

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### 6.2.73 SETOSC: set internal oscillator (B0h)

| B0 H | SETOSC( Set Internal Oscillator) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0 |
| 1st parameter | 1 | ↑ | 1 | - | I_UADJ[3:0] | | | | N_UADJ[3:0] | | | | 46 |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | OSC_EN | 00 |

Description

These command is used to set internal oscillator related setting
**OSC_EN**: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop.

**N_UADJ[3:0]:** Internal oscillator frequency adjusts in Normal / Partial mode.
**I_UADJ[3:0]:** Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.

| UADJ3 | UADJ2 | UADJ1 | UADJ0 | Internal Oscillator Frequency | Display Frame rate |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50% x 10MHz | 30Hz |
| 0 | 0 | 0 | 1 | 58% x 10MHz | 35Hz |
| 0 | 0 | 1 | 0 | 67% x 10MHz | 40Hz |
| 0 | 0 | 1 | 1 | 75% x 10MHz | 45Hz |
| 0 | 1 | 0 | 0 | 83% x 10MHz | 50Hz |
| 0 | 1 | 0 | 1 | 92% x 10MHz | 55Hz |
| 0 | 1 | 1 | 0 | 100% x 10MHz | 60Hz |
| 0 | 1 | 1 | 1 | 108% x 10MHz | 65Hz |
| 1 | 0 | 0 | 0 | 116% x 10MHz | 70Hz |
| 1 | 0 | 0 | 1 | 125% x 10MHz | 75Hz |
| 1 | 0 | 1 | 0 | 133% x 10MHz | 80Hz |
| 1 | 0 | 1 | 1 | 142% x 10MHz | 85Hz |
| 1 | 1 | 0 | 0 | 150% x 10MHz | 90Hz |
| 1 | 1 | 0 | 1 | 158% x 10MHz | 95Hz |
| 1 | 1 | 1 | 0 | 167% x 10MHz | 100Hz |
| 1 | 1 | 1 | 1 | 175% x 10MHz | 105Hz |

Restrictions: Must enable SETEXTC command

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.74 SETPOWER: set power control (B1h)

| B1 H | SETPOWER (Set power control ) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1 |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | DP_STB | 00 |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | TRI | XDK | - | BT[2:0] | | | 11 |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | VRH[5:0] | | | | | | 1B |
| 4th parameter | | | | | - | - | NVRH[5:0] | | | | | | 1B |
| 5th parameter | 1 | ↑ | 1 | - | GASEN | - | - | - | - | AP[2:0] | | | 83 |
| 6th parameter | 1 | ↑ | 1 | - | FS1[3:0] | | | | FS0[3:0] | | | | 3C |
| 9th parametert | 1 | ↑ | 1 | - | | VCOMG | 1 | PON | DK | 0 | 0 | STB | 09 |

Description

**DP_STB,:** These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained.

**XDK, TRI:** Specify the ratio of step-up circuit for VSP voltage generation.

| TRI | XDK | Step up circuit 1 | Capacitor connection pins |
|---|---|---|---|
| 0 | 0 | 2 x VCI | C11P, C11N |
| 0 | 1 | 2 x VCI | C11P, C11N, C12P, C12N |
| 1 | 0 | 3 x VCI | C11P, C11N, C12P, C12N |
| 1 | 1 | Setting inhabited | Setting inhabited |

**VRH[5:0]:** Specify the VSPROUT voltage adjusting. VSPROUT voltage is for gamma voltage
**NVRH[5:0]:** Specify the VSNR voltage adjusting. VSNR voltage is for gamma voltage

| TRI=0 | | | | | |
|---|---|---|---|---|---|
| VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) | VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) | VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) |
| 0 | 3.09/-3.09 | B | 3.61/-3.61 | 16 | 4.13/-4.13 |
| 1 | 3.14/-3.14 | C | 3.66/-3.66 | 17 | 4.17/-4.17 |
| 2 | 3.19/-3.19 | D | 3.70/-3.70 | 18 | 4.22/-4.22 |
| 3 | 3.23/-3.23 | E | 3.75/-3.75 | 19 | 4.27/-4.27 |
| 4 | 3.28/-3.28 | F | 3.80/-3.80 | 1A | 4.31/-4.31 |
| 5 | 3.33/-3.33 | 10 | 3.84/-3.84 | 1B | 4.36/-4.36 |
| 6 | 3.38/-3.38 | 11 | 3.89/-3.89 | 1C | 4.41/-4.41 |
| 7 | 3.42/-3.42 | 12 | 3.94/-3.94 | 1D | 4.45/-4.45 |
| 8 | 3.47/-3.47 | 13 | 3.98/-3.98 | 1E | 4.50/-4.50 |
| 9 | 3.52/-3.52 | 14 | 4.03/-4.03 | 1F | STOP |
| A | 3.56/-3.56 | 15 | 4.08/-4.08 | 20~3F | STOP |

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| TRI=1 | | | | | |
|---|---|---|---|---|---|
| VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) | VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) | VRH[5:0] NVRH[5:0] (Hex) | VSPROUT VSNROUT (V) |
| 0 | 3.09/-3.09 | 12 | 3.94/-3.94 | 24 | 4.78/-4.78 |
| 1 | 3.14/-3.14 | 13 | 3.98/-3.98 | 25 | 4.83/-4.83 |
| 2 | 3.19/-3.19 | 14 | 4.03/-4.03 | 26 | 4.88/-4.88 |
| 3 | 3.23/-3.23 | 15 | 4.08/-4.08 | 27 | 4.92/-4.92 |
| 4 | 3.28/-3.28 | 16 | 4.13/-4.13 | 28 | 4.97/-4.97 |
| 5 | 3.33/-3.33 | 17 | 4.17/-4.17 | 29 | 5.02/-5.02 |
| 6 | 3.38/-3.38 | 18 | 4.22/-4.22 | 2A | 5.06/-5.06 |
| 7 | 3.42/-3.42 | 19 | 4.27/-4.27 | 2B | 5.11/-5.11 |
| 8 | 3.47/-3.47 | 1A | 4.31/-4.31 | 2C | 5.16/-5.16 |
| 9 | 3.52/-3.52 | 1B | 4.36/-4.36 | 2D | 5.20/-5.20 |
| A | 3.56/-3.56 | 1C | 4.41/-4.41 | 2E | 5.25/-5.25 |
| B | 3.61/-3.61 | 1D | 4.45/-4.45 | 2F | 5.30/-5.30 |
| C | 3.66/-3.66 | 1E | 4.50/-4.50 | 30 | 5.34/-5.34 |
| D | 3.70/-3.70 | 1F | 4.55/-4.55 | 31 | 5.39/-5.39 |
| E | 3.75/-3.75 | 20 | 4.59/-4.59 | 32 | 5.44/-5.44 |
| F | 3.80/-3.80 | 21 | 4.64/-4.64 | 33~3F | STOP |
| 10 | 3.84/-3.84 | 22 | 4.69/-4.69 | | |
| 11 | 3.89/-3.89 | 23 | 4.73/-4.73 | | |

**Note:Internal VREF can be modified by Custom's special request.**
**VSPR={**Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/4.8) if** TRI=0.
**VSNR={**Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/5.8) if** TRI=1.
**Note: Internal nVREF can be modified by Custom's special request.**
**VSNR={**Decimal(-NVRH[5:0])x0.05-3.3 **}*(nVREF/4.8) if** TRI=0.
**VSNR={**Decimal(-NVRH[5:0])x0.05-3.3 **}*(nVREF/5.8) if** TRI=1.

**BT[2:0]:** Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation.

| BT2 | BT1 | BT0 | VSP | VGH | VGL |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 5.1V | 3DDVDH | -3DDVDH |
| 0 | 0 | 1 | 5.1V | 3DDVDH | -2DDVDH |
| 0 | 1 | 0 | 5.1V | 3DDVDH | -2DDVDH |
| 0 | 1 | 1 | 5.1V | VCI + 2DDVDH | -VCI-2DDVDH |
| 1 | 0 | 0 | 5.1V | VCI + 2DDVDH | -2DDVDH |
| 1 | 0 | 1 | 5.1V | VCI + 2DDVDH | VCI-2DDVDH |
| 1 | 1 | 0 | 5.1V | 2DDVDH | -2DDVDH |
| 1 | 1 | 1 | 5.1V | 2DDVDH | VCI-DDVDH |

**Note:** When VCI = 2.8V, TRI=0

**FS0[3:0]:** Set the operating frequency for VSP and VSN voltage generation.

| FS03 | FS02 | FS01 | FS00 | Operation Frequency for VSP and VSN |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | fosc/16 |
| 0 | 0 | 0 | 1 | fosc/32 |
| : | | | | : |
| 0 | 1 | 1 | 1 | fosc/128 |
| 1 | 0 | 0 | 0 | fosc/288 |
| 1 | 0 | 0 | 1 | fosc/320 |
| : | | | | : |
| 1 | 1 | 1 | 1 | fosc/512 |

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**FS1[3:0]:** Set the operating frequency for VGH/VGL voltage generation.

| FS13 | FS12 | FS11 | FS10 | Operation Frequency for VGH |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | fosc/16 |
| 0 | 0 | 0 | 1 | fosc/32 |
| 0 | 0 | 1 | 0 | fosc/64 |
| 0 | 0 | 1 | 1 | fosc/128 |
| : | : | : | : | : |
| 1 | 1 | 0 | 1 | fosc/448 |
| 1 | 1 | 1 | 0 | fosc/480 |
| 1 | 1 | 1 | 1 | fosc/512 |

**AP[2:0]:** Adjust the amount of current driving for the operational amplifier in the power supply circuit.

| AP2 | AP1 | AP0 | Constant Current of Operational Amplifier |
|---|---|---|---|
| 0 | 0 | 0 | Operation of the operational amplifier stops |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small |
| 0 | 1 | 1 | Small |
| 1 | 0 | 0 | Medium |
| 1 | 0 | 1 | Medium High |
| 1 | 1 | 0 | Large |
| 1 | 1 | 1 | Small |

**STB:** When STB = "1", the HX8357-C into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator.
In the standby mode, the GRAM data and register content will be keeping.

**GASEN:** This stands for abnormal power-off monitor function when the power is off.

**DK:** Specify on/off control of step-up circuit 1 for VSP voltage generation. For detail, see the Power Supply Setting Sequence.

| DK | Operation of step-up circuit 1 |
|---|---|
| 0 | ON |
| 1 | OFF |

**PON:** Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation.
For detail, see the Power Supply Setting Sequence.

| PON | Operation of step-up circuit 2 |
|---|---|
| 0 | OFF |
| 1 | ON |

**VCOMG:** Specify on/off control of step-up circuit 3 for VSN voltage generation. For detail, see the Power Supply Setting Sequence.

| VCOMG | Operation of step-up circuit 3 |
|---|---|
| 0 | OFF |
| 1 | ON |

| | |
|---|---|
| Restrictions | Must enable SETEXTC command |

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Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.75 SETDISPLAY: set display related register (B2h)

| B2H | SETDISCTRL ( Set display control ) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2 |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | ISC3 | ISC2 | ISC1 | ISC0 | 00 |
| 2nd parameter | 1 | ↑ | 1 | - | PT1 | PT0 | - | - | - | - | PTG | REF | 83 |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | NL[5:0] | | | | | | 3B |
| 3rd parameter | 1 | ↑ | 1 | - | - | SCN[6:0] | | | | | | | 00 |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | GON | DTE | D1 | D0 | - | - | 20 |

Description

This command is used to set display related register

**D[1:0]:** When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level.
When D[1:0]= '01', the internal display of the HX8357-C is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

| D1 | D0 | Source Output | Internal Display Operations | Gate-Driver Control Signals |
|---|---|---|---|---|
| 0 | 0 | VSSD | Halt | Halt |
| 0 | 1 | VSSD | Operate | Operate |
| 1 | 0 | =PT(0,0) | Operate | Operate |
| 1 | 1 | Display | Operate | Operate |

**GON, DTE:**

| GON | DTE | Gate Output |
|---|---|---|
| 0 | x | Fixed to VGH |
| 1 | 0 | Fixed to VGL |
| 1 | 1 | Normal Operation (VGH/VGL) |

**PT[1:0] :** Specify the Non-display area source output in partial display mode.

| | | Source Output Level | | | | | |
|---|---|---|---|---|---|---|---|
| REV_Panel | GRAM Data | Display area | | Non-display Area | | | |
| | | | | PT1-0=(0,*) | | PT1-0=(1,0) | PT1-0=(1,1) |
| | | Positive | Negative | Positive | Negative | -- | |
| 1 (Normally Black Panel) | 18'h00000 . 18'h3FFFF | V63P . V0P | V0N . V63N | V63P | V0N | GND | Hi-z |
| 0 (Normally White Panel) | 18'h00000 . 18'h3FFFF | V0P . V63P | V63N . V0N | V63P | V0N | | |

**REF:** Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

**PTG:** Specify the scan mode of gate driver in non-display area.

| PTG | Gate Outputs in Non-display Area |
|---|---|
| 0 | Normal Drive |
| 1 | Fixed VGL |

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**ISC[3:0]:** Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1.The polarity is inverted every scan cycle.

| ISC3 | ISC2 | ISC1 | ISC0 | Scan Cycle | $f_{FLM}$ = 60Hz |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 frame | 17ms |
| 0 | 0 | 0 | 1 | 5 frames | 83ms |
| 0 | 0 | 1 | 0 | 9 frames | 150ms |
| 0 | 0 | 1 | 1 | 13 frames | 217ms |
| 0 | 1 | 0 | 0 | 17 frames | 283ms |
| 0 | 1 | 0 | 1 | 21 frames | 350ms |
| 0 | 1 | 1 | 0 | 25 frames | 417ms |
| 0 | 1 | 1 | 1 | 29 frames | 483ms |
| 1 | 0 | 0 | 0 | 33 frames | 550ms |
| 1 | 0 | 0 | 1 | 37 frames | 616ms |
| 1 | 0 | 1 | 0 | 41 frames | 683ms |
| 1 | 0 | 1 | 1 | 45 frames | 750ms |
| 1 | 1 | 0 | 0 | 49 frames | 816ms |
| 1 | 1 | 0 | 1 | 53 frames | 883ms |
| 1 | 1 | 1 | 0 | 57 frames | 950ms |
| 1 | 1 | 1 | 1 | Setting inhibited | |

**NL[5:0]:** Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

| NL5 | NL4 | NL3 | NL2 | NL1 | NL0 | LCD Drive Lines |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 8 lines |
| 0 | 0 | 0 | 0 | 0 | 1 | 16 lines |
| 0 | 0 | 0 | 0 | 1 | 0 | 24 lines |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 0 | 1 | 0 | 472 lines |
| 1 | 1 | 1 | 0 | 1 | 1 | 480 lines |
| Other Setting | | | | | | 480 lines |

**SCN[6:0]:** Specifies the gate line where the gate driver starts scan.

| SCN[6:0] | Scanning Start Position | |
|---|---|---|
| | GS=0 | GS=1 |
| 00h~63h | G(1+SCN[6:0]*4) | G(SCN[6:0]*4+NL[5:0]*8) |
| Others | Setting inhibited | Setting inhibited |

| | |
|---|---|
| Restrictions | Must enable SETEXTC command |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.76 SETRGB: set RGB interface (B3h)

| B3 H | SETRGBIF( Set RGB interface related register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3 |
| 1st parameter | 1 | ↑ | 1 | - | SDO_EN | BYPASS | EPF[1:0] | | | - | RM | DM | 00 |
| 2nd parameter | 1 | ↑ | 1 | - | - | - | - | - | DPL | HSPL | VSPL | EPL | 00 |
| 3rd parameter | 1 | ↑ | 1 | - | RCM | | HBP[5:0] | | | | | | 06 |
| 4th parameter | 1 | ↑ | 1 | - | | | VBP[5:0] | | | | | | 06 |

Description

This command is used to set RGB interface related register

**SDO_EN:** SDO Pin Enable.

| SDO_EN | Input Pin | Ouput pin |
|---|---|---|
| 0 | SDA | SDA |
| 1 | SDA | SDO |

**RM** setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

| RM | Interface for RAM access |
|---|---|
| 0 | DBI Interface (MPU) |
| 1 | DPI Interface (RGB) |

**DM** bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.

| DM | Display Mode |
|---|---|
| 0 | Internal oscillation clock |
| 1 | DPI interface |

**BYPASS:** Select the display data pathe whether memory or direct to display in RGB interface.

| BYPASS | Interface Select |
|---|---|
| 0 | Memory |
| 1 | Direction to display |

**RCM:** Select RGB interface mode.

| RCM | Interface Select |
|---|---|
| 0 | RGB mode 1(VS+HS+DE) |
| 1 | RGB mode 2(VS+HS) |

| BYPASS | RCM | RM | DM | Ram | Display |
|---|---|---|---|---|---|
| x | x | 0 | 0 | MPU | Internal |
| x | x | 0 | 1 | MPU | V-sync interface |
| 0 | 0 | 1 | 1 | RGB1 | RGB1 |
| 0 | 1 | 1 | 1 | RGB2 | RGB2 |
| 1 | 0 | 1 | 1 | RGB1 | RGB1 |
| 1 | 1 | 1 | 1 | RGB2 | RGB2 |

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**EPL:** Specify the polarity of Enable pin in RGB interface mode.

| EPL | ENABLE pin | Display image | Operation |
|---|---|---|---|
| 0 | High | Enable | Write data to D17-0 |
| 0 | Low | Disable | Disable |
| 1 | High | Disable | Disable |
| 1 | Low | Enable | Write data to D17-0 |

**VSPL:** The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

**HSPL:** The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

**DPL:** The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

**HBP[5:0]**: Set the delay period from falling edge of HSYNC signal to first valid data in DPI I/F mode 2

| HBP[5:0] | No. of clock cycle of DOTCLK |
|---|---|
| 00d | Setting Inhibited |
| 01d | Setting Inhibited |
| 02d | 2 |
| 03d | 3 |
| 04d | 4 |
| : | : |
| 62d | 62 |
| 63d | Setting Inhibited |

**VBP[5:0]**: Set the delay period from falling edge of VSYNC signal to first valid line in DPI I/F mode 2

| VBP[5:0] | No. of clock cycle of HSYNC |
|---|---|
| 00d | Setting Inhibited |
| 01d | Setting Inhibited |
| 02d | 2 |
| 03d | 3 |
| 04d | 4 |
| : | : |
| 61d | 61 |
| 62d | 62 |
| 63d | 63 |

**EPF[1:0]:** 65K color mode data format

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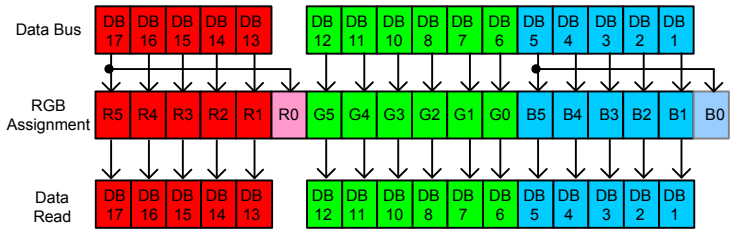
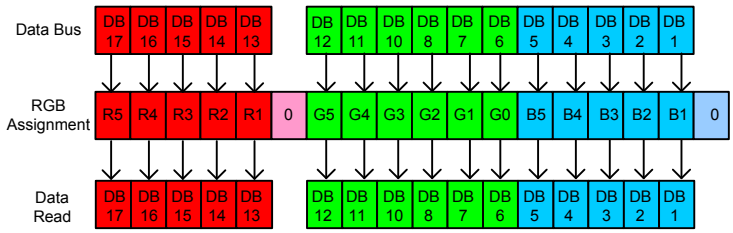
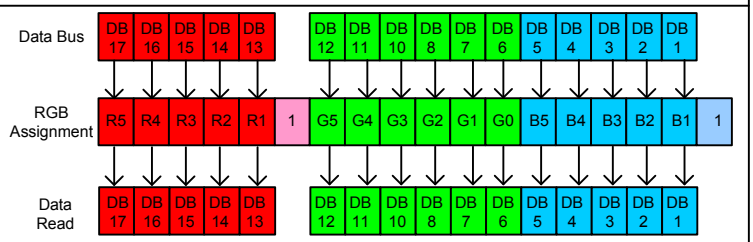
| EPF1 | EPF0 | 16 bits color mapping |
|---|---|---|
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |



| | |
|---|---|
| Restrictions | Must enable SETEXTC command |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.77 SETCYC: set display cycle register (B4h)

| B4 H | SETCYC( Set display cycle register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4 |
| 1st parameter | 1 | ↑ | 1 | - | ZINV | - | I_NW[1:0] | | - | - | N_NW[1:0] | | 02 |
| 2nd parameter | 1 | ↑ | 1 | - | - | RTN[6:0] | | | | | | | 40 |
| 3rd parameter | 1 | ↑ | 1 | - | - | - | - | - | OSC_ DIV2 | - | DIV[1:0] | | 00 |
| 4th parameter | 1 | ↑ | 1 | - | N_DUM[7:0] | | | | | | | | 2A |
| 5th parameter | 1 | ↑ | 1 | - | I_DUM[7:0] | | | | | | | | 2A |
| 6th parameter | 1 | ↑ | 1 | - | GDON[7:0] | | | | | | | | 0D |
| 7th parameter | 1 | ↑ | 1 | - | GDOF[7:0] | | | | | | | | 96 |

Description

This command is used to set display related register

**ZINV:** Set Z-inversion mode.

| ZINV | Z-inversion |
|---|---|
| 0 | Disable |
| 1 | Enable |

**N_ NW[1:0]:** Specify LCD driving inversion type in Normal/ Partial mode.
**I_ NW[1:0]:** Specify LCD driving inversion type in Idle / Partial Idle mode.

| NW[1:0] | LCD driving Inversion Type |
|---|---|
| 0d | Column inversion |
| 1d | 1-dot inversion |
| 2d | 2-dot inversion |
| 3d | 4-dot inversion |

**OSC_DIV2:** Set the internal clock divide by 2.

**DIV[1:0]:** Specify the division ratio of internal clocks mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with these bits.

fosc = R-C oscillation frequency

| DIV1 | DIV0 | Division Ratio | Internal Display Operation Clock Frequency |
|---|---|---|---|
| 0 | 0 | 1 | fosc / 1 |
| 0 | 1 | 2 | fosc / 2 |
| 1 | 0 | 4 | fosc / 4 |
| 1 | 1 | 8 | fosc / 8 |

**RTN[6:0]:** Specify clock number of one line period for internal operation.
Clock cycles=1/internal operation clock frequency(fosc)

| RTN[6:0] | Clock number per Line |
|---|---|
| 00h~7Fh | 192+RTN[6:0]*2 |
| Default:64h | 320 |

**N_DUM[7:0]:** Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
**I_DUM[7:0]:** Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

| DUM[7:0] | Line number in blanking period |
|---|---|
| 000d | Setting Inhibited |
| 001d | Setting Inhibited |
| 002d | 2 |
| 003d | 3 |

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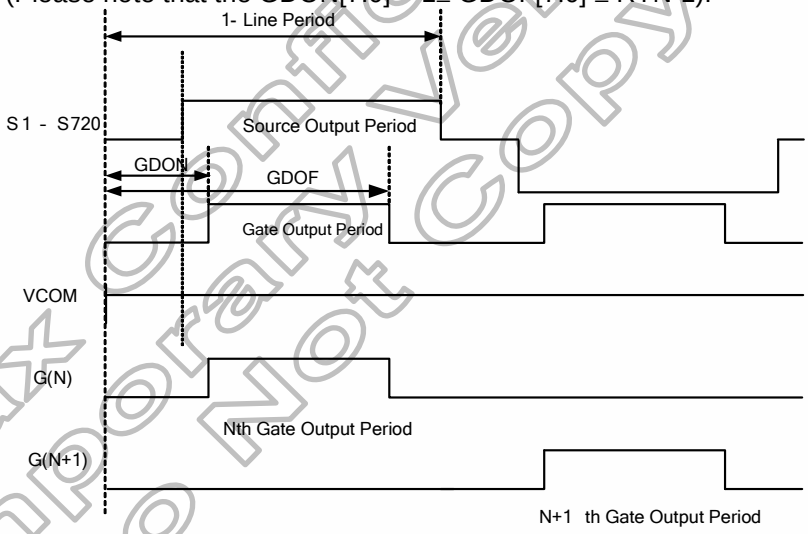
| | |
|---|---|
| 004d | 4 |
| : | : |
| 190d | 190 |
| others | Setting Inhibited |

**Formula for the Frame Frequency during internal display mode:**
Frame frequency = fosc/( RTN × DIV × (320+DUM) ) [Hz]
fosc: RC oscillation frequency

**GDON[7:0]**: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting "00h", "01h", "02h" is inhibited).

**GDOF[7:0]**: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).




Restrictions: Must enable SETEXTC command

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.78 SETCOM: set VCOM voltage related register (B6h)

| B6 H | SETCOM ( Set VCOM Voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6 |
| 1st parameter | 1 | ↑ | 1 | - | - | VCOM[6:0] | | | | | | | 4B |
| 2nd parameter | 1 | 1 | ↑ | - | - | - | - | - | - | VCOM_OTP_TIMES[2:0] | | | |

**Description**

This command is used to set VCOM Voltage.

**VCOM[6:0]:** DC VCOM voltage setting.

| VCOM[6:0] | | | | | | | VCOM Voltage |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | -2.500 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | -2.480 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2.460 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | -2.440 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | -2.420 |
| : | | | | | | | : |
| : | | | | | | | : |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | -0.060 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | -0.040 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | -0.020 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | VSSA |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | VSSA |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | VSSA |

**VCOM_OTP_TIMES[2:0]:** Read VCOM OTP programmed times.

| VCOM_OTP_TIMES[2:0] | VCOM OTP programmed times |
|---|---|
| 3'b000 | Not programmed |
| 3b001 | 1 time |
| 3'b010 | 2 times |
| 3'b011 | 3 times |
| 3'b100 | 4 times |

**Restrictions**

Must enable SETEXTC command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.79 SETOTP: set OTP setting (B7h)

| B7 H | SETOTP ( Set OTP related setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7 |
| 1st parameter | 1 | ↑ | 1 | - | OTP_KEY[7:0] | | | | | | | | FF |
| 2nd parameter | 1 | ↑ | 1 | - | OTP_MASK[7:0] | | | | | | | | 00 |
| 3rd parameter | 1 | ↑ | 1 | - | OTP_INDEX[7:0] | | | | | | | | 00 |
| 4th parameter | 1 | ↑ | 1 | - | LOAD_IDS | VPP_EN | OTP_POR | OTP_PWE | OTP_PTM[1:0] | | VPP_SEL | OTP_PROG | 00 |
| 5th parameter | 1 | 1 | ↑ | - | OTP_DOUT[7:0] | | | | | | | | 00 |
| Description | This command is used to set the OTP control .<br><br>**OTP_KEY[7:0]:** "AAh" OTP register access enable and other registers access disable.<br>**OTP_MASK[7:0]:** Bit programming mask. If "1", means don't programming this bit.<br>**OTP_INDEX[7:0]:** Set index of OTP to be programmed.<br>**LOAD_DIS:** When written to "1", OTP load disable.<br>**VPP_EN:** When written to "1", OTP power OP is enable.<br>**OTP_POR:** for OTP read control. When set to from "0" to "1", OTP data can be read the related OTP index at OTP_DOUT[7:0].<br>**OTP_PROG :** When this bit set to "1", it will programmed to the setting OTP index from related register value.<br>**OTP_PWE :** Internal use, not open.<br>**OTP_PTM[1:0] :** Internal use, not open.<br>**VPP_SEL :** When set to '1', VPP input voltage is fed to OTP.<br>**OTP_DOUT[7:0] :** OTP read data. | | | | | | | | | | | | |
| Restrictions | Must enable SETEXTC command | | | | | | | | | | | | |
| Register Availability | Status | | | | | | | | Availability | | | | |
| | Normal Mode On, Idle Mode Off, Sleep Out | | | | | | | | Yes | | | | |
| | Normal Mode On, Idle Mode On, Sleep Out | | | | | | | | Yes | | | | |
| | Partial Mode On, Idle Mode Off, Sleep Out | | | | | | | | Yes | | | | |
| | Partial Mode On, Idle Mode On, Sleep Out | | | | | | | | Yes | | | | |
| | Sleep In or Booster Off | | | | | | | | Yes | | | | |

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### 6.2.80 SETEXTC: enable extention command (B9h)

| B9 H | SETEXTC ( Set extended command set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9 |
| 1st parameter | 1 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| 2nd parameter | 1 | ↑ | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 |
| 3rd parameter | 1 | ↑ | 1 | - | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 57 |

**Description**

This command is used to set extended command set access enable.

| Extend cmd | Command description |
|---|---|
| Enable | After command (B9h), must write 3 parameters (FFh,83h,57h) by order |
| Disable(default) | After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh,83h,47h) |

**Restrictions**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.81 SETDGC: set DGC related setting (C1h)

| C1 H | SETDGC ( Set DGC) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1 |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | DGC_EN | 00 |
| 2nd parameter | 1 | ↑ | 1 | - | DGC_LUT_R00[7:0] | | | | | | | | 00 |
| 3rd parameter | 1 | ↑ | 1 | - | DGC_LUT_R01[7:0] | | | | | | | | 08 |
| : | 1 | ↑ | 1 | - | : | | | | | | | | : |
| 34th parameter | 1 | ↑ | 1 | - | DGC_LUT_R32[7:0] | | | | | | | | FC |
| 35th parameter | 1 | ↑ | 1 | - | DGC_LUT_G00[7:0] | | | | | | | | 00 |
| 36th parameter | 1 | ↑ | 1 | - | DGC_LUT_G01[7:0] | | | | | | | | 08 |
| : | 1 | ↑ | 1 | - | : | | | | | | | | : |
| 67th parameter | 1 | ↑ | 1 | - | DGC_LUT_G32[7:0] | | | | | | | | FC |
| 68th parameter | 1 | ↑ | 1 | - | DGC_LUT_B00[7:0] | | | | | | | | 00 |
| 69th parameter | 1 | ↑ | 1 | - | DGC_LUT_B01[7:0] | | | | | | | | 08 |
| : | 1 | ↑ | 1 | - | : | | | | | | | | : |
| 100th parameter | 1 | ↑ | 1 | - | DGC_LUT_B32[7:0] | | | | | | | | FC |
| Description | **DGC_EN:** Digital gamma correction enable.<br>'0': Disable<br>'1': Enable<br><br>For more information about these registers, refer to "5.10.2Gray Voltage Generator for Digital Gamma Correction" section | | | | | | | | | | | | |
| Restrictions | Must enable SETEXTC command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.82 SETID: set ID (C3h)

| C3 H | SETID ( Set ID) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3 |
| 1st parameter | 1 | ↑ | 1 | - | ID1[7:0] | | | | | | | | 00 |
| 2nd parameter | 1 | ↑ | 1 | - | ID2[7:0] | | | | | | | | 00 |
| 3rd parameter | 1 | ↑ | 1 | - | ID3[7:0] | | | | | | | | 00 |
| 4th parameter | 1 | 1 | ↑ | - | - | - | - | - | - | ID_OTP_TIMES[2:0] | | | 00 |

**Description**

This command is used to set ID.

**ID_OTP_TIMES[2:0]:** Read ID OTP programmed times.

| ID_OTP_TIMES[2:0] | ID OTP programmed times |
|---|---|
| 3'b000 | Not programmed |
| 3'b001 | 1 time |
| 3'b010 | 2 times |
| 3'b011 | 3 times |
| 3'b100 | 4 times |

**Restrictions**

Must enable SETEXTC command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.83 SETDDB: Set DDB (C4h)

| C4h | SETDDB ( Set DDB) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 |
| 1st parameter | 1 | 1 | ↑ | - | DDB1[7:0] | | | | | | | | - |
| 2nd parameter | 1 | 1 | ↑ | - | DDB2[7:0] | | | | | | | | - |
| 3rd parameter | 1 | 1 | ↑ | - | DDB3[7:0] | | | | | | | | - |
| 4th parameter | 1 | 1 | ↑ | - | DDB4[7:0] | | | | | | | | - |
| Description | This command is used to set DDB value. | | | | | | | | | | | | |
| Restrictions | SETEXTC turn on to enable this command. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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### 6.2.84 SETCABC: set CABC related setting (C9h)

| C9 H | SETCABC( Set CABC Related Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9 |
| 1st parameter | 1 | ↑ | 1 | - | BC_ ON | PWMDIV[2:0] | | | 1 | 1 | INVP LUS | 1 | 0F |
| 2nd parameter | 1 | ↑ | 1 | - | PWM_PERIOD[7:0] | | | | | | | | 23 |

**Description**

This command is used to set CABC parameter

**BC_ON:** The control reigister for LED driver when IC needs enable signal.
**'0':** CABC_ON pin='L'
**'1':** CABC_ON pin='H'

**INVPLUS:** The backlight PWM output polarity select.
**'0',** The backlight PWM output is low level active.
**'1',** The backlight PWM output is high level active.

**PWMDIV[2:0]:** Internal PWM_CLK divider for CABC clock.

| PWMDIV[2:0] | | | Brightness Control Clock |
|---|---|---|---|
| 0 | 0 | 0 | PWM_CLK / 1 |
| 0 | 0 | 1 | PWM_CLK / 2 |
| 0 | 1 | 0 | PWM_CLK / 4 |
| 0 | 1 | 1 | PWM_CLK / 8 |
| 1 | 0 | 0 | PWM_CLK / 16 |
| 1 | 0 | 1 | PWM_CLK / 32 |
| 1 | 1 | 0 | PWM_CLK / 64 |
| 1 | 1 | 1 | PWM_CLK / 128 |

**PWM_PERIOD[7:0]:** The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV )) x (256x(PWM_PERIOD[7:0]+1)).

**Restrictions**

Must enable SETEXTC command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.85 SETPanel: set panel characteristic (CCh)

| CCH | SETPANEL( Set Panel characteristic register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | SM_PANEL | SS_PANEL | GS_PANEL | REV_PANEL | BGR_PANEL | 00 |
| Description | This command is used to set Panel characteristic related register<br>**REV_PANEL:** The source output data polarity selected.<br>'0': normally white panel.<br>'1': normally black panel.<br>**BGR_PANEL:** The color filter order direction selected.<br>'0': S1:S2:S3='R':'G':'B'<br>'1': S1:S2:S3='B':'G':'R'<br>**GS_PANEL:** The gate driver output shift direction selected.<br>'0': G1→G480<br>'1': G480→G1<br>**SS_PANEL:** The source driver output shift direction selected.<br>'0': S1→S960<br>'1': S960→S1<br>**SM_PANEL**: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin. | | | | | | | | | | | | |
| Restrictions | Must enable SETEXTC command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.86 SETGamma: set gamma curve (E0h)

| E0H | SETGAMMA ( Set Gamma Curve Related Setting ) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 |
| 1st parameter | 1 | 1 | ↑ | - | - | VRP0[6:0] | | | | | | | |
| 2nd parameter | 1 | 1 | ↑ | - | - | VRP1[6:0] | | | | | | | |
| 3rd parameter | 1 | 1 | ↑ | - | - | VRP2[6:0] | | | | | | | |
| 4th parameter | 1 | 1 | ↑ | - | - | VRP3[6:0] | | | | | | | |
| 5th parameter | 1 | 1 | ↑ | - | - | VRP4[6:0] | | | | | | | |
| 6th parameter | 1 | 1 | ↑ | - | - | VRP5[6:0] | | | | | | | |
| 7th parameter | 1 | 1 | ↑ | - | - | VRP6[6:0] | | | | | | | |
| 8th parameter | 1 | 1 | ↑ | - | - | VRP7[6:0] | | | | | | | |
| 9th parameter | 1 | 1 | ↑ | - | - | VRP8[6:0] | | | | | | | |
| 10th parameter | 1 | 1 | ↑ | - | - | VRP9[6:0] | | | | | | | |
| 11th parameter | 1 | 1 | ↑ | - | - | VRP10[6:0] | | | | | | | |
| 12th parameter | 1 | 1 | ↑ | - | - | VRP11[6:0] | | | | | | | |
| 13th parameter | 1 | 1 | ↑ | - | - | VRP12[6:0] | | | | | | | |
| 14th parameter | 1 | 1 | ↑ | - | - | VRP13[6:0] | | | | | | | |
| 15th parameter | 1 | 1 | ↑ | - | - | VRP14[6:0] | | | | | | | |
| 16th parameter | 1 | 1 | ↑ | - | - | VRP15[6:0] | | | | | | | |
| 17th parameter | 1 | 1 | ↑ | - | - | VRN0[6:0] | | | | | | | |
| 18th parameter | 1 | 1 | ↑ | - | - | VRN1[6:0] | | | | | | | |
| 19th parameter | 1 | 1 | ↑ | - | - | VRN2[6:0] | | | | | | | |
| 20th parameter | 1 | 1 | ↑ | - | - | VRN3[6:0] | | | | | | | |
| 21th parameter | 1 | 1 | ↑ | - | - | VRN4[6:0] | | | | | | | |
| 22th parameter | 1 | 1 | ↑ | - | - | VRN5[6:0] | | | | | | | |
| 23th parameter | 1 | 1 | ↑ | - | - | VRN6[6:0] | | | | | | | |
| 24th parameter | 1 | 1 | ↑ | - | - | VRN7[6:0] | | | | | | | |
| 25th parameter | 1 | 1 | ↑ | - | - | VRN8[6:0] | | | | | | | |
| 26th parameter | 1 | 1 | ↑ | - | - | VRN9[6:0] | | | | | | | |
| 27th parameter | 1 | 1 | ↑ | - | - | VRN10[6:0] | | | | | | | |
| 28th parameter | 1 | 1 | ↑ | - | - | VRN11[6:0] | | | | | | | |
| 29th parameter | 1 | 1 | ↑ | - | - | VRN12[6:0] | | | | | | | |
| 30th parameter | 1 | 1 | ↑ | - | - | VRN13[6:0] | | | | | | | |
| 31th parameter | 1 | 1 | ↑ | - | - | VRN14[6:0] | | | | | | | |
| 32th parameter | 1 | 1 | ↑ | - | - | VRN15[6:0] | | | | | | | |
| 33th parameter | 1 | 1 | ↑ | - | CGN1[1:0] | | CGN0[1:0] | | CGP1[1:0] | | CGP0[1:0] | | |
| 34th parameter | 1 | 1 | ↑ | - | | | | | | | | GMA_RELOAD | |

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<table>
<tr><td>Description</td><td>

**GMA_RELOAD:** Enable this gamma register function.

| Positive/Negative Polarity | Description |
|---|---|
| VRP0/VRN0 | Variable resistor (VR0)for V0 offset adjustment |
| VRP1/VRN1 | Variable resistor (VR1)for V1 offset adjustment |
| VRP2/VRN2 | Variable resistor (VR2)for V2 offset adjustment |
| VRP3/VRN3 | Variable resistor (VR3)for V4 offset adjustment |
| VRP4/VRN4 | Variable resistor (VR4)for V6 offset adjustment |
| VRP5/VRN5 | Variable resistor (VR5)for V13 offset adjustment |
| VRP6/VRN6 | Variable resistor (VR6)for V20 offset adjustment |
| VRP7/VRN7 | Variable resistor (VR7)for V27 offset adjustment |
| VRP8/VRN8 | Variable resistor (VR8)for V36 offset adjustment |
| VRP9/VRN9 | Variable resistor (VR9)for V43 offset adjustment |
| VRP10/VRN10 | Variable resistor (VR10)for V50 offset adjustment |
| VRP11/VRN11 | Variable resistor (VR11)for V57 offset adjustment |
| VRP12/VRN12 | Variable resistor (VR12)for V59 offset adjustment |
| VRP13/VRN13 | Variable resistor (VR13)for V61 offset adjustment |
| VRP14/VRN14 | Variable resistor (VR14)for V62 offset adjustment |
| VRP15/VRN15 | Variable resistor (VR15)for V63 offset adjustment |

</td></tr>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

</td></tr>
</table>

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### 6.2.87 SETCOLOR: Set Color (EBh)

| EBh | SETCOLOR (Set Color) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15~D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EB |
| 1st parameter | 1 | 1 | ↑ | - | Bkx1 | Bkx0 | Bky1 | Bky0 | Wx1 | Wx0 | Wy1 | Wy0 | - |
| 2nd parameter | 1 | 1 | ↑ | - | Bkx9 | Bkx8 | Bkx7 | Bkx6 | Bkx5 | Bkx4 | Bkx3 | Bkx2 | |
| 3rd Parameter | 1 | 1 | ↑ | - | Bky9 | Bky8 | Bky7 | Bky6 | Bky5 | Bky4 | Bky3 | Bky2 | |
| 4th Parameter | 1 | 1 | ↑ | - | Wx9 | Wx8 | Wx7 | Wx6 | Wx5 | Wx4 | Wx3 | Wx2 | |
| 5th Parameter | 1 | 1 | ↑ | - | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | |
| 6th Parameter | 1 | 1 | ↑ | - | Rx1 | Rx0 | Ry1 | Ry0 | Gx1 | Gx0 | Gy1 | Gy0 | |
| 7th Parameter | 1 | 1 | ↑ | - | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | Rx3 | Rx2 | |
| 8th Parameter | 1 | 1 | ↑ | - | Ry9 | Ry8 | Ry7 | Ry6 | Ry5 | Ry4 | Ry3 | Ry2 | |
| 9th Parameter | 1 | 1 | ↑ | - | Gx9 | Gx8 | Gx7 | Gx6 | Gx5 | Gx4 | Gx3 | Gx2 | |
| 10th Parameter | 1 | 1 | ↑ | - | Gy9 | Gy8 | Gy7 | Gy6 | Gy5 | Gy4 | Gy3 | Gy2 | |
| 11th Parameter | 1 | 1 | ↑ | - | Bx1 | Bx0 | By1 | By0 | Ax1 | Ax0 | Ay1 | Ay0 | |
| 12th Parameter | 1 | 1 | ↑ | - | Bx9 | Bx8 | Bx7 | Bx6 | Bx5 | Bx4 | Bx3 | Bx2 | |
| 13th Parameter | 1 | 1 | ↑ | - | By9 | By8 | By7 | By6 | By5 | By4 | By3 | By2 | |
| 14th Parameter | 1 | 1 | ↑ | - | Ax9 | Ax8 | Ax7 | Ax6 | Ax5 | Ax4 | Ax3 | Ax2 | |
| 15th Parameter | 1 | 1 | ↑ | - | Ay9 | Ay8 | Ay7 | Ay6 | Ay5 | Ay4 | Ay3 | Ay2 | |
| Description | **Bkx[9:0]:**<br>Set the Bkx bits of black color characteristics.<br><br>**Bky[9:0]:**<br>Set the Bky bits of black color characteristics.<br><br>**Wx[9:0]:**<br>Set the Wx bits of white color characteristics.<br><br>**Wy[9:0]:**<br>Set the Wy bits of white color characteristics.<br><br>**Rx[9:0]:**<br>Set the Rx bits of red color characteristics.<br><br>**Ry[9:0]:**<br>Set the Ry bits of red color characteristics.<br><br>**Gx[9:0]:**<br>Set the Gx bits of green color characteristics.<br><br>**Gy[9:0]:**<br>Set the Gy bits of green color characteristics.<br><br>**Bx[9:0]:**<br>Set the Bx bits of blue color characteristics.<br><br>**By[9:0]:**<br>Set the By bits of blue color characteristics.<br><br>**Ax[9:0]:**<br>Set the Ax bits of A color characteristics.<br><br>**Ay[9:0]:**<br>Set the Ay bits of A color characteristics. | | | | | | | | | | | | |
| Restrictions | SETEXTC turn on to enable this command. | | | | | | | | | | | | |

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Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

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### 6.2.88 SETREADINDEX: Set SPI Read Index (FEh)

| FEh | SET SPI READ INDEX (Set SPI READ Command Address) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE |
| 1st parameter | 1 | 1 | ↑ | - | CMD_ADD[7:0] | | | | | | | | - |
| Description | SET SPI READ Command Address for User Define Command. | | | | | | | | | | | | |
| Restrictions | SETEXTC turn on to enable this command | | | | | | | | | | | | |
| Register Availability | Status: Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In or Booster Off — Availability: Yes | | | | | | | | | | | | |

### 6.2.89 GETSPIREAD: SPI Read Command Data (FFh)

| FFh | GETSPIREAD (Read Command Data) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| 1st parameter | 1 | ↑ | 1 | - | CMD_DATA1[7:0] | | | | | | | | - |
| : | 1 | ↑ | 1 | - | : | | | | | | | | - |
| nth parameter | 1 | ↑ | 1 | - | CMD_DATAn[7:0] | | | | | | | | - |
| Description | Read SPI Command Data for User Define Command. | | | | | | | | | | | | |
| Restrictions | SETEXTC turn on to enable this command. | | | | | | | | | | | | |
| Register Availability | Status: Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In or Booster Off — Availability: Yes | | | | | | | | | | | | |

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# 7. Layout Recommendation

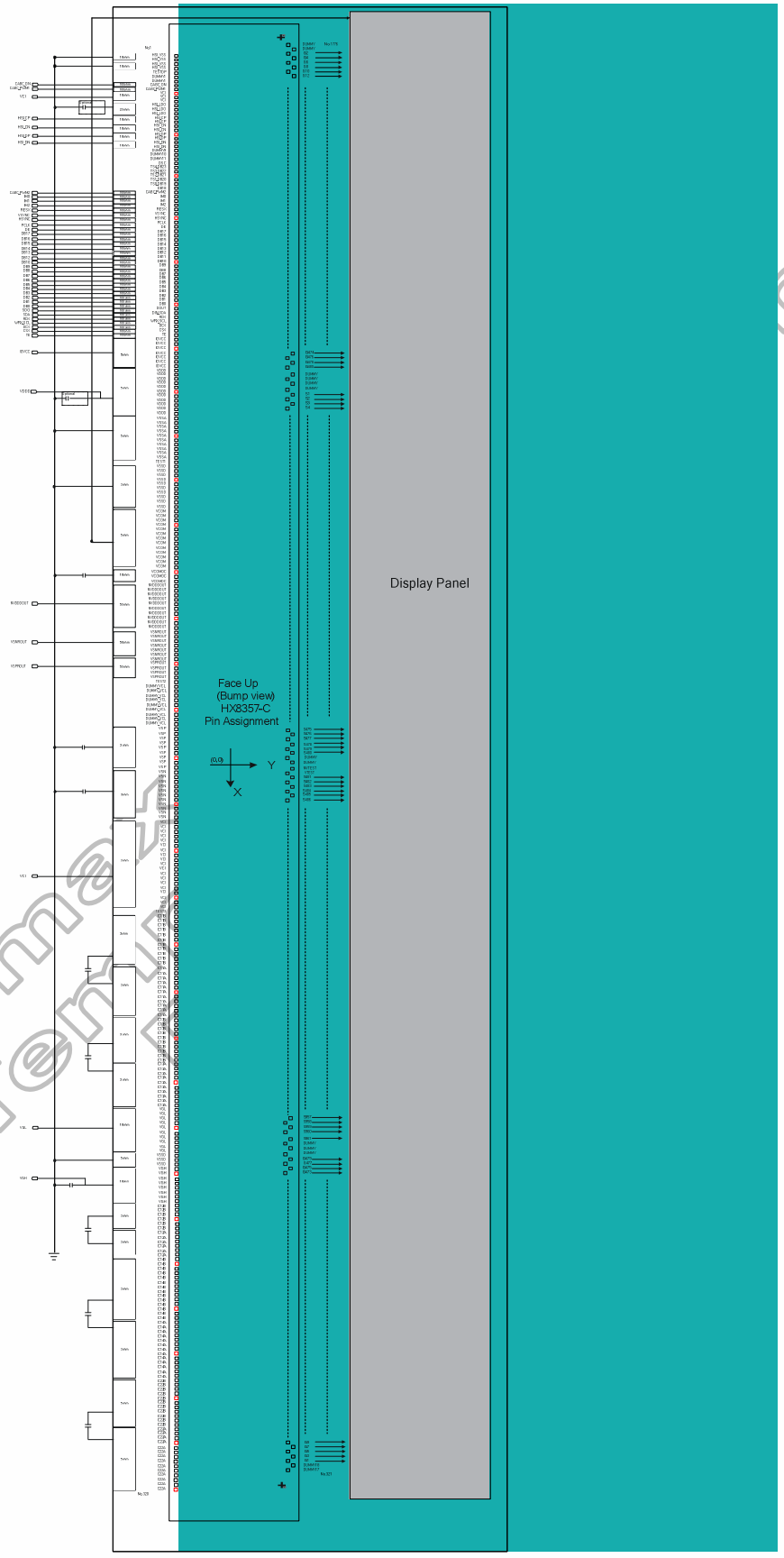


**Figure 7.1: Layout recommendation of HX8357-C**


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## 7.1 Maximum layout resistance

| Name | Type | Maximum Series Resistance | Unit |
|---|---|---|---|
| IOVCC | Power supply | 5 | Ω |
| VCI | Power supply | 3 | Ω |
| HSI_VCC | Power supply | 10 | Ω |
| VSSA | Power supply | 5 | Ω |
| HSI_VSS | Power supply | 10 | Ω |
| VSSD | Power supply | 3 | Ω |
| OSC | Input | 100 | Ω |
| IM[2:0] | Input | 100 | Ω |
| RDX, WRX_SCL, DCX, CSX, DIN_SDA | Input | 100 | Ω |
| RESX | Input | 100 | Ω |
| TE, CABC_PWM, CABC_ON,DOUT | Output | 100 | Ω |
| DB[17:0] | I/O | 100 | Ω |
| HSI_DN,HSI_DP,HSI_CN,HSI_CP | I/O | 10 | Ω |
| PCLK, DE, VSYNC, HSYNC | Input | 100 | Ω |
| VGH | Output | 10 | Ω |
| VGL | Output | 10 | Ω |
| HSI_LDO | Capacitor connection | 20 | Ω |
| VCOMDC | Capacitor connection | 10 | Ω |
| VSN | Capacitor connection | 3 | Ω |
| VSP | Capacitor connection | 3 | Ω |
| VDDD | Capacitor connection | 5 | Ω |
| VSPROUT,VSNROUT, NVDDDOUT | Output | 50 | Ω |
| C13A, C13B, C14A, C14B | Capacitor connection | 3 | Ω |
| C11A, C11B ,C12A, C12B | Capacitor connection | 3 | Ω |
| TEST[3:1] | Input | 100 | Ω |
| DUMMY_VCL, DB18, TS0_DB19, TS1_DB20,TS2_DB21,TS3_DB22,TS4_DB23 | Dummy | 100 | Ω |
| TS[7:5] | Output | 100 | Ω |
| VCOM | Panel connection | 5 | Ω |
| C22B, C22A | Capacitor connection | 5 | Ω |
| DUMMY | Dummy | 100 | Ω |
| VTEST, NVTEST | Test Pin | 100 | Ω |

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## 7.2 External components connection

| Capacitor | Recommended voltage | Capacity |
|---|---|---|
| C1 (C13A/B) | 10V | 1 µF (B characteristics) |
| C2 (C11A/B) | 10V | 1 µF (B characteristics) |
| C3 (VSP) | 10V | 1 µF ~ 2.2uF (B characteristics) |
| C4 (C14A/B) | 10V | 1 µF (B characteristics) |
| C5 (C12A/B) | 10V | 1 µF (B characteristics) |
| C6 (VSN) | 10V | 1 µF~2.2uF (B characteristics) |
| C7 (C22A/B) | 16V | 1 µF (B characteristics) |
| C8 (VGH) | 25V | 1 µF (B characteristics) |
| C9 (VCOMDC) | 6V | 1 µF (B characteristics) |
| C10(VDDD) | 6V | 1 µF (B characteristics) |
| C11(HSI_LDO) | 6V | 1 µF (B characteristics) |

Note: If not use High speed interface (MDDI/DSI), the Chsi_ldo can remove

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# 8. Electrical Characteristic

## 8.1 Absolute maximum ratings

| Item | Symbol | Unit | Spec. | | | Note |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Power Supply Voltage 1 | IOVCC~VSSD | V | -0.3 | - | +4.6 | Note(1),(2) |
| Power Supply Voltage 2 | VCI ~ VSSA | V | -0.3 | - | +4.6 | Note(3) |
| Power Supply Voltage 3 | VSP ~ VSSA | V | -0.3 | - | +6.6 | Note(4) |
| Power Supply Voltage 4 | VSSA ~ VSN | V | -0.3 | - | +6.6 | Note(5) |
| Power Supply Voltage 5 | VGH ~ VSSA | V | -0.3 | - | +18.5 | Note(6) |
| Power Supply Voltage 6 | VSSA ~ VGL | V | -16.5 | - | 0 | Note(7) |
| Logic Input Voltage | $V_{IN}$ | V | -0.3 | - | IOVCC+0.5 | - |
| Logic Output Voltage | Vo | V | -0.3 | - | IOVCC+0.5 | - |
| Operating Temperature | Topr | ℃ | -40 | - | +85 | Note(8),(9) |
| Storage Temperature | Tstg | ℃ | -55 | - | +110 | Note(8),(9) |

**Note:** (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure VSP ≥ VSSA.
(5) To make sure VSSA ≥ VSN.
(6) To make sure VGH ≥ VSSA.
(7) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(8) For die and wafer products, specified up to +85℃.
(9) This temperature specifications apply to the TCP package.

**Table 8.1: Absolute maximum ratings**

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## 8.2 DC characteristics(T.B.D)

| Parameter | Symbol | Conditions | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **Power & Operating Voltages** | | | | | | |
| IO Operating voltage | IOVCC | I/O supply voltage | 1.65 | 1.8 | 3.3 | V |
| Driver Operating voltage | VCI | Operation voltage | 2.5 | 2.8 | 3.3 | |
| Source Drive Voltage | VSPROUT | Dual Pump | | | | |
| | VSPROUT | Triple Pump | | | | |
| | VSNROUT | Dual Pump | | | | |
| | VSNROUT | Triple Pump | | | | |
| Gate Drive High Voltage | VGH | VCI=2.8V Dual Pump (Typ:BT=001) | | | | |
| | | IVGH=80uA | | | | |
| Gate Drive Low Voltage | VGL | VCI=2.8V Dual Pump (Typ:BT=001) | - | - | - | |
| | | IVGL=-80uA | | | | |
| Drive Supply Voltage | \|VGH-VGL\| | - | - | - | 30 | |
| **Input / Output** | | | | | | |
| High level input voltage | VIH | - | 0.7IOVCC | - | IOVCC | V |
| Low level input voltage | VIL | - | VSSD | - | 0.3IOVCC | |
| High level output voltage | VOH | IOH = -1.0mA | 0.8IOVCC | - | IOVCC | |
| Low level output voltage | VOL | IOL = +1.0mA | VSSD | - | 0.2IOVCC | |
| Input leakage current | IIL | - | -1 | - | 1 | µA |
| Oscillator frequency | fOSC | Frame rate at 60hz,default Vs and Hs setting Ta=25℃ | | | | MHz |
| **Booster(VCI=2.8V)** | | | | | | |
| VSP boost voltage | VSP | Dual Pump IVSP=1mA | | | | V |
| | | Triple Pump IVSP=1mA | | | | |
| VSN boost voltage | VSN | Dual Pump IVSN=-1mA | | | | |
| | | Triple Pump IVSN=-1mA | | | | |
| **VCOM Generator(VCI=2.8V)** | | | | | | |
| VCOM amplitude | VCOM | No load, | -2.5 | - | 0 | V |
| **Source Driver(Typ:Ta=25℃ VCI=2.8v)** | | | | | | |
| Output voltage deviation (mean value) | DVOS | VSSD+1.0 ~ VSPROUT-1.0 | - | +/- 10 | +/- 20 | mV |
| | | VSSD+0.1V ~ VSSD+1.0 VSPROUT-1.0 ~ VSPROUT-0.1V | - | +/- 30 | +/- 50 | mV |
| Output voltage range | VOS | - | 0.1 | - | VSP-0.1 | V |
| Output offset voltage | Voff | - | | +/-30 | +/-50 | mV |
| **Current Consumption(Typ: $T_A$=25℃ IOVCC=VCI=2.8V)** | | | | | | |
| Normal operation | Iiovcc | GRAM data =0000h Frame rate=60Hz | - | TBD | - | mA |
| | Ivci | | - | TBD | - | mA |
| Sleep in (DBI interface) | Iiovcc | - | - | - | 2 | µA |
| | Ivci | - | - | - | 20 | µA |
| Sleep in (MDDI interface) | Iiovcc | - | - | - | 2 | µA |
| | Ivci | - | - | - | 50 | µA |
| Sleep in (DSI interface) | Iiovcc | - | - | - | 2 | µA |
| | Ivci | - | - | - | 50 | µA |

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## 8.3 AC characteristics(T.B.D)

### 8.3.1 DBI Type B interface characteristic

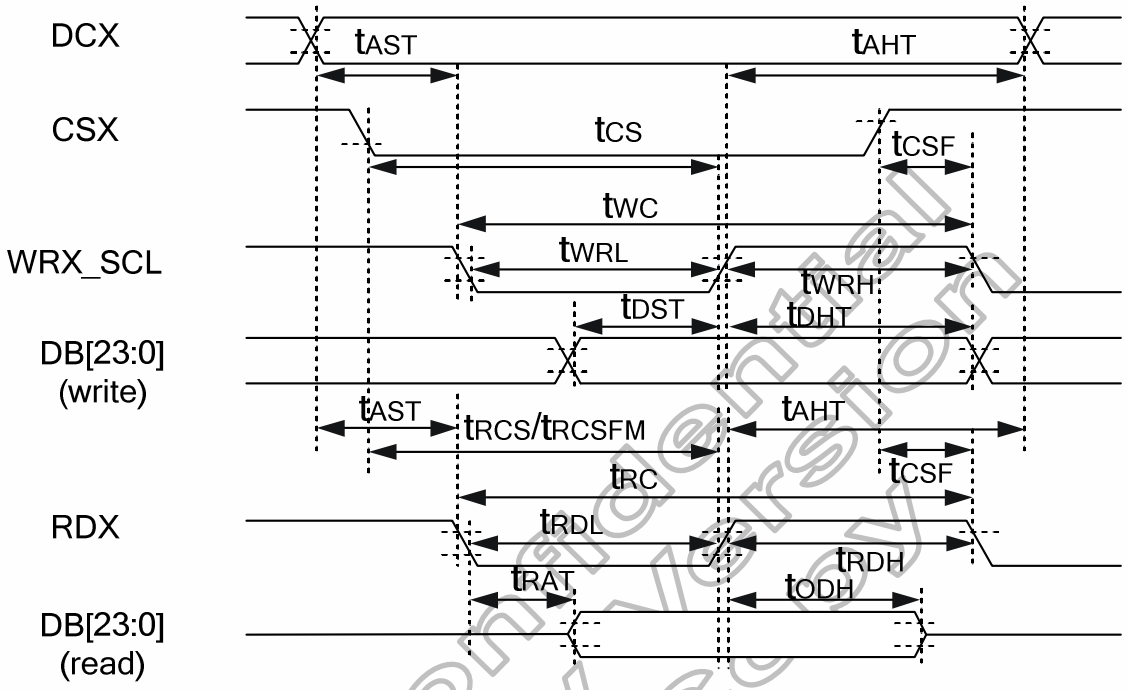


**Figure 8.1: DBI Type B interface characteristics**

**(VSSA=0V, VDD1=1.8V, VDD3=2.8V, $T_A$=25℃)**

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| DCX | $t_{AST}$ | Address setup time | 0 | - | ns | - |
| | $t_{AHT}$ | Address hold time (Write/Read) | 10 | - | | |
| CSX | $t_{CS}$ | Chip select setup time (Write) | 10 | - | ns | - |
| | $t_{RCS}$ | Chip select setup time (Read register) | 45 | - | | |
| | $t_{RCSFM}$ | Chip select setup time (GRAM) | 355 | - | | |
| | $t_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | | |
| WRX_SCL | $t_{WC}$ | Write cycle (write register) | 50 | - | ns | - |
| | $t_{WC}$ | Write cycle (write GRAM@SLPOUT) | 47 | - | | |
| | $t_{WC}$ | Write cycle (write GRAM@SLPIN) | 100 | - | | |
| | $t_{WRH}$ | Control pulse “H” duration | 15 | - | | |
| | $t_{WRL}$ | Control pulse “L” duration | 15 | - | | |
| RDX | $t_{RC}$ | Read cycle (read register) | 160 | - | ns | - |
| | $t_{RC}$ | Read cycle (GRAM) | 450 | - | | |
| | $t_{RDH}$ | Control pulse “H” duration | 90 | - | | |
| | $t_{RDL}$ | Control pulse “L” duration(read register) | 35 | - | | |
| | $t_{RDL}$ | Control pulse “L” duration(GRAM) | 345 | - | | |
| DB[23:0] | $t_{DST}$ | Data setup time | 10 | - | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| | $t_{DHT}$ | Data hold time | 10 | - | | |
| | $t_{RAT}$ | Read access time(read register) | - | 40 | | |
| | $t_{RAT}$ | Read access time(GRAM) | - | 340 | | |
| | $t_{ODH}$ | Output disable time | 20 | 80 | | |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

**Table 8.2: DBI Type B interface characteristics**

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### 8.3.2 DBI Type C interface characteristics

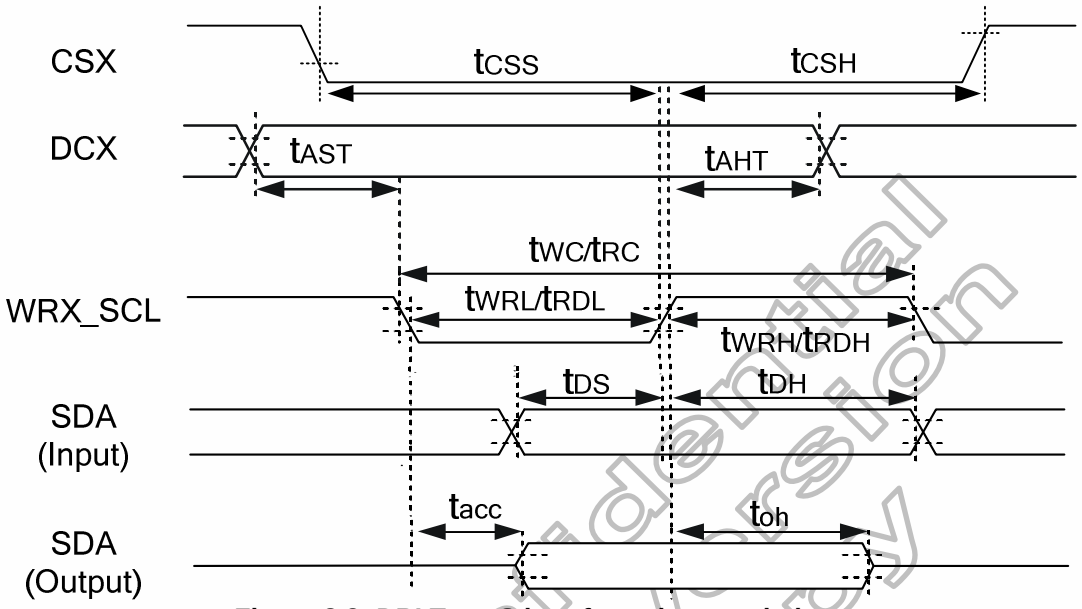


**Figure 8.2: DBI Type C interface characteristics**

**(VSSA=0V, IOVCC=1.8V, VCI=2.8V, $T_A$ = 25℃)**

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $t_{CSS}$<br>$t_{CSS}$<br>$t_{CSH}$<br>$t_{CSH}$ | Chip select setup time (Write)<br>Chip select setup time (Read)<br>Chip select hold time (Write)<br>Chip select hold time (Read) | 15<br>60<br>15<br>65 | -<br>-<br>-<br>- | ns | - |
| DCX | $t_{AST}$<br>$t_{AHT}$ | Address setup time<br>Address hold time (Write/Read) | 0<br>10 | -<br>- | ns | - |
| WRX_SCL (Write) | $t_{WC}$<br>$t_{WRH}$<br>$t_{WRL}$ | Write cycle<br>Control pulse “H” duration<br>Control pulse “L” duration | 66<br>15<br>15 | -<br>-<br>- | ns | - |
| WRX_SCL (Read) | $t_{RC}$<br>$t_{RDH}$<br>$t_{RDL}$ | Read cycle<br>Control pulse “H” duration<br>Control pulse “L” duration | 150<br>60<br>60 | -<br>-<br>- | ns | - |
| SDA (Input) | $t_{DS}$<br>$t_{DH}$ | Data setup time<br>Data hold time | 10<br>10 | -<br>- | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| SDA (Output) | $t_{ACC}$<br>$t_{OH}$ | Read access time<br>Output disable time | 10<br>15 | 50<br>50 | ns | |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

**Table 8.3: DBI Type C interface characteristics**

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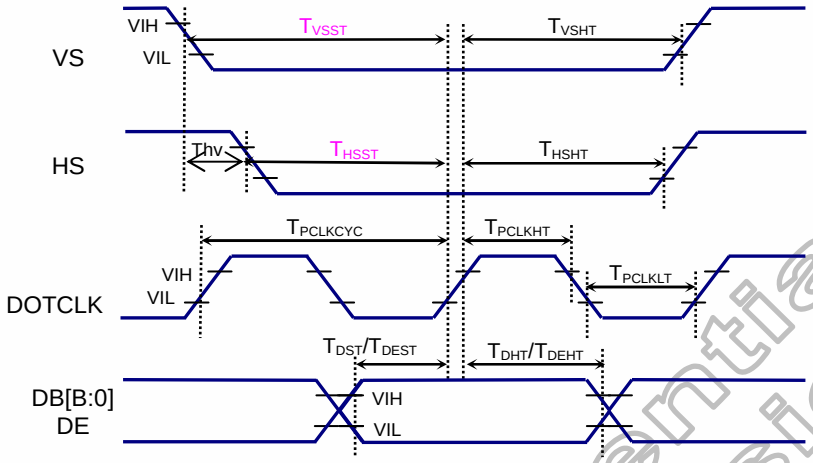
### 8.3.3 DPI interface characteristics



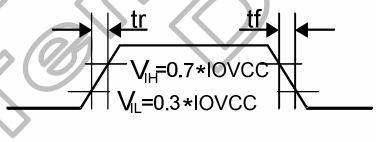

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,$T_A$ = -30 to 70℃)

| Item | Symbol | Condition | Spec. | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Pixel low pulse width | $T_{CLKLT}$ | | 15 | - | - | ns |
| Pixel high pulse width | $T_{CLKHT}$ | | 15 | - | - | ns |
| Vertical Sync. set-up time | $T_{VSST}$ | | 15 | - | - | ns |
| Vertical Sync. hold time | $T_{VSSHT}$ | | 15 | - | - | ns |
| Horizontal Sync. set-up time | $T_{HSST}$ | | 15 | - | - | ns |
| Horizontal Sync. hold time | $T_{VSSHT}$ | | 15 | - | - | ns |
| Data Enable set-up time | $T_{DEST}$ | | 15 | - | - | ns |
| Data Enable hold time | $T_{DEHT}$ | | 15 | - | - | ns |
| Data set-up time | $T_{DST}$ | | 15 | - | - | ns |
| Data hold time | $T_{DHT}$ | | 15 | - | - | ns |
| Phase difference of sync signal falling edge | Thv | | 0 | - | 320 | Dotclk |

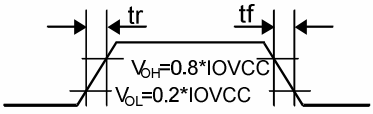
**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

**Table 8.4: DPI interface characteristics-1**

Input Signal Slope




Output Signal Slope

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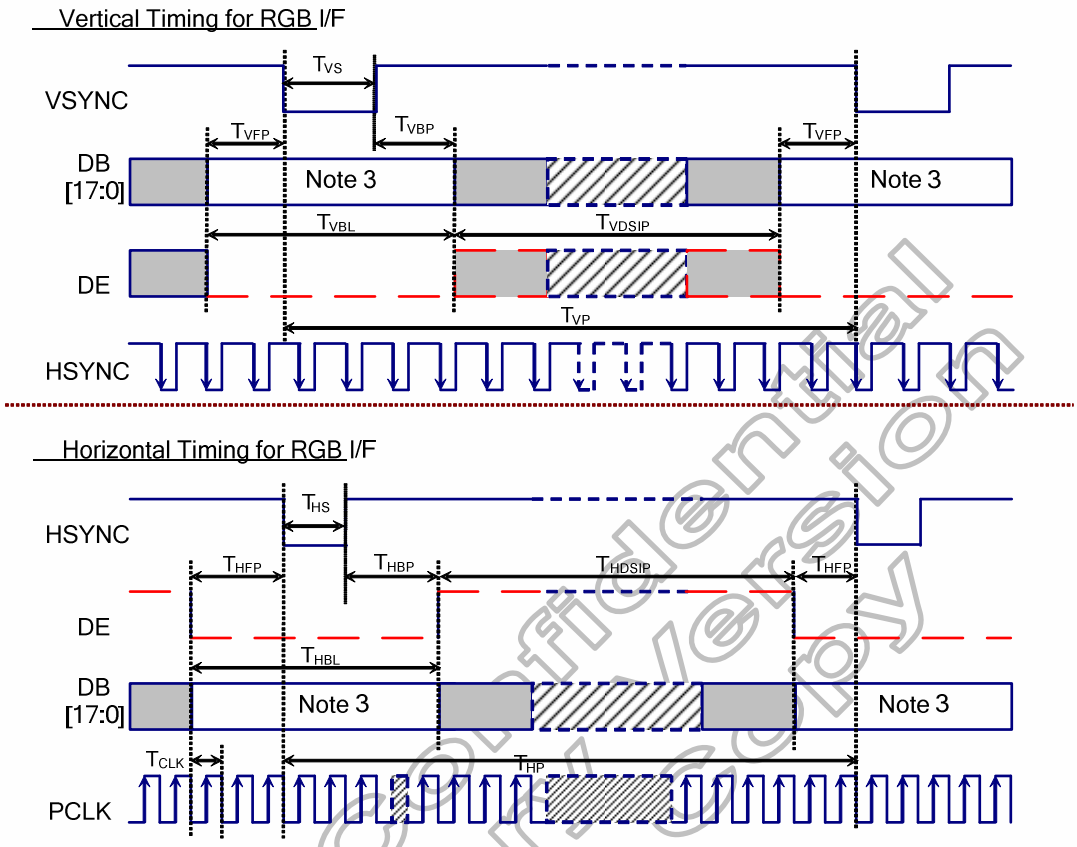


**Figure 8.3: General timings for RGB I/F**

| Item | Symbol | Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Type. | Max | |
| **Vertical Timing** | | | | | | |
| Vertical cycle period | $T_{VP}$ | - | 486 | - | - | HS |
| Vertical low pulse width | $T_{VS}$ | - | 2 | - | - | HS |
| Vertical front porch | $T_{VFP}$ | - | 2 | - | - | HS |
| Vertical back porch | $T_{VBP}$ | - | 2 | - | - | HS |
| Vertical blanking period | $T_{VBL}$ | $T_{VBP} + T_{VFP}$ | 6 | - | - | HS |
| Vertical active area | $T_{VDISP}$ | - | - | 480 | - | HS |
| | | | - | | - | HS |
| | | | | | - | HS |
| Vertical refresh rate | $T_{VRR}$ | Frame rate | 50 | 60 | - | Hz |
| **Horizontal Timing** | | | | | | |
| Horizontal cycle period | $T_{HP}$ | - | 326 | - | - | DOTCLK |
| Horizontal low pulse width | $T_{HS}$ | - | 2 | - | - | DOTCLK |
| Horizontal front porch | $T_{HFP}$ | - | 2 | - | - | DOTCLK |
| Horizontal back porch | $T_{HBP}$ | - | 2 | - | - | DOTCLK |
| Horizontal blanking period | $T_{HBL}$ | $T_{HBP} + T_{HFP}$ | 6 | - | - | DOTCLK |
| Horizontal active area | $T_{HDISP}$ | - | - | 320 | - | DOTCLK |
| Pixel clock cycle TVRR=60Hz | $f_{CLKCYC}$ | - | - | - | - | MHz |

**Note:** (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of PCLK.

**Table 8.5: DPI interface characteristics-2**

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### 8.3.4 Reset input timing

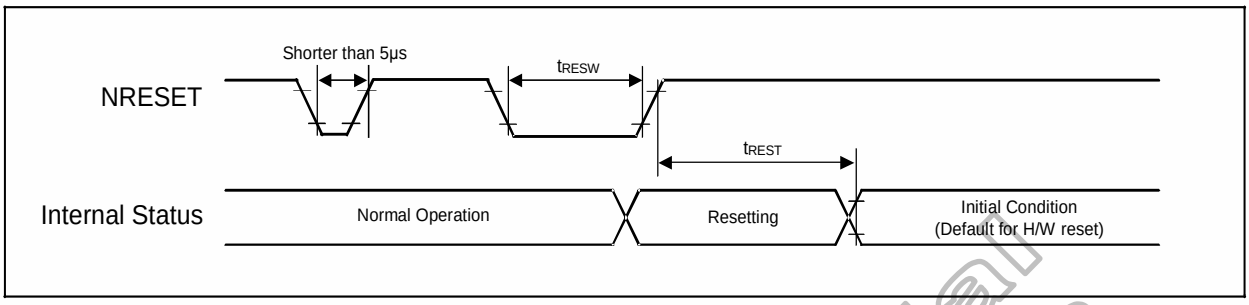



**Figure 8.4: Reset input timing**

| Symbol | Parameter | Related Pins | Spec. | | | Note | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| tRESW | Reset low pulse width(1) | NRESET | 10 | - | - | - | µs |
| tREST | Reset complete time(2) | - | 5 | - | - | When reset applied during SLPIN mode | ms |
| | | - | 120 | - | - | When reset applied during SLPOUT mode | ms |

**Table 8.6: Reset input timing**

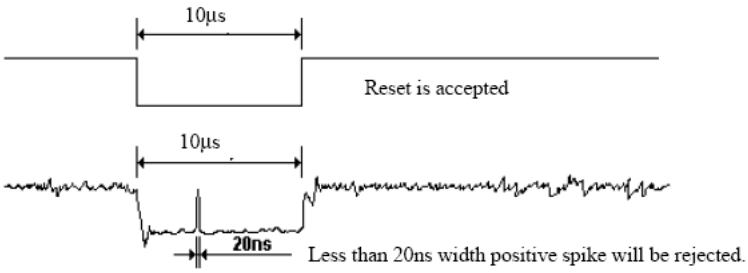
**Note: (**1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

| NRESET Pulse | Action |
|---|---|
| Shorter than 5 µs | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:




(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

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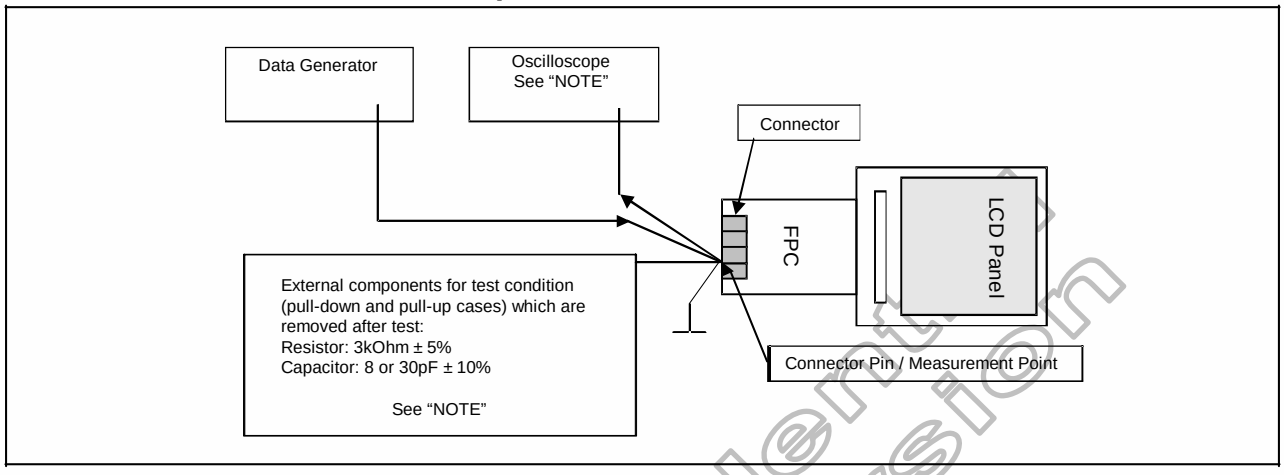
## tACC, tOH measurement condition

### Measurement condition set-up




**Note:** Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

**Figure 8.5: tACC and tOH measurement condition set-up**

### Minimum value measurement

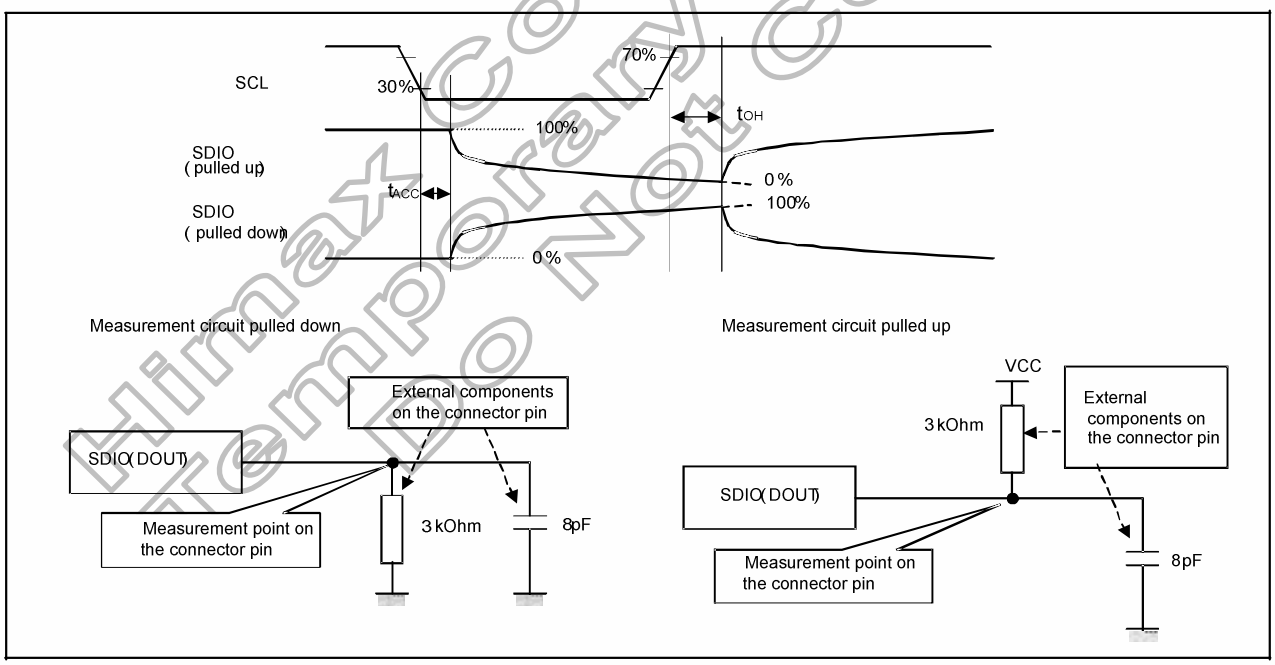



**Figure 8.6: tACC and tOH minimum condition set-up**

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## Maximum value measurement

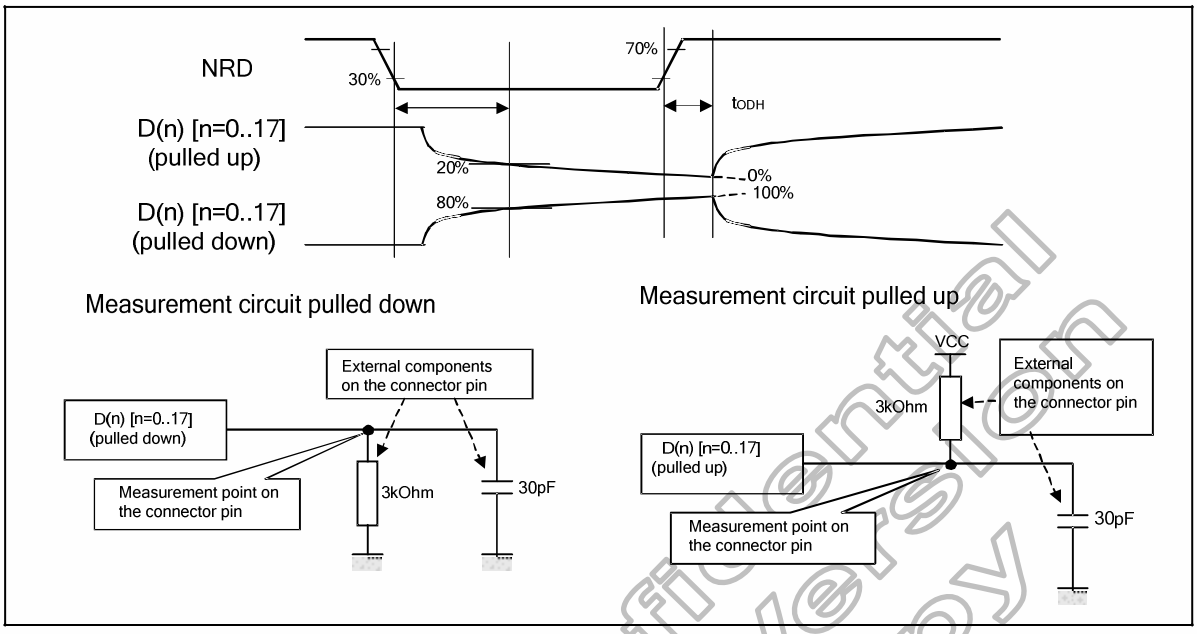


**Figure 8.7: tACC and tOH maximum value measurement**

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### 8.3.5 DSI D-PHY electrical characteristics

#### 8.3.5.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

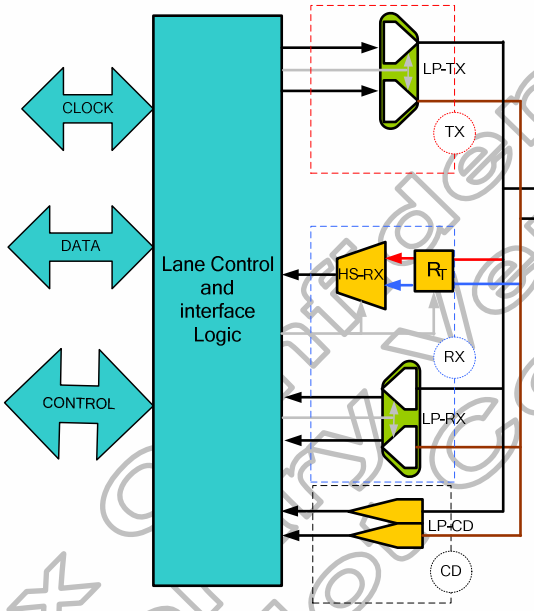


**Figure 8.8: Electrical functions of a fully D-PHY transceiver**

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.7 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

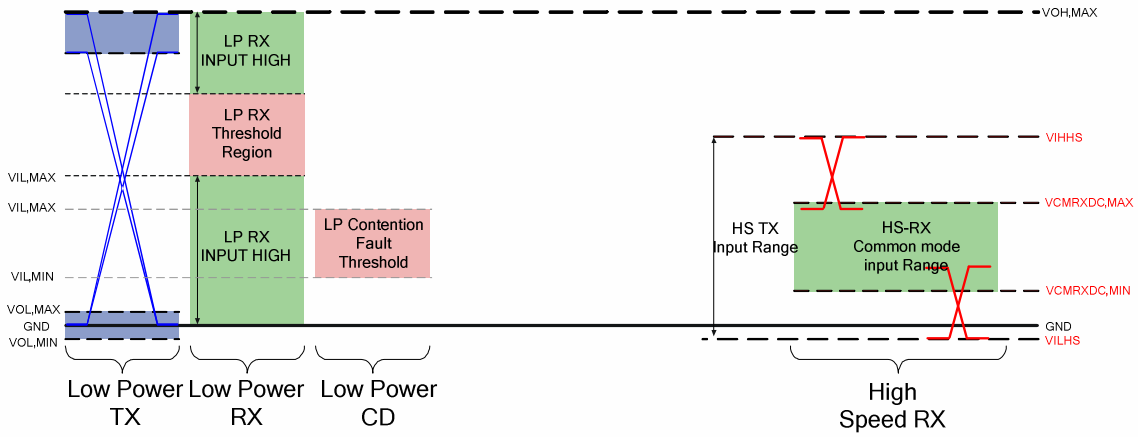


**Figure 8.9: Shows both the HS and LP signal levels**

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### 8.3.5.2 The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Thevenin output low level | -50 | | 50 | mV | |
| $V_{OH}$ | Thevenin output high level | 1.1 | 1.2 | 1.3 | V | |
| $Z_{OLP}$ | Output impedance of LP-TX | 110 | | | Ω | 1 |

Note: Though no maximum value for $Z_{OLP}$ is specified, the LP transmitter output impedance shall ensure the $t_{RLP}/t_{FLP}$ specification is met.

**Table 8.7: LP Transmitter DC Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $t_{RLP}/_{tFLP}$ | 15%-85% rise time and fall time | | | 25 | ns | 1 |
| $\delta V/\delta t_{SR}$ | Slew rate @ CLOAD = 0pF | 30 | | 500 | mV/ns | 1, 3, 5, 6 |
| | Slew rate @ CLOAD = 5pF | | | 300 | mV/ns | 1, 3, 5, 6 |
| | Slew rate @ CLOAD = 20pF | | | 250 | mV/ns | 1, 3, 5, 6 |
| | Slew rate @ CLOAD = 70pF | | | 150 | mV/ns | 1, 3, 5, 6 |
| | Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only) | 30 | | | mV/ns | 1, 2, 3 |
| | Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only) | 30 | | | mV/ns | 1, 3, 7 |
| | Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only) | 30 – 0.075 * (VO,INST – 700) | | | mV/ns | 1, 8, 9 |
| $C_{LOAD}$ | Load capacitance | | | 70 | pF | |

Note:
1. $C_{LOAD}$ includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than $T_{LPX}$ due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
5. This value represents a corner point in a piecewise linear curve.
6. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
7. When the output voltage is between 400 mV and 700 mV.
8. Where $V_{O,INST}$ is the instantaneous output voltage, $V_{DP}$ or $V_{DN}$, in millivolts.
9. When the output voltage is between 700 mV and 930 mV.

**Table 8.8: LP Transmitter AC Specifications**

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### 8.3.5.3 The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

### 8.3.5.4 High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IDTH}$ | Differential input high threshold | | | 70 | mV | |
| $V_{IDTL}$ | Differential input low threshold | -70 | | | mV | |
| $V_{ILHS}$ | Single-ended input low voltage | -40 | | | mV | 1 |
| $V_{IHHS}$ | Single-ended input high voltage | | | 460 | mV | 1 |
| $V_{CMRXDC}$ | Common-mode voltage HS receive mode | 70 | | 330 | mV | 1, 2 |
| $Z_{ID}$ | Differential input impedance | 80 | 100 | 125 | Ω | |

NOTE:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

**Table 8.9: HS Receiver DC Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $\Delta V_{CMRX(HF)}$ | Common mode interference beyond 450 MHz | | | 100 | $mV_{PP}$ | 1 |
| $C_{CM}$ | Common mode termination | | | 60 | pF | 2 |

Note:
1. ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
2. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

**Table 8.10: HS Receiver AC Specifications**

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### 8.3.5.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.8 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

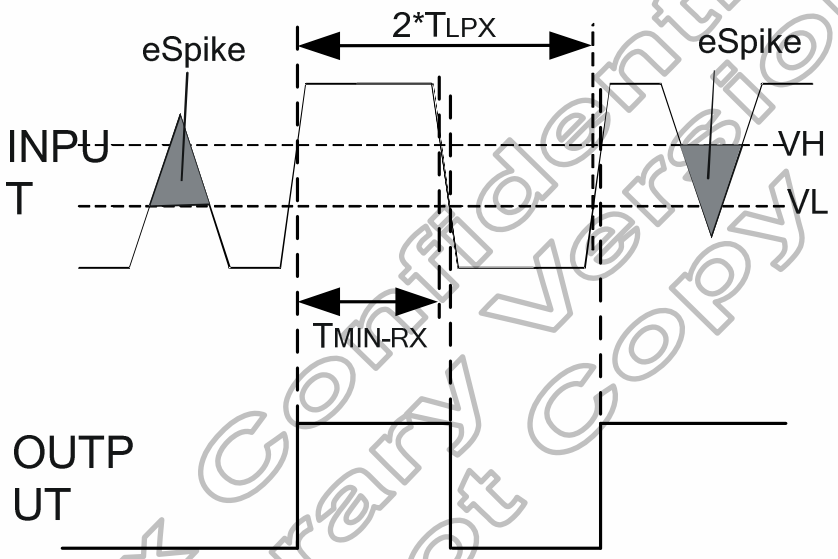


**Figure 8.10: Input Glitch Rejections of Low-Power Receivers**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Logic 0 input threshold | | | 550 | mV | |
| $V_{IH}$ | Logic 1 input threshold | 880 | | | mV | |

**Table 8.11: LP Receiver DC Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $e_{SPIKE}$ | Input pulse rejection | | | 300 | V.ps | 1, 2, 3 |
| $T_{MIN}$ | Minimum pulse width response | 20 | | | ns | 4 |
| $V_{INT}$ | Peak-to-peak interference voltage | | | 200 | mV | |
| $f_{INT}$ | Interference frequency | 450 | | | MHz | |

Note:
1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

**Table 8.12: LP Receiver AC Specifications**

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### 8.3.5.6 Line Contention Detection

Contention can be inferred from any of the following conditions:

1. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than VIL.

2. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VILF.

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IHCD}$ | Logic 1 contention threshold | 450 | | | mV | |
| $V_{ILCD}$ | Logic 0 contention threshold | | | 200 | mV | |

**Table 8.13: Contention Detector DC Specifications**

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### 8.3.5.7 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

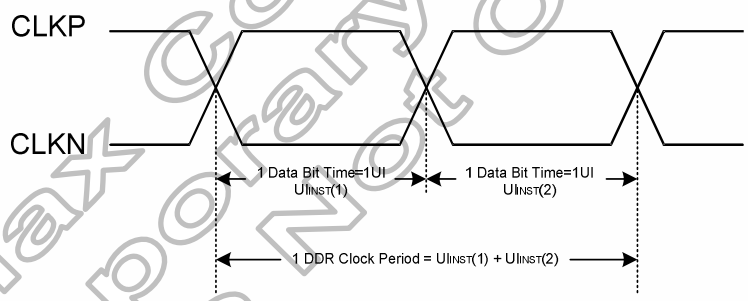


**Figure 8.11: DDR Clock Definition**

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.15.

| Parameter | Symbol | Min | Nom | Max | Unit | Note |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | | | 12.5 | ns | 1, 2 |

Note:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

**Table 8.14: Re verse HS Data Transmission Timing Parameters**

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The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

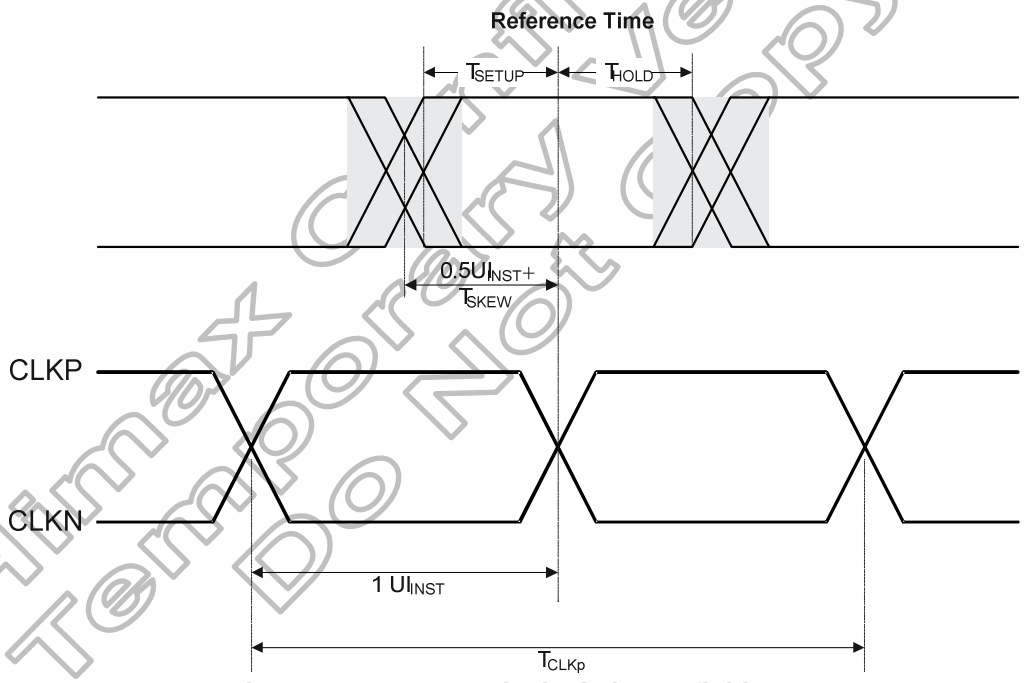


**Figure 8.12: Data to Clock Timing Definitions**

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### 8.3.5.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UIINST, i.e. ±0.2*UIINST for degradation contributed by the interconnect.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Data to Clock Setup Time [receiver] | $T_{SETUP[RX]}$ | 0.15 | | | UIINST | 1 |
| Clock to Data Hold Time [receiver] | $T_{HOLD[RX]}$ | 0.15 | | | UIINST | 1 |

Note:
1. Total setup and hold window for receiver of 0.3*$UI_{INST}$.

**Table 8.15: Data to Clock Timing Specifications**

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# 9. Ordering Information

| Part No. | Package |
|---|---|
| **HX8357-C010 PDxxx** | PD : mean COG<br>xxx : mean chip thickness (μm), (default: 250 μm) |

# 10. Revision History

| Version | Date | Description of Changes |
|---|---|---|
| 01 | 2010/11/23 | New setup. |
| | 2010/12/22 | Modify Pin assignment |
| | 2010/01/24 | Modify Pin assignment<br>Modify User define command<br>Modify Layout Recommendation<br>Modify DBI AC timing<br>Add DSI electrical characteristics |
| | 2010/02/09 | Modify Pin assignment<br>Modify Layout Recommendation |
| | 2010/03/09 | Modify Pin assignment<br>Modify User define command<br>Modify DC characterics<br>Modify Layout Recommendation |
| | 2010/04/07 | Modify Pin assignment<br>Update OTP table<br>Modify Layout Recommendation |
| | 2010/05/03 | Modify Layout Recommendation |

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