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Printed Circuit Design Techniques for the Control of Electromagnetic Interference

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Abstract

This paper addresses the existence, origin, predictability, and control of generated electromagnetic interference (EMI) in high-speed digital designs. The performance bounds imposed by signal integrity issues are integrated with printed circuit board (PCB) design techniques to control the radiation and reception of EMI. Detailed guidelines for PCB design are presented. Optional and newly emerging PCB design approaches are discussed with a focus on high frequency (40+MHz clock) digital systems.

Author

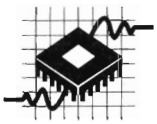
Current Activities:
Michael Conn (Mikon Consulting) offers problem diagnosis, mentorship services, and tutorials in analog design, analog-to-digital interfacing, signal integrity engineering, circuit modeling and analysis, all facets of electromagnetic compatibility engineering, and electronic systems engineering. Research, development, and implementation of challenging (and proprietary) concepts through the pre-production phase is a specialty.

Author Background:
Mike specializes in advanced power electronics designs for precision control systems, ordnance initiation, and dc power control and distribution. His experience with sub-microsecond switching of high power systems has necessarily led to the in-depth study of electromagnetic interference effects and their control through proper circuit and packaging design.

Mike has 34 years experience in research, development, test, and evaluation in aerospace, military, and high-technology commercial electronic systems. He has a BSEE and MSEE from Stanford University, plus 42 post-MS Honors Units from Stanford and the University of Santa Clara.

Slide #1

Printed Circuit Design Techniques for the Control of Electromagnetic Interference



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Slide #2

Presentation Overview

Melding EMC with Signal Integrity

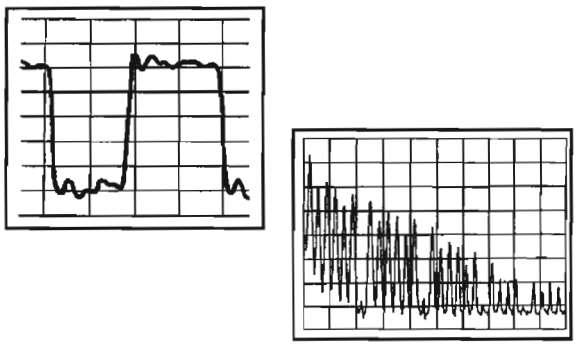
- Inadvertent antenna creation
- Differential- and common-mode radiation
- Printed circuit board characteristics
- Field confinement and interception
- Current limiting and confinement
- PCB design guidelines
- Bench-top evaluation

Allowable time constraints limit the scope of this paper to a focus on differential-mode and common-mode radiation as primary EMI design drivers for printed circuit boards.

Real-world design techniques will be correlated to their theoretical basis for preferred designs.

Slide #3

Time versus Frequency Domain



The commonly observed voltage traces in a digital circuit are related in a complex way with the radiated fields from those traces. The impedance levels, propagation times, trace and structure resonances, and coupled circuits all affect the magnitude and constituent frequencies of the radiated fields.

Time-domain reflectometry evaluation is normally done for signal integrity and noise margin evaluation, but spectral analysis of voltage and current waveforms is required for assessment of electromagnetic compatibility.

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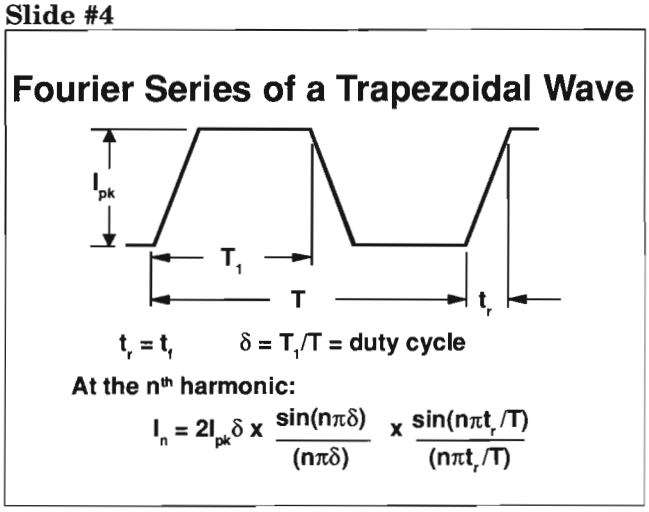
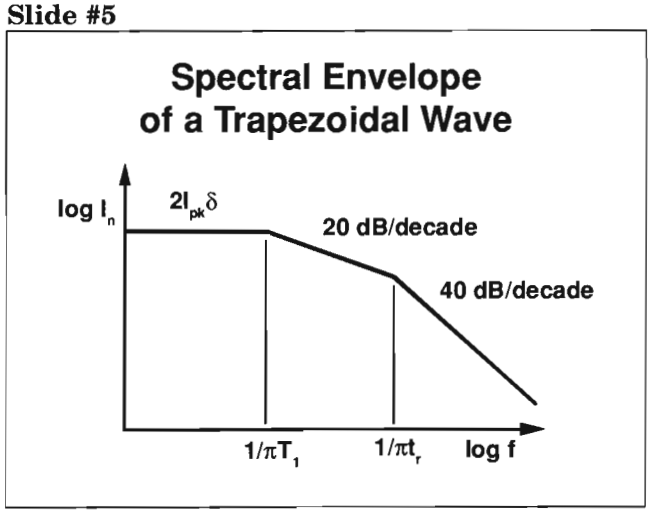


The prediction of radiation from a circuit requires identification of the frequency content and absolute magnitudes of coefficients through a Fourier transform of the time-domain waveform. This sample trapezoidal waveform assumes equal rise and fall times.

Slide #5



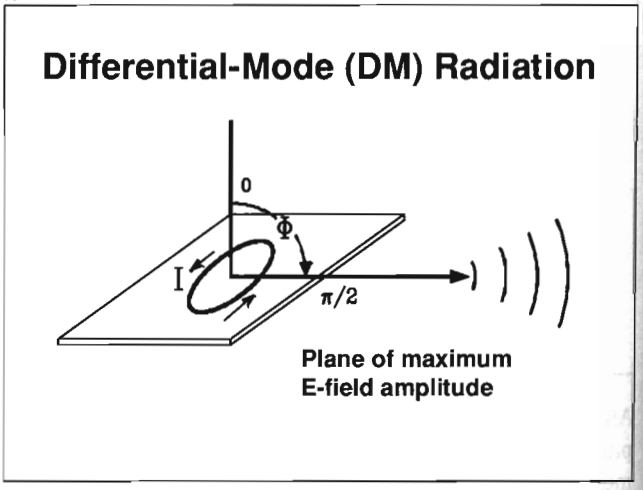
The magnitude of the Fourier coefficients are bounded by the curve shown. The sin X over X terms cause periodic attenuation/ripple in the actual magnitudes that you would measure. No energy is contained at frequencies less than the fundamental, and 99% of the energy is contained below f = $1/\pi t_r$.

The curve rises as frequency decreases until frequency $1/\pi T_1$ (the pulse width) is reached, and the curve plateaus at the value $2I_{pk}\delta$ for all lower frequencies. The details on derivation of this spectral envelope can be found in the Fourth National IRE Symposium on RFI, June 1962.

Note that the edge rate (or rise time, t_r) is a key driver (or limiter) for the frequencies of concern. This fact alerts designers to use the slowest edge rate devices that are suitable for their application in order to minimize their potential EMI problems. As a point of reference, a 1 ns rise time yields a break frequency of 318 MHz.

CAUTION: The rolloff of the spectral content illustrated in the slide can be offset by the efficiency of radiation exhibited by the radiating "antenna"—to be covered in later slides.

Slide #6



Take a simple loop and pass an alternating current though the loop. The current may consist of the harmonic frequency components of a digital signal on a printed circuit board (PCB).

The magnitude of radiation from the loop will vary in proportion to the current. The radiated electric field intensity at a distance d from the loop will be maximum when measured in the plane of the loop.

Slide #7

DM Radiation Prediction

Far-Field Characterization

$E = 1.316 \times 10^{-14} \times (A I_f f^2/d) \sin\Phi$ Volts/Meter

- A = Loop area, square meters
- d = Distance from loop center, meters
- I_f = Current at frequency f, amperes
- f = Frequency (of harmonic), Hertz
- Φ = Angle from loop axis

There are three ill-defined distances referred to when studying EMI. They are near-field, intermediate-field, and far-field. In the near-field, some radiation terms roll off inversely with d cubed; the intermediate terms roll off inversely with d squared; and the far-field terms roll off inversely with d. Most certification tests at frequencies of concern are made in or near the far-field region. The boundary for the far-field region depends on the frequency and commences at $\lambda/2\pi$. At this distance, the radiated field approximates a plane (TEM) wave. For example, at a measuring distance of three meters (standard FCC test distance), the far-field definition applies to all frequencies above 15.92 MHz. At 10 meters, frequencies above 4.775 MHz qualify.

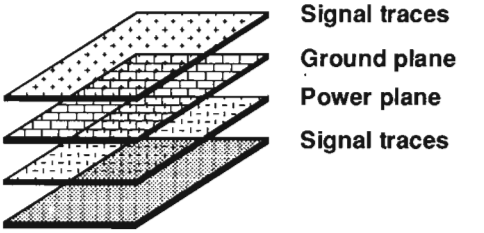
Note that the I_f in the equation is a particular current at a particular frequency (harmonic). Also, the magnetic field magnitude in the far-field region is simply $H = E/120\pi$, (the E-field divided by the radiation resistance of free space).

A sample calculation of the radiated field from the third harmonic (100 MHz) of a 254 mm (10 inches) long by 0.635 mm (0.025 inches) wide loop carrying a 33.3 MHz, 4 V_{p-p} signal into a 50 ohm load yields 41.6 dBμV at the 3 meter test distance used for FCC Class B certification tests. Only 43.5 dBμV is allowed at 100 MHz. The radiation will increase approximately in proportion to the square-root of the number of traces.

The equation given assumes the far-field. Therefore, assuming a worst-case reflection off the ground plane that *doubles* the signal is a recommended, conservative design approach that allows for a contribution of the intermediate ($1/d^2$) radiation terms and reinforcing ground reflections.

Slide #8

Multilayer Printed Circuit Board I



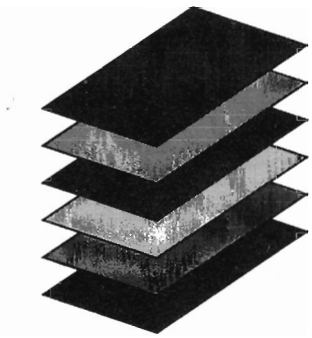
Multilayer circuit boards radically change the character of circuit loops. The ground and power distribution conductors are typically embedded as planes. The return currents for signal traces now flow through a ground plane that is in close proximity to the trace itself. The smaller area of the current loop substantially reduces the magnitude of radiation from the loop. The plane of the current loop is now normal to the PCB; therefore, DM-radiation will be emitted directly off the face of the board instead of being emitted in the plane of the board.

The use of ground and power planes provides the low-impedance power distribution necessary for good power supply decoupling.

The use of outer surface traces is commonly observed; however, placing ground and power planes on the outer surfaces affords superior EMI performance.

Slide #9

Multilayer Printed Circuit Board II



Enclosing signal traces between power and ground planes achieves a locally shielded enclosure that reduces radiation, radiated susceptibility, and ESD susceptibility.

The inverting of surface trace layers with their adjacent ground or power planes converts the traces to stripline configuration. The detailed configurations, attributes, and compromises between these two trace types will be discussed shortly. Note, however, that the signal traces are now *buried under a shield*, relative to the outside world. What better way to achieve 30 to 45 dB of attenuation and susceptibility isolation, and ESD protection?

The artwork for the individual layers of normal multilayer boards does not change if the design uses through-hole components, as opposed to surface-mounted parts. The latter require additional vias to be installed. This may seem an extreme penalty, but the preference for burying traces will become more obvious later.

Slide #10

PCB Trace Configurations

Traces are Transmission Lines ($\lambda/4$ < trace length)

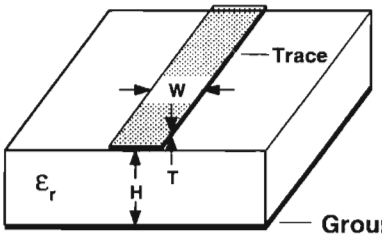
- Transmission Line Configurations
  - Microstrip
  - Stripline
- Trace Characteristics
  - Fields and impedances
  - Signal propagations
- What's Best and Why

When designing high-speed circuits, the signal interconnections must properly be treated as transmission lines.

High-speed interaction effects become a signal integrity concern when the signal rise or fall time become less than about *twice* the propagation time on a given trace. At this point, the trace length approaches 1/4 wavelength for the highest frequencies contained in the signal. For the astute digital design engineer, this fact provides a guideline for partitioning of functional subcircuits to minimize signal integrity concerns.

Slide #11

Microstrip Structure



$Z_0 = 87(\varepsilon_r + 1.41)^{-0.5} \times \text{Ln}[5.98H/(0.8W + T)]\ \Omega$

$T_{PD} = 1.017(0.475\varepsilon_r + 0.67)^{0.5}$ ns/foot

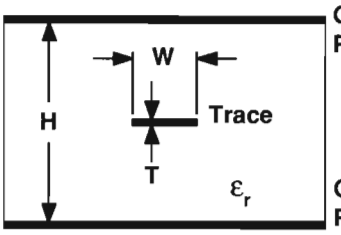
Approximations to the complex microstrip characteristic equations are acceptable for most applications. The relations presented in this slide are accurate within 3% for a W:H ratio of two or less. As an example, the propagation delay for FR-4 material is 1.73 ns/foot (or 144 ps/inch = 56.7 ps/cm) for a propagation velocity of approximately 7 inches/ns (or 18 cm/ns).

CAUTION: The relative dielectric constant of the chosen materials for the PCB should be controlled in critical applications as 5% tolerances are common and 20% tolerances are possible.

Signals with 1 ns rise time should be limited to 9 cm (3.5 inch) traces for microstrip constructed using FR-4 (ε_r = 4.65 nominal) material, unless signal integrity techniques are carefully applied.

Slide #12

Stripline Structure



$Z_0 = 60(\varepsilon_r)^{-0.5} \times \text{Ln}\{4H/[0.67\pi(0.8W + T)]\}\ \Omega$

$T_{PD} = 1.017(\varepsilon_r)^{0.5}$ ns/foot

The added ground plane (or power plane) relative to the microstrip construction naturally adds capacitance between the signal trace and ground, resulting in a lower characteristic impedance. This same capacitive loading also slows the propagation down the trace (about 27% longer for FR-4).

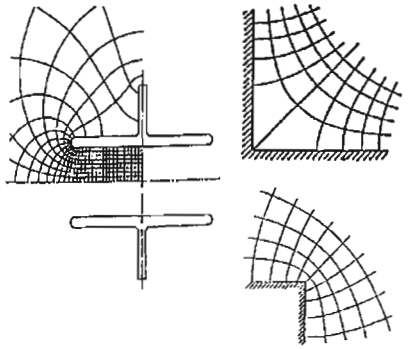
The velocity is about 183 ps/inch for FR-4 material with ε_r = 4.65.

Be aware that multiple (gate) loads on a given trace effectively add a distributed capacitance load along the trace that will further increase the propagation delay by the factor $(1 + C_D/C_O)^{0.5}$, where C_D is the distributed capacitance loading per unit length and C_O is the normal distributed capacitance per unit length of the trace. This same distributed load capacitance slightly lowers the line characteristic impedance.

Signals with 1 ns rise time should be limited to 7 cm (2.75 inch) traces for stripline constructed using FR-4 material, unless signal integrity techniques are carefully applied.

Slide #13

Visualizing Field Shapes



Orthogonal plotting of the EM field patterns around geometric shapes will give you insight into potential coupling problems before they arise. The symmetrical nature of the patterns simplifies the learning process.

Sketching of field patterns can lead you to solutions for difficult shielding, isolation, and impedance matching problems. Consider the differences in performance characteristics between multiple microstrips and multiple striplines as a practical example.

As a practical matter, the use of field solver software in the prediction of transmission line characteristic impedances, propagation velocities, and cross-coupling effects is desirable (and perhaps mandatory) in finalizing a sophisticated design. However, the creative design work that *leads* to the construction of probable design layouts will be accomplished faster with an understanding of field patterns.

Slide #14

Microstrip versus Stripline

Signal Integrity and EMI Considerations

Microstrip exhibits...

- Faster normal-mode propagation
  - Longer traces for an allowable delay
- Higher Z_o...and wider range

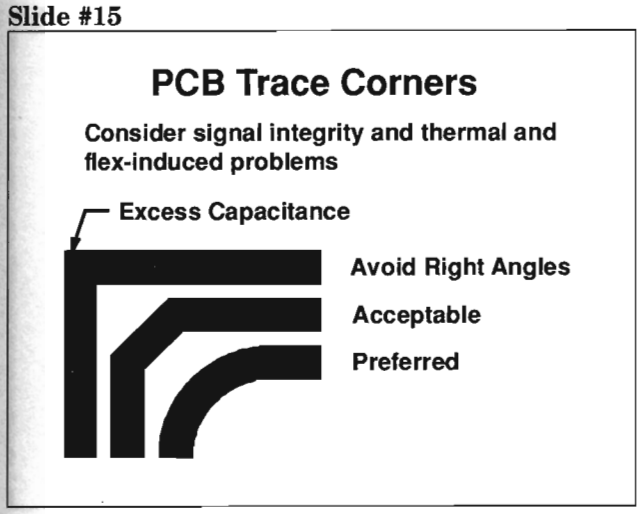
BUT...

- More transition edge degradation
  - Faster odd-mode propagation
- More crosstalk
- More radiation
- Lower trace density

Visualization of the fields generated by the microstrip and stripline configurations makes these comparisons seem relatively intuitive. For example, the fields emanating from the microstrip surface are not guided to a controlled return conductor, but rather tend to terminate on adjacent traces (more crosstalk). Some of these fields escape the surface of the PCB totally and propagate or radiate outward.

To reduce the crosstalk associated with microstrip, the spacing between adjacent traces is necessarily widened, resulting in lowered interconnection density.

Slide #15

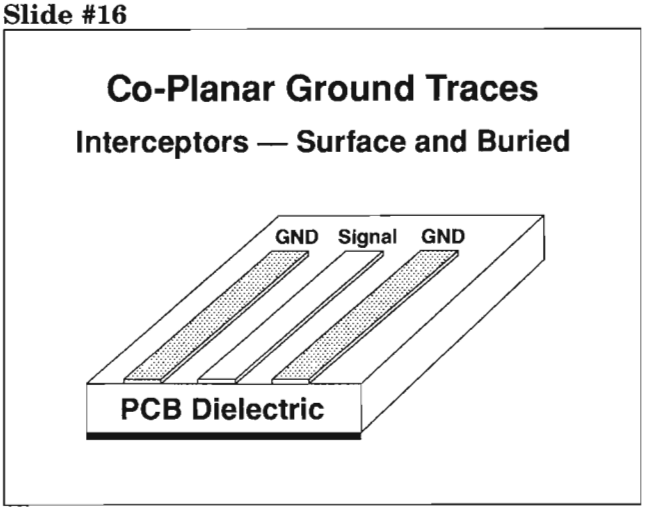


The use of 90-degree corners causes excess capacitance to be introduced to the trace and represents a small, but unnecessary, impedance change in the characteristic impedance of the transmission line. The use of 45-degree turns with a minimum segment length of twice the trace width is better (and is offered by most auto-routing CAD programs). Continuously curved traces with an inside radius of at least the trace width is the best approach.

Spacing between adjacent active traces should not be less than the trace width to minimize crosstalk, but little additional benefit is gained for spacing of more than three times the trace width.

Although the electromagnetic effects of the 90-degree corners are secondary to most signal integrity effects, the use of such corners in high temperature or flex-circuit applications lead to degradation and reliability problems with cracks caused by stresses.

Slide #16

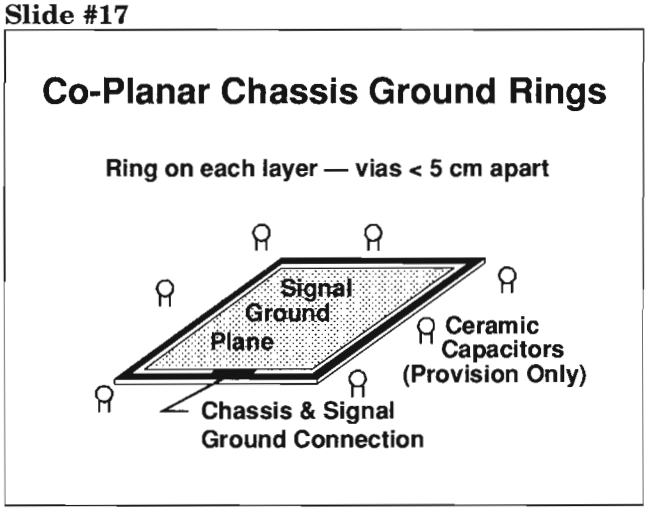


If a trace conducting high frequency currents is to be routed on the surface of a printed circuit board (PCB), Mikon recommends grounded traces be routed parallel to it to reduce both radiation and crosstalk. The ground traces should be connected to ground fill areas or ground planes at *varied* intervals not to exceed $\lambda/4$ at the highest frequency or harmonic expected. This recommendation applies to single- and double-sided PCBs, as well as microstrip lines. For example, use of vias-to-ground at spacings of five centimeters (two inches) or less with FR-4 ($\varepsilon_r = 4.65$) would be satisfactory for harmonic frequencies approaching 685 MHz. However, waveform rise times should be greater than 1.5 ns to limit the magnitudes of such harmonics.

The adjacent grounded traces can be placed closer to the signal trace than other signal traces for more effective interception of emerging fields. The slight lowering of the line characteristic impedance can be compensated by thinning down the signal trace. The thinner, closer-spaced traces minimize the surface area required for this configuration while simultaneously adding more loss or damping to the signal line.

Asymmetrical striplines (buried microstrip) will also benefit from reduced crosstalk using this technique.

Slide #17

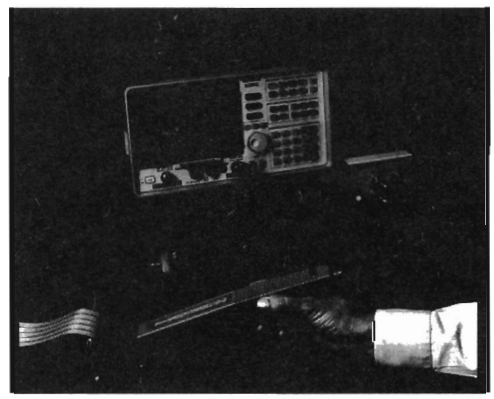


For field interception, Mikon recommends chassis ground rings, preferably wider than 2.54 mm (0.1 inch), be placed on the periphery of *each layer* of the circuit board and interconnected with vias at *varied* spacings up to 5 cm (2 inches) maximum.

This construction presents a formidable shield (or field interceptor) to prevent radiation (or susceptability) at the circuit boundaries. Experience (and recent publications of studies) has demonstrated up to 20 dB greater emissions from edge-located traces relative to traces well within the PCB borders. The chassis ground rings also act as a preferred path (interceptor) for electrostatic discharge, yielding a more robust design.

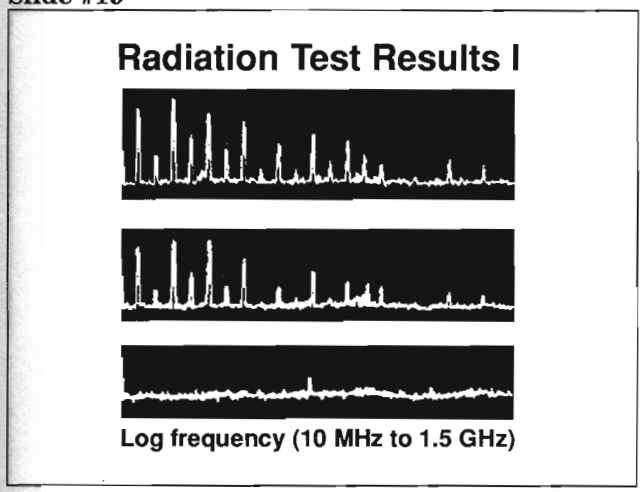
Since unwanted resonances may be created with this construction, *provisions* for "detuning" with ceramic rf capacitors or damping with low-value resistors should be made between this shield ring and the normal circuit signal ground plane. Capacitor values could range from 50 pF to 1000 pF depending on the frequencies of concern. Suitable damping resistor values range from 10 to 50 ohms, depending on the apparent RF impedance of the transmission line formed by the chassis ground rings and the signal ground plane.

Slide #18



Here is a typical test setup of a spectrum analyzer system. The HP 84100B system illustrated includes two close-field magnetic probes, a pre-amplifier, a spectrum analyzer, and an EMC "personality" card. The card customizes the general purpose spectrum analyzer to EMC measurements by including FCC, VDE, and CISPR test limits, and calibration compensation data for various antennas and probes. The appropriate test distances and receiver bandwidths required by the applicable test are also preprogrammed.

Slide #19

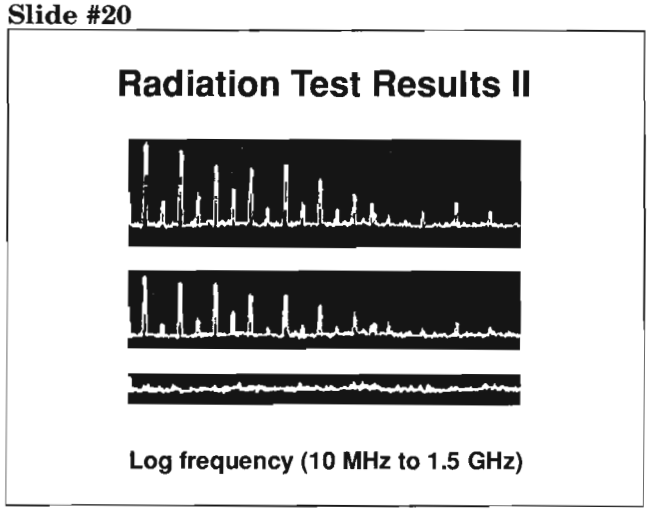


A PCB was designed with FR-4 materials to compare crosstalk, radiation, relative trace densities, and overall signal integrity of microstrip, guarded (coplanar ground traces) microstrip, stripline, and guarded stripline. After a successful verification of trace impedances by TDR evaluation, the respective radiation characteristics of the four transmission line implementations were tested with a benchtop spectrum analyzer system with the lines unterminated, except for surface pads with approximately 3 pF of capacitance.

The graphic above shows typical near-field test results for the standard microstrip, the guarded microstrip, and the standard stripline, all implemented with a duplicate, parallel trace to assess the effects of inter-trace coupling on 50 mil centers. A controlled rise and fall time generator was used to produce 1 ns rise and fall times with a 50% duty cycle operating at 66 MHz. The guarded stripline case is not shown as the performance, as determined separately by detailed TDR tests, was substantially better than the basic stripline configuration.

With minor deviations, the guarded microstrip improved (lowered) the radiation level relative to the standard microstrip by 6 to 8 dB to frequencies beyond 1 GHz. The stripline, as anticipated, made the radiation virtually undetectable. The noise floor was approximately 14 dBμA/meter, and the measuring height was fixed (by a writing tablet) at 0.25 inch for all tests.

Slide #20



This second graphic compares the same transmission lines as in the previous slide, but with terminations added (47 ohm surface mount resistors). There are some minor differences in the amplitude distribution versus frequency, but the overall energy in the radiation fields detected were basically unchanged.

Note that a local ambient broadcast signal (near the center of the bottom trace in the prevous slide) was not present. They had apparently reduced their signal strength for broadcast during the evening hours.

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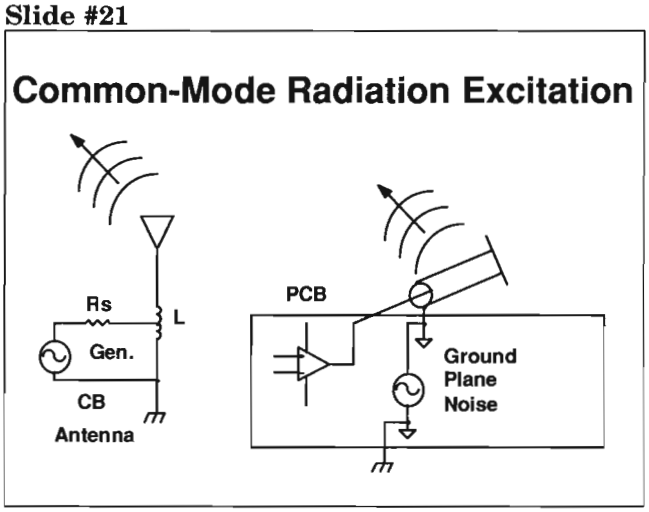
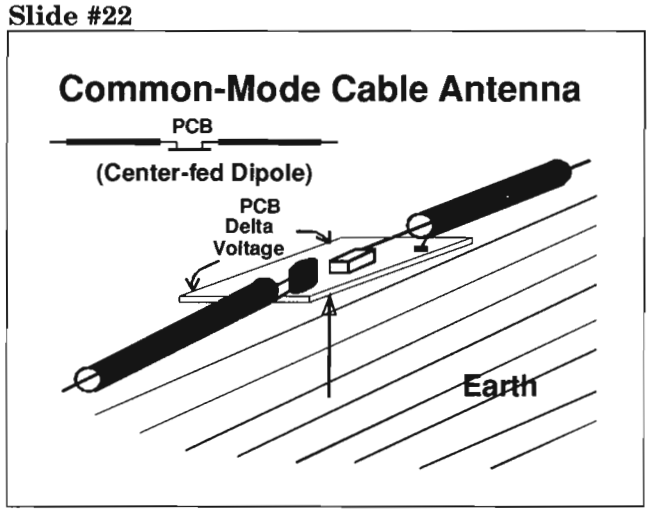
Slide #21



A portable citizen's-band (CB) transmitter typically uses an inductively loaded whip (or monopole) antenna that is considerably shorter than one-quarter wavelength. The inductor is tapped near the grounded, low-impedance end of the inductor for proper impedance matching to the generator source impedance.

Excitation of the ground plane on a circuit board can excite rf energy on cable leads and shields that then behave as monopole or dipole antennas.

Slide #22



This slide illustrates how ground plane noise can excite a pseudo-dipole antenna configuration. The magnitude of this phenomenon will depend on the containment and suppression techniques (if any) employed in the final design.

Note that the magnitude of the noise generated is limited to allowable design noise margins for proper logic functionality, but the ultimate success or failure in the radiated EMI tests is *not* directly correlateable to the noise margins.

Slide #23

Common-Mode (CM) Radiation

Monopole Antenna Radiation

$E = 4\pi \times 10^{-7}(fLI_f/d)\cos\Phi$ volts/meter

- f = Frequency, Hertz
- L = Cable length, meters
- d = Distance from cable, meters
- I_f = CM current in cable at frequency f, amperes
- Φ = Angle from normal to cable

Note the proportionality to frequency and the larger coeficient (by 100 million to one!) relative to the equation for DM radiation, which is repeated below for convenience.

$E = 1.316 \times 10^{-14} \times (AI_f f^2/d)\sin\Phi$ volts/meter for DM radiation

As an illustration, assuming the angle for maximum field strength (zero degrees), a 1 meter cable carrying only 10 μA of common-mode current at 100 MHz will yield a field strength of 52.44 dBμV/meter at the three-meter distance required for FCC testing. The FCC Class B limit at 100 MHz is 43.5 dBμV/meter. For comparison, recall that a 33.3 MHz clock signal on a 50 ohm line that formed a 10-inch-by-0.025-inch loop would yield a DM signal of 41.6 dBμV/meter at 100 MHz at 3 meters. The 100 MHz (third harmonic) DM current is calculated to be 16.98 mA, or approximately 1700 times higher than the 10 μA CM current assumed.

Slide #24

Impulse Excitation of CM Radiation

- Displacement currents, power
  - Switching regulator/power supply
  - Non-synchronous, full-bridge motor driver
- Shoot-through current, power
  - Power MOSFET half-bridge switching
- Shoot-through current, medium power
  - Totem-pole MOSFET gate driver
- Synchronized gate transitions

Transient currents from any source that generates high di/dt conditions will generate ground and trace "bounce" voltages. The high di/dt generates a broad range of high-frequency currents that excite structures and cables to radiate in the common-mode manner.

For example, an on-board switching regulator producing a 500 mA dc output current at 5 Vdc can (depending on its mode of regulation) have a peak current when switching of 2 A or more. Switching the 2 A from one device into another (for example, a flywheeling diode) in 10 ns represents 4 A in 10 ns. The switching frequency may be anywhere from 20 kHz to 1 MHz. The obvious ground disturbance caused by this current redirection is further aggravated by the displacement current generated by the dV/dt of the switching device used to switch the primary inductance. The displacement current can create common-mode currents through a multitude of paths, depending on the insulators and shields used in the packaging of the devices. The design and termination of transformer shields, and the heatsinking of power transistors, have become specialty tasks with the proliferation of switching supplies and regulators.

Slide #25

Methods to Control CM Radiation

Control Accomplished via Tradeoffs

- Cable regulations/specifications
- Low-Z ground and power planes
- Use of differential/balanced circuits
- Physical circuit current confinement
- Use of ferrites

If possible, control or specify the lengths, construction, and impedances of cables.

Use at least three skin-depths of copper at the frequencies of concern on the outer ground/power layers for maximum shielding and minimum CM impedance. Mikon recommends two-ounce copper (0.0726 mm or 2.86 mils thick) for most applications. Two-ounce copper provides three skin-depths down to 7.5 MHz, one-ounce copper down to 29.75 MHz, and half-ounce copper only down to 119 MHz.

Differential circuits are *not* always easily achieved, but they are designed to balance the flow of ground currents so as to cancel out, resulting in low CM voltage excitation.

Confinement of high-frequency currents to a local area of the PCB by moating limits the capability of those currents to excite an efficient radiator.

Ferrites are used to directly suppress CM energy by both reactive impedance and absorptive losses.

Slide #26

Moating — Current Confinement

Interface Moats & Internal Moats

- Confine/corral current dispersion
- Guide I/O currents to a local area
- Bypass heavily for a "quiet" ground

The term "moat" as used here is the *removal* of a strip of copper on the power or ground planes that surround a particular circuit; for example, a switching regulator. The intent is to force the normal ground and power currents associated with the operation of the circuit into a specific area that can then be either heavily decoupled or chassis-grounded. The moat confines the high-frequency currents produced by the circuit so they cannot flow through adjacent circuits, potentially causing interference and radiation.

The moating technique is particularly effective at I/O connectors. The interface cable shield and the connector shell can be tied to the chassis ground directly, and the signal return/ground wires can be terminated at a focused "quiet" ground point that is heavily bypassed. The net result is a very low noise level at the cable interface, which minimizes the potential for radiation from the cable.

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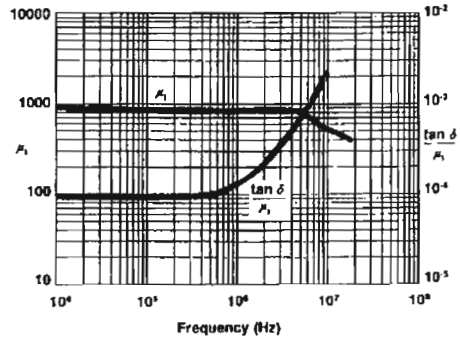
Slide #27

Fair-Rite Products Material 43



Most ferrite compositions are categorized as "soft" magnetic materials as opposed to "hard," or permanent magnet, materials. As such, they require very little energy to alter their magnetic flux density (B). The narrowness of the familiar magnetic hysteresis curve is an indicator of the amount of energy required to alter the flux. So, the smaller the area within the hysteresis loop, the lower the energy required to traverse the loop. This "soft" nature allows efficient use of ferrites as transformers and inductors at medium to high frequencies. However, as the frequency continues to increase, losses in the ferrite start to dominate its impedance and the inductor looks more like a resistor. This range of characteristics allows ferrites to fill a variety of roles in high frequency circuits.

Both the reactive and resistive (absorptive) characteristics of the ferrite serve to suppress the higher frequencies. These features can be used to effectively reduce the bandwidth and higher frequency energy content of digital signals, thereby suppressing unwanted radiation at high frequency.

The plots above illustrate the initial permeability (always measured at low flux density) and loss factor versus frequency for a popular nickel-zinc ferrite mix recommended for suppression over the 30 MHz to 200 MHz range.

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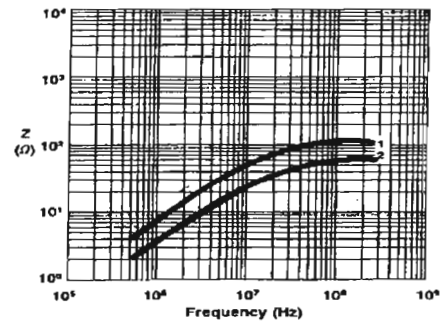
Typical Fair-Rite SM Beads™ Z(f)



The two curves are representative of two material 43 beads and illustrate the effect of an increasing inductive reactance at the lower frequencies transitioning to a resistive absorption effect at the higher frequencies.

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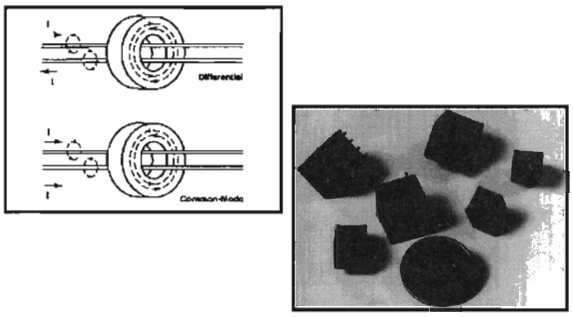
Ferrite Chokes for CM Current



Ferrites are very effective when used to reduce CM currents. By placing the ferrite around a signal *and* the return conductor carrying a differential signal, the fields developed in the ferrite core by the opposing currents cancel; hence, no affect is observed. However, the CM currents on the leads are in phase and their fields add. Therefore, any CM currents on the lines will experience an inductive reaction at low frequencies and a resistive loss at higher frequencies. The resistive (absorptive) transition occurs at frequencies above those where the selected ferrite material would be suitable for normal inductors or transformers.

The relatively low magnitudes of typical CM currents allow multiple turns through (or around) a ferrite core to be used before any threat of core saturation arises. The realized inductance increases as the square of the number of turns until self-resonance is reached and can achieve substantial impedance to the flow of CM current. The absorptive losses lower the Q of the resonance and extends the blocking impedance into higher frequencies, commonly achieving suppression over bandwidths exceeding a decade.

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Ferrite Common-Mode Chokes

Ferrite absorbers come in all shapes, sizes, and material mixes. Solid (unbroken), split, hinged, and gapped versions are available for surface and through-hole PCB mounting. They are commonly used in cable clamp-on applications.

Multiple vendors supply ferrites especially designed for suppression at the interface connector pins. Both commercial and military-class connector add-ons are available.

Ferrite cores can also be effectively used in differential circuits for bandwidth limiting and high-frequency damping/absorption. Multiple-lead and multiple-turn ferrite cores are commonly used at digital data line interfaces for both transmit and receive lines. Use of these ferrites suppresses propagation from the transmitters, and incoming transients and CM noise is countered before penetrating the PCB circuits.

For higher current (power) circuits, gapping of the magnetic path through the ferrite is used to substantially extend the allowable dc current through the conductors before saturation reduces the suppression efficiency.

Slide #31

PCB Fab/Layout Techniques I

Recommended Techniques

- Maximize use of stripline construction
  - Minimize surface conductors
- Border PCB with chassis ground strips
- Centrally locate clock circuits
  - Use remote distribution centers
  - Distribute symmetrically
    - Cancels fields
    - Shortens loops
    - Preserves signal integrity

Buried traces (stripline) confines fields and substantially reduces radiation from interconnections on the circuit board.

Chassis ground rings play a terminator/interceptor role to fields trying to leave the PCB. They also offer a protective intercept to ESD intrusion.

Clock circuits generate the highest toggle rates of all circuits and are the primary source of noise generation in most digital circuits. Clock timing and skew are critical factors affecting digital circuit performance and must be carefully controlled to achieve maximum design margins and robustness. These factors are best controlled by centrally locating the clock oscillator and distributing radially. Radiated fields from the outwardly flowing currents tend to cancel. Propagation delays are minimized and forced to be more synchronous throughout the board. Use of remote drivers for distribution minimizes the trace currents that are forced to travel long runs on large boards; therefore, their respective interference potential is reduced.

Slide #32

PCB Fab/Layout Techniques II

Recommended Techniques Cont'd

- Keep high toggle-rate traces in-board
  - up to 20 dB reductions
- Locate line drivers/receivers at ports
  - Reduces CM noise
- Localize high frequency currents
  - Decouple locally
  - Use moating where practical
- Use shielded components
- Use bulk capacitors at/near ports
- Use ferrites on input/output lines

Recent studies by IBM have documented a logarithmic dependence of the radiation from a microstrip (6 mils wide) as it was moved from the center of the board towards the edge. An increase of up to 20 dB in radiation was reported. The same test series performed on stripline indicated no change in the far-field radiation as the traces were placed nearer the PCB edges. Therefore, stripine (versus microstrip) construction offers more flexibility in placement of functional circuits on the PCB.

Locating properly decoupled line drivers and receivers as close as is practical to their physical I/O interface reduces the coupling to other circuits on the board. This placement simultaneously reduces radiation from *and* susceptibility to the circuit board.

Localized decoupling with high self-resonance-frequency capacitors (for example, leadless ceramics) at individual integrated circuit packages confines that device's noise and maximizes noise margins. Where moating of a complete subcircuit is employed, sometimes filtering the subcircuit power via an inductor followed by a large (4.7 μF to 8.2 μF) tantalum capacitor can achieve additional decoupling. Of course the bulk capacitor must be accompanied by suitable RF bypass capacitors within the same circuit.

Where possible in high frequency circuits, use grounded, shielded component housings. The housing intercepts errant fields, shunting them to ground. Large plastic quad flat-packs (PQFP) are devices that typically will require installation in a shielded equipment enclosure for compliance, whereas the same devices in a grounded pin grid array (PGA) package may achieve compliance.

Bulk capacitors reduce system power fluctuation effects (typically <10 MHz).

Slide #33

PCB Fab/Layout Techniques III

Recommended Techniques Cont'd

- **Use narrow traces (4 to 8 mils)**
  - **Increases high frequency damping**
  - **Reduces capacitive coupling**
- **Minimize crosstalk**
  - **Use orthogonal crossovers for traces**
  - **Trace spacing-to-height ratio > 2**
    - **> 3 adds little additional benefit**
  - **Intersperse ground traces**

Narrow traces offer many advantages. For example, these advantages can include higher density interconnections (and more dense packaging), higher Z_0 for lower currents/source loading, increased losses/damping at the higher frequency harmonics, and less coupling to other lines that pass at right angles (crossovers).

Caution: Be aware that for surface traces (micro-strip), the magnitude of radiation increases with Z_0.

Visualizing the field patterns associated with traces at a height H over a ground plane helps illustrate the recommended spacing-to-height ratio of 2 to 3. Closer than 2:1 will substantially increase crosstalk, and larger than 3:1 will impact the allowed density of interconnections.

Adding parallel ground traces better isolates critical signal traces for superior crosstalk and susceptibility performance.

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PCB Fab/Layout Techniques IV

Advanced Techniques

- **Use of low-dielectric materials**
  - **Faster propagation**
  - **Higher Z_0 values**
- **Multi-Wire™ techniques**
  - **Kollmorgen, Hitachi**
  - **High density, controlled Z_0**
- **Low impedance, Buried Capacitance™ ground/power plane sandwiches**
  - **Reduction in bypass capacitor count**
  - **Patented processing technology**

Short propagation delays are synonymous with proper packaging for high-speed designs. Signal integrity concerns are minimized and radiation efficiencies are reduced allowing use of thinner traces of higher Z_0 value (lower source loading) with obviously higher trace densities. These desirable features require careful attention to component grouping/placing and must still address the mounting problem of crosstalk as traces are brought ever closer together. Stripline offers a substantial advantage over microstrip for narrow trace-to-trace spacings, especially for separations less than or equal to the dielectric thickness.

The use of lower dielectric materials, such as teflon and Duroid (2.2 - 2.5), Kapton (3.1 - 3.4), and other polyimide (3.8 typical) materials, offer distinct advantages over epoxy-fiberglass materials (4 - 6). These materials yield lower propagation delays, superior (lower) coefficients of thermal expansion, and higher operating temperature capability (>120°C). FR-4 (4.4 - 4.7 typical) requires strain-relieving leads on larger components to prevent long-term solder joint cracking problems caused by thermal cycling. These leads present inductance that compromises high-speed performance.

PCBs constructed with Multi-Wire™ techniques (Kollmorgen and Hitachi) typically combine epoxy-fiberglass layers with traces *and* polyimide-insulated wires (and sometimes coax) fused into the layered PCB construction. Low- and high-density interconnects and fast, controlled-impedance lines can be melded into the same PCB.

A recently patented innovation (Buried Capacitance™) that allows higher active component densities simultaneously with lowered production costs has been developed by Zycon Corp.

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PCB Fab/Layout Techniques V

Advanced Techniques Cont'd

- Buried Capacitance™ features
  - Eliminates 90 - 100% of bypass capacitors (lower parts cost)
  - Higher active device density
  - Single-side SMT assemblies
    - One thermal/solder pass
  - Lower fab. time/cost
  - Increased reliability and MTBF
  - Most effective at 40 MHz and up

The use of localized, distributed capacitance in plate-form has been seen for years in "under-the-chip" parts from Rogers and other companies, but the extension of this concept to entire planes of circuit boards has been difficult because of quality control problems. The Zycon Corporation (See "Recommended Resources" at the end of this paper.) has refined and copatented a repeatable foil-dielectric-foil process that is now being liscensed world-wide to implement built-in decoupling in PCBs.

The low-inductance, distributed capacitance nature of the product achieves superior radio frequency decoupling, allowing deletion of discrete decoupling capacitors that exhibit self-resonance, typically between 10 MHz and 30 MHz. By integrating the decoupling capability into the structure of the PCB itself, the majority of the capacitors can be eliminated from the assembly.

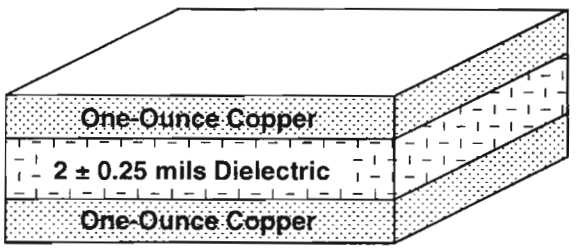
Because active parts can now occupy the space freed up by the capacitor deletions, the effective packaging density takes a quantum step upward. In many cases, assemblies with surface-mounted parts on both sides of a PCB can be transferred to a single side, requiring only one thermal/solder pass during manufacturing. This situation alone can nearly double the production rate of some manufacturing lines.

The parts count reduction can directly save costs, but the greatest gain may be in the improved reliability of the assembly achieved by the use of fewer parts. Further, the technical performance quality and repeatability of the decoupling function is improved by the lack of variations in discrete component self-resonances (and their interactions), and by the superior low impedance presented from a few tens of megahertz on up.

Slide #36

Buried Capacitance Construction

$C = A\varepsilon/d$ and is approximately 0.5 nF/in²



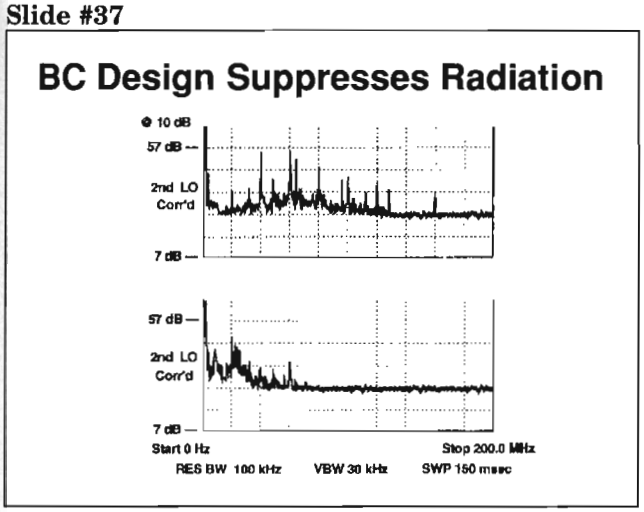
On a typical PCB, the V_{CC} and ground planes are each replaced by a "sandwich" containing a V_{CC} plane and a ground plane. The sandwiches are comprised of 1-ounce, premium-grade copper foils separated by a 2-mil dielectric. The premium foil is used for quality control of surface irregularities. Each sandwich yields in excess of 0.5 nF per square inch, and the respective planes (V_{CC} and ground) are connected in parallel. Allowing for via and through-hole clearances, a typical net of 0.9 to 1.0 nF is realized for 2 sandwiches connected in parallel.

As noted earlier, the use of ground planes to reduce circuit loop sizes, provide predictable impedances for the control of signal integrity, and (for the proper construction) provide a shield or enclosure for

superior EMI performance is critical to the high-speed digital designer. The particular multi-layer PCB configuration shown above carries out those recommendations while adding 2 foil layers (assuming 2 sandwiches for the construction) whose cost is at least partially offset by the reduction in decoupling capacitors required in the final assembly.

For the Mikon-recommended construction, the sandwiches are located on the outside layers of the PCB and offer a *double shield* that should prove superior to a single layer shield of 2-ounce copper.

Slide #37



This "Before and After" example of a digital PCB design used in a line of computers is excerpted from the July 1991 issue of *Printed Circuit Design*. The boards used in the test were fabricated with dielectric and copper foils from the same lots, and tested in the same test setup. The standard 11-inch-by-14-inch PCB had 6 layers and the artwork for both boards was identical.

The board circuit contained multiple oscillators ranging from 14.745 MHz to 40 MHz, with the processor clocked at 20 MHz. The standard board was completely loaded and included 141 bypass capacitors. The BC board used only 4 capacitors; namely, two 0.1 μF and two 0.01 μF. Even though low inductance connections were used for the 4 capacitors, their effect was minimal above 30 MHz. The response recorded was located approximately 4 inches from the capacitors; however, the results indicated were reported to be virtually identical to that found at all points on the PCB. Additional capacitors were reported to further reduce the emissions in the 10 MHz to 20 MHz range.

The BC manufacturing process used in the PCB of this example used a dielectric thickness of 2 ± 0.5 mils. Today the process is achieving thicknesses of 2.0 ± 0.25 mils.

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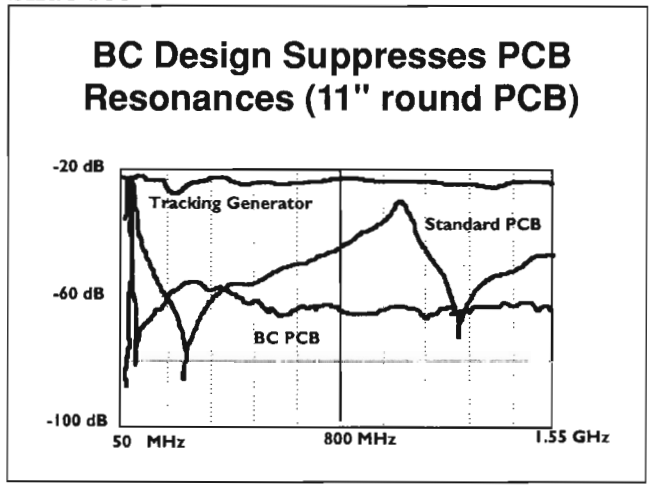
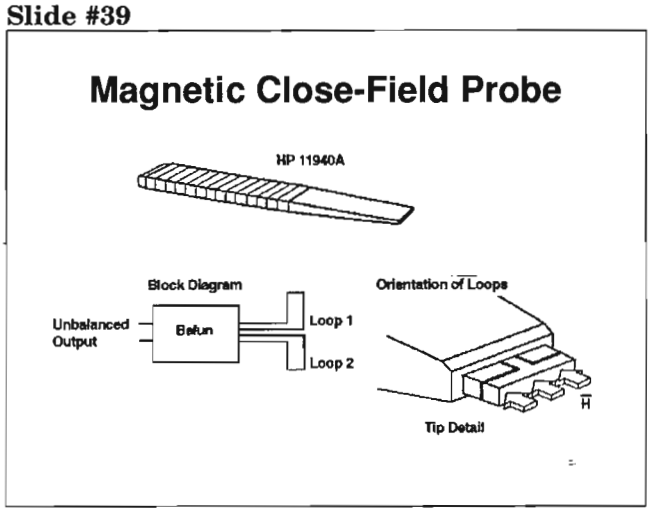


This slide provides a good example of resonance effects that occur on standard PCBs versus the same configuration of PCB using buried capacitance.

Slide #39

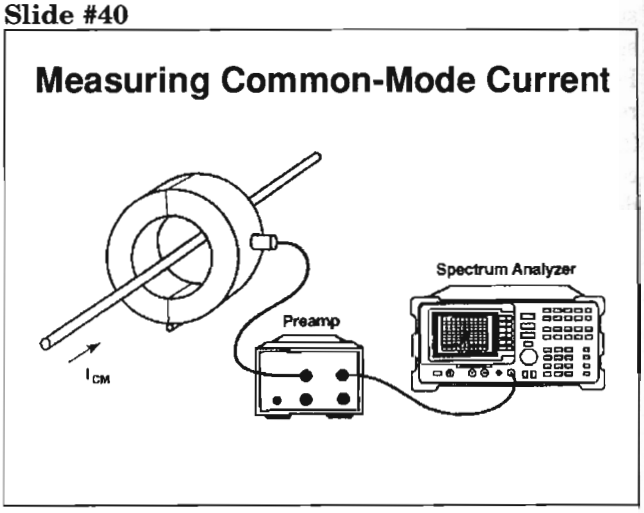


Close-field probes are valuable "sniffers" that allow detection of trouble spots in your circuit. Most probes are comprised of one or more magnetic loop antennas. The better probes use two loop antennas driving a balun (balanced to unbalanced) transformer to reject any coupling of common mode voltage that may interfere with the accuracy of the measuring instrument. The HP 11940A and 11941A probes are good examples of this type of close-field probe.

The sensitivity of some probes can vary widely with frequency; therefore, a knowledge of this variation and a means to compensate for it are required for convenient and repeatable measurements. Programmable compensation and memory retention of the compensation values are desireable features of the spectrum analyzer used with such probes. Some test systems allow the controlling software to compensate for these responses. The HP 859X series of spectrum analyzers, coupled with an EMC "personality" plug-in card, have this capability built in.

Other special probes for measuring surface currents are available. These probes also use balun techniques with magnetic loop antennas. They allow detailed maps of current flow in ground planes, conductive cases, and connector shells to be determined.

Slide #40



Clamp-on probes are commonly used in military EMI certification tests. These same probes can now conveniently be used to directly measure the presence and characteristics of CM current on equipment interface cables. Calculations of the expected radiation levels can then be made and compared to the applicable EMC requirements.

To minimize loading, the probes are generally constructed as a transformer with a large turns ratio. Therefore, a probe with a typical output impedance of 50 ohms only imposes a small fraction of an ohm in the cable/wire under test. The probe sensitivity is characterized by a "transfer impedance." The probe output voltage is the product of the transfer impedance and the common-mode current flowing through the cable/wire.

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Conclusion & Summary

Electromagnetic Compatibility Requires Knowledgeable Tradeoffs

- Any surface conductor will radiate
- Must meld signal integrity and EMC
  - Z_O and T_{PD} considerations
- Identify potential antennas/radiators
- Visualize, confine, and intercept fields
  - Think "ESD, shields, & skin depth"
- Model & analyze critical areas
- Evaluate with available tools early

The successful generation of an electromagnetically compatible design requires the integration of a multitude of technical disciplines in a balanced manner. Some technical goals *cannot* be met if manufacturing techniques are dictated at the outset of a design. Therefore, the design engineer must be able to identify, trade off, and integrate viable approaches to the ultimate, manufacturable solution. The use of a few hours of EMI consulting at the first design review often prevents major cost and schedule impacts later in a program.

The use of modeling and analysis tools and bench-top test equipment can speed and simplify the engineering task, provided adequate competence and confidence is developed along with the models. "Sanity checks" on the predictions of analytical tools are a must—do not become only "terminal-literate."

A conscious effort should be made to predict the potential problem areas where EMC difficulties may arise. These areas should then be evaluated to a depth commensurate with their potential for disruption of the project. Always remember, "One person's signal is another person's interference!"

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Recommended Resources

Software Analysis Tools:

Field-solver for matrix parameters
Circuit simulators for analysis

Test Equipment & Assessories:

TDR system (HP 54120)
Spectrum analyzer system (HP 84100B)
Miscellaneous field probes

Multiple software packages ranging from a few hundred (US) dollars to tens of thousands of dollars are available. Many of the more sophisticated programs require reasonably constant use to achieve operator efficiency, but the less powerful ones are still useful and are more easily mastered. Some offer a separate program for determining matrix parameters and another program for evaluating crosstalk, but most integrate these capabilities. The availability of separate matrix parameter data allows you to build a model for insertion into a more sophisticated circuit simulation program. Circuit simulators again cover a wide range of capabilities at comensurate prices. Proper use of circuit simulators relies heavily on the modeling ability of the user. You should constantly make "sanity" checks on the predicted results of simulators. In particular, be aware of the prepackaged models for semiconductors included with the programs. Also, some of the better programs are *not* SPICE-based, but will import, run, and export SPICE models (like, Micro-Cap IV).

Time-domain reflectometry systems are "designers choice" as the speed, resolution, criticality, and cost factors needed for a given design are subjective. The more sophisticated (and more expensive) systems can sometimes pay for themselves by quickly yielding data difficult to obtain with alternate techniques. As an example, the HP 5412X series offers a range of options.

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For proper bench-top evaluation of most potential EMI problems, a spectrum analyzer system is highly recommended. A test range in excess of 1 GHz is normally required. Various sizes (and frequency ranges) of probes are available from multiple suppliers; for example, Hewlett-Packard, Electro-Mechanics Company, and Fischer Communications Company.

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Recommended Resources Cont'd

Buried Capacitance™ PCBs:

Zycon Corporation (USA 408/241-9900)
ISOLA WERKE AG (Germany (0 24 21) 808-0)

Ferrite Components:

Fair-Rite Products (USA 914/895-2055)
European Contact (USA 914/895-1974)

Consulting, Tutorials, Design:

Mikon Consulting (USA 408/727-5697)

Zycon Corporation, located in Santa Clara, California, USA, fabricates printed circuit boards using their patented buried capacitance techniques to achieve higher component densities simultaneously with superior EMI suppression relative to standard manufacturing techniques. Their processes are licensed worldwide—call for the latest list of European suppliers.

Fair-Rite Products Corporation, located in Wallkill, New York, USA, produces a wide variety of ferrite products in several different formulations to cover all practical frequencies. Their products are marketed worldwide — FAX for identification of multiple European distributors.

Mikon Consulting offers original design and troubleshooting services, as well as tutorials in electronic design techniques. Packaging for rugged environments, signal integrity and EMC engineering, mechanical and electrical/electronic system modeling, transient thermal modeling, and proprietary R&D for new electronic products are routine tasks. Complex design problems requiring the integration of multiple engineering disciplines are a specialty. Over 90% of Mikon's clients are repeat customers, testifying to the viability and cost-effectiveness of Mikon's services.

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