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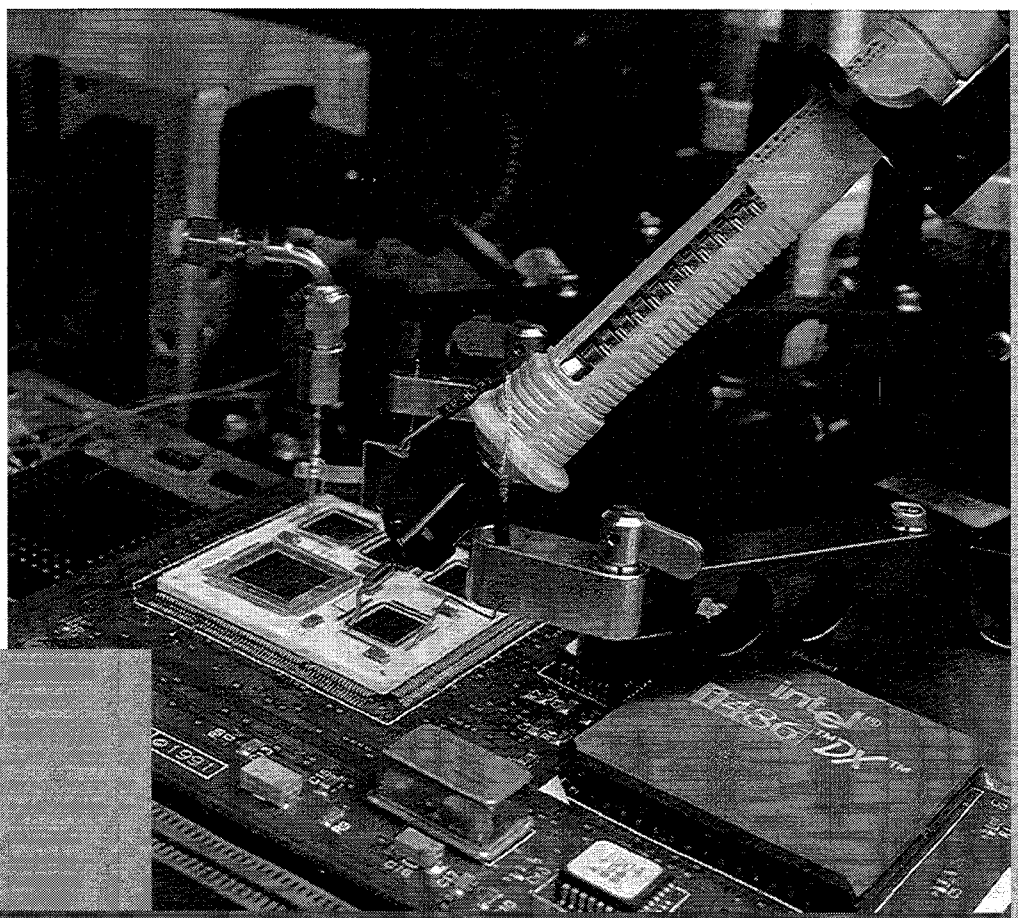
# 1993 High Speed Digital Design Symposium



**Technical Papers**

**High Speed System Design Track**

**Digital Communications Design Track**


# Physical Layer Design Issues for Serial Communications: A SONET Case Study

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## Abstract

Today's evolving communication networks require highly reliable physical layer transmission of digital bits. With speeds increasing to phenomenal rates, reliability is becoming increasingly difficult to design into the physical layer. This paper discusses some of the most significant physical layer issues that must be considered when designing a serial communications system, including jitter management, byte and cell synchronization, clock recovery, and others.

## Authors

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*Current Activities:*
Neil Quarmby is Strategic Technical Marketing Manager for European Telecommunications Transmission and Switching Applications. He is currently managing the development of full-custom circuitry containing high-speed analog PLLs which are targeted for use in the TGB2000 BiCMOS ASIC family.

*Author Background:*
Neil joined Texas Instruments Ltd. in 1978 after graduating from Nottingham University. Neil managed a group of engineers working on Digital Signal Processor and Graphics System Processor support. He was elected to Member, Group Technical Staff (1987) and the scope of his role expanded to include all European Military customers. His current assignment is to develop, coordinate and market silicon solutions in the broadband communications arena.


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Howard Rubin holds the title of Member of Technical Staff in the Semiconductor Group at Texas Instruments. Howard provides application engineering assistance in the design and test of LAN and WAN internetworking products using TI's advanced networking components.

*Author Background:*
Howard graduated with the BSEE degree from Pennsylvania State University (1969) and earned an MBA at Rider College (1988). He has served as representative on LAN standards and testing committees and teaches numerous workshops on Token Ring LAN and ATM WAN architecture and design.

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Rick Curtis holds the position of Member of Group Technical Staff of the Semiconductor Group at Texas Instruments. Rick is currently involved in product definition and development for SONET/SDH/ATM catalog products.

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Rick holds a BSEE degree from the University of Arkansas (1983) and a MSEE degree from Southern Methodist University (1992). Rick has been employed at Texas Instruments since 1983.

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*Author Background:*
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# Physical Layer Design Issues for Serial Communications: A SONET Case Study

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## Physical Layer Design Issues for Serial Communications: A SONET Case Study

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Slide #2

## Overview

- SONET networks
  - Network span
  - Generic model
- Physical layer issues
  - Frame structures
  - Alarms and indications
  - Noise sources and specifications
- TDC BiCMOS components
  - TDC1555 clock recovery chip
  - TDC2302B line interface chip
- Conformance measurements
  - Jitter tolerance/attenuation test
  - RMS jitter test
  - SONET framing, alarm and indications test

A review of the SONET network span is provided to depict the functional requirements of particular network elements. A more focused development of a generic serial transmission model is used to delineate the lower layer procedures that may be implemented in VLSI. An examination of bit, byte and frame structure expected in the SONET STS-3 and SDH STM-1 data streams sets the stage for discussion of frame synchronization tasks. Signaling information relating to alarms and indications between network elements is discussed. Noise sources impacting the recovery of a stable clock is graphically presented to enhance the appreciation of practical clock recovery solutions. Levels of jitter attenuation and tolerance in clock and data recovery systems is related to testing methodologies to ensure conformance to industry standards and practice.

A brief overview of TI's BiCMOS process technology will familiarize the reviewer of features and benefits of this advanced architecture making possible high speed silicon building blocks for SONET, SDH and ATM networking solutions. A functional block diagram of the TDC1555 highlights the performance tasks of this TI clock recovery chip. Another component, the TDC2302B, is introduced which accepts serial information from the clock recovery chip and converts the data to parallel format is also described. The relationship of these devices to the TDC3003 SONET overhead terminator is briefly presented. A practical arrangement for measuring jitter, jitter tolerance and jitter attenuation using HP instrumentation as implemented in Texas Instrument's Sherman, Texas facility is presented.

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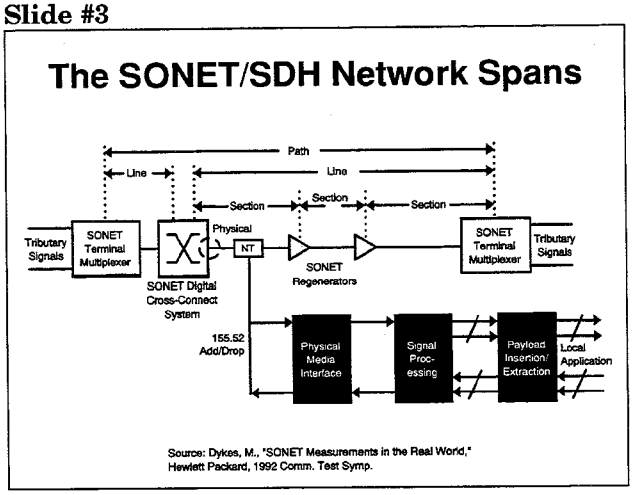


### Category Interfaces

*Category I* equipment is used in the 1.5.. to 45.. Mb/s (DS-1 and DS-3) interfaces to SONET NEs.

*Category II* equipment is used in the OC-N and STS-N interfaces for synchronous SONET interfaces to regenerators for the purpose of connection to and between carriers.

### Network Elements

Terminal Multiplexers are used to combine lower rate data streams to higher data rate capacity lines. Digital cross connects provide switching capability to route tributary data streams among higher rate STS-3c carriers. Regenerators are used to restore bit-level signal quality so as to equalize the effects of channel distortion and accumulated phase jitter. Regenerator applications may involve only physical and section layer design rules. The Add Drop Multiplexer (A/DM) network element is used to add or drop, say DS-1 signals from, say STS-1 signals. Since it connects to the telecommunications network, it extracts and transfers the network clock to subsequent stations. The requirements for the A/DM may be more rigorous than the local application, since exacting standards for transferred phase noise performance exist for equipment generating a clock to the carrier network. Local Applications are those generally associated with end user applications, hence host burden, cost and packaging issues are primary considerations. These may be Internetworking or workstation applications that feed the main SONET data stream, but terminate the data to a local area network gateway or user application.

### Layers

A layered interface exists in the SONET/SDH bit framing structure and application-specific devices can be designed to encode/decode specific bit patterns into bytes and words carrying data. At the physical layer, the electrical or optical interface is made to the STS or STM signals. As such, issues of power level, pulse shape, line coding and channel equalization are considered. Details involving the LED driver for the Fibre Optic Cable may also be considered. The section layer involves design rules for access to the medium such as framing, scrambling, section error monitoring and communication of section level overhead. The line layer provides synchronization and multiplexing functions required by the path layer so as to provide transport services for STS SPE payloads. Such functions as overhead for maintenance and protection purposes are inserted in the line layer signaling. The transport of network services between SONET higher layer protocols or terminal multiplexing equipment is provided by at the path layer. End-to-end tributary services such as DS1, DS3, etc are enabled by means of POH path overhead information.

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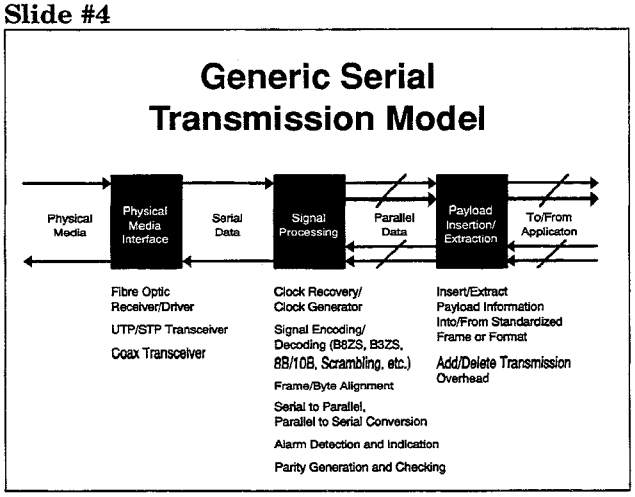


### Physical Media Interface

A Fiber Optic (FO) interface is typically required in SONET networks and is required to convert the optical transmitter and receiver energy to electrical pulses that can be interpreted by electrical clock and data recovery circuits. Many applications in local networks currently have metallic transmission media installed, and these will be used for short distance transmission service. The transceivers for interface with Unshielded Twisted Pair (UTP) media have the additional task of equalizing for channel distortion and intersymbol interference. Data transmission on coaxial cable rather than balanced twisted pair will feature more uniform channel characteristics with less noise. However, the added cost of the transmission medium will have to be realized.

### Signal Processing

After the medium has been properly terminated, the next step is to recover the network clock and to regenerate it for data validation and subsequent frame synchronization. The inherent noise quality of the clock recovery circuit as well as its response to phase jitter are critical to the robustness of the network and effect its ultimate dimension. Various methods are used for line encoding of the serial bit stream which yield significant gains in channel utilization and error detection and correction, such as B8ZS, B3ZS, and 8B/10B. Bit level, modulo 2 scrambling is used in the encoding/decoding process to eliminate the effect of extended zeros or ones that can cause clock synchronization failures due to insufficient data cell transitions. As mentioned previously, layer overhead and payload data is embedded in the received SONET superframe. Signal processing procedures are required to identify the locations of these data bytes to generate byte and frame synchronization signals to flag the appearance of this information. High speed data is transmitted serially to avoid multiple parallel paths in the communication medium. However parallel processing of the these decoded bits is necessary in order to reach the channel capacity using byte and multi-byte wide processors. Embedded in the frames passed between stations are alarms and indications which communicate the status of the line interface and subsequently data integrity. Upon detection of an alarm condition, a status flag is inserted in the frame to communicate to a far-end network element that terminates the service the need to initiate automatic service management processes. Internal parity checking and lockout are used to protect the process of bit/byte conversion and data handling procedures.

### Payload Access

Access to payload information and the insertion and extraction of data frames is the major function of the overhead terminator. End user applications require a data interface that optimizes attached system bus limitations. By stripping the Framing information needed to access the SONET network from the actual payload information, the data manipulation procedures of the host protocol processor may be more efficiently executed. In the process of building SONET frames for transmission to the network, the section, line and path overhead bytes need to be inserted with the payload frames before converting them to/from the serial transmission physical layer.

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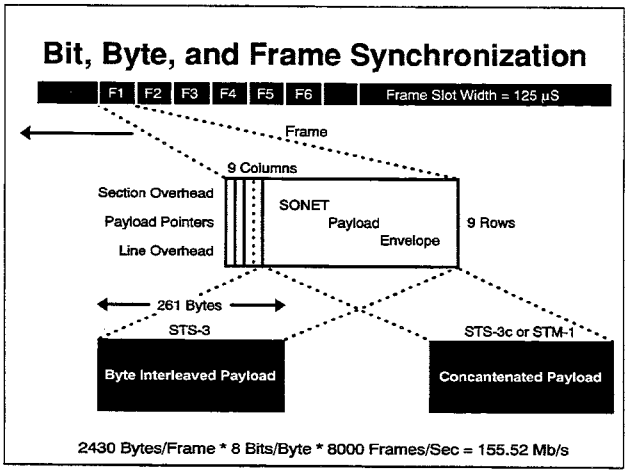


## SONET/SDH Serial Data Stream

The STS-3 or STM-1 rate is transmitted at a rate of 155.52 Mb/s (nominal). The information is transmitted bit-by-bit using a CMI, coded mark inversion line code. After conversion to the electrical signal, the data pulses are nominally "rectangular" (although at 155 Mb/s they are anything but rectangular) and must fit in a Transmitter pulse mask which is defined for a binary zero and binary one symbol. These signals are very low in amplitude (0.5 V) and have a fast rise time of 2 ns. Since this data stream must propagate through the established carrier line equipment, a 125 µs frame slot width is imposed on the data pattern. This essentially defines the framing rate of 8K frames per second and further defines the size of the SONET frame able to be transported at this rate. Naturally as the line rate increases to 622 Mb/s and higher, larger data frames may be constructed, but the 125 µs frame slot width requirement remains fixed.

## SONET/SDH Frame

However at 125 µs and 155.52 Mb/s, each frame carries a total of 2430 bytes organized in 9 rows of 270 bytes per row. The first nine columns contain overhead and pointer information that allows access to the SONET channel as described above. The section overhead identifies the Framing, STS-1 Identifiers, Section Error Monitoring, Orderwire, Section User Channel, and Section Data Communication Channel bytes. The location of these bytes is critical to maintaining coordination with other section terminating functions, as well as transporting STS-3 frames across the physical medium. The line overhead contains Pointer Offset, Point Action, Line Error Monitoring, APS Channel, Line Data Communications Channel, Orderwire and bytes reserved for Growth. The location of these bytes is critical to maintaining coordination with other line terminating functions, as well as locating the start of the payload envelope data. The payload pointers provide a means for flexible and dynamic alignment of STS Synchronous Payload Envelope within the STS envelope capacity. These allow the SPE to float within the STS envelope capacity to accommodate phase and rate variations.

## SONET Payload Envelope

The payload envelope is the bearer capacity for transmitted user information. Two types of data organization follows: The STS-3 byte interleave format allows for transmission of multiple tributaries, referred as virtual tributary (VT), within a single SPE. The information is byte interleaved which ensures fairness in the allocation of channel capacity among multiple subrate sources. If the SPE capacity is to used for the STS-3c or STM-1 payload format, a concatenated SPE is possible. The ensures that the subrate services are kept together, whereby the SPE must be multiplexed, switched, and transported through the network as a single entity.

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## SONET/SDH Alarms and Indications

- Alarm Indications
  - LOS Loss of Signal
- Tracking Mode Frame Monitoring
  - RFE Received Frame Error
  - OOF Out of Frame Error
  - LOF Loss of Frame Error

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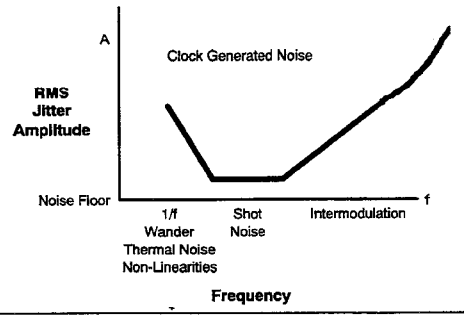
## Noise and Distortion in SONET/SDH Clock Recovery
### One of Two




### Alarm Indications

A Loss of Signal condition occurs when the receiver loses clock or data transitions (high or low) for a period of 25 µs, which corresponds to about 38-bit cells of signal loss.

### Tracking Mode Frame Monitoring

A Receive Frame Error occurs coincident with loss of frame synchronization and is signaled by the local receiver coincident with the third A2 framing byte of the Section Overhead. If four consecutive frames have framing errors, OOF becomes active high. It will remain active for at least two frames to verify framing integrity. The LOF indicator becomes active high if OOF is high for 3 ms, which relates to 24 frames worth of error. It remains high until eight consecutive error-free framing patterns are received.

### Jitter - General

Jitter is the uncertainty associated with a signal's bit cell value that results in the loss of data recognition at terminating network elements. Jitter is often measured on the extracted clock as the level of RMS Jitter Amplitude within a narrow bandwidth of frequency. The noise may be characterized by checking the Jitter Amplitude at discrete frequencies, then plotting on a continuum. A variety of sources contribute to phase instability as measured from one bit cell to the next. Jitter can result from system stimuli such as error bursts, phase hits, and outages. However data pattern transitions can also cause jitter. Accumulation of jitter in a chain of regenerating stations can occur if each station must synchronize to and transfer data with respect to the locally recovered clock. Channel impairments such as return loss, flat loss, crosstalk, and other problems exacerbate the generation of clock jitter. The use of fiber optic transmission greatly reduces the effect of channel impairments.

### RMS Jitter Amplitude

On the vertical axis, a measure of jitter amplitude is presented relative to the noise floor. The noise floor is the lowest level of discernible noise in instrumentation circuits. All noise from the clock extraction circuit must be measured against this noise floor. The clock recovery circuit performs as would a filter to pass the desired signal (clock) from

all other signals (noise). The selectivity of this filtering process is a measure of its ability to attenuate interfering noise that shows up as clock jitter.

### Frequency of Jitter Noise

Along the frequency domain are possible causes of jitter. Wander, Thermal Noise, and Nonlinearity result in low frequency phase jitter. These effects are easily tracked by succeeding clock recovery circuits, and are transferred to down stream network entities. Shot noise is more burst-like in occurrence and typically falls within the bandwidth of the clock recovery filter. Fortunately the level of shot noise is nearer the noise floor and presents less of a problem to clock recovery circuits. Intermodulation noise results from channel distortion and environmental interference and so is difficult to eliminate in practical installations. This noise occurs at increasingly higher frequencies and may fall outside the bandwidth of clock recovery circuits. A tradeoff exists in the design of receiver circuits deploying narrow bandwidth clock recovery circuits to filter some of this noise, yet pass an allowable amount to the next station.

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**Noise and Distortion in SONET/SDH Clock Recovery**
**Two of Two**

| CLOCK EXTRACTION METHODS | ADVANTAGES | DISADVANTAGES |
|---|---|---|
| SAW Filters | Jitter Tracking, Outband Jitter, Attenuation | I/O Drive Limited, Excitation Dependent, High Cost, Large and Fragile |
| Silicon PLLs | Frequency Stability, Superior I/O, Macro Call, Capability, Low Cost | Phase Drift, $V_{CC}$/GND Noise, False/Injection, Locking |
| VCXO Oscillators | High Frequency, Stability | High Cost, Low Jitter Tolerance |
| RC/Active Filters | Low Cost, Traditional Design | High Transfer Jitter, Analog Adjustment, Requires Jitter, Absorbing Circuits |

### Jitter-Noise and Filter Implementations

The design of a good clock recovery circuit implies raising its ability to tolerate incoming jitter while limiting the jitter it transfers to the next line interface. If we consider the clock recovery circuit as an active filter, and if the energy in the baseband signal is substantial, then a low cost solution can be realized from lumped parameter networks and a gain-controlled amplifier. Unfortunately, this approach suffers from higher transferred jitter, thus requiring dejitterizer circuits, and is a more difficult design task from a producibility standpoint. Surface Acoustic Wave (SAW) filters are often used in high speed data circuits because they exhibit excellent out of band noise rejection with wide bandwidth passband characteristics for good dynamic tracking ability. Since they are essentially high Q passive filters, they must be driven and buffered by amplifiers. Inadequate drive capability and dependence on continuous excitation are their major weaknesses. These devices are also more difficult to produce in volume due to their high cost and fragile structure. Silicon PLL filters answer the call for practical, realizable clock receiver solutions. They exhibit inherently superior drive capability and may often be integrated with higher density logic functions to create application-specific ICs that are optimized for a particular line rate and

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function. With careful design, these devices can achieve good frequency stability and out-of-band jitter rejection characteristics. Superior process technology and control is a must in manufacturing of these devices to avoid sensitivities to power supply noise, phase offset and false or injection locking difficulties.

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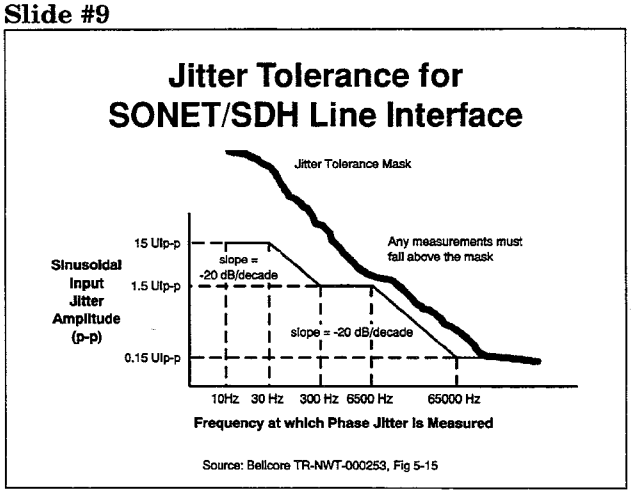


### Jitter Tolerance

The Jitter Tolerance (JTOL) specification for receiver performance is a measure of how much jitter in a data signal can be tolerated by the clock recovery circuit before errors in data validation occur. To assure minimum bit error rate in the presence of noise, the JTOL must always be greater than the worst case transfer jitter.

### Jitter Tolerance Mask

The JTOL mask is a benchmark of jitter tolerance performance against which a solution's actual sensitivity to jitter can be compared. A value above the mask is satisfactory, that is more peak-peak jitter is required to induce bit errors in the data validation process. Bit error rates less than one in 1010 are generally considered satisfactory in most applications. However NO occurrence of errors may the target in the development stages for a new product.

### Sinusoidal Jitter Input

The ordinate axis of the JTOL mask is calibrated in unit intervals of sinusoidal jitter. A phase modulator is typically used to stress a data stream of predictable pattern. The Unit Interval is a relative measure of phase jitter with respect to the width of a bit cell at the subject line rate, which for 155.52 Mb/s is 6.43 ns. The sinusoidal jitter is measured at the frequency breakpoints and elsewhere as indicated on the JTOL mask. At each frequency of measurement, the level of sinusoidal jitter is increased until an intolerable BER occurs.

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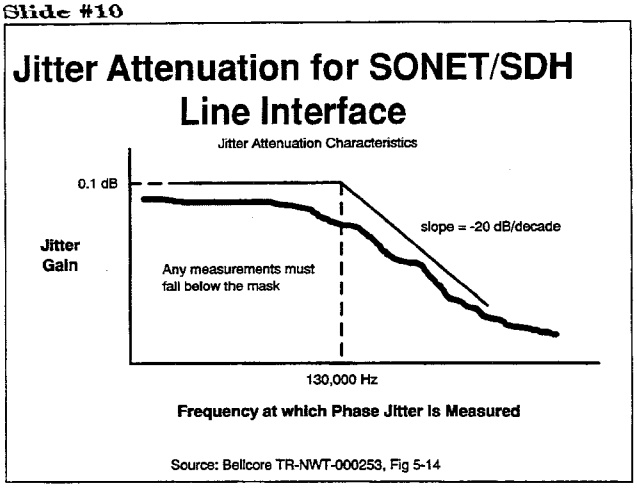


### Jitter Attenuation

Jitter attenuation is a relative measurement made at discrete frequencies between the incoming data stream and that which is clocked back out to the network. The inherent noise level of the clock recovery circuit itself adds statistically to the received jitter and becomes part of the transferred jitter if there is no elastic store for de-jitterizing the transmitted pulses. The jitter attenuation of a clock recovery circuit limits the amount of jitter passed to the next line interface when the local clock is used to synchronize the transmitting of serial data to the network

### Jitter Attenuation Mask

The Jitter Attenuation mask sets benchmark performance in a manner similar to the JTOL mask, however this one sets the maximum level of jitter allowable at any given SONET network entity. All measurements must fall below the mask to be acceptable.

### Sinusoidal Jitter Input

The measure of quality in the Jitter Attenuation test is gain in dB. For gain to be an attenuation, the value must of course be less than unity, as indicated on the mask.

### Frequency of Jitter Output

The jitter attenuation is measured at the frequency breakpoints and elsewhere as indicated on the Jitter Attenuation mask. At each frequency of measurement, the level of sinusoidal jitter output is compared to the input.

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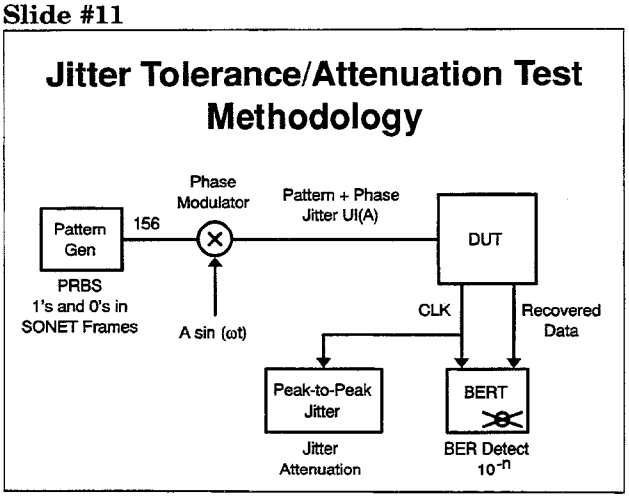


### Jitter Input

The minimum level of phase jitter that can be applied to a data stream without exceeding the BER limit is mapped against frequency and compared to the JTOL mask. The test requires many data points to properly map out the jitter tolerated for comparison with the JTOL mask. These tests are frequently repeated in the development cycle as efforts to improve a solution's jitter tolerance may involve tuning channel equalizer and loop filter values, adjusting board layouts and selecting interface devices for low loss. A consistent means for data generation, collection and reporting is needed to expedite this process. The pattern generator is used to generate the pseudo random bit sequence that must be received with minimal bit errors at the receiver.

A Pseudo Random Bit Sequence (PRBS) is used as the data pattern to stress the receiver and provide a rich source of baseband energy for clock recovery. The input signal is modulated at incremented frequencies and at a phase deviation in UIs until bit errors are detected by the bit error rate tester. A sinusoid is used to simplify the generation and analysis of the phase jitter. The sinusoid frequency and amplitude are accurately controlled, often by digital means for repeatability.

### Device Under Test

The Device Under Test (DUT) is the target receiver with clock recovery and data validation circuits active. It is not necessary to include the framing and alarm functions as they are dependent on these clock/data processes, however they are important and will be tested elsewhere. The derived clock signal is used by the BER tester (BERT) to synchronize it to the recovered data outputted by the DUT. The recovered data signal is analyzed by the BERT to detect bit slipping resulting from the receiver's inability to recover or track the desired clock signal in the presence of sinusoidal jitter.

### Bit Error Rate Test

The PRBS is known by the Bit Error Rate Detector so it can track the recovered data and detect bit errors in the data validation process. The level of BER is often expressed as two or fewer error seconds over a 30 seconds measurement interval. This related to BER levels of performance slightly more than one error in approximately 1010 transmitted bits.

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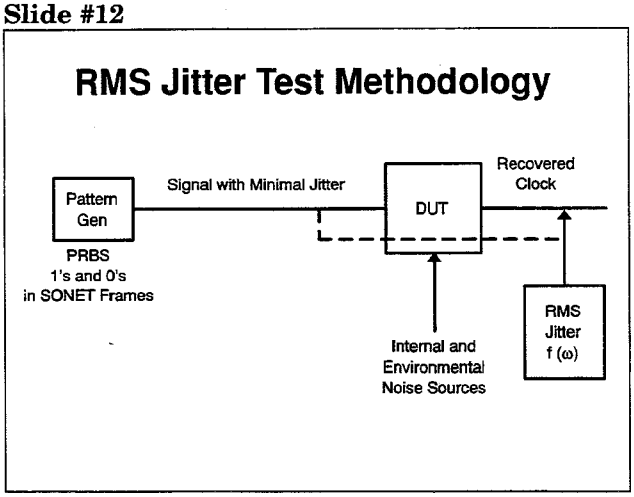


### RMS Jitter Measurement

As indicated in the diagram, this is a measurement of jitter transferred from the input to the output of conformant SONET regenerator. A value of jitter attenuation is computed for comparison with the acceptable levels as previously described. The RMS Jitter instrument is used to measure input jitter vs output jitter as a function of frequency. The spectrum of jitter generated by the DUT (and subsequently transferred to the network) provides useful information about noise sources and characteristics of the clock recovery circuit. These must be analyzed carefully to meet the requirements of industry standard organizations.

### PRBS or Other Pattern Input

The pattern generator is used to generate a clean PRBS that is tracked with minimal bit errors at the receiver, in a manner similar to the JTOL test above.

### Device Under Test

A test of transferred jitter may require measurement at the recovered data output of the receiver, also. This is particularly the case when measuring transferred jitter in the presence of a PRBS data pattern. The RMS jitter spectrum may be measured at the recovered clock if it is accessible in the receiver design under test. Analysis of clock noise under stable input conditions is useful for determining the quality of a receiver implementation.

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## BiCMOS Products for SONET/SDH

- BiCMOS EPIC-IIB Process Technology
- ECL/Pseudo-ECL Compatibility
- Proven Architecture

### Proven Architecture

TI is considered by most of the major telecommunications design companies as the leader in high performance, application specific integrated circuit (ASIC) design and fabrication. The TGB1000 has been used successfully to implement dozens of ASIC and complex gate array functions. TI has introduced a family of Gate Array products based on this process technology which range in complexity up to and beyond 100K usable gates. In the case of Gate Arrays a triple level metalization scheme is used to interconnect this sea of gates. This allows TI to develop a wide variety of different structures for the logic functionality and performance requirements of data handling, static RAM and analog functions that are co-resident on a single substrate.

### EPIC IIB BiCMOS for TDC2302B SONET/SDH

The EPIC IIB is a process technology able to integrate the features of high speed logic, fast FIFO's multiport memory and VCO and charge pump circuitry. TI's BiCMOS approach results in low power dissipation/consumption designs, also. This process technology may be used for effective solutions for clock recovery, frame alignment, overhead termination and elastic store — as typically required in SONET/SDH applications.

### BiCMOS EPIC-IIB Process Technology

A TI patented process serves as the foundation for TI's ABT and LinBiCMOS high speed and intelligent-function logic and linear products. The ABT family allows bipolar device structures for tighter, more uniform timing characteristics which results in higher speed circuit implementations. CMOS structures realize lower power implementations of complex logic functions which result in higher density, integratable macro cells.

### ECL/Pseudo ECL Compatibility

Bipolar Emitter Coupled Logic (ECL) structures are used to implement non-saturating, high speed transceivers and data buffers for high data rate interface. Bridging the gap between ECL structures and standard TTL I/O, Pseudo ECL (PECL) converters are available. These are referred to Vcc instead of ground.

### Cost Effective

Although additional processing levels add more cost to the BiCMOS technology, systems requiring a high level of integration are more cost effective than pure CMOS or Bipolar configurations.

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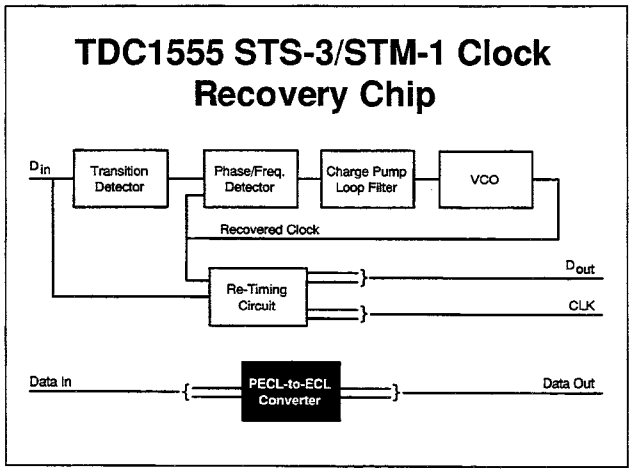


### TDC1555

The TDC1555 is a clock and data recovery device for use at the 155.52 Mb/s high speed data rates associated with SONET and SDH systems. The clock recovery functions are implemented with analog PLLs using TI's BiCMOS process technology. This device complements other TI BiCMOS devices for complete line interface solutions at the 155.52 Mb/s rate. It serves also as the key building block for TI's continued development of high density VLSI solutions for SONET/SDH and ATM applications that meet the jitter attenuation and jitter accommodation requirements of Bellcore Specification TA-NWT-000253.

### Phase-Locked Loop

The transition detector terminates the incoming differential serial data input, slices the level to a binary representation and buffers the signal for driving the phase/frequency detector. The data input may be ECL or Pseudo-ECL compatible and is automatically adjusted. A phase/frequency detector is used to sample the incoming serial data and output an error signal to the charge pump circuit to maintain the Voltage Controlled Oscillator (VCO) in synchronism. A frequency Loss-Of-Lock (LOL) indicator detects when the loop has brought the VCO close to the desired embedded clock in the incoming serial bit stream. The charge pump and associated loop stabilization filter smooth the error pulses derived from the freq/phase lock detector and output the dc voltage sensed by the VCO to modify its frequency. An external capacitor input is provided for additional stabilization if necessary to reduce jitter enhancement (peaking) effects. The dc voltage is used to speed up or slow down the VCO oscillator. This has the effect of adjusting its clock position within the central one-third of bit cell for data validation.

### Data Validation Latch

This recovered clock is fed back to the phase detector and presented to the retiming circuit for data validation. The recovered clock provides the decision timing for comparison with the instantaneous value of the received data. Hence the timing signal must have very low inherent phase jitter and be well-centered in the middle of the receive window eye pattern for maximum jitter tolerance.

### Auxiliary Functions

Although the major function of this device is clock recovery, a differential PECL to ECL mode buffer is provided for the transmit channel. This is particularly useful where the framing device does not have the capability of interfacing optical transmitter circuits requiring the ECL interface.

### Packaging Options

The TDC1555 is available in the 24-pin wide-body surface mount or dual-in-line packages.

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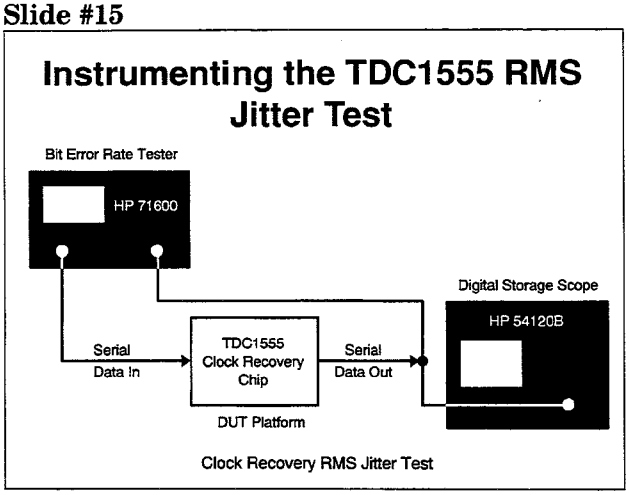



### RMS Jitter Test

Clock recovery RMS jitter test measures performance under different input conditions. This test measures the RMS jitter on the validated data signal that is correlated with incoming data pattern, whether a PRBS of successively increasing extent or of long strings of zeros or ones. A DSO is used to analyze the waveform and determine the RMS level of Jitter occurring on the sampled signal.

### Input Conditions

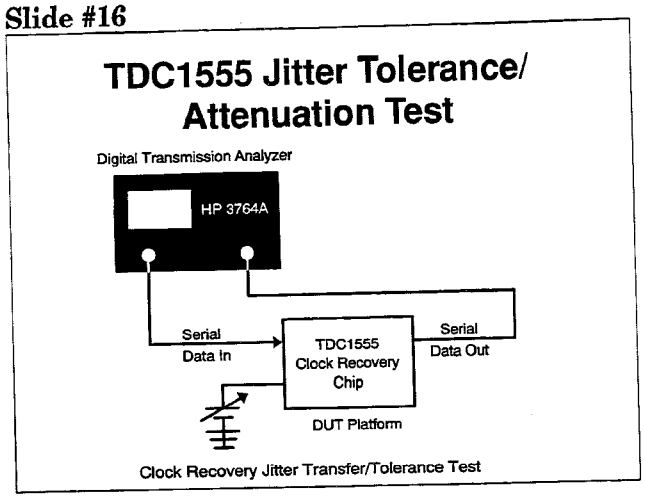
A serial data stream is generated by the Bit Error Rate Tester (actually a data pattern generator). The use of the pseudo-random bit pattern provides a consistent means for generating random data patterns and for exploration of worst case sequences to stress the clock recovery circuit. The following bit streams are used: 27-1, 210-1, 215-1, 223-1, 231-1. Strings of "1's" or "0's" are also used to determine whether the phase detector/charge pump circuitry are able to tolerate jitter with consistent margin when stressed at group delay limits. The BER capability of the pattern generator is also used to ensure a sufficiently low error rate condition when evaluating the RMS jitter level of the clock recovery system measured.

### Analysis

The HP 71600 Series Error Performance Analyzer consists of pattern generator, synthesized clock source, and error detector modules configured in the HP 75000 modular measurement system. It features standard pseudo-random test patterns up to 231-1 bits long. Complementary clock and data outputs simplify connection to the TDC1555 high-speed logic device, which reduces the DUT platform design to one of good RF practice and stripline techniques for wiring to/from the silicon device.

The automatic features of the HP 54120B Series High-Bandwidth Digitizing Oscilloscope (DSO) help make the data collections and statistical processing of data more accurate and repeatable. In this application, the DSO captures the serial output data and processes the sample to determine RMS jitter on a bit-cell by bit-cell basis at the line rate of 155 Mb/s, doing so for a variety of input signal patterns. The data pattern effects on the instrumentation are ignored — only the impact of data pattern on the data recovery process results.

Slide #16



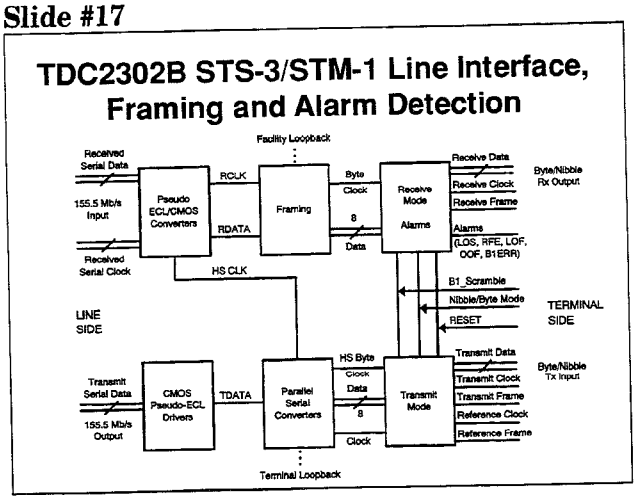

### Jitter Tolerance/Jitter Attenuation Test

This test measures the peak-peak jitter tolerance and the intrinsic jitter attenuation (transfer) by the clock recovery system of the TDC1555. The clock recovery jitter tolerance test measures the level of input jitter allowable before bit recognition errors occur due to insufficient eye height or bit slipping in the PLL. The clock recovery jitter attenuation test measures the noise and distortion passed to the reconstructed clock as a result of random and data-correlated jitter response of the PLL loop filter. In a manner similar to the previous RMS Jitter Test, the DTA generates the data pattern. However unlike the RMS Jitter test, the DTA also analyzes the RMS jitter on the output data stream and evaluates the jitter tolerance and jitter attenuation characteristics as a function of frequency.

### Analysis

The automatic features of the DTA help make the tasks of data collection and statistical processing more efficient for production test environment. The DTA is capable of pattern generation and coded sequences, while also monitoring the data recovery circuit for occurrences of error "hits." The DTA is also capable of performing the CCITT 0.171 recommended tests using internal filters for selective jitter measurements.

Slide #17




## TDC2302B

The TDC2302B STS-3/STM-1 Line Interface provides the nibble/byte framing interface between the data and clock serial bit stream of the TDC1555 and the higher layer protocol decode functions of the attached system. This device is based on TranSwitch Corporation's CMOS TXC03201, but utilize TI's high performance 0.8 µm BiCMOS process technology. Framing error indication, if enabled, is also implemented on this VLSI device.

### Receive Channel

The device's main function on the receive channel is to extract framing synchronization and to convert the incoming serial information to clock and data in byte/nibble parallel format. Two synchronization modes are supported: tracking and non-tracking. When tracking, the TDC2302B will find the initial frame and verify it on successive frames for frame alignment errors. In the non-tracking mode, it finds the frame, but no subsequent monitoring of the signal is provided. Descrambling and B1 parity detection functions are provided internally to the TDC2302B if enabled. The incoming serial data is monitored at the PECL input to determine transition density, and a Loss-Of-Signal (LOS) indication is generated if below the nominal 25 µs. When in the tracking mode, the TDC2302B outputs a Receive Frame Error (RFE), Out-Of-Frame error (OOF), or Loss-Of-Frame error (LOF) if frame alignment errors are found. ECL/PECL converters simplify the connection of external ECL interface devices to internal CMOS gate structures. Facility mode loopback is possible which routes line-side received data to the terminal side and outgoing transmit channel. This feature is useful for line side diagnostics.

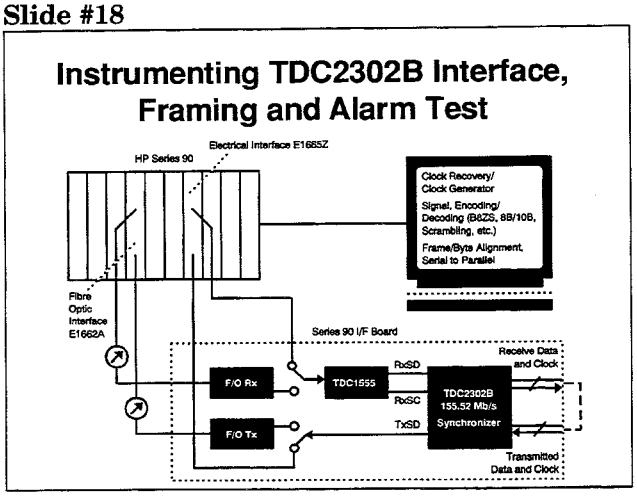
### Transmit Channel

In the transmit mode, the device accepts byte/nibble data and clock from the terminal side and embeds a frame synch signal to establish proper timing for the scrambling and B1 parity generation. These scrambling and B1 parity generation functions are provided internally to the TDC2302B if enabled. The transmit block nibble/byte information is converted to serial data using the receive clock inputted above. This ensures synchronism to the line side network. Terminal mode loopback is possible which routes terminal-side transmit data to the line side and local receive channel. This feature is useful for terminal side diagnostics. PECL/ECL converters simplify the connection of internal CMOS gate structures to external ECL interface devices.

### Packaging Configuration

The TDC2302B is packaged in an 84-pin plastic leaded chip carrier (PLCC) using 50-mil-pin spacing.

Slide #18




### Line Interface, Framing and Alarm Test

Here we test the ability of the line interface device's clock, framing and alarm indication capability to meet requirements of ANSI T1.105-1991 Bellcore TR-NWT-000253 and CCITT G.708. The test verifies the solution's ability to insert the required parity bits and perform the scrambling/ descrambling operations needed to build proper SONET/SDH frames. Such tests as frame alignment, payload mapping, pointer generation and analysis are desired. Block data moves are performed by the test instrumentation to prove that data manipulation is possible at low bit error rate when operating a terminal side loopback, but external to the line device. The Sensitivity of the Clock Recovery is tested under stress conditions of a PRBS data stream of successively increasing extent, or of long strings of zeros or ones and the resulting BER is determined. Values of the framing bytes are changed and errors are inserted which force internal alarms to indicate the occurrence. Loss of Signal, Loss of Frame and Out of Frame alarms conditions are detected. Other indications such as bit Interleave parity codes and far end block error are also checked.

### Procedure

The HP Series 90 SONET/SDH analyzer is outfitted by the Electrical Interface and Fibre Optic Interface modules for driving the HP Series 90 Interface Board. This Interface Board is used as the hardware environment for the optical interface, clock recovery and line interface devices. An external loopback is made at the terminal side of the TDC2302B. Procedures for ECL hardware design should be observed in arranging circuits and instrumentation at the SONET/SDH line rates. Good termination practice is required when preparing the Interface board testing environment. All terminations are 50-ohm and stripline practice for 200+ MHz data transmission.

### Analysis

The HP Series 90 with associated Fibre Optic or Electrical Interface plug-ins generate a data pattern and receive the reconstructed signal to compute the Bit Error Rate. Selection is made between an optical interface or electrical interface to determine the impact of successive stages on the derived BER figure of merit. A PC/Windows-based user interface loads the interface modules with conformance test suites.

The HP Series 90 Analyzer provides ATM and SONET/SDH measurement capability for testing B-ISDN networks. Use of this test package simplifies the generation and analysis of these serial bit streams and embedded cells. The flexibility of the Series 90 to support a wide variety of optical and electrical interfaces and HP-IB remote control makes generation of comprehensive testing suites practical.

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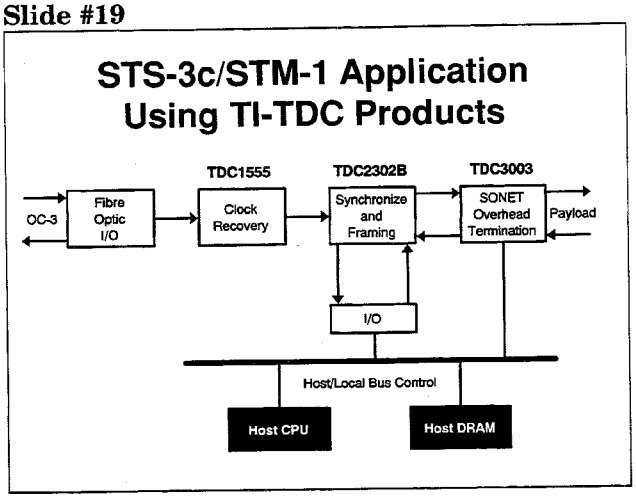
Slide #19




### ElectroOptic Interface

The TDC components require external translation of the optical serial data. The fiber interface converts the optical input to either an ECL or Pseudo ECL level for connection to the TDC1555 clock recovery chip.

### Clock Recovery

Use of the TDC1555 allows the extraction of the 155.52 Mb/s clock and retiming validation of the data for presentation to the TDC2302B Line Interface. The data is still in its serial format, however the extracted clock is needed to interface the transmitted information synchronous with the SONET/SDH network.

### Synchronization and Framing

The TDC2302B accepts the serial bit stream, decodes the framing synch and handles the scrambling and parity bit detection as described earlier in this presentation. The decoded bytes are presented to the TDC3003 SONET Overhead Terminator as a parallel interface.

### Overhead Termination

The TDC3003 provides section, line and path overhead processing on the STS-3/STS-3c/STM-1 signal. It provides additional line AIS, loss of pointer, path AIS, loss of multiframe, and yellow (path remote) indications. B2 and B3 parity-counting and pointer movements are detected also. Using the framing and clock reference pulses from the TDC2302B, this device can determine pointer justification for the SPE of the STS-3/STM-1 frame. Up to 261 bytes corresponding to one STS-3c/STM-1 payload (plus VC-4 overhead) SPE or three 87 byte STS-1 SPEs are passed to the attached system via the Local Bus I/O Interface. A similar, but reverse process exists in the transmit channel direction going back out to the line side.

### Local Bus I/O Interface

A typical workstation applications will require either an 80 x 86 or 680 x 0 compatible micro-processor interface. The interface provided by the TDC3003 allows for 10 bits of address and 8 bits of data in an interrupt-driven data transfer process. Alternately, the information may be passed to another application via a shared memory architecture using an additional DMA controller and memory interface solution.

Slide #20

## A SONET Case Study Conclusion

- Low cost solutions are required for desktop BISDN services that include interface with SONET payload envelopes which may contain ATM packetized data
- User demand for High Bandwidth Line Interface Solutions will stimulate the introduction of VLSI devices that meet applicable Bellcore, ANSI and CCITT standards
- Texas Instruments has developed an 0.8 μ BiCMOS process technology that could handle data rates in excess of 1.2 GHz.
- Demonstrating conformance to Industry Standards is made easier by use of HP Instrumentation. There is consistency in measurement when data is collected using this approach, which allows comparative data analysis.
- There is a DEMO Table that shows the test set up discussed in this paper.

Slide #21

## Recommended Resources

- Test Equipment
  - HP 71603B 3 GHz BERT
  - HP 54120-series High Bandwidth Scope
  - HP 3764A Digital Transmission Analyzer
  - HP 75000 Series 90 SONET/SDH Analyzer
- Integrated Circuit Products
  - TI TDC1555 STS-3/STM-1 Clock Recovery Chip
  - TI TDC2302B STS-3/STM-1 Line Interface Chip
  - TI TDC3003 SONET/SDH Overhead Terminator Chip
- Evaluation Board
  - TranSwitch TXC-21061 SONET/SDH Eval. Board

### SONET Networks

Low cost solutions are required for desktop B-ISDN services that include interface with SONET payload envelopes that may contain ATM packetized data.

### Physical Layer Issues

User demand for high bandwidth line interface solutions will stimulate the introduction of VLSI devices that meet applicable Bellcore, ANSI and CCITT standards.

### TDC Components

Texas Instruments has developed a BiCMOS process technology that could be used at data rates up to the GHz range.

### Instrumenting for Conformance and Performance Measurements

Demonstrating conformance to industry standards is made easier by use of HP instrumentation. Data collected using this approach is consistent in measurement and allows comparative data analysis.