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Understanding Evolving ATM Standards and ATM Design Verification

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Abstract

In the last two years, ATM has become the fastest evolving communication standard. Understanding where the standard is in its development can become a significant barrier to designing ATM-compatible equipment. This paper describes the latest advancements in the development of ATM standards and discusses tools that can provide ATM design verification.

Authors

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Rick Tinsley is Director of Marketing responsible for TranSwitch's ATM product line.

Author Background:
Rick received his BSEE from Rensselaer Polytechnic Institute and MBA from the University of Dallas. Formerly with Texas Instruments, he held various marketing, sales, and business development positions. Prior to TI, he was an Analog Designer at General Electric.

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Dan Upp is Vice President of Technology Development and a founder of TranSwitch Corporation.

Author Background:
Dan received his BSEE and MSEE from Ohio State University and worked on satellite communications systems and antenna array systems at the OSU ElectroScience Labs. Subsequently, he was employed by North Electric Co. in the hardware design of the DSS-1 (later referred to as the ITT 1210) switching system. Dan spent ten years at the ITT Advanced Technological Center where he was Director of Exploratory Systems, responsible for VLSI, hardware, and software development for packet switching, telephone switching, LAN and PABX products.

Slide #1

Understanding Evolving ATM Standards and ATM Design Verification

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Slide #2

Outline

- Evolution of ATM Technology
- BISDN Protocol Reference Model
  - Physical Layer
  - ATM Layer
  - ATM Adaptation Layer
- Summary & References

This paper explains the rationale for the development of ATM as a new, fast-packet networking technology. ATM standards are reviewed, including physical layers, the ATM layer, and the ATM adaptation layer. Reference material is listed on the last two pages.

Slide #3

Current Technology

- Circuit switched
  - Fixed bandwidth
  - Low latency
- Packet switched
  - Simpler multiplexing
  - Delay variations and high latency

Current network technology generally falls into two classifications: circuit-switched technology in the traditional telephony arena and packet switching in the LAN/data networking community.

Circuit switching is characterized by fixed graduations of bandwidth, such as a 64kbit/s voice channel with prescribed subrate and superrate multiplexings. Circuit switching requires a continuous hold of the physical path for each connection, regardless of actual bandwidth used. This provides very low latency, and thus excellent performance for voice and other isochronous information.

Packet switching is more efficient with respect to bandwidth utilization since access is limited to the time required to transmit a given packet or frame. Switching and multiplexing are also simpler since routing is software oriented, but much slower as a result. Packet-or frame-oriented protocols include X.25, Frame Relay, Ethernet, Token Ring, and FDDI. All are characterized by higher latency and delay variations as compared to circuit switching.

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What Would Be the Characteristics of an Ideal Network Technology?

- Routable at smallest possible level
- Low latency
- Common, scaleable access
- Global interconnectivity

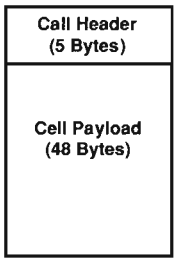
If you could define an ideal network technology, you would combine the best features of existing circuit and packet standards for optimum efficiency. To obtain maximum utilization of network bandwidth, you should route information at the smallest "molecular" level, or in other words, you should use very small, fixed-sized packets. This allows dynamic multiplexing or grooming of multiple signals on the same physical media. Small, fixed-size packets also enable the short, predictable delays required by constant bit-rate services.

Such a network technology would be well suited to all types of data, including voice, video, and bursty data. To be successful, governing standards would have to be internationally accepted and global in scope.

Slide #5

ATM: A New Network Technology

- 53-byte cell
- All types of data
- Transport & switching
- International standards



Asynchronous Transfer Mode (ATM) is a new networking technology based on international standards. It is intended and expected to be suitable for all types of information and provides the infrastructure for broadband networks beyond the year 2000.

With ATM, all information transfers are performed using standard 53-byte cells, each having prescribed structures and methods of formation. All switching and multiplexing is done one cell at a time with each cell being routed independently. All information required by the network to relay a cell from node to node is contained in the cell itself. Bandwidth and access may be dynamically allocated.

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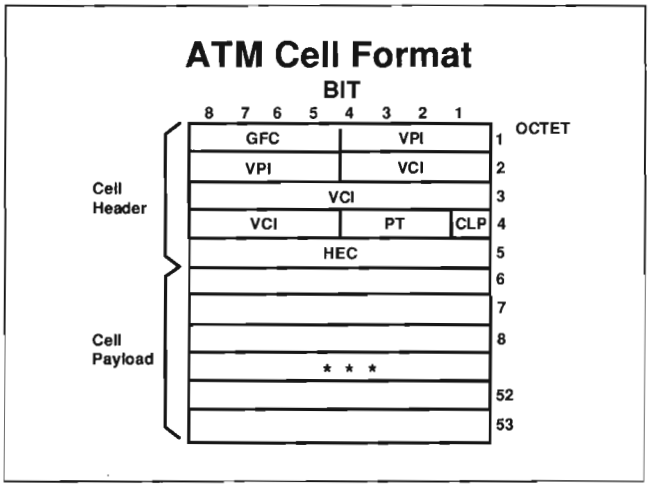


The ATM cell header is composed of the following fields:

GFC Generic Flow Control (UNI only)
Note: The GFC is replaced with an additional 4 bits of VPI at NNI.

VPI Virtual Path Identifier

VCI Virtual Circuit Identifier

PT Payload Type

CLP Cell Loss Priority

HEC Header Error Control (8-bit CRC).

The remaining 48 bytes form the cell payload.

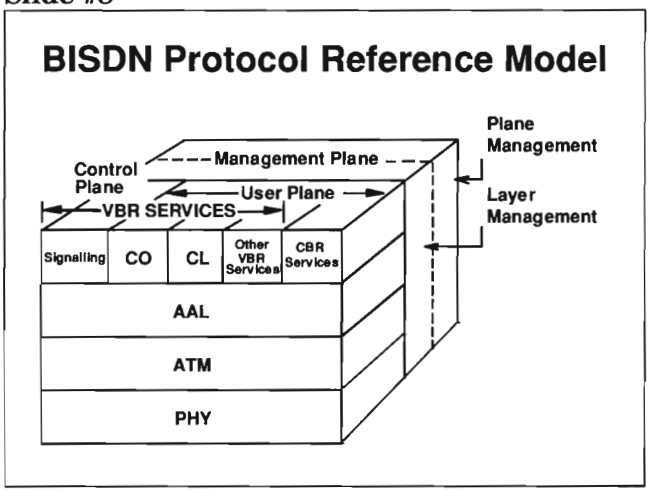
Slide #7

BISDN: Broadband Integrated Services Digital Network

- Driven by CCITT and ANSI T1S1
- High bandwidth, multimedia platform
- Connection-oriented service

ATM has been chosen by standards committees, including ANSI T1 and CCITT SG XVIII, as an underlying transport technology within many Broadband Integrated Services Digital Network (BISDN) protocol stacks. Transport technology relates to the switching and multiplexing techniques at the data link layer.

Slide #8

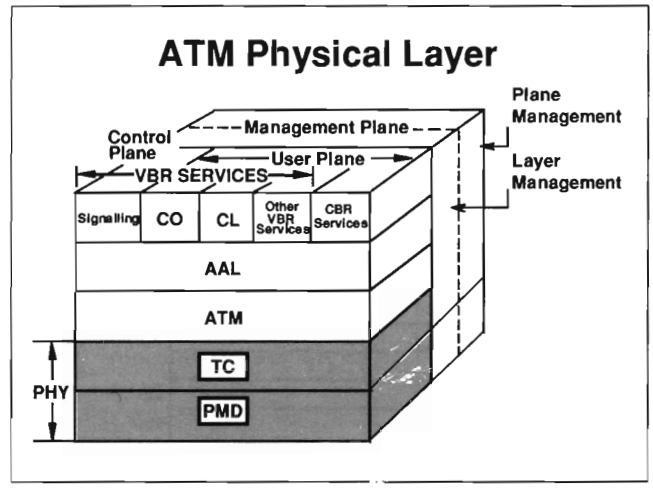


Implementing an ATM bearer service requires the specification of an ATM layer and a related physical layer. These two layers are service-independent and contain functions applicable to all upper layers.

The ATM Adaptation Layer (AAL) adapts the ATM bearer service to provide various networking services including Constant Bit Rate (CBR) and Variable Bit Rate (VBR) services.

The user plane provides the transfer of user-application information. The control plane deals with call establishment, call release, and other connection control functions. The management plane provides management functions and allows the interchange of information between the user plane and control plane.

Slide #9



The ATM Physical Layer consists of two sublayers: Transmission Convergence (TC) and Physical Media Dependent (PMD). ATM cell mappings correspond to existing physical layer standards such as SONET and SDH (synchronous optical networking hierarchies for North America and Europe, respectively), DS3 and E3 (level 3 asynchronous digital interface standards), Block Coding, and others.

The PMD sublayer deals with bit transmission over a physical link, such as fiber optic cable, coax, or copper twisted pair. Issues and specifications, such as line coding, electro-optic conversion, pulse masks, and clock recovery, fall within this sublayer.

Transmission Convergence generates and receives transmission frames and contains all the functions necessary to adapt the service offered by the physical layer to the service required by the ATM layer. In other words, the TC sublayer provides 53-byte cells to the ATM layer. All overhead functions associated with the transmission format are included.

Cell delineation is performed by the TC sublayer based on either explicit control signals or by identification of the HEC. For some physical layer standards such as SONET, the ATM cell payload must be scrambled prior to transmission and descrambled upon reception. Also included in the TC sublayer are HEC generation and verification. This is the 8-bit Cyclic Redundancy Check (CRC) that forms the fifth byte of the ATM cell header.

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ATM Physical Layers

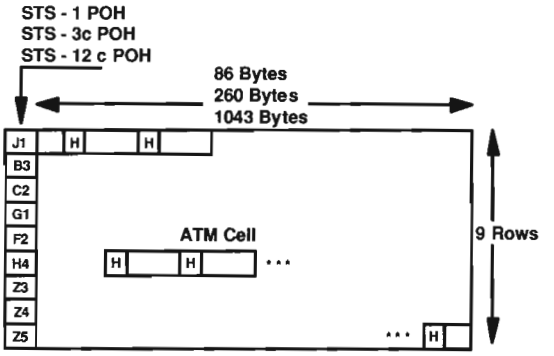
- SONET/SDH
- Asynchronous
- Block Coded

The physical layers currently defined to transport ATM cells fall into three categories: synchronous, asychronous, and block coded. The synchronous and asynchronous standards are borrowed from existing telecom transmission specifications. Block coding, such as the 100 Mbit/s, 4B/5B standard, is used in FDDI LAN applications. One of the strengths of ATM is that all switching and multiplexing is compatible via 53-byte cells, regardless of which physical layer is used to transport the cells. Physical layer compatibility is only necessary on a given physical link. For this reason, a variety of different physical layers, including some yet to be defined, may be deployed in production networks to address different price and performance requirements.

At present, most development work is directed at ATM cell mappings for various rates of the SONET/ SDH hierarchy, various asynchronous standards such as DS3 and E3, and the 100 Mbit/s block coded protocol.

Slide #11

ATM Cell Mapping — SONET/SDH

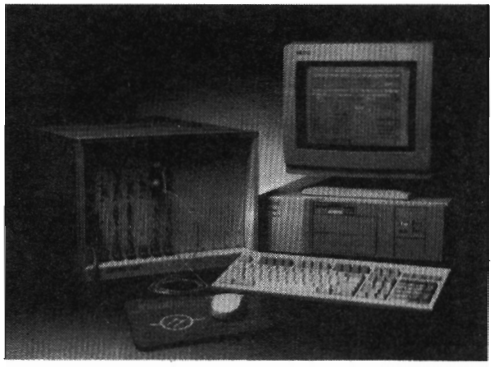


SONET (or SDH as it is referred to outside North America) is a set of international optical network interface standards enabling global network interconnection. It is expected that SONET/SDH interfaces will provide a means for attaining global interoperability in the long run for both public and private networks.

ATM cells are mapped into the Synchronous Payload Envelope (SPE) in a continuous fashion as shown. Upon termination of the SONET frame, cell boundaries are identified and delineated by observing the HEC sequence. The cell payload is scrambled to improve the efficiency of the HEC framing algorithm, as well as randomizing the data for more reliable transport.

Slide #12

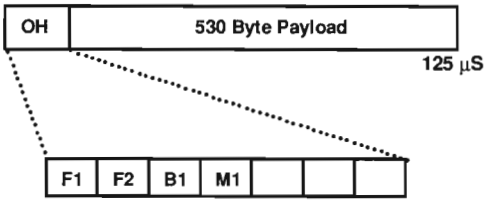
HP 75000 Series 90 ATM Analyzer



HP's ATM analyzer, shown above, can analyze ATM cell streams over a variety of physical interfaces including DS-3, SONET/SDH at 155 and 622 Mbit/s and Pure-ATM at 155 Mbit/s. Physical layer design verification can be performed to ensure that the physical transport system is capable of transmitting ATM cell streams. Physical layer tests include: exercising all of the SONET/SDH overhead functionality, all the PLCP overthead functionality within the DS-3 mapping, and physical OAM functionality within the Pure-ATM cell stream.

Slide #13

ATM Cell Mapping — E3



Although SONET/SDH is considered the preferred transport for ATM cells, it is not yet widely deployed. As a result, ATM cell mappings have been defined for the traditional Plesiochronous Digital Hierarchy (PDH) or asynchronous transmission standards. E3 is a 34.368 Mbit/s standard that is used in Europe and elsewhere. A new frame structure, shown above, is defined, whereby seven overhead bytes are followed by ten contiguous ATM cells. The cells are delineated by identifying the HEC within each cell. The cell payloads are scrambled to provide security against false cell delineation and cell payload replicating the frame alignment word.

Similar mapping has been proposed for other asynchronous and plesiochronous rates.

Slide #14

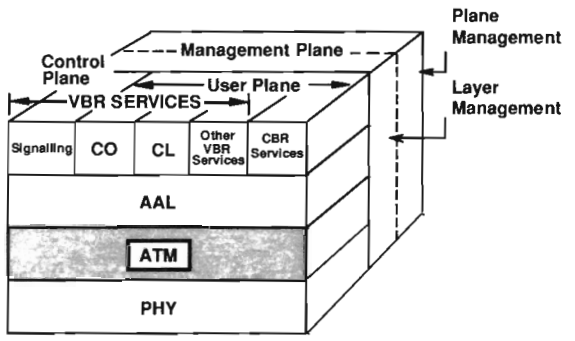
100 Mbit/s Private UNI Interface

- Less complex than SONET/SDH
- FDDI PMD Specification
- 4B/5B line coding — 125 Mbaud line rate
- Explicit asynchronous cell delineation

Since a private User-Network Interface (UNI) does not require the operations and maintenance complexity (nor the link distance provided by telecom standards, such as SONET/SDH), a LAN-like standard has been defined. The 100 Mbit/s standard is based on FDDI physical layer specifications and is intended to use multimode fiber and eventually copper. Unlike the various telecom standard cell mappings, the 100 Mbit/s interface specifies cell delineation based on explicit codes preceding each 53-byte cell. The cell transmission rate is fully asynchronous, and idle codes are sent continuously when no traffic exists. The 100 Mbit/s standard is an economical physical interface for lower performance LAN applications.

Slide #15

ATM Layer



The ATM Layer provides transparent and sequential transfer of fixed-size data units between source and destinations with an agreed upon Quality of Service (QOS) and throughput. The ATM layer is service-independent meaning that all information transfers utilize the same cell formats and procedures.

Slide #16

Functions of the ATM Layer

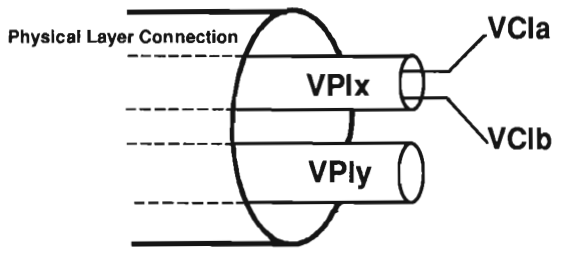
- Cell Construction
- Connection Management
- Cell Rate Adaptation
- Switching and Multiplexing
- Performance Monitoring & Network Operation
- Generic Flow Control

The functions of the ATM Layer are numerous and are categorized as follows:

1. Cell Construction
2. Connection Management
   Connection Assignment/Removal
3. Cell Rate Adaptation
   Unassigned Cell Generation/Extraction
4. Switching and Multiplexing
   Cell Reception
   Cell Header Validation
   Cell Relaying
   Cell Forwarding
   Cell Multiplexing/Demultiplexing
   Cell Copying
5. Performance Monitoring & Network Operation
   Delay Handling
   Cell Loss Priority Handling
   Usage Parameter Control
   Explicit Forward Congestion Notification
   Cell Payload Type Discrimination
6. Generic Flow control

Slide #17

ATM Networking Connection Identifiers

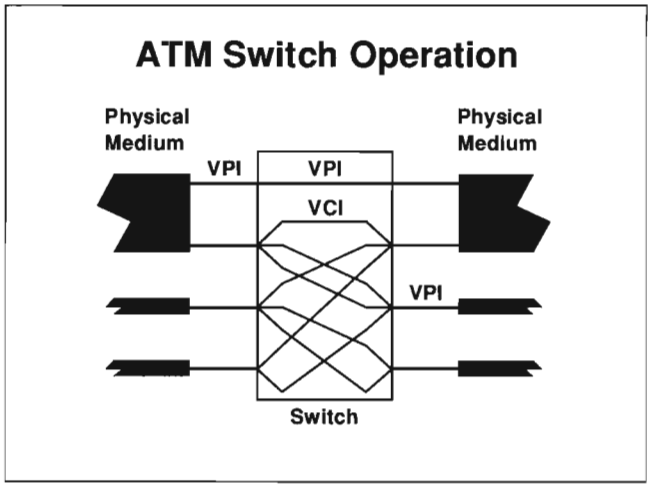


With ATM cell multiplexing, multiple information transfers may exist simultaneously on a given physical link. For this reason, it becomes necessary to distinguish between different transfers in a logical fashion.

A Virtual Channel (VC) is the basic unit of ATM switching and refers to an individual logical circuit. VCs are distinguished by a Virtual Channel Identifier (VCI), which is a routing field in the header of each cell. VCIs are defined unidirectionally on a link-by-link basis.

A Virtual Path (VP) is a logical association or bundle of VCs. The Virtual Path Identifier (VPI) field in the header of each cell is used to distinguish between different VPs.

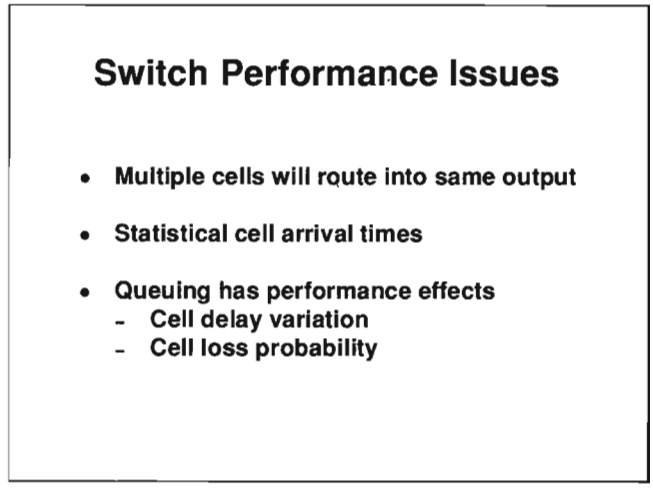
Slide #18



In ATM networking, the switching function relates cells received on every port to the destination outlet port number and VPI or VCI number. The relations between the VPI/VCI assignments for a given inlet port and the VPI/VCI assignments for each outlet port are established as part of call setup.

Switching may be performed on the basis of Virtual Paths or Virtual Channels. With Virtual Path switching, Virtual Paths are not demultiplexed; cells are routed to outlet ports based only on VPI number. With Virtual Channel switching, Virtual Paths are demultiplexed and cells are routed based on combinations of VPI and VCI numbers.

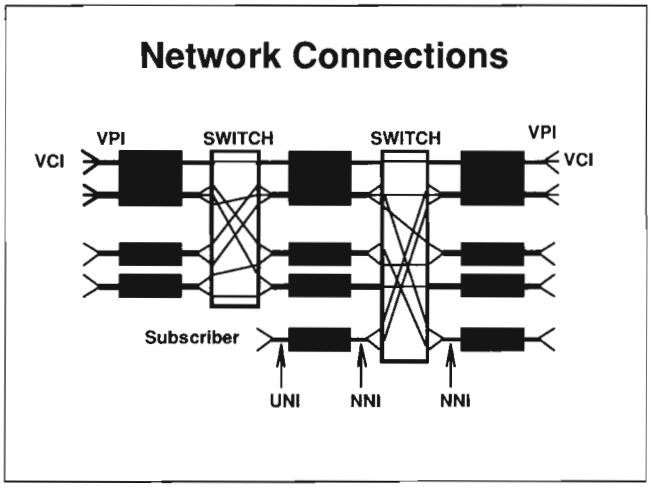
Slide #19



Since cells from multiple inlet ports may route to the same outlet port and the arrival time of all incoming cells is of a statistical nature, queuing is required to resolve the inevitable contention by multiple cells for the same outlet port. Cell queues are normally implemented in first-in first-out (FIFO) fashion and this produces two performance effects: cell delay variation and cell loss probability. Cell delay variation is a function of statistical FIFO length, while cell loss probability occurs due to FIFO overflow. In a simplistic sense, a tradeoff exists between cell delay variation and cell loss probability in an ATM switch.

Switch architects must balance traffic managment parameters, such as average cell rates, peak cell rates, and burst duration per VPI/VCI, with required cell delay variation and cell-loss probability limits for proper network operation.

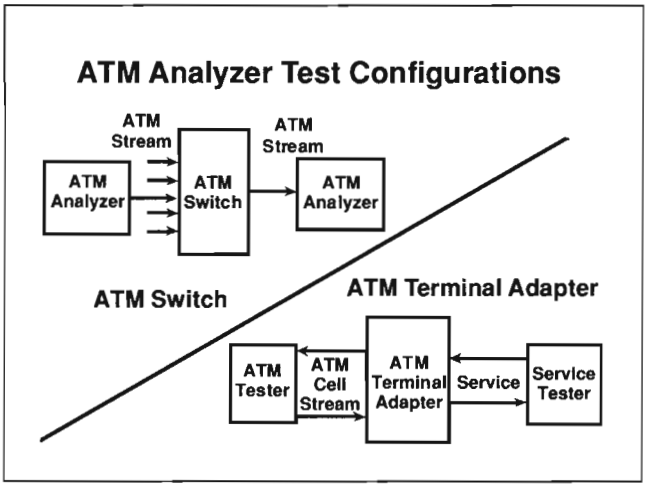
Slide #20



A Virtual Channel Connection (VCC) is an end-to-end connection formed by concatenating a series of VC links. Grade-of-Service (GOS), bandwidth, cell delay, and other traffic parameters are negotiated and allocated for each VCC.

A Virtual Path Connection (VPC) is an analogous concatenation of VP links. A VPC must sustain the GOS of the highest VCI which it contains.

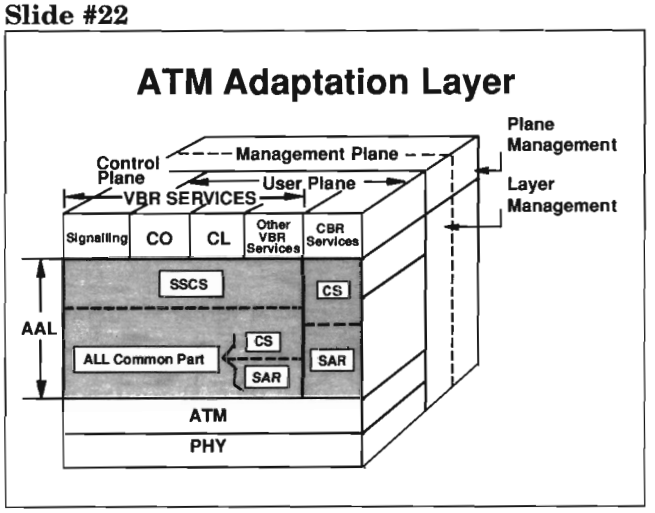
Slide #21



The ATM analyzer, a VXI-based measurement system, can be configured by its user to perform a variety of ATM design verification functions. It can be used to verify the ATM-layer functions performed by an ATM switch including: cell switching, cell performance analysis, and cell congestion evaluation. ATM Optical Load generators can be used to overload the ATM switch.

The ATM Analyzer's terminal adapter testing capabilities will be discussed later in this presentation.

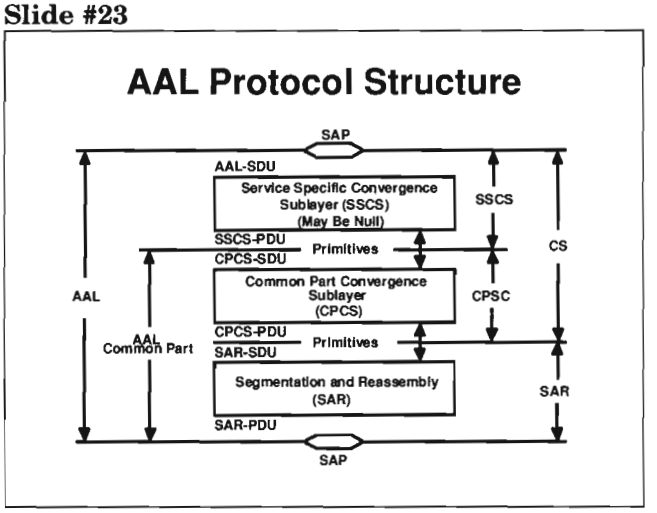
Slide #22



The ATM Adaptation Layer (AAL) defines the processes by which network terminal equipment segments user information into standard data units suitable for transport by the ATM Layer. The AAL matches diverse service requirements to the common format of an ATM cell payload. Networking efficiency is high since all types of information may utilize common resources and protocols for switching, multiplexing and physical layer mapping.

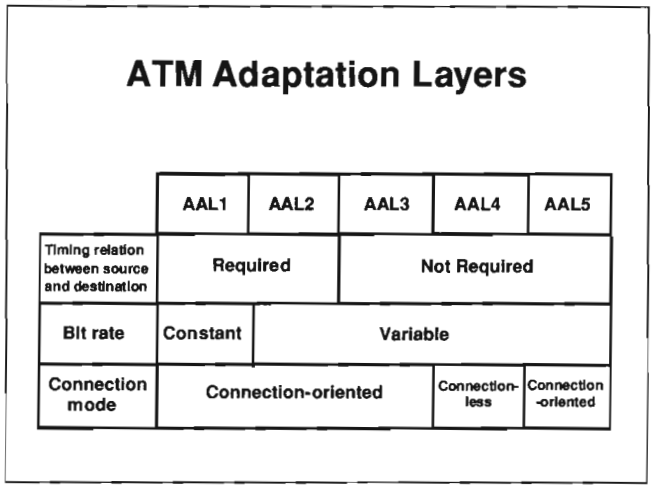
The sublayering of the AAL depends on the service; in particular, CBR and VBR services are handled separately.

Slide #23



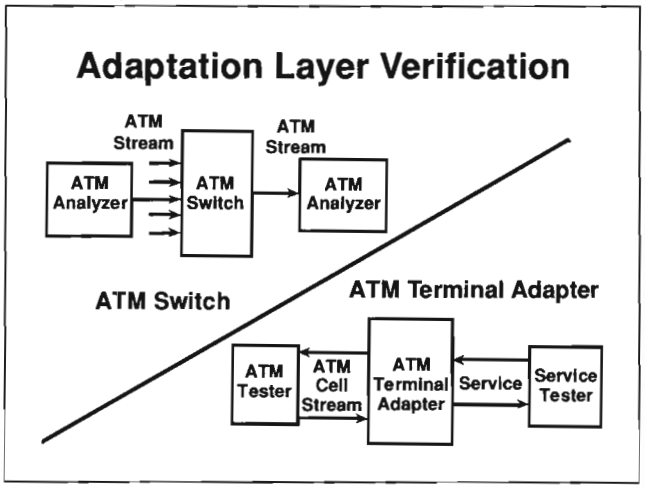
The VBR service AAL protocol structure is shown. The Service Specific Convergence Sublayer (SSCS) may optionally provide services or may be null. Services of the SSCS include assured and nonassured data transport. The CPCS sublayer converts user information of an indetermined length into standard packets or into CS-PDUs to be segmented. The SAR sublayer in turn segments CS-PDU packets into 48-byte data units which form the payload of ATM cells.

Slide #24



Multiple AALs have been defined to address various requirements as shown. AAL1 is for transfer of audio, continuous bit rate video, and other services having a constant rate related to network timing. AAL2 is used to transport variable bit rate information which has timing related to network timing. AAL3/4 is used for transport of data, MPEG compressed (bursty) video. AAL5 is an alternative data transfer methodology which has been promoted by commercial LAN interests.

Slide #25



Testing higher layer ATM protocols can be accomplished using either the HP ATM Analyzer or an HP Broadband Protocol Tester.

HP's ATM analyzer provides design verfication of the AAL type 0, type 1, type 3, type 4 and type 5 adaptation layers. Included in the test suite is functional verification of the service segmentation and reassembly process and verification of the ATM adaptation protocols.

For testing above the ATM Layer, HP will introduce the HP Broadband Protocol Tester in April, 1993. The new test system is designed to help you develop Broadband switches, network equipment and networks. This tester is also the first DUAL-PORT, Broadband tester that provides fully BI-DIRECTIONAL and REAL-TIME measurements of:

- Higher-layer Broadband protocols
- Switch performance throughput
- Conformance testing

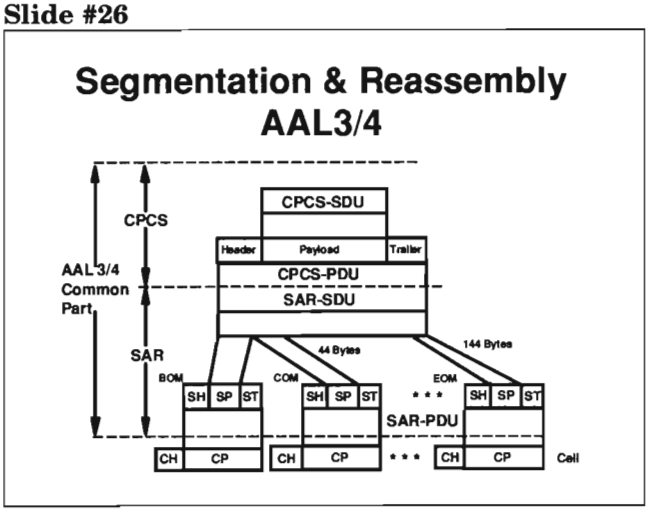
The tester also provides verification for all AAL types 3/4 and 5.

B-ISDN services testing includes:

- User network signalling (Q.93B, ATM Forum)
- Connectionless services (SMDS, CBDS, and I.cls/1.364)
- Limited test capabilities for the ATM layer and the physical layers

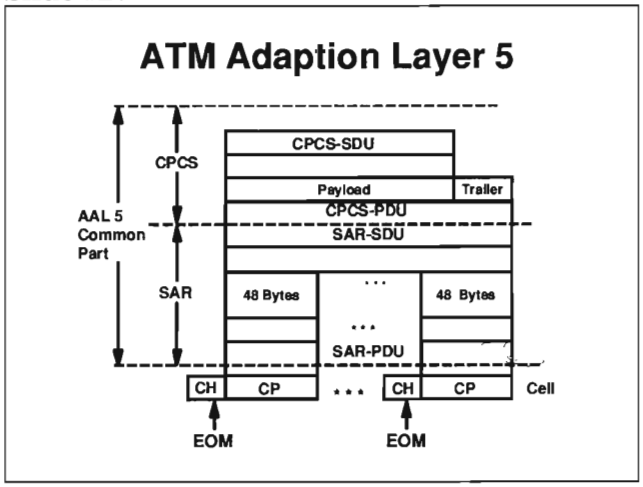
The HP B-ISDN protocol tester is packaged as either a VXI-based system or as a self-contained portable system.

Slide #26



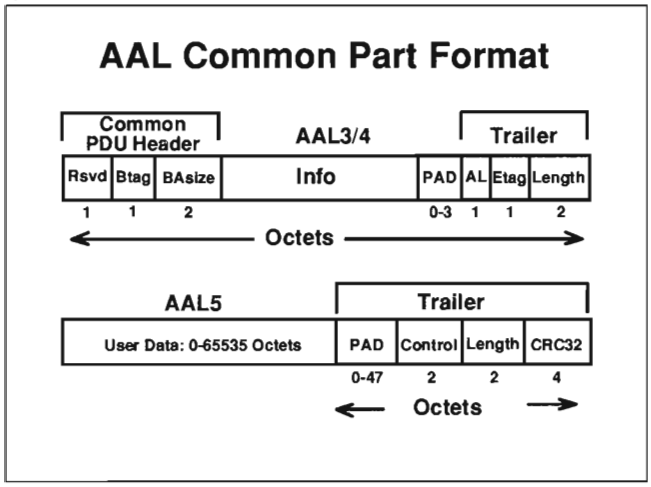
The AAL3/4 segmentation and reassembly process is illustrated. The CPCS-PDU is segmented into contiguous groups of 44 bytes. A 2-byte header and a 2-byte trailer are appended to the 44 bytes forming a SAR-PDU or ATM cell payload. The SAR header and trailer contain information relating to reassembly and cell payload error checking.

Slide #27



AAL5, which has also been referred to as Simple Efficient Adaptation Layer (SEAL), was developed by the computer and datacom community. The BISDN AAL3/4 protocol previously proposed for VBR traffic was perceived as being incomplete and inefficient for data communications. As a result, AAL5 was proposed particularly for local usage. AAL5 uses the full 48 bytes of cell payload and has no SAR-PDU header or trailer. Reassembly is based on VCI only and there is no MID field as in AAL3/4. One bit in the Payload Type field in the ATM cell header is used to distinguish between End-of-Message (EOM) cells and all others.

Slide #28



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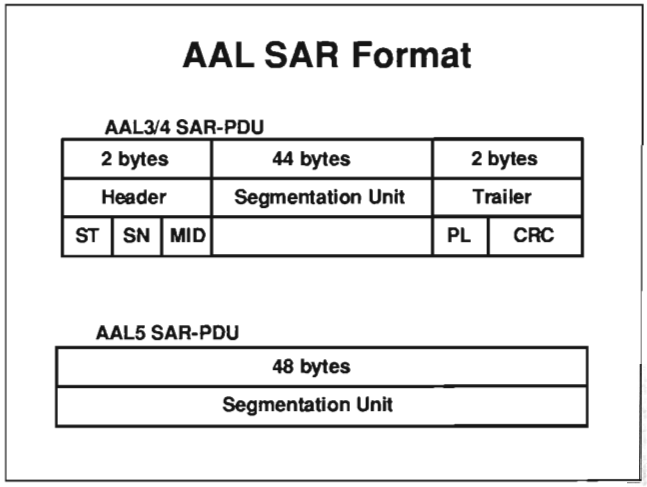

The CPCS-PDU or packet formats for AAL3/4 and AAL5 are shown above. The AAL3/4 information field is padded to a multiple of 4 bytes and bracketed by a header and trailer. Payload error checking is performed by a 10-bit CRC within each cell, not at the packet level. The BAsize field indicates the size of the packet such that upon reception of the first cell, the amount of information to follow is determined.

An AAL5 packet has no header, only a trailer. The length of the packet is not known until the final cell is sent, or is received as the case may be. Within the trailer is a 32-bit CRC covering the entire packet. There is no individual cell payload error checking or other information, which means that a full 48 bytes of payload may be used instead of only 44 in the case of AAL3/4. The packet is padded to a multiple of 48 bytes such that the AAL5 CPCS-PDU always fits exactly into an integer number of ATM cell payloads.

The SAR-PDU or cell payload for AAL3/4 contains 44 bytes of user data and the following header and trailer fields:

Segment Type . . . . . 2 bits
Sequence Number . . . . . 4 bits
Message Identifier . . . . . 10 bits
Payload Length . . . . . 6 bits
Payload CRC . . . . . 10 bits

The AAL5 SAR-PDU simply contains 48 bytes of user data.

Slide #30

TranSwitch ATM Components

- Physical layer: SONET/SDH, E3, DS3, etc.
  - Framers
  - Overhead terminators
  - Multiplexing & mapping functions
  - Transceivers
- ATM layer
  - Cell delineation/mapping
- ATM adaptation layer
  - Segmentation & reassembly controllers

TranSwitch designs and produces VLSI components for advanced telecom and datacom applications. A full family of physical layer devices are available for SONET/SDH, E3, and DS3 and all may be used in ATM applications. Cell delineation functions which implement transmission convergence and ATM layer functionality have been developed and a high performance AAL controller (SARA Chipset) which supports AAL3/4, AAL5, and CBR traffic at rates up to 155 Mbit/s is in production now. Evaluation boards, user documentation, and applications support are available for all devices.

TranSwitch's products may be configured in a variety of architectures to realize standards-based terminal, LAN, transmission, and switching applications. Such products can significantly reduce the development cost as well as the time-to-market for new system products, and allow system manufactures to concentrate on additional value added functionality above the defined ATM standards.

Slide #31

Deployment Trends

- LAN internetworking — mostly data
- Cell switching vs. shared media
- Variety of physical layers
- Wide area access will develop more slowly

At present, the focus for near-term ATM deployment is on LAN internetworking or backbone applications. Initially, ATM is expected to be competitive with FDDI on a price and performance basis and be deployed in similar networking environments. The switching capabilities of ATM will be used to improve the performance, scaleability, and management of private, local, and campus networks. In particular it is the switching characteristics which distinguish ATM from existing shared media LAN technologies. A variety of physical layers will be deployed to address varying price/performance requirements, while maintaining compatibility at the cell level for switching and multiplexing. Public wide-area network access will grow over time, although it will not be ubiquitous for many years.

Slide #32

Summary

- ATM is being driven by internetworking
- Deployment will enable new applications
- Strong standards support
- No real technology alternatives
- New design verification challenges

ATM is a new networking technology which is suitable for all types of information and is based on international standards. A strong commercial focus is accelerating standardization and deployment of initial systems. ATM has been selected as the underlying transport technology for BISDN and is expected to eventually be widely deployed in private and public networks around the world. Designers and developers can derive significant utility from tools which can recognize and verify ATM protocols.

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References

- CCITT
- ATM Forum
- IEEE

CCITT

I.113: Vocabulary of Terms for Broadband Aspects of ISDN
I.121: Broadband Aspects of ISDN
I.150: B-ISDN Asynchronous Transfer Mode Functional Characteristics
I.211: B-ISDN Service Aspects
I.311: B-ISDN General Network Aspects
I.321: B-ISDN Protocol Reference Model and its Applications
I.327: B-ISDN Functional Architecture
I.361: B-ISDN ATM Layer Specification
I.362: B-ISDN ATM Adaptation Layer (AAL) Functional Description
I.363: B-ISDN ATM Adaptation Layer (AAL) Specification
I.413: B-ISDN User-Network Interface
I.432: B-ISDN User-Network Interface - Physical Layer Specification
I.610: OAM Principles of the B-ISDN Access

ATM Forum

ATM User-Network Interface Specification

IEEE

IEEE 802.6: Distributed Queue Dual Bus Subnetwork of a Metropolitan Area Network

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References (Cont.)

- ANSI
- Bellcore

ANSI

T1S1.5/92-001 AAL SSCOP Baseline Document
T1.ATM-199X ATM Layer Functionality and Specification
T1.AL4-199X AAL 3/4 Common Part
T1.CBR-199X AAL for Constant Bit Rate Services Functionality and Services
T1S1.5/92-005 Connectionless Service Layer Functionality and Services
T1S1.5/92-010 AAL5 Common Part Functionality and Services
T1S1.5/92-111 Constant Bit Rate AAL Architecture

Bellcore

TR-TSY-000772: Generic Requirements in Support of Switched Multi-Megabit Data Service
TR-TSY-000773: Local Access Switching System Generic Requirements in Support of SMDS
FA-NWT-001109: Broadband ISDN Transport Network Elements Framework Generic Criteria
FA-NWT-001110: Broadband ISDN Switching System Framework Generic Criteria
FA-NWT-001111: Broadband ISDN Access Signalling Framework Generic Criteria for Class II equipment
TA-NWT-001112: Broadband-ISDN Used to Network Interface and Network Node Interface Physical Layer Generic Criteria
TA-NWT-001113: Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols Generic Requirements
SR-NWT-001763: Preliminary Report on Broadband ISDN Transfer Protocols

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Recommended Resources

- Equipment and Accessories
  - HP 75000 Series 90 ATM Analyzer
  - HP Eclipse Protocol Analyzer
- Other Resources
  - HP's BISDN Seminar
  - TranSwitch's ATM Technology and Applications Seminar

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