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Alternatives for Data Transfer in High-Speed Systems

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Abstract

PEP Modular Computers has been designing VME systems since the early 1980s, specializing in the design of compact solutions for a wide range of market segments. These compact solutions use 3U VME (single height Eurocard) style boards and therefore suffer from relatively slow data transfer capability, fundamentally due to the limited size of the data and address busses. Recent enhancements to the VMEbus specification (Revision D) have boosted the data transfer capability from about 20 Mbytes/s to 40 Mbytes/s. However as performance expectations of systems increase, even this significant improvement cannot avoid the fact that backplane connection still represents a bottleneck in many designs. The tremendous performance growth of CPUs and other system components, along with ever increasing customer expectations, can be held primarily responsible for this view.

Design activities to enhance the data transfer capability over the parallel bus soon started to show the physical limitations of increasing operating frequencies. This paper looks at the way the problem was overcome and how it lead to the birth of a new chipset which offers considerable potential for the future.

Authors

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Current Activities:
Josef Kreidl is president and major owner of PEP Modular Computers, the leading 3U VMEbus manufacturer for high quality industrial, medical, aerospace and telecommunication applications worldwide.

Author Background:
Josef was born in Innsbruck, Austria and studied electrical engineering at HTL Innsbruck. From 1970 - 1975, he was a design engineer at Olympia and Telefunken. In 1975, he founded PEP.

Gunter Rucker

Current Activities:
Gunter Rucker is technical director and part owner of PEP Modular Computers and is responsible for all VME designs and the AUTOBAHN transceiver chip.

Author Background:
Gunter studied electrical engineering at the Technical University of Augsburg. From 1968 - 1982, he was a design engineer at Olympia and a department manager at MBB. In 1982, he joined PEP Modular Computers.

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Robert Kraus is an engineering manager responsible for Logic Integrated Circuits in Europe. A key area is the development and design of new products for communications and computer peripheral applications.

Author Background:
Robert was born in Munich, Germany and studied communication engineering at FH Muncih. He started with Motorola in 1985 as a design engineer, developing a precision AC test simulator for integrated circuits.

Andreas Gunther

Current Activities:
Andreas Gunther is a product engineer at Motorola and is responsible for the development and application of parallel bus interface IC and microprocessor support IC.

Author Background:
Andreas was born in Brehna, Germany. He studied physics and electronics and graduated from the Technical University Chemnitz in Germany.

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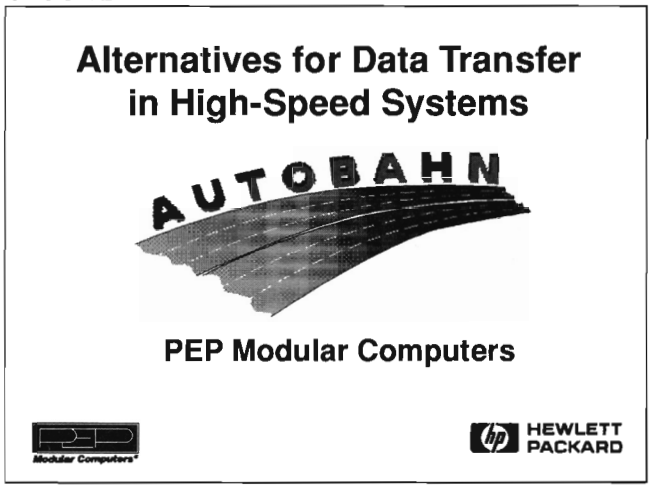

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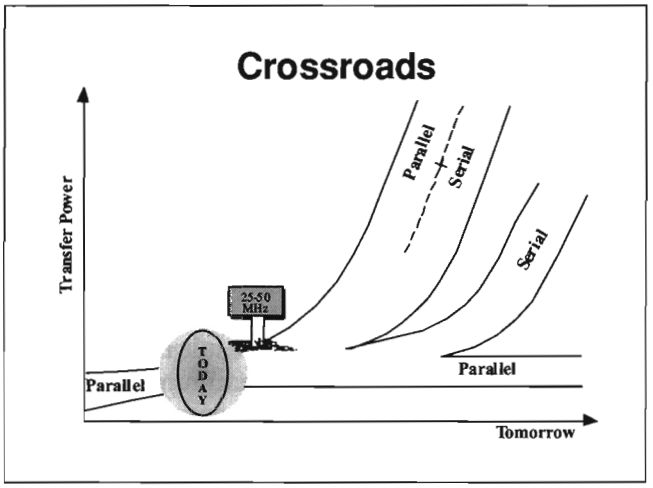

As system performance expectations increase, so must the performance of the technologies used to achieve the increase. In particular, the methods and technologies used to transfer data within digital systems have experienced continual enhancement to achieve higher and higher data throughput rates. However, something of a crossroads has now been reached, where major electrical and physical limitations threaten this continual improvement. As the 25 to 30 MHz data rate boundary is crossed, new techniques become essential, but more importantly, new technologies become viable options for the performance systems of the future.

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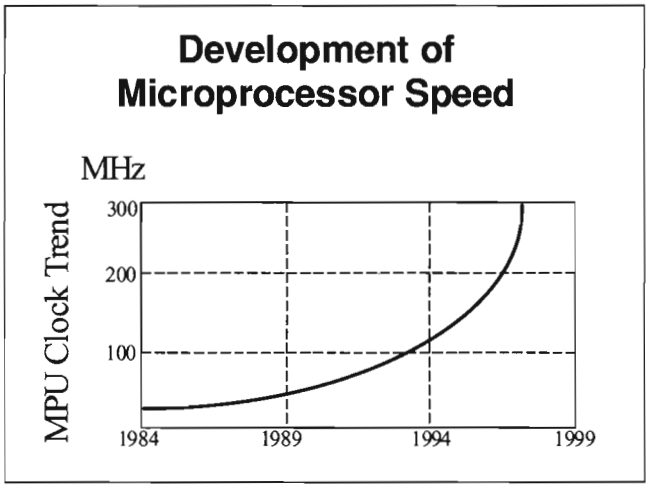

With the performance of modern microprocessor-based systems increasing rapidly, designers are able to realize more and more sophisticated and complex applications. Real-time processing, high-resolution imaging, and powerful parallel processing are all more easily achievable.

All these systems have one thing in common: the need to move data around the system extremely quickly. In practice, it is this need that effectively limits the performance of the system. It is common to all systems, whether that is a single-board computer or a multiprocessor design employing a proprietary or standard backplane. These inherent limitations have their roots in the analog world of complex interaction between conventional semiconductor technologies and the effects of the PC board they are mounted on.

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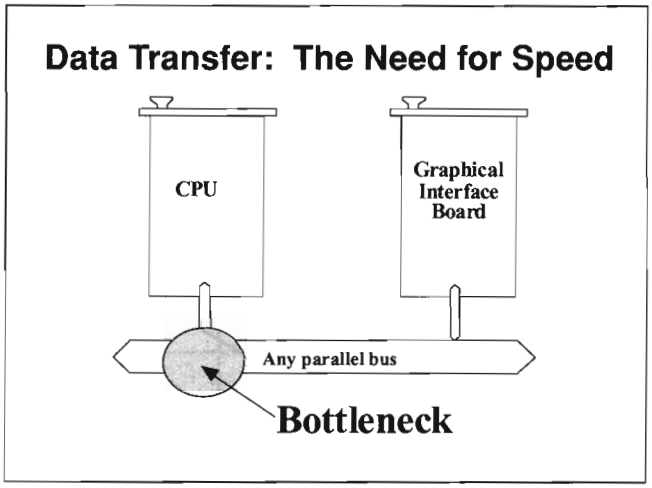

Consider a bus-oriented graphics application, where a central processor interfaces to a graphics processing board via a backplane connection. For normal operation, transfer rates in the region of 160 MByte/s between the CPU and the graphics card would be needed. For an HDTV application, this requirement could be much higher.

This level of data throughput clearly cannot be achieved because a typical 32-bit bus system, such as that employed in a VME or MULTIBUS II system, delivers a maximum of 80 MByte/s when running at 20 MHz.

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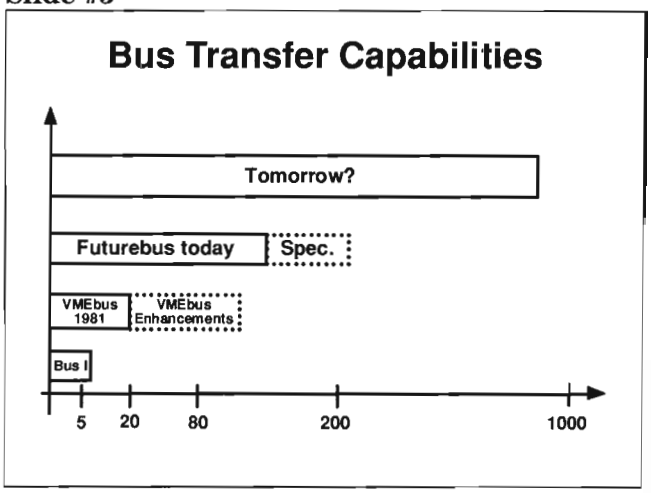

The flexibility and versatility of parallel data transfer in multiple card systems made it the preferred choice for virtually all microprocessor applications, ranging from conventional PC systems to industry-standard backplanes, such as VME and Futurebus. However, as stated, data transfer rates are somewhat limited and increasingly fail to meet the design engineer's data throughput requirements. Therefore, conventional backplanes oftentimes become the main performance bottleneck for high-performance systems.

Enhancements to the standard backplane, such as that of FutureBus and VME, result in performance gains and increased maximum transfer rates. Typically however, these improvements, while useful, have been fairly modest. Early 8- and 16-bit buses allowed maximum transfer rates of only about 20 MByte/s. The latest VME enhancements allow transfer rates of up to 80 MByte/s. Today, FutureBus+ operation is specified at up to 160 MByte/s transfer rates, by using 64 data lines. However, this leads to a significant increase in the physical size of the system and the possibility of increased electrical problems due to the high toggle frequencies.

To achieve the high data rates that will be required for tomorrow's systems, two or possibly three times the performance of currently available systems will be a minimum requirement.

Slide #6

Backplanes vs. "PCB" Buses

- Backplanes run into problems at 20-25 MHz
- PCB boards show the same problems — just at higher frequencies

A typical parallel backplane design starts to experience signal integrity problems where clock rates break the 20 MHz barrier. This is approximately 10 to 20 MHz below the frequency at which severe signal integrity problems start to occur on a conventional PC board. This occurs because a backplane typically represents a more complex electrical environment, with many more discontinuities and longer signal paths. However, these same problems start to become more evident in all systems as clock rates rise and signal rise times reduce. Current high-end systems employing standard processors with clock rates around 66 MHz have already moved into the area where problems start to occur.

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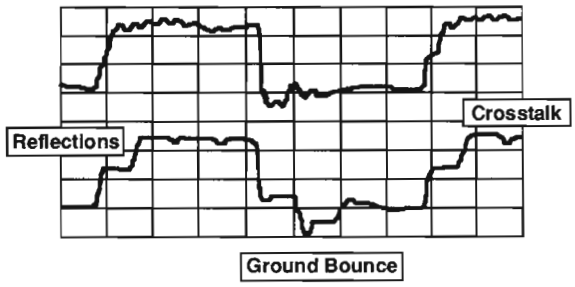
Signal Distortions in Real Systems



The root causes of poor signal integrity in high-speed systems are well known. Reflections, ground bounce, and signal crosstalk all contribute to the effect. The manifestation of these effects can be unreliable system behaviour or poor EMC/EMI performance. Analysing the mechanisms by which these problems arise reveal complex interaction between all system components, including semiconductor packages, connectors, cabling, and the PC trace itself. With increasing frequency and bus width, these intrinsic effects come to dominate the attention of the design engineer.

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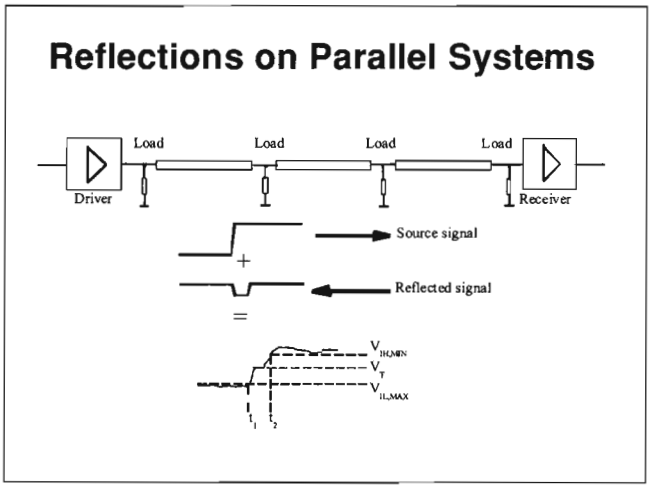

Reflections occur on any line that is not properly matched or terminated. In reality, it is never possible to achieve a perfect transmission line in a multipoint backplane environment. Every connector represents an additional electrical load and discontinuity. The larger the backplane, the more connections are present, and therefore, the more sources of reflection.

A typical example is shown above where the limited drive capability of standard TTL and CMOS devices can never achieve a stable -high+ condition at the initial transition. In order to establish a stable signal, a certain delay time must be allowed so that all reflections can settle. If this delay is not taken into account, the undefined state between t1 and t2, exactly around the switching threshold for standard TTL or CMOS, may result in metastability or incorrect switching of subsequent stages. This need for a settling period is, of course, directly proportional to the speed of the system and to the environment of faster operation. The more loads added to a backplane system, the more settling time is stretched, thus limiting the performance. Potential solutions utilise powerful bus drivers with low output impedance. However, the required drive current is becoming beyond the capabilities of standard logic bus devices and the total power requirement of a wide 32- or 64-bit bus would be prohibitive.

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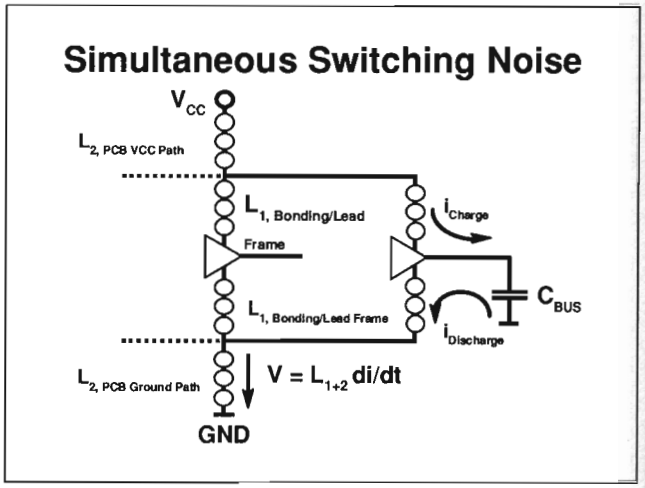

Most EMI/EMC problems are directly attributable to simultaneous switching noise, or ground bounce. IC technologies have migrated towards faster and faster risetimes, driven by system design requirements toward higher speed to achieve more powerful microprocessor systems. However, the package evolution did not follow this technology trend. In most cases, the standard IC package is still the DIL (Dual In Line) package or surface mount SOIC (small outline) package. These packages, in particular, suffer from relatively high inductive load per pin, mainly due to the length of the bondwire inside the package. The consequences can be easily seen by referring to the following basic equation,

$$v = L\, di/dt\,,$$

where L is the inductance and di/dt is the rate of change of current.

It can easily be seen that as system risetimes decrease (dt) even small values of bondwire inductance could potentially lead to very large voltage spikes. For example, the high ioL current of buffered outputs simultaneously switching can lift the GND level to cause the output to change state. As predicted, this effect gets worse with signal risetime, and with technologies, such as CMOS, that employ full GND-to-VCC and VCC-to-GND output transitions. This becomes the single most critical signal integrity problem in the system.

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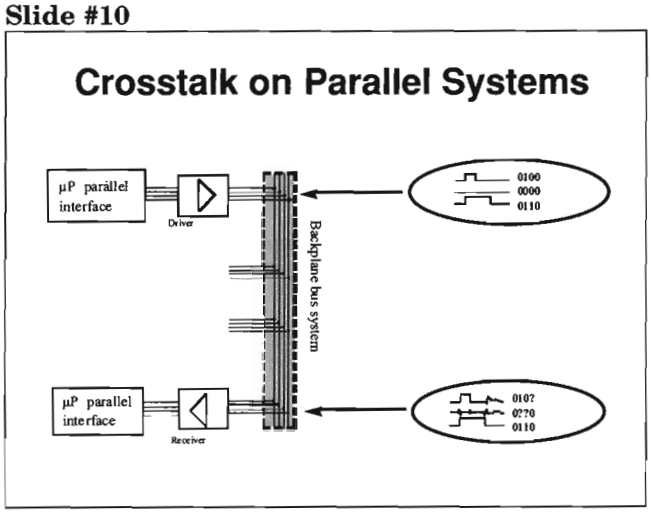

Crosstalk is the electrical coupling of signals between one trace and another and occurs wherever signals are routed in close proximity to one another. Between two lines on a PC board there exists a coupling capacitance and a mutual inductance, through which electrical energy is exchanged. The size of these inductance and capacitance values depends on the geometry chosen for the board layout and the trace spacing employed. Large parallel buses are especially susceptible to crosstalk problems, with complex coupling impedances present. CMOS inputs are very sensitive to crosstalk effects because of their high input impedance. Even small amounts of coupled energy from an active parallel line can build up a critical parasitic signal that could cross the switching threshold and could cause the device to toggle. This kind of bit error can only be detected by comparing the original source signal to the received signal. The failure rate received within a given time interval — the Bit Error Rate (BER) — provides an invaluable guide to the degradation of performance in any bus system.

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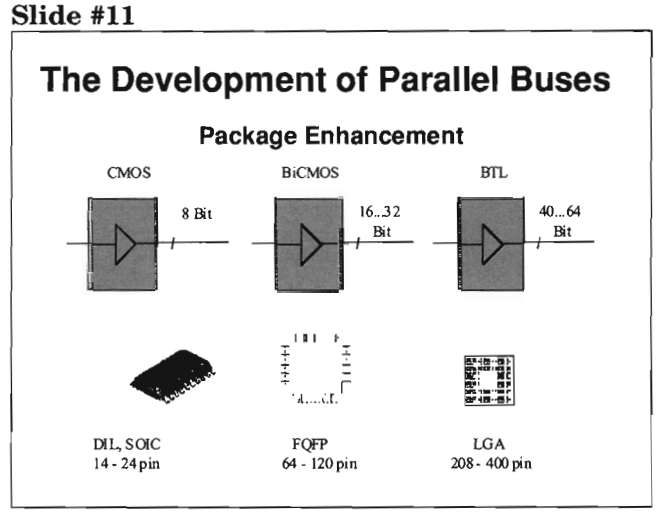

Because there is no complete alternative to parallel buses in most microcomputer systems, IC manufacturers are being challenged to develop enhanced products more robust against this type of disturbance. Although these signal integrity problems can never be fully eliminated on parallel buses, there are ways to at least reduce their impact and thus extend the maximum performance of the system.

For the IC manufacturer, one of the most important areas to improve is the device packaging itself. Recalling that simultaneous switching noise is the single most important signal integrity problem, a significant performance gain can be realized by reducing the VCC and GND pin inductance, formed by the bondwire. This can be done by increasing the number of supply pins or minimizing the interaction between different output buffers on the same chip. Using a square outline package can also help, as these have short, uniform length bondwires, which minimize the inductive effects and help to maintain balanced propagation delay times, even on wide output buffers.

A useful side effect of using a square package is that flat packages have much lower thermal resistance which helps to reduce the power dissipation problems that are also a feature of any high-speed bus application.

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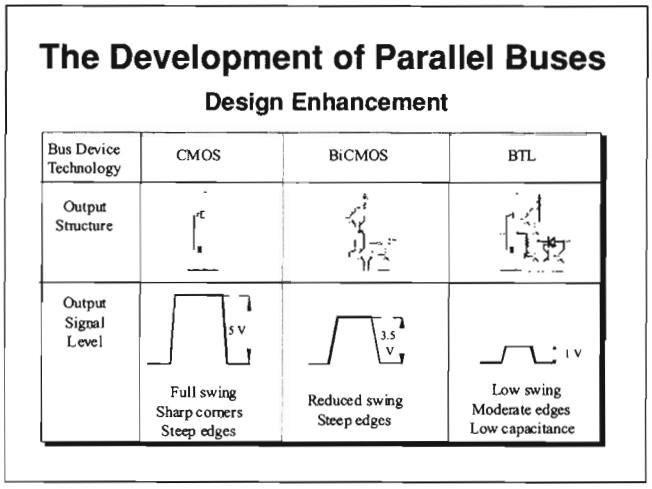

Beyond packaging the IC, design and process technology can help to minimize parasitic effects. CMOS is most used for its economic power consumption, bipolar technology for its drive capability. Combining the two yields BiCMOS, where CMOS technology is used internally and output buffers are created using powerful bipolar transistors. Ideally, both advanced packaging and chip technology are used to achieve maximum performance. An example here would be the ALExISTM (Advanced Low Power EXpandable Interface Solution) product line from Motorola, that offers 16- to 20-bit-wide bus interfaces and transceivers in BiCMOS housed in a 64-pin Fine Pitch Quad Flatpack. A development of this will be BTL (Bus Transceiver Logic). As well as employing BiCMOS technology, this family also uses reduced voltage swing open collector outputs. These outputs also include a serial diode that significantly reduces capacitive load of disabled outputs, thus reducing excessive peaks of charge and discharge currents.

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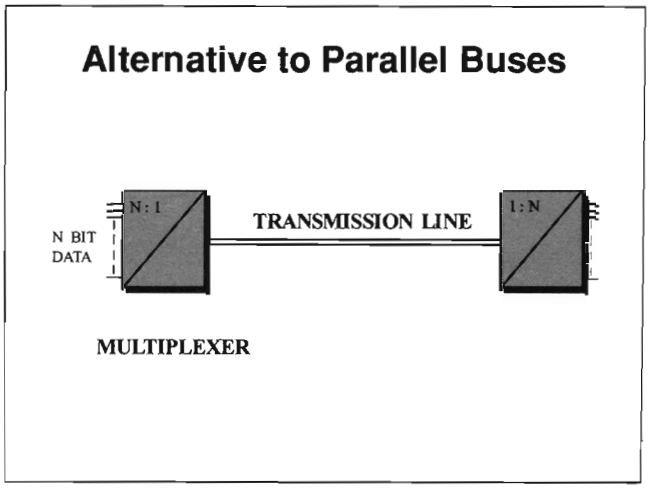
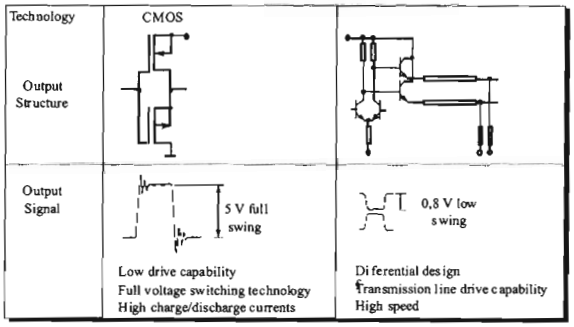


State-of-the-art process and package technologies may help to extend date rates to the 50 to 100 MByte/s range, which is a considerable improvement. However, there are physical limits to a backplane and any other parallel system that simply cannot be overcome.

Today's microprocessor systems use 16- or 32-bit-wide buses for data transfer, that result in a considerable board space requirement and the burden of the undesirable parasitic effects causing the signal integrity to deteriorate. These problems increase with speed and line length. Simply said, the more lines being used, the more problems to cope with. One alternative, and hardly a new one at that, is to employ serial data transmission, the premise being that it is easier to control the signal integrity of a single line than it is for a parallel bus. Obviously, it is an attractive solution, but one which brings with it a new dimension of ultra-high speed. Converting a 200 MByte/s signal (32 bit x 50 MBit/s NRZ parallel bus) results in a serial data stream of 1.6 GBit/s, equivalent to a frequency of 800 MHz on the serial line. This is completely out the range of any standard TTL, CMOS or BiCMOS technology, requiring a completely different approach.

Slide #14

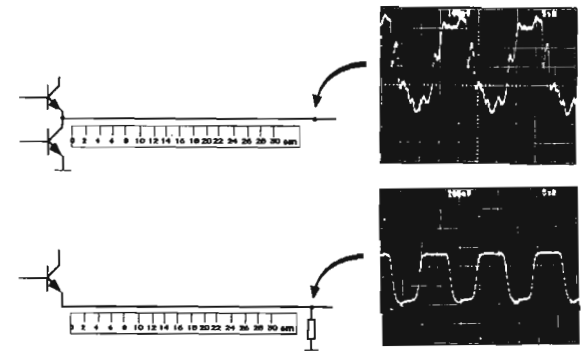
ECL vs. CMOS Output Structures



An enabling technology for these high frequencies is ECL. Here, a basically bipolar technology is used with a different circuit design, so that the output transistors are not switching type but are biased to operate in their linear range. This concept allows maximum switching speed of the transistor limited only by its cut-off frequency. In addition, ECL outputs can operate in differential mode, with output voltage swings of only 0.8 V, that guarantees excellent noise immunity to disturbances of the board environment and vice-versa. This is further supported by the fact that with such low impedance, ECL outputs can drive true terminated transmission lines with 50-ohm impedance, an ideal environment for high-frequency transmission.

Slide #15

An Alternative Solution: ECL



The theoretical benefits of ECL are proven in real-world systems. With their fast on/off switching speed, conventional TTL/CMOS outputs contain very large high-frequency content, reaching well into the RF range. At the same time, uncontrolled impedances around the board cause reflections which heavily disturb the signal. As can be seen in the example above, a 25-MHz signal is routed around a board and after only 25 to 30 cm, a realistic distance for many PC boards and most backplanes, it is already badly corrupted and possibly unacceptable for the reliable operation of subsequent stages. Compare this to the superior performance of an ECL driven line. Even at 10 times the clock rate and 3 times the distance, the signal integrity is good. While the bit rate of this signal is very high, the reduced voltage swing technology means that it exhibits negligible RF emissions to the environment.

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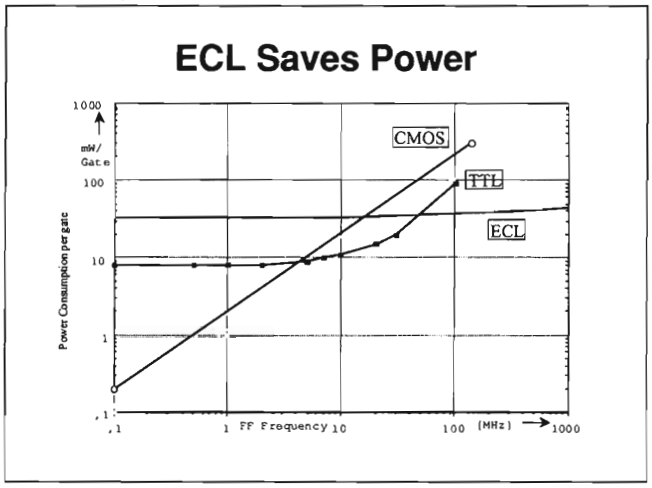

A historical concern of ECL has been its power consumption. Comparing ECL with CMOS and TTL structures, this is a valid concern at low frequencies. Under all conditions, the ECL transistors are biased, leading to relatively constant supply current requirement. CMOS devices however, with their complementary transistor structure, have a very low power consumption at low operating frequencies.

This picture changes drastically with frequency: CMOS transistors always switching full swing outputs have to completely charge and discharge all internal and external capacitors at every cycle, thus leading to a linear increase in the power consumption. Bipolar type TTL structures look somewhat better at certain frequencies; however, the switching output transistors also lead to excessive power drain beyond certain frequencies. This frequency is technology-dependent, but in the range around 30 to 70 MHz. This is not the case for ECL, where the output transistors are not actually switching rather just modulating around a bias point, the power consumption is very nearly constant over the operating range of the device. Depending on the individual application, the breakeven point in power drain occurs at around 30 to 40 MHz. Beyond that, ECL can dominate.

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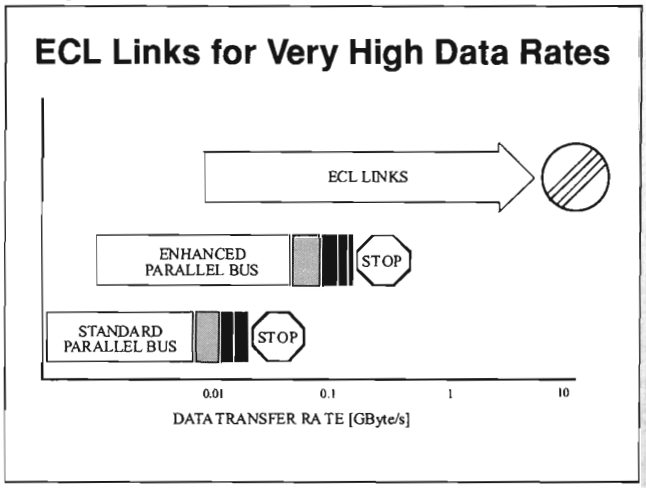

Looking at the best solutions for realizing data transmission, there is a scale of economy for both the parallel as well as the serial concept. Parallel buses at clock frequencies up to 60 to 80 MHz and further will be the first choice for bridging short on-board data exchange between microprocessor and peripherals. Serial, high-speed links will be used where maximum data throughput is required or longer distances are to be bridged such as board-to-board or board-to-external peripheral. There may be future supercomputers where the serial concept will be the most efficient solution, even on-board.

Latest ECL processes have cutoff frequencies of 25 GHz, such as Motorola's MOSAIC V technology (0.7 um, four layer bipolar; Motorola Oxide Self Aligned IC), which currently allows data rates of 10 GBit/s and beyond. Applications requiring such ultimate performance already exist today for example, real-time, high-resolution image processing, crosspoint switches for telecommunication PBX systems, and any type of large parallel processing system.

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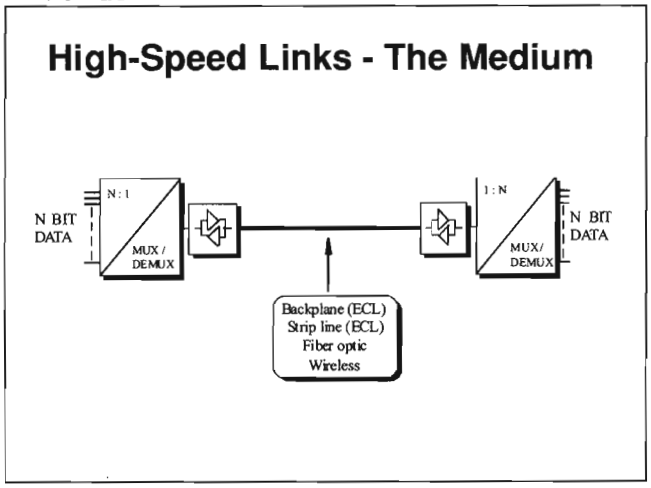

Once parallel data words are multiplexed into a high-speed serial data stream, some considerations are required on how to transport it, as its effective frequency may reach some 100 MHz to 2 GHz. With differential ECL, data transmission over distances of 0.5 to 1 m can be achieved on backplanes and PC boards as long good transmission lines are maintained. Even considering the additional components required for MUX/DEMUX functions, the serial link offers a good alternative for wide parallel multipoint or point-to- point connections through crowded, densely populated microcomputer boards. For longer distances, fibre optic links or wireless transmission is the recommended medium, where the multiplexed serial data could be fed directly into a laser driver or RF modulator.

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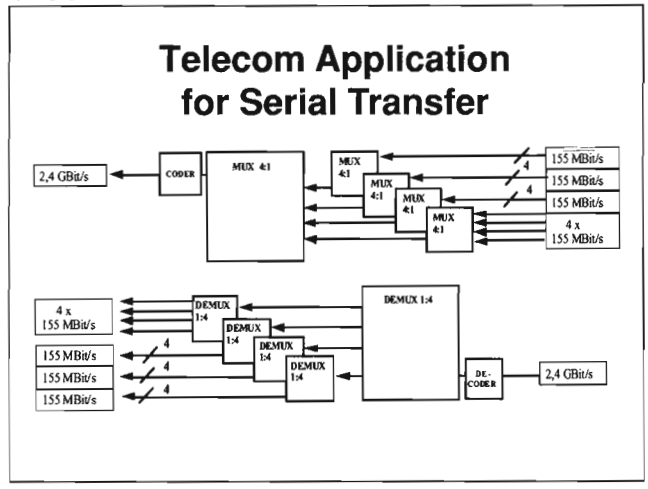
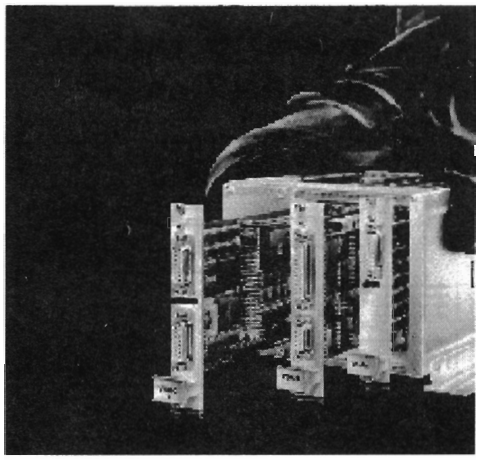


Independent of the application—Telecom Switching Systems, HDTV, Video conferencing and digital mobile phone systems, such as GSM and DECT—international standards in Europe and USA have defined standard platforms to enable the different systems using common transmission channels to interface to each other. These standards named SDH (Synchronous Digital Hierarchy) in Europe and SONET (Synchronous Optical Network) in the USA are compatible on certain layers having fixed data rates:

Example:	STM-1	155 MBit/s	OC - 3
	STM-4	622 MBit/s	OC - 12
	STM-16	2.480 MBit/s	OC - 48
	STM-64	9.952 MBit/s	

These standards are based on multiplexing parallel data through several layers, utilizing high-density fibre optic links for transmission, allowing powerful and highly efficient data links to be realized using latest technologies in all stages of the system.

Slide #20



PEP Single Height

Since 1975, PEP has produced modular microcomputer systems for a wide range of applications based on the small, single-height DIN form factor, using one single 96-pin connector. This allows a very compact and efficient design of complex high quality systems.

Through tremendous performance increases in the PEP product range throughout the 1980s, the parallel bus became the bottleneck. Many applications could not be solved this way. Very early on, we had to accept that the frequency increase of the parallel bus had physical limitations, for example, no solution.

Therefore, as many other companies, PEP was investigating resolving the problem with a specialized proprietary parallel bus. This would lead to a non-standard solution, with increased costs and power consumption. Many companies worldwide spent hundreds of man-years to develop such proprietary busses to meet their requirements. PEP was looking for a solution within the standard. The alternative solution was to combine the parallel bus, with an ultra-high-speed serial link, utilizing all advantages of either transfer method.

Alternative	Result
Proprietary Parallel Bus	Non-standard High costs, high power consumption
Combination of Serial and Parallel Busses	Standard Fully compatible, cost effective, easy implementation

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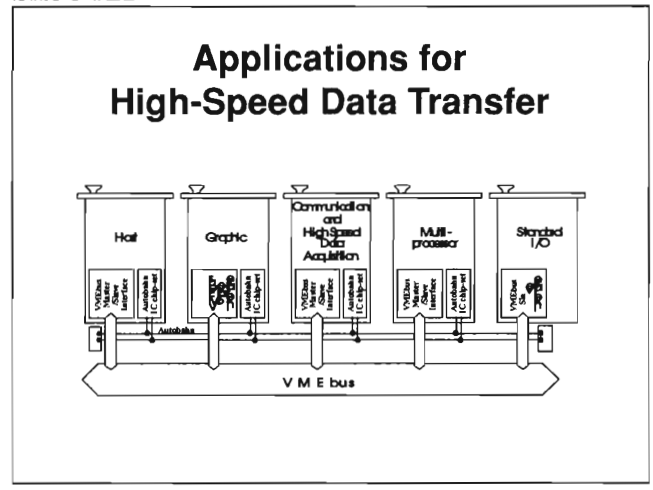

This block diagram of a VMEbus system shows some typical applications where high-speed data transfers are needed between different components on the bus.

Graphics and Vision Systems

A single picture in color or printing quality format requires several MBytes of digitized data. In most graphics and vision system applications, numerous pictures/sec must be processed or displayed. This results in data transfer rates of 100 to 200 MByte/s between graphic and camera boards, as well as other system functions, like CPU or communications boards.

Multiprocessing - Parallel Processing

Due to the increasing power of microprocessors and to the use of several microprocessors on a single VME board, the amount of processed data found on a VMEbus board has grown enormously. Therefore, transfer rates between different CPU boards and other system functions also range from 100 MByte/s and upward.

Communications - High-Speed Data Acquisition

New high-speed communication links and data acquisition methods operate in bandwidth ranges of 100 Mbit/s to several Gbit/s. This amount of data must first be linked to a standard board on a VMEbus system, then transferred on the bus to another system function (CPU). This leads to bus transfer needs of hundreds of MByte/s. Typical high-speed applications are DAT, HDTV, FDDI, and so forth. In communications, logic analyzers and high-end research applications (such as super-colliders) require extremely high bandwidths for bus systems.

All of these application examples identify existing parallel bus structures as the throughput bottleneck of the system.

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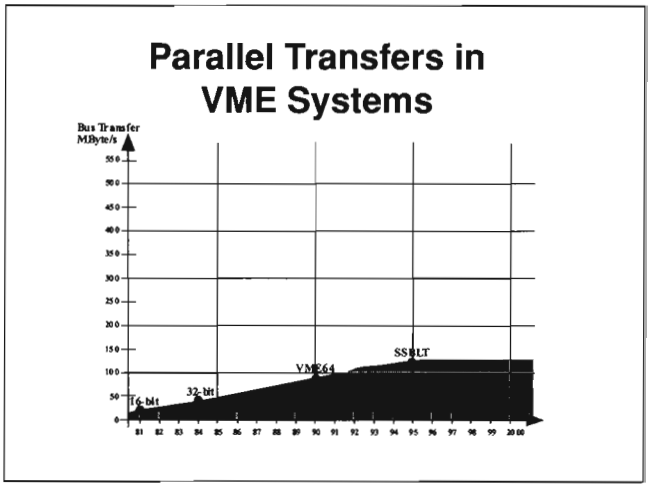


For a VME or any other standard backplane manufacturer or user, a key requirement of any design is its use of the standard interface. In the case of VME, enhancements to this interface have led to steady performance improvement. But none could really offer the ultimate performance requirement because of the constraints of standardization. Changes to the specification allow a system standard function to change but this process can be slow. Employing new technologies, such as the Motorola BTL (Bus Transceiver Logic) can offer significant improvement; but again, this path leads away from standardization and can potentially lead to significant cost issues.

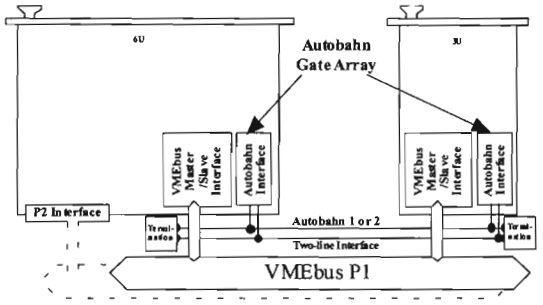
Slide #23

AUTOBAHN Concept

These constraints led to a different approach to the problem, from which the Autobahn concept emerged. The standardization issues of VME could be avoided by using parts of the system not defined in the VMEbus specification. The possibility of two spare backplane pins was of course known; thus, the idea of using them for serial data transfer between compatible boards became reality. The main benefit of this approach was that the defined parallel system remained unaltered, and hence the serial interface promised performance in addition to that already available.

Slide #24

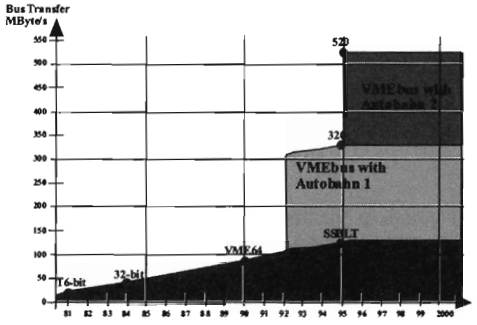
Implementation



In concept, the implementation was very straightforward with the inclusion of MUX/DEMUX capability on any board wishing to utilize the additional interface. However, the concept was complicated because to achieve the required data throughput of 32-bits at 50 MHz, a maximum frequency of 900 MHz on the backplane serial line would be required. However, the potential benefits of such a system justified the development investment.

Slide #25

Combination Serial/Parallel Transfers



The future solution is combining parallel transfers with ultra-high-speed serial data links.

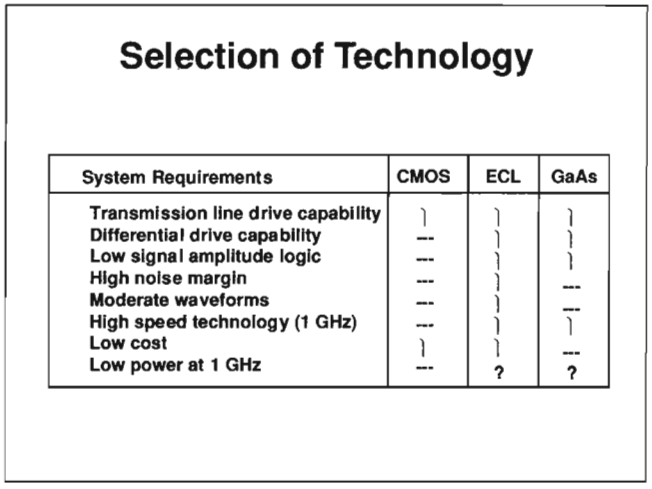
Combining both systems allows utilization of the best of each method.

The parallel bus is used twice; for parallel transfers (standard VME) and to arbitrate for and set up the high-speed serial link, including error handling.

As the serial bus does not need a protocol overhead for collision detection, the amount of net transferred data is nearly 100%.

Since parallel and serial transfer can run independently of each other, the performance of both transfers can be added. This leads to a very economical alternative for high-speed data transfers, eliminating the bottleneck in existing bus systems.

Slide #26



The low output impedance and the high current drive capability of ECL makes it an ideal technology for driving transmission lines.

The differential amplifier does not switch on an off, but simply steers between two paths. This current stability greatly simplifies the design and avoids bounce effects. With common node noise rejection of 1 V or more, ECL line receivers are less susceptible to common node noise.

The higher the amplitude, the larger the reloading circuit of a line, which can lead to problems such as over/undershoot, crosstalk, and radiation. The ECL output signal, with an amplitude of less that 1 V, carries the design.

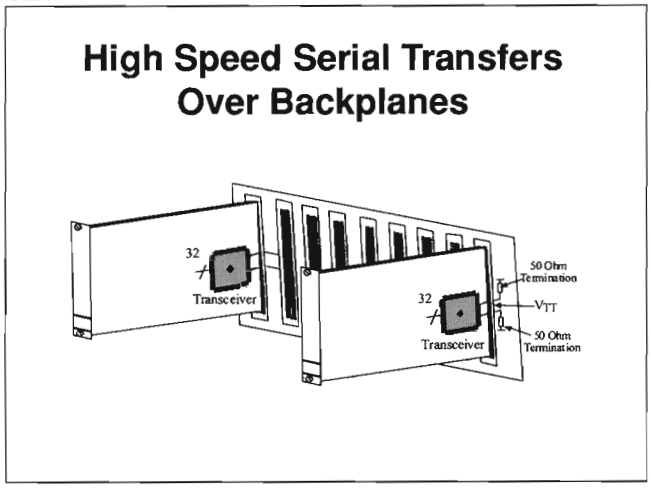
The noise margin is defined as the difference between a voltage level of the output of the sending device and the required voltage level of the input of the receiving device.

With an output voltage of more than 600 mV (typically 1 V) and a specified input hysteresis of 150 mV, ECL technology offers an excellent noise margin. Using the differential line driver capabilities, this is valid for both logical states.

Thanks to a very low specified input hysteresis of 150 mV, convenient waveforms, even sine waves, may be used to reduce jitter, ground bounce and crosstalk.

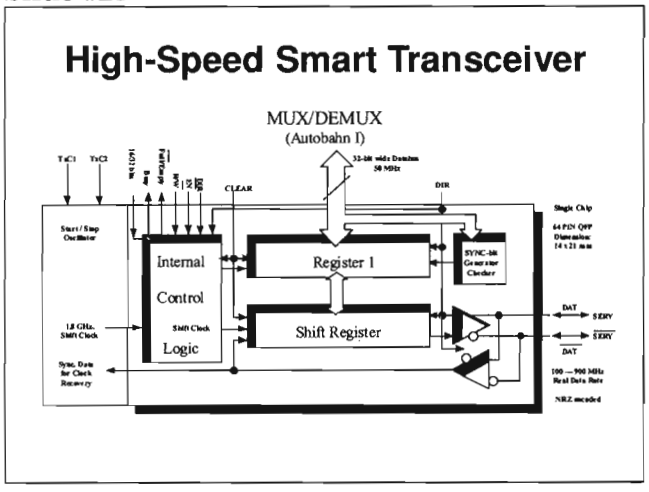
ECL devices, manufactured in MOSAIC V technology, offer an on-chip toggle frequency of 25 GHz. This gives a high transmission safety for AUTOBAHN data transfers and no need for additional circuitries, such as CRC or parity logic.

Slide #27



A standard 21 slot VME backplane is assembled with all the female DIN connectors fitted, thus allowing a partially loaded system to be expanded by adding extra cards. This complicates the design of the 50-ohm differential transmission lines because each of these connectors represents a signal stub, and hence a large potential reflection source when unterminated. For this reason it was decided to terminate each transmission line on the backplane, as close as possible to the DIN connector, thus preventing the problems associated with trace stubs. When a board is plugged in that uses the Autobahn serial interface, the signals are routed to the transceiver chip that is mounted within 25 mm of the DIN connector. When a card is plugged in that is not compatible with the Autobahn serial interface, it has no loading effect. As a result, it makes no electrical connection to the serial bus which is terminated in its characteristic impedance on the backplane. In this way, signal integrity is maintained at a high level throughout the system. Since the ECL signal is in this way terminated on the left and right end of the backplane, the signal transfer characteristic is independent of the slot transmitting the data; in other words, there are no slot-dependent transmit/receive requirements.

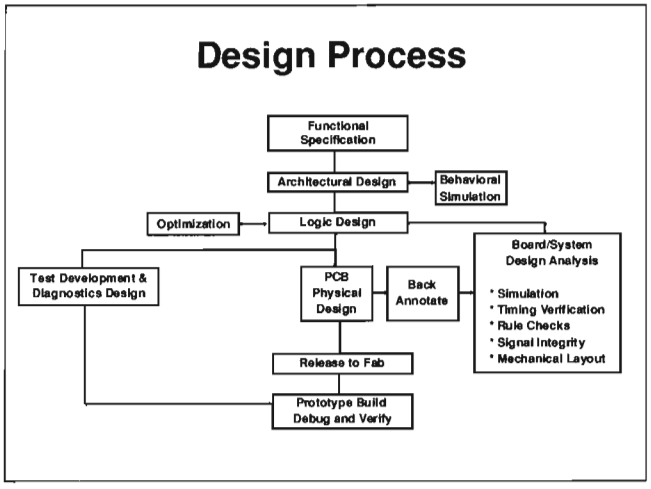
Slide #28



The high-speed transceiver allows a contiguous serialization of a 32-bit wide parallel data bus and vice versa. At a transfer rate of 200 MByte/s, the frequency on the parallel bus is on the order of 50 MHz, while on the serial bus, it is up to 900 MHz. Data is in NRZ format with one start bit added for each transmitted byte to allow received clock regeneration. This is achieved by an on-chip start/stop oscillator with a 3.2 GHz frequency, which is resynchronized by each start bit of the received data stream. This eliminates the need for an external VCO, Phase-Locked-Loop (PLL), and filters. In addition, it significantly reduces transfer time delays and jitter.

A critical part of the transceiver design was its power consumption. The Motorola PECL technology used offers extremely low power consumption coupled with the requirement for only a single +5 V supply. The 64-pin QFP chip consumes about 1 W when fully loaded, most of which is attributable to the parallel interface. This illustrates another reason to serialize high-speed data transfer.

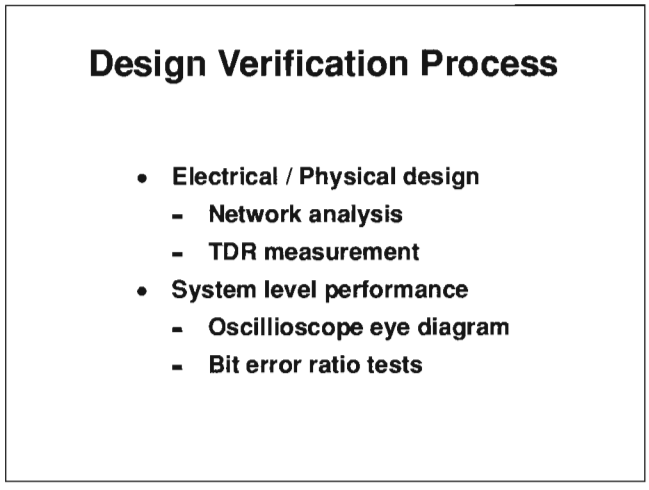
Slide #29



To ensure a reliable and robust design, the most important part of the design process was the PCB physical design, its simulation and modeling and the verification of timing and signal integrity performance. Mechanical layout was critial; although, in this case where a standard VME product was being enhanced, certain constraints were present. Design criteria can be separated into electrical and mechanical topics; although, as frequency increases, the line between the two becomes blurred.

Simulation and modeling of the combined effects is essential in the early stages using tools such as the Hewlett-Packard MDS or HDT Simulation products. The remainder of the paper concentrates on the measurement and verification of the post-simulation design.

Slide #30

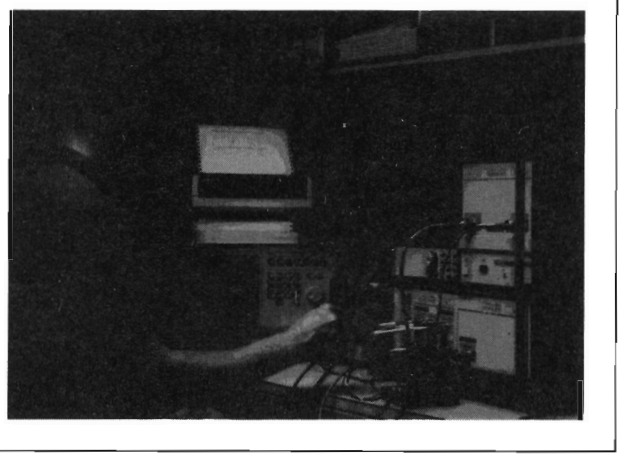


The design verification of the components and complete system were completed in four logical steps. This first step was to verify the electrical properties of the backplane and confirm that the mechanical design chosen yielded a good electrical design. At higher frequencies, these two points are very closely linked. The main measurement techniques used here were Network Analysis and Time Domain Reflectometry (TDR). These measurements were used to measure attenuation at the predicted maximum data rate and to evaluate the impedance characteristics along the transmission line, which should represent a uniform, controlled impedance.

At a system level, transmission quality and bit error performance must be evaluated. This is achieved by looking at oscilloscope eye-diagrams to confirm signal integrity and noise margin performance, and by employing Bit Error Rate tests to display the received bit error rate of a known PRBS (Pseudo Random Bit Sequence) after transmission through the system, at a maximum data rate.

All of these tests represent those steps which must be undertaken by any designer creating a high-speed digital data transfer system. Only by comparing the predicted simulation results with real measurements and modifying the design accordingly can a completely functional and robust design be created.

Slide #31



Two instruments were chosen to perform much of the design validation processes. The HP 54120-series digitizing oscilloscope and TDR can perform Time Domain Reflectometry, Time Domain Transmission, and eye pattern analysis. In addition, it can also be used as a high-bandwidth scope, at up to 50 GHz. The HP 71600-series BER tester can perform a wide variety of BER measurements under all kinds of varying conditions, using industry standard algorithms.

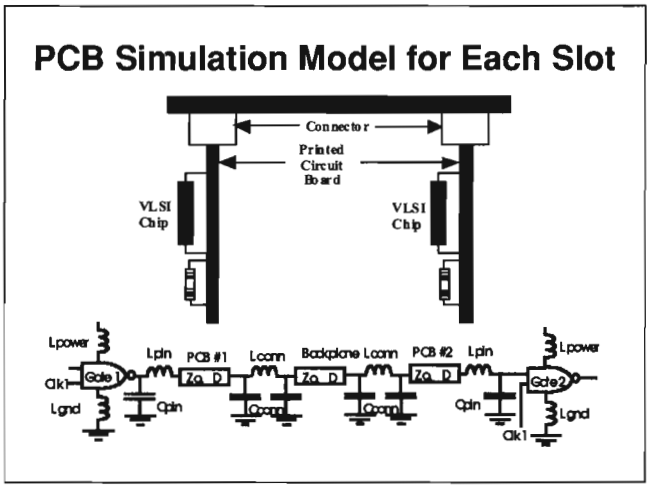
Slide #32

Mechanical Criteria

- Material properties
- Stub lengths
- Trace layouts
- Design rules definition
- Termination

With higher speeds come new concerns that have to be understood in order to make your model and simulation tools provide accurate representations of the design. Mechanical characteristics of the design are becoming increasingly significant aspects which these modelling tools must account for in order for the simulations to be accurate. These mechanical aspects of the design are starting to become part of modelling/simulation software packages, like HP's MDS and HFSS. Even common software tools, like HSPICE, are including some of the physical descriptions of the design in order to provide better accuracy, and consequently faster design cycles. Basically, the inclusion of these mechanical conditions help the software tools understand the electromagnetic properties of a design, which is a key aspect as speeds increase. When these considerations are included in the early design phase, fewer board cuts are required and designs are more likely to work.

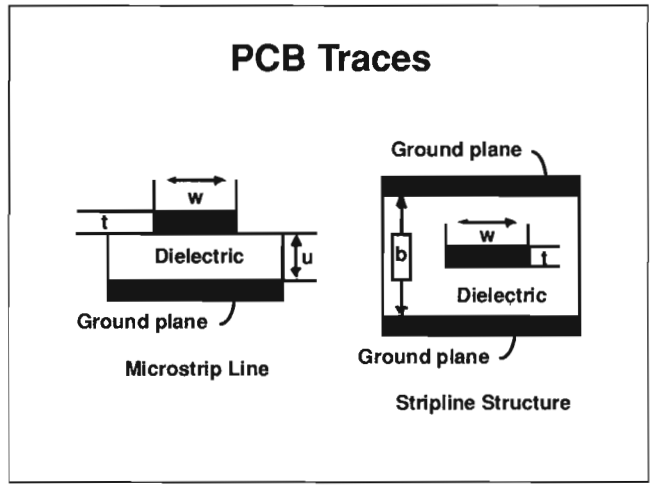
Slide #33



During the early stages of the design, a modified 21-slot VME backplane was used to confirm the system's feasibility. Theory showed that 1 GHz transfers were feasible on a 50 ohm transmission line, as long as certain design guidelines for line loading and the receivers were followed. A simple model was used to simulate the transmission line properties at the bit rates that were proposed and these verified using a coaxial 50 ohm cable between the slots. The simulation showed that in order to achieve 1 GHz transfer rates, the capacitance and inductance of the VME board and connector pair should not exceed 2 pF and 15 nH, respectively.

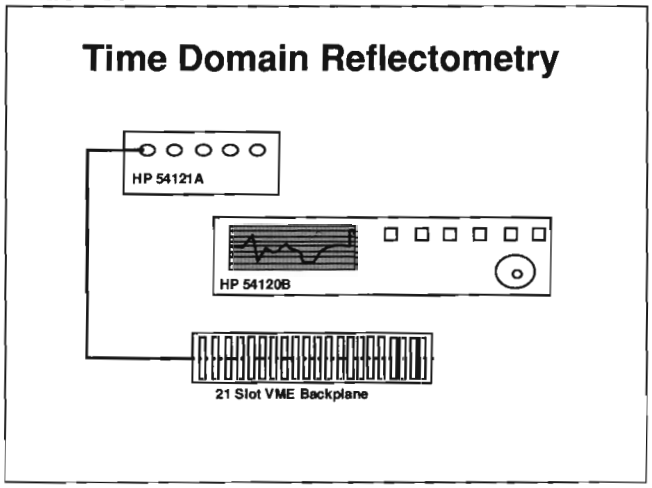
The use of coaxial cable was, however, too expensive and highly impractical for the application. Therefore, other alternatives were considered.

Slide #34



A microstrip line is the easiest printed circuit interconnection to manufacture, as it consists simply of a ground plane and flat signal conductor separated by a dielectric. Its performance with respect to crosstalk, impedance continuity, and emissions can be significantly improved by sandwiching the trace between two conducting layers. This creates a stripline structure. It was this structure that was chosen for the backplane design.

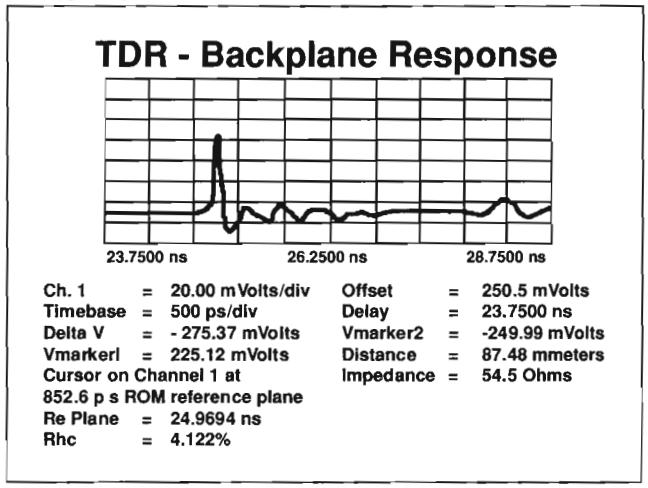
Slide #35



Following the initial simulation of the backplane, it was extremely important to verify the accuracy and validity of the models used. A TDR measurement was chosen for this purpose because of its accuracy and intuitive ease of interpretation. The measurement allowed the impedance along the backplane to be measured and the irregular effects of the connectors to be evaluated. This information could then be fed back into the simulation process if necessary as an aid to refining the simulator models.

The setup chosen is shown above, where the backplane was connected to the TDR channel of an HP 54121T Oscilloscope. A major benefit of the HP 54120-series is that it allows normalization of measured results to take account of real-life risetimes that are different from the risetime produced by the instrument's TDR step generator. In this case, the TDR step has a risetime of approximately 35 ps, whereas the Autobahn chipset has risetimes in the region of 150 ps. Therefore, normalization allows evaluation of the Autobahn backplane at realistic system risetimes.

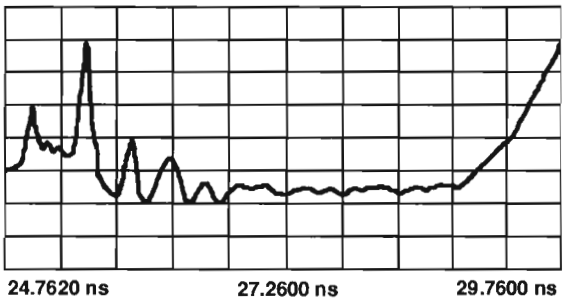
Slide #36



Shown in the diagram is the impedance of the backplane with no connectors fitted and with the end of the line terminated in its characteristic impedance. As can be seen from the diagram, the line exhibits a good uniform impedance, as simulated, even including the effects of signal stubs. Away from the launch point, these stubs cause an impedance variation of approximately 4 ohms. The first spike on the trace is the SMA connector used as the launch point. These connectors typically exhibit an inductive load as shown. The effect of the connector stubs is a small capacitance.

Slide #37

TDR - Backplane with Connectors



With connectors fitted, the impedance of the transmission line is very much more disturbed. In the diagram above, which is scaled at the same rate as the previous diagram, all connectors are fitted to an unterminated backplane and the TDR signal is launched through a standard VME male/female DIN connector. The overall effect is a general lowering of the impedance of the transmission line due to the capacitive loading of the connectors. This measurement compares the worst-case performance to a 35 ps edge which is considerably faster than the effective edge rate of the line. As the edge speed is reduced by normalization, the impedance discontinuities become less pronounced in their effect.

The TDR measurements allowed verification of the basic model used but indicated that the connector model needed some refinement. At the time of writing this paper, a new connector is under development which will improve the impedance profile of the backplane.

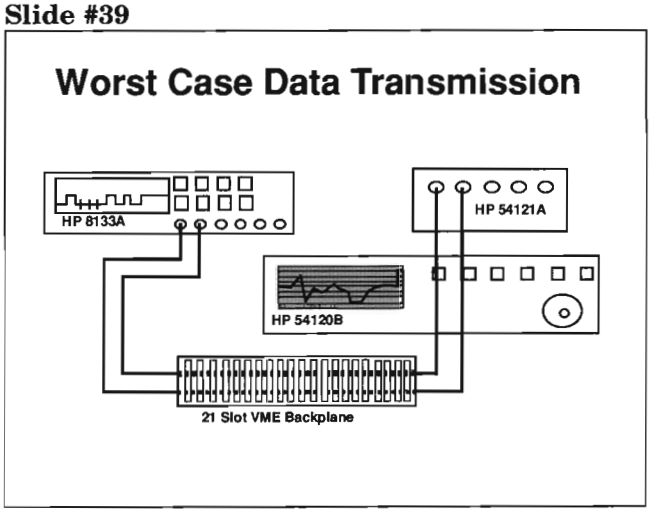
Slide #38

Electrical Criteria

- Noise margins
- Line terminations
- Impedance characteristics
- Signal / Waveform integrity
- Reflection, crosstalk

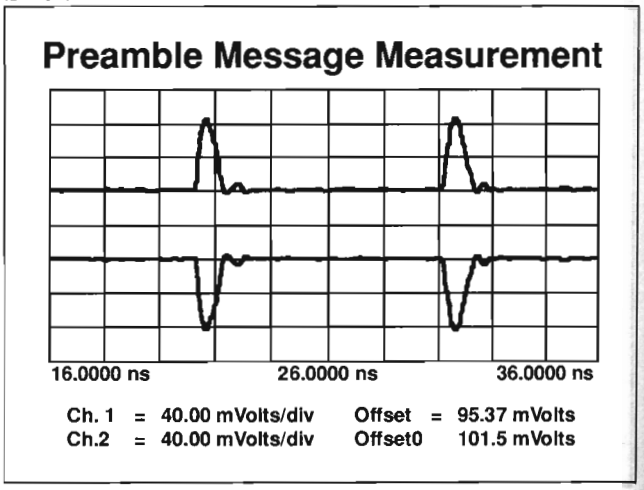
The topics discussed so far have primarily dealt with a standalone backplane with no active load connected. Connecting the driver/receiver boards with active transceivers completes the actual transmission line, and allows realistic system performance measurements to be made. The one aim of the design is to maintain good signal integrity under all operating or load conditions. Worst-case scenarios must be identified and performance verified under these conditions. In the case of a backplane-based system, this will almost certainly occur when all slots are occupied with operating transceivers. Noise margin calculations completed in the initial logic design phases must be validated under load conditions and the effects of impedance mismatch induced reflection or crosstalk reevaluated under real-life operating conditions.

Slide #39



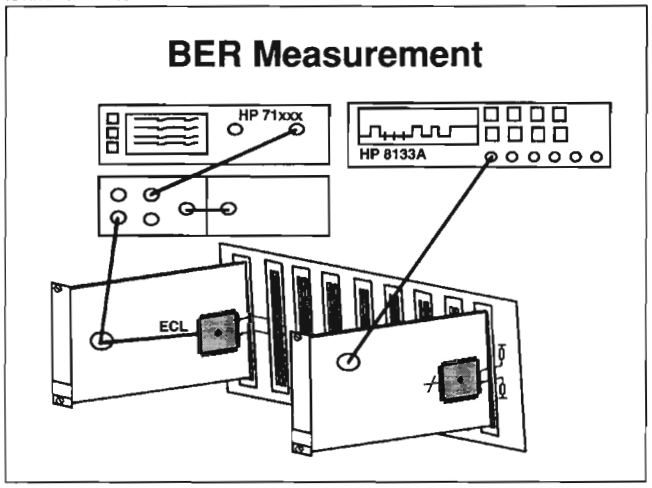
The next level of testing involved evaluating a loaded backplane's performance with real-life signals applied. The TDR measurements indicated a less than ideal transmission environment, even though the normalized measuremnets promised better performance. The following stimulus measurements allowed the backplane to be evaluated under realistic conditions. An HP 8133A was used to provide stimulus to an ECL driver/receiver set driving the differential lines on the backplane. This gave the flexibility of not only generating a bit-sequence at up to 3 GHz, but allowed pulse width variations to be simulated and their effects evaluated.

Slide #40



The diagram above shows the transmission of a preamble message across the backplane at 1.4 GBit/s which corresponds to a serial line frequency of 700 MHz or a parallel data transfer rate of approximately 155 MBytes/s. It can be seen that the signal transmission quality is good, even allowing for the connector mismatch problems of the backplane. The preamble message is a sequence of zeros separated by the Autobahn clock regeneration synchronization bit and represents one of the possible worst-case signals that can be present on the link.

Slide #41



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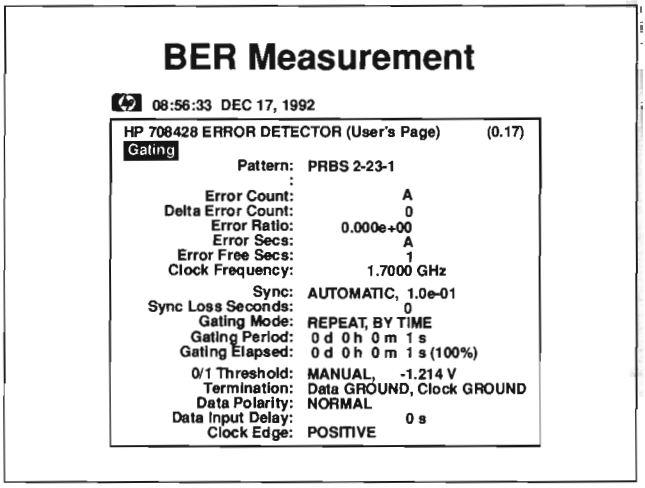

The measurements so far have proved qualitatively that the transmission of data at these rates is possible over the backplane. However, this must be verified quantitatively. This is done by use of a Bit Error Rate Test, where a PRBS (Pseudo Random Bit Sequence) is transmitted over the serial line from the HP 8133A through the ECL transceivers and the backplane and received by an HP 71600-series High-Speed BER Tester. This instrument detects a PRBS being transmitted by the pattern generator (it can also generate a full range of PRBS signals itself) and performs a comparison with the signal received and the predicted actual value, thus giving a quantitative measure of the quality of the data transmission.

The above shows a BERT listing made on the system discussed so far with the backplane driven by the ECL transceiver devices. It indicates that the current revision of the system can operate at 1.7 GBits/s before it starts to experience bit errors. At 1.8 GBits/s the received bit error rate was measured at 300 errors per million bits transmitted. With no connectors fitted, the error free figure was extended to 2.3 GBits/s, which tends to confirm the findings of the measurements made with the oscilloscope and data generator and those of the TDR. Note that on the HP BERT system, the displayed bit frequency has a 1:1 relationship with the bit rate.

In practice, a true PRBS is not possible across the Autobahn link because there is always a sync bit added to each byte of the message for clock regeneration purposes. This clock regeneration method guarantees received data bits are always sampled in the center of the bit period, which improves bit error performance and helps minimize signal jitter.

Slide #43

Conclusions

- **High bit rates possible over VME backplane**
- **Correct choice of measurement tools allows fast identification of key problem areas**
- **ECL limited swing process proves to be an enabling technology**
- **Diversity of applications in current and future designs**

The study has shown that the transfer of data over the serial bus using the technology discussed in the paper is possible at the high data rates predicted. Initial measurements have identified the din connector as a source of concern in the overall system and a definite area for attention. At the time of going to press, a new low, inductance version of the male connector was under development. Simulation allowed a first attempt at modelling the system, but the measurement equipment allowed the validity of these modules to be tested and the system problem areas to be identified in both qualitative and quantitative manner.

Apart from the backplane application discussed here, this method of high-speed data transmission has been shown to hold great potential. Limited-swing differential ECL, using the latest silicon processes, is an enabling technology that not only gives a new lease on life to the VME system, but promises much for high-speed PC board systems between microprocessors or high-speed subsystems. Here, the transmission line design will be much simpler because of the lack of complex connector structures used on the backplane.