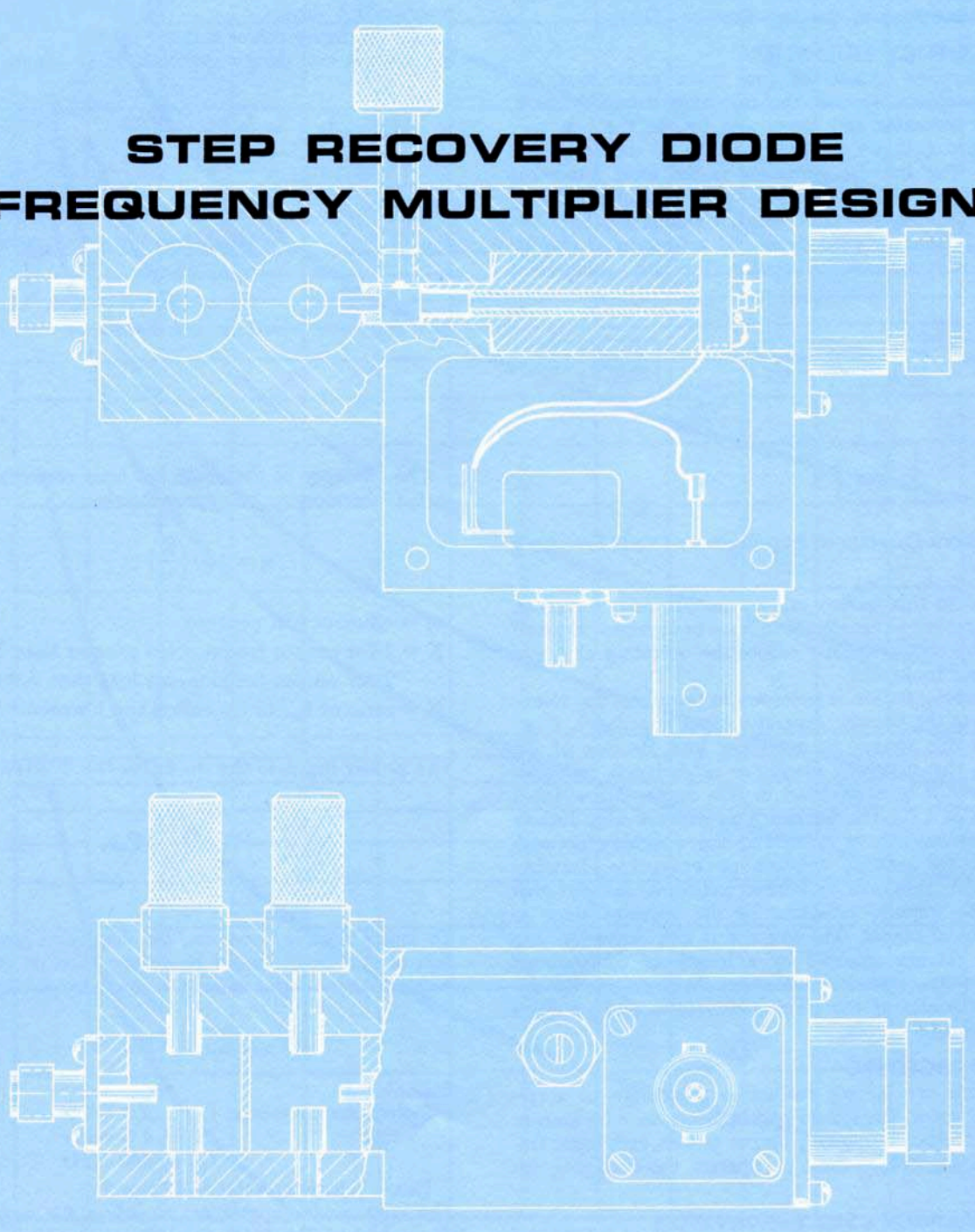
HEWLETT PACKARD HP ASSOCIATES

APPLICATION NOTE 913

15 MAY 67

STEP RECOVERY DIODE FREQUENCY MULTIPLIER DESIGN



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INTRODUCTION

Energy at one frequency can be converted to energy at a higher frequency by utilizing the properties of an impulse. An ideal impulse (i.e., a pulse having infinite height, infinitesimal width and unity area) has a frequency spectrum containing all frequencies. When an impulse is repeated at a frequency f_1, then the frequency spectrum will show components at integrals of f_1. The production of an impulse requires a very fast and properly timed switch. The Step Recovery Diode is such a switch. The Appendix has a more complete description of the Step Recovery Diode.

THE FREQUENCY MULTIPLIER

The multiplier consists of four main parts: first, the impulse generator; second, the matching network; third, the output resonator and filter; and fourth, the bias network. Figure 1 shows a block diagram of the frequency multiplier. The impulse generator is the most important and, at the same time, the most difficult part of the multiplier. The impulse generator which contains the Step Recovery Diode, converts the sinusoidal waveform of the RF drive source at f_1 into an impulse. Typically, component

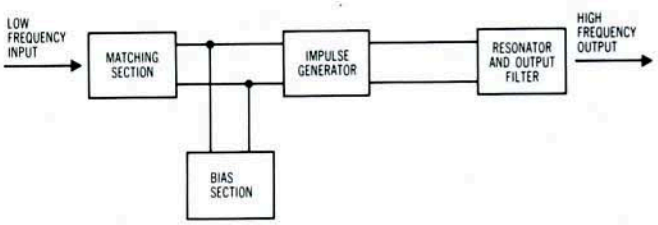


Figure 1. Block Diagram of Step Recovery Diode Frequency Multiplier.

values used in this section are very small, and, therefore, difficult to realize physically. Care must be exercised as small losses in this section greatly reduce the operating efficiency of the entire multiplier.

The matching section is necessary to transform the source impedance to the impulse generator input impedance. Components in this section must be low loss. Because of the many ways that matching filters can be designed, only two approaches will be considered in this paper. Below input frequencies of 1.0 GHz, the matching network uses discrete circuit elements. Above 1.0 GHz, the matching network uses distributed coaxial, stripline, or waveguide elements.

The output resonator and filter section is the part that converts the impulse produced by the previous stage to pure sinusoidal output. The impulse is first converted into a damped ringing sinusoid by a length of transmission line that acts as a resonator. The filter then removes the undesired harmonics of the ringing waveform and produces a pure sinusoidal output.

DESIGN PROCEDURE

Before one can go any further in the design of a frequency multiplier, the system requirements must be known. These are: output frequency, output power, and input frequency. Having chosen these parameters, the designing can proceed.

(A) The Selection of a Step Recovery Diode

The choice of a particular diode is dependent on the power output required, the frequency of operation, the diode's reverse bias capacitance, and the maximum power dissipation of the diode. The theoretical output power that can be obtained is:

$$\left(P_{OUT}\right) = \left[V_{BR}\left(1 - 2\,V_{BR}\,\pi\,fo\,10^{-13}\right)\right]^2 f_{IN}\,C_{-10} \quad (1)$$

V_{BR} = diode breakdown in Volts
f_o = output frequency in Hertz
f_{IN} = input frequency in Hertz
C_{-10} = diode capacitance at $V_R = 10$ Volts

Refer to Figure 2 for curves of (P_{OUT}) max. vs. f_o for several HPA diodes.

The maximum power that the device can handle, assuming a worst case design approach, is $(P_{DISS})_{MAX.}$

$$\left(P_{DISS}\right)_{MAX.} = \frac{T_{J\,MAX} - T_{CASE}}{\theta_{JC}} \quad (2)$$

$\left(P_{DISS}\right)_{MAX.}$ = Maximum power dissipation
$T_{J_{MAX.}}$ = Maximum junction operating temperature in °C
T_{CASE} = Case temperature in °C
θ_{JC} = Thermal resistance in °C/watt

The efficiency of the diode has been empirically derived in the laboratory to be approximately

$$\eta = 100\left(\frac{K}{N}\right) \quad (3)$$

η = efficiency in percent
K = 1 for output frequencies greater than 5.0 GHz;
2 for output frequencies less than 5.0 GHz
N = ratio of f_{out} to f_{in}, called the harmonic number

The power input to the diode for the desired output is:

$$P_{IN} = \left(\frac{N}{K}\right) P_{OUT} \quad (4)$$

To insure reliable operation, the maximum power dissipation of the diode should be greater than or equal to the required power input minus the power output; i.e.,

$$\left(P_{DISS}\right)_{MAX.} \geq P_{IN} - P_{OUT} \quad (5)$$

Example

System Requirements: $f_o = 2.0$ GHz
$P_o = 4.0$ watts
$f_{IN} = 400$ MHz

Diode Selection: Refer to Figure 2
The only diode capable of providing the desired output power is the HPA 0300. From Equation (4),

$$P_{IN} = \frac{N}{K} P_O = \frac{\frac{f_o}{f_{in}}}{K} P_O = \frac{\frac{2.0}{0.4}}{2}(4.0) = 10\ W$$

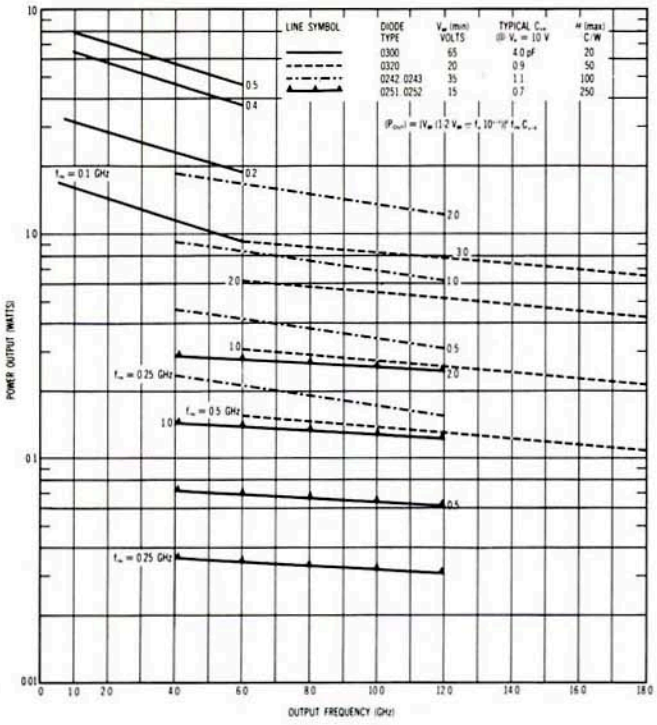


Figure 2. Theoretical Power Output Versus Output Frequency for HPA Step Recovery Diodes. (This figure has been reproduced full size on Page 21 as a design aid.)

Actual P_{IN} must be higher than this to account for circuit losses; By Equation (5), $(P_{DISS})_{MAX.} = 6$ watts. Figure 3 shows that the conditions of Equation (5) are easily satisfied by the HPA 0300, with ample derating of junction temperature.

HPA DIODE	T_J (max) (°C)	P_{DISS} (max) at T_C = 20°C (watts)	θ_{JC} (°C/W)
0300	200	9.0	20
0320	200	3.6	50
0240, 0241	175	3.0	60
0242, 0243	175	1.8	100
0251, 0252, 0253	175	0.72	250

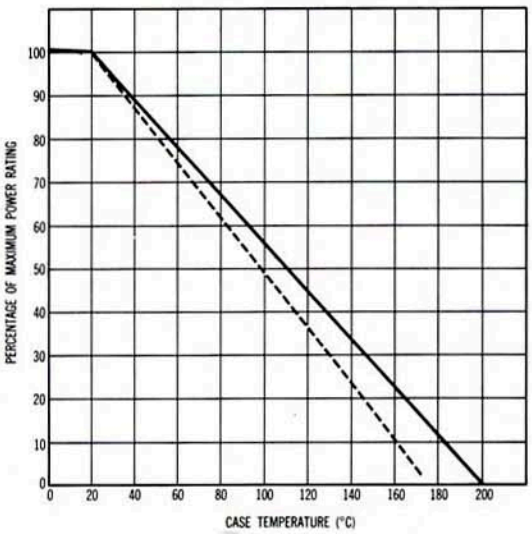


Figure 3. Maximum Power Dissipation Derating Curve.

(B) The Impulse Generator

This section, shown in Figure 4, contains three circuit elements; the Step Recovery Diode (SRD), the drive inductor (L), and the high frequency shorting capacitor (C_T). Having already chosen the diode, the next step is determining the size of the drive inductor. Figure 5 is a curve relating the drive inductance to two parameters, output frequency (f_o) and diode reverse capacitance (C_{-10}).

Example

$f_o = 2.0$ GHz
Diode type HPA 0300
Diode reverse capacitance (typical) = 4 pF
From Figure 5, L = 1.43 nH

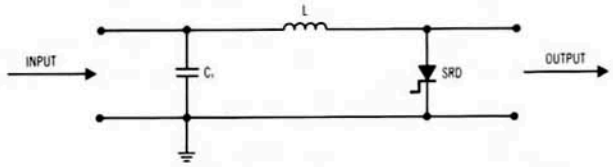


Figure 4. Impulse Generator.

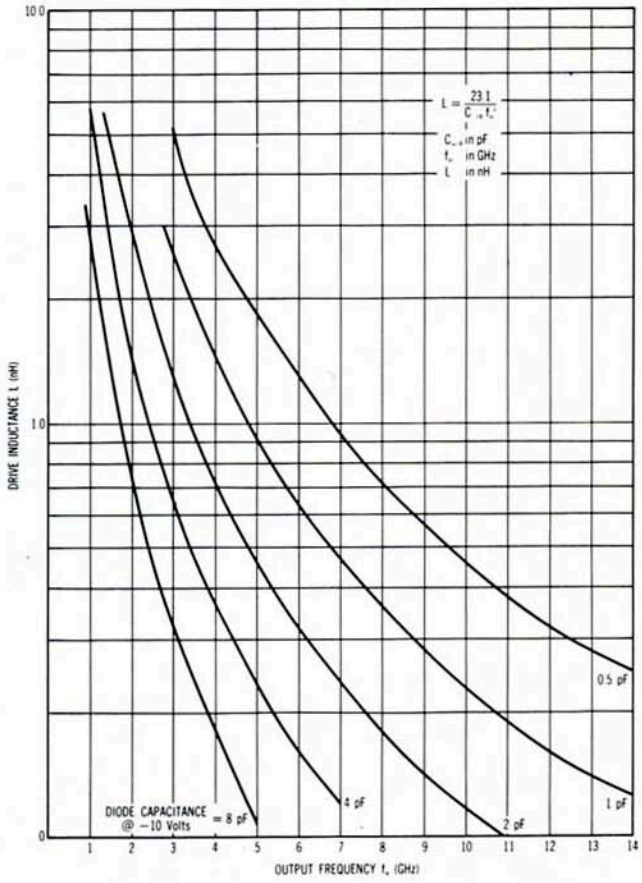


Figure 5. Drive Inductance L Versus Output Frequency f_o. (This figure has been reproduced full size on Page 22 as a design aid.)

The capacitor, C_T, is used for two reasons. First, it is chosen to make the input impedance of the impulse generator purely resistive. Second, the capacitor acts as a short at the output frequency. Thus, the RF output of the frequency multiplier cannot get back into the input section. Figure 6 shows C_T as a function of the drive inductance and the input frequency.

Example

$f_{OUT} = 2.0$ GHz
$f_{IN} = 0.4$ GHz
$L = 1.43$ nH
From Figure 6, $C_T = 55$ pF

Care must be taken in choosing a physical element for C_T. The capacitor must have very high Q (low loss) for the circuit to work properly. A better value of C_T may be found empirically.

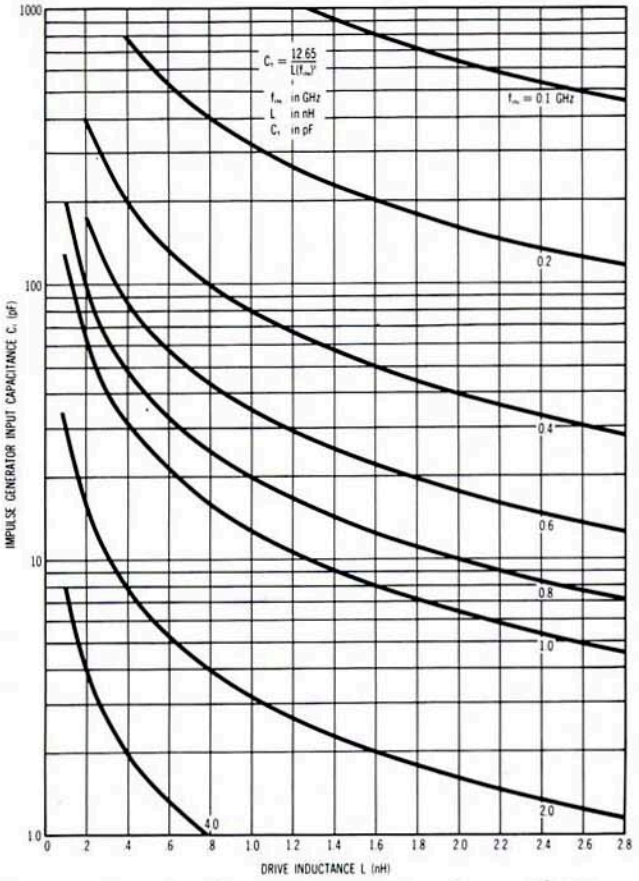


Figure 6. Impulse Generator Input Capacitance C_T Versus Drive Inductance L. (This figure has been reproduced full size on Page 23 as a design aid.)

(C) The Matching Section

This part of the frequency multiplier can be realized in many different ways. When the input frequency is below 1.0 GHz, it is common practice to use lumped circuit elements. The designer can use an almost infinite number of techniques for matching from the RF source to the impulse generator. Trading a good impedance match for low circuit losses, the designer can use many sections of exotic type filters. Or, if the highest input-output efficiency is required, he can use a single section L-C filter. A requirement for broadband matching will usually necessitate a multi-section matching transformer.

The input impedance to the impulse generator is:

$$Z_{IN} = R_{IN} = \frac{1}{2\pi N f_o C_{-10}} \tag{6}$$

N = Harmonic number
f_o = Output frequency
C_{-10} = Diode reverse capacitance at −10 volts.

Example

$f_o = 2.0$ GHz
$N = 5$
Diode Type HPA 0300
Diode Reverse Capacitance at −10 volts
= 4 pF (typical)
From equation (6) $R_{IN} = 4\,\Omega$

For the purposes of this paper, and assuming that the single section L-C matching transformer shown in Figure 7 is adequate, then:

$$L_m = \frac{\sqrt{R_g R_{IN}}}{2\pi f_{IN}} \tag{7}$$

$$C_m = \frac{1}{2\pi f_{IN} \sqrt{R_g R_{IN}}} \tag{8}$$

Example

$R_{IN} = 4\,\Omega$
$R_g = 50\,\Omega$
$f_{IN} = 400$ MHz
$L_m = 5.63$ nH
$C_m = 28.1$ pF

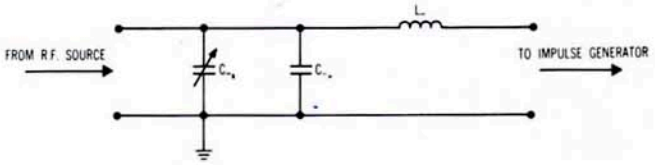


Figure 7. Typical Input Matching Section for Step Recovery Diode Frequency Multiplier.

To provide some degree of tuning, C_{mA} is made about 0.85 C_m and C_{mB} is made about 0.25 C_m. As with C_T, the capacitors used in the matching section should be of highest Q (low loss) possible. This type of matching section will not provide the best possible broadband match to the impulse generator but does have very low insertion loss.

(D) The Output Resonator and Filter

The operation of this part of the frequency multiplier is best visualized in the time domain and not in the frequency domain. Consider the resonator as a length of transmission line of characteristic impedance f_o. The impulse generated by the diode will travel back and forth along the line between the diode and the filter. If the length of the line is chosen to be a quarter wavelength at the output frequency, then the signal on the line will be a damped sinusoid. The input impedance of the filter will determine the damping rate. Theoretical analysis and laboratory experimentation have yielded the following conditions.

$$Z_O = 52.8 \sqrt{\frac{L}{C_{-10}}} \tag{9}$$

Z_O = characteristic impedance of the quarter wave line (in ohms).
L = drive inductance (in nH).
C_{-10} = diode reverse capacitance at −10 volts (in pF)

$$R_L = \frac{4N Z_o^2}{\pi Z_o - 3N} \quad (10)$$

R_L = input impedance of filter
N = harmonic number

Example

Diode type HPA 0300
Diode reverse capacitance at — 10 volts = 4 pF
Drive inductance = 1.43 nH
N = 5
From Equation (9), $Z_0 = 31$ ohms
From Equation (10), $R_L \simeq 230$ ohms

The free space quarter wavelength at 2.0 GHz is 1.475 inches. When the quarter wavelength is incorporated into the frequency multiplier, its effective length will depend on circuit conditions. Laboratory experience has shown that the transmission line may be odd integral numbers of a quarter wave in length. Half wavelengths do not provide the correct phasing at the input of the filter. From a practical standpoint, the resonating transmission line should be as short as possible to minimize losses.

The output filter may be of almost any design that meets the input impedance requirements as dictated by Equation (10). If the system can handle the unwanted harmonics, then a simple, single cavity filter is adequate. Greater rejection of unwanted harmonics requires sophisticated filter designs. Further explanation of the operation of the resonator line and output filter may be found in the Appendix.

(E) The Bias Section

Biasing of the Step Recovery Diode may be accomplished in two ways: self-bias using a resistor, or fixed bias with an external power supply. Self-biasing has the advantages of low cost, temperature compensation, and self-adjustment for different input power levels. The only disadvantage is that diode-to-diode variations will necessitate different values of bias resistance if optimum performance is required. A capacitor in series with the RF source is necessary to dc isolate the source from the bias circuitry.

The value of the bias resistance, as derived in the Appendix, is:

$$R_b = \left(\frac{2}{\pi N^2 C_{-10}}\right) \tau \quad (11)$$

R_b = Bias resistance
N = Harmonic number
C_{-10} = Diode reverse capacitance at −10 volts
τ = Effective minority carrier lifetime

Figure 8 is plot of ($R_b \times C_{-10}$) product versus τ with N as a variable parameter.

Example

Diode Type HPA 0300
Diode Reverse capacitance at −10 volts = 4 pF
Diode Effective Minority Carrier Lifetime
= 100 ns(min.)
Harmonic number = 5
From either Equation (11) or Figure 9, $R_b = 636$ ohms.

Depending on where the bias resistor is placed in the circuit, it may be practical to put in a trimmer resistor. In that case, a 270-ohm fixed resistor in series with a 1,000-ohm variable resistor would be more than adequate to account for any diode-to-diode variations.

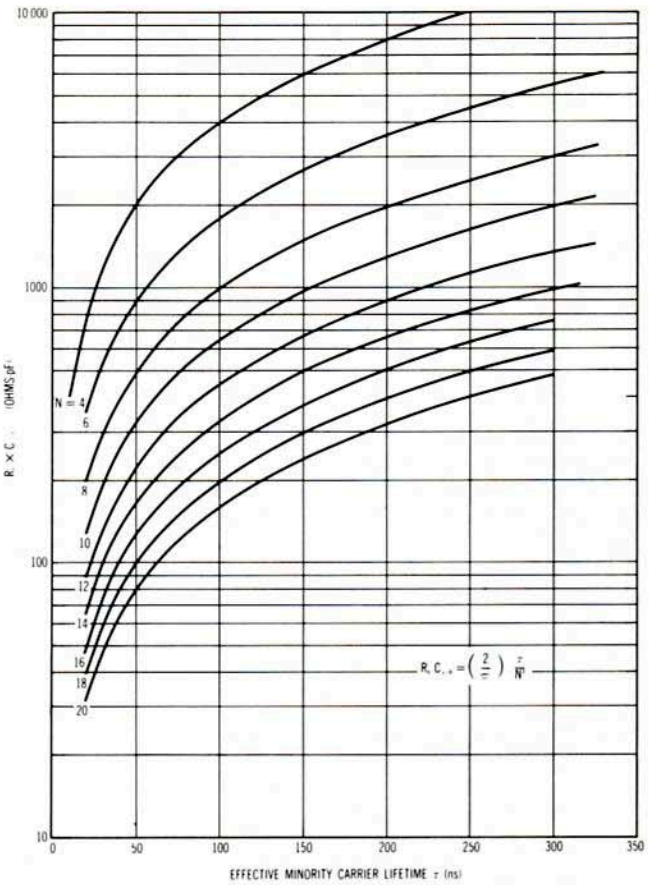


Figure 8. ($R_b \times C_{-10}$) Product Versus Effective Minority Carrier Lifetime τ. (This figure has been reproduced full size on Page 24 as a design aid.)

Temperature compensation is accomplished by choosing a bias resistor whose temperature coefficient matches that of the diodes. The prime temperature dependent parameter of the diode is the effective minority carrier lifetime, τ. The bias resistor is related to τ by Equation (11). Experimentation has shown that τ will increase at a rate of one-half to one percent per degree centigrade; i.e.,

$$\tfrac{1}{2}\%/°C \leq \frac{\Delta\tau}{\Delta T} \leq 1\%/°C$$

$\Delta\tau$ = Effective minority carrier lifetime change
ΔT = Temperature change

The junction temperature T_J should never exceed (T_J) max. given on the data sheet. The bias resistor can be placed across C_T, as shown in Figure 9a, or across C_M, as shown in Figure 9b. In either case, the parasitic inductance and capacitance should be minimized. Good thermal contact of the resistor body to the frequency multiplier case is required for correct temperature compensation. As an added measure, all critical metal parts, such as cavity posts and tuning screws, should be made from low thermal expansion material like invar.

A fixed, external bias supply can be made to track the diode's temperature variation but at a much higher cost. However, laboratory evidence indicates that greater spectral purity is possible with a fixed bias supply than with a self-

biasing resistor. This is especially true when extremely well regulated, low output impedance power supplies are used for biasing. Parasitic reactances of the self bias resistor is one probable cause of unwanted spurious signals.

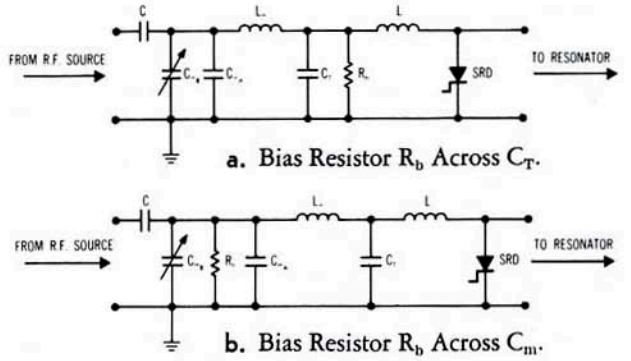


Figure 9. Bias Resistor Circuit Placement.

DESIGN EXAMPLES

I. S-Band Frequency Multipliers

The design of these multipliers is used to show the feasibility of Step Recovery Diode operation in telemetry transmitters. The output power requirements at 2 GHz are at two different levels: one around 2 watts and the other at greater than 5 watts. The lower output level multiplier is designed first.

Requirements: $f_o = 2.0$ GHz
$P_o = 2$ watts

Design

1. From Figure 2, choose the HPA 0300 diode for operation at $f_{IN} = 200$ MHz.
2. Harmonic Number $N = \frac{f_o}{f_{IN}} = 10$
3. Empirical efficiency by Equation (3)
$\eta = \frac{K}{N} 100\% = \frac{200}{10} = 20\%$
4. Minimum required input power by Equation (4)
$P_{IN} = \frac{N}{K} P_o = 10$ watts
5. Figure 3 shows that HPA 0300 diode will satisfy Equation (5)
6. The reverse bias diode capacitance at $V_R = 10$ volts is typically 4.0 pF. Figure 5 shows that the drive inductance $L = 1.43$ nH.
7. From Figure 6, $C_T = 220$ pF
8. Equation (6) yields $Z_{IN} = R_{IN} \approx 2$ ohms
9. Using the simple L-C matching network of Figure 7:
$L_m \approx 8$ nH $\quad C_m = 80$ pF
10. The bias resistor is placed across the matching section capacitor through a RF choke. The data sheet for the HPA 0300 diode shows that the minimum effective minority carrier lifetime is 100 ns. Using Figure 8: $(R_b)_{min} = 160$ ohms
A variable bias resistor is used to accommodate diode-to-diode variations in the lifetime.
11. The effective resonator line length is a quarter wave length at 2.0 GHz. The characteristic impedance is 31.3 ohms by Equation (9).
12. The output filter is a simple, coupled cavity type. The input impedance to the filter is approximately 500 ohms by Equation (10).

Figure 10 shows the mechanical and electrical layout of the frequency multiplier. The matching section and impulse generator schematics are shown in Figure 11. Although the component values of the matching section were first calculated as above, the best experimental results were obtained with the values shown in Figure 11. The discrepancy between theoretical and experimental values is probably due to an imprecise expression for the impulse generator input impedance.

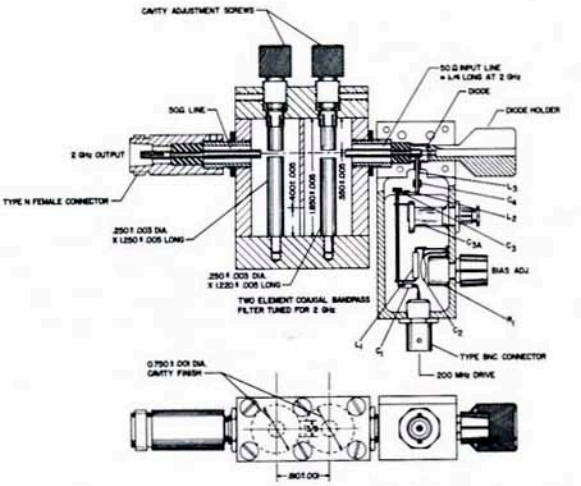


Figure 10. Mechanical and Electrical Layout of an S-Band X10 Harmonic Multiplier.

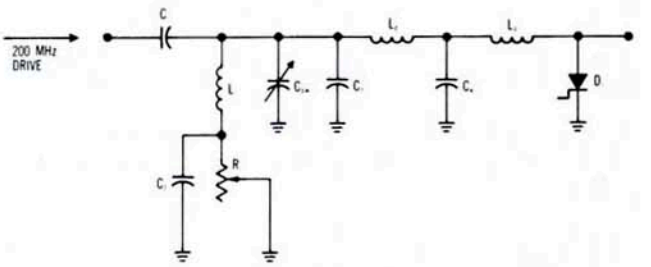


Figure 11. Input Circuit for a 200 MHz to 2.0 GHz Harmonic Multiplier.

C_1—0.001 μF Ceramic DC Blocking Capacitor
C_2—0.001 μF Ceramic DC Blocking Capacitor
C_3—50 pF Ceramic Chip Capacitor
C_{3A}—1 — 20 pF Johansen Capacitor
C_4—250 pF Ceramic Chip Capacitor (Note 1)
L_1—1 μH RF Choke
L_2—15 — 20 nH (2 turns of 0.020 wire on 0.1" diameter)
L_3—1 — 2 nH (short length of heavy bus wire [Note 1])
R_1—2 kΩ Variable Bias Resistor
D_1—HPA 0300 Step Recovery Diode

NOTE 1. The ceramic chip capacitor C_4 is inserted between the heavy bus wire inductor, L_3, and the ground plane. The position of C_4 along the length of the bus wire determines the value of L_3. For optimum performance, the value of L_3 must be adjusted to tune with the diode's reverse bias capacitance.

Typical performance of HPA 0300 diodes in this multiplier is shown in Figure 12. The test equipment set-up is shown in Figure 13. Observations on the spectrum analyzer show that the closest harmonics (at 1.8 and 2.0 GHz) are down 55 dB from the 2.0 GHz design frequency. Greater harmonic rejection can be obtained with a more sophisticated output filter. The difference between the estimated and actual power input requirements can be attributed to circuit losses and to the use of a 50-ohm quarter wave line instead of the required value.

The five-watt frequency multiplier design follows the same procedure. Figure 2 indicates that the 0300 can supply more than five watts at 2.0 GHz when driven at 400 MHz ($N = 5$).

1. Diode selection HPA 0300 from Figure 1
2. Harmonic number $N = 5$
3. $\eta = \frac{200}{5} = 40\%$
4. $P_{IN} = 12.5$ watts
5. Figure 3 shows that the chosen diode satisfies Equation (5).
6. From Figure 5, $L = 1.43$ nH
7. From Figure 6, $C_T = 55$ pF
8. Equation (6) yields $R_{IN} = 4$ ohms
9. Using the simple L-C matching network of Figure 7: $L_m \approx 5.6$ nH $\quad C_m \approx 28.1$ pF
10. The minimum bias resistance necessary is found from Figure 8. $(R_b)_{min} = 350$ ohms. A variable resistor is used.
11. The effective resonator line length is a quarter wavelength at 2.0 GHz. The characteristic impedance is 31.3 ohms from Equation (9).
12. The output filter is a simple, coupled cavity type. The input impedance to the filter is approximately 230 ohms from Equation (10).

The mechanical and electrical layout of Figure 10 and the schematic in Figure 11 applies to this multiplier; only the values of the matching section components are changed. The typical performance of this multiplier is shown in Figure 12. The test equipment set-up is the same as before. The nearest harmonics (1.6 and 2.4 GHz) could not be observed on the spectrum analyzer.

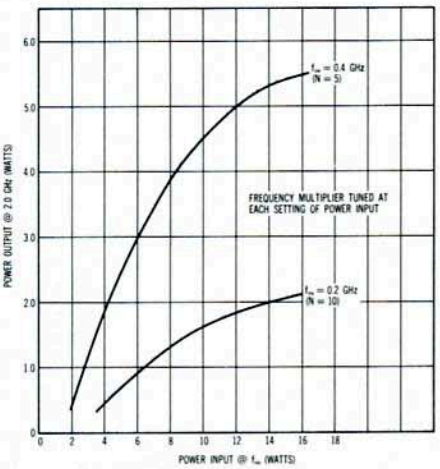


Figure 12. Typical Performance of Two Different Step Recovery Diode Frequency Multiplier Designs. The X10 Multiplier shown in Figure 10; the X5 Multiplier shown in Figure 14 with component values described in text.

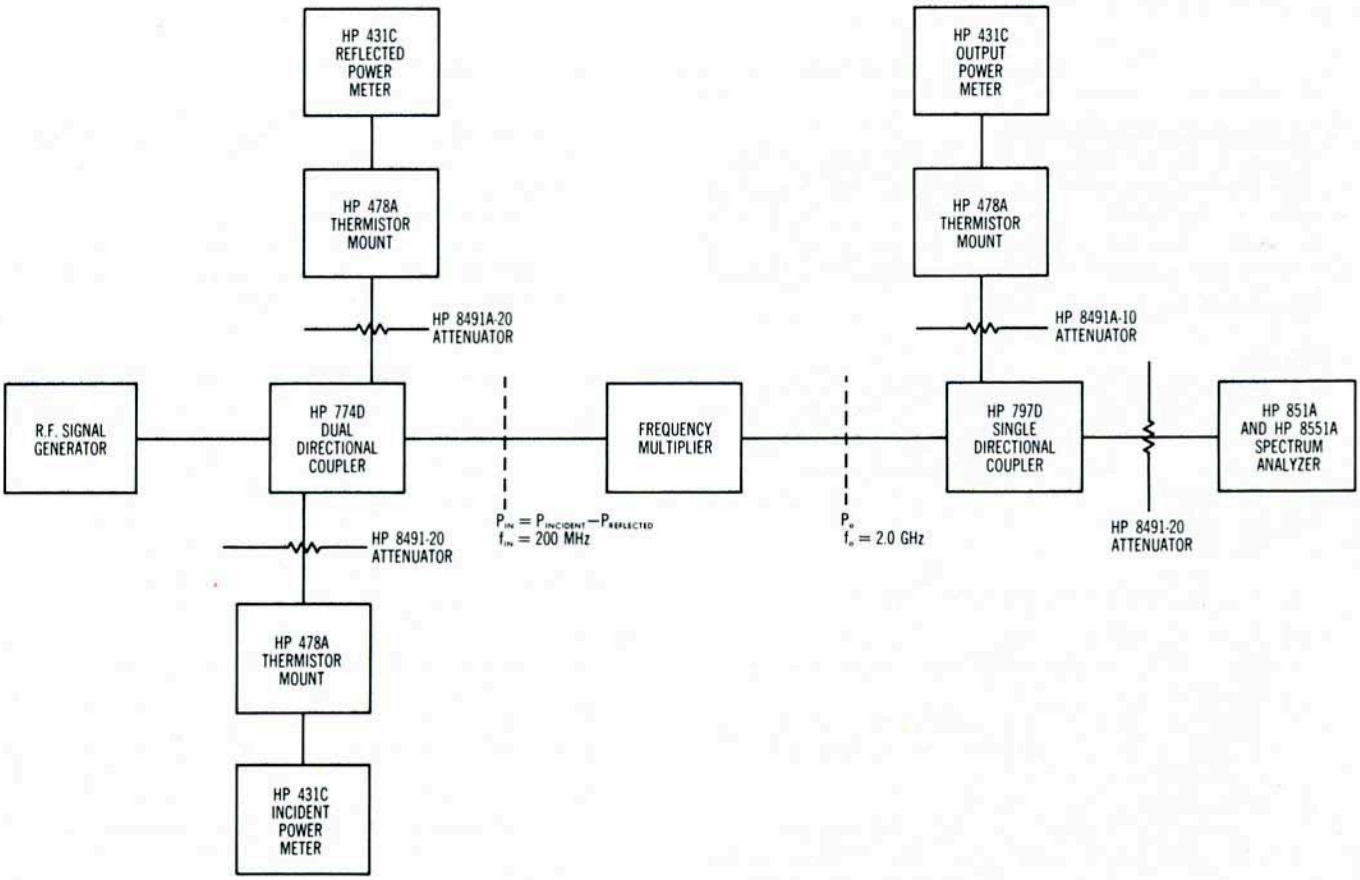


Figure 13. RF Test Equipment Set-up.

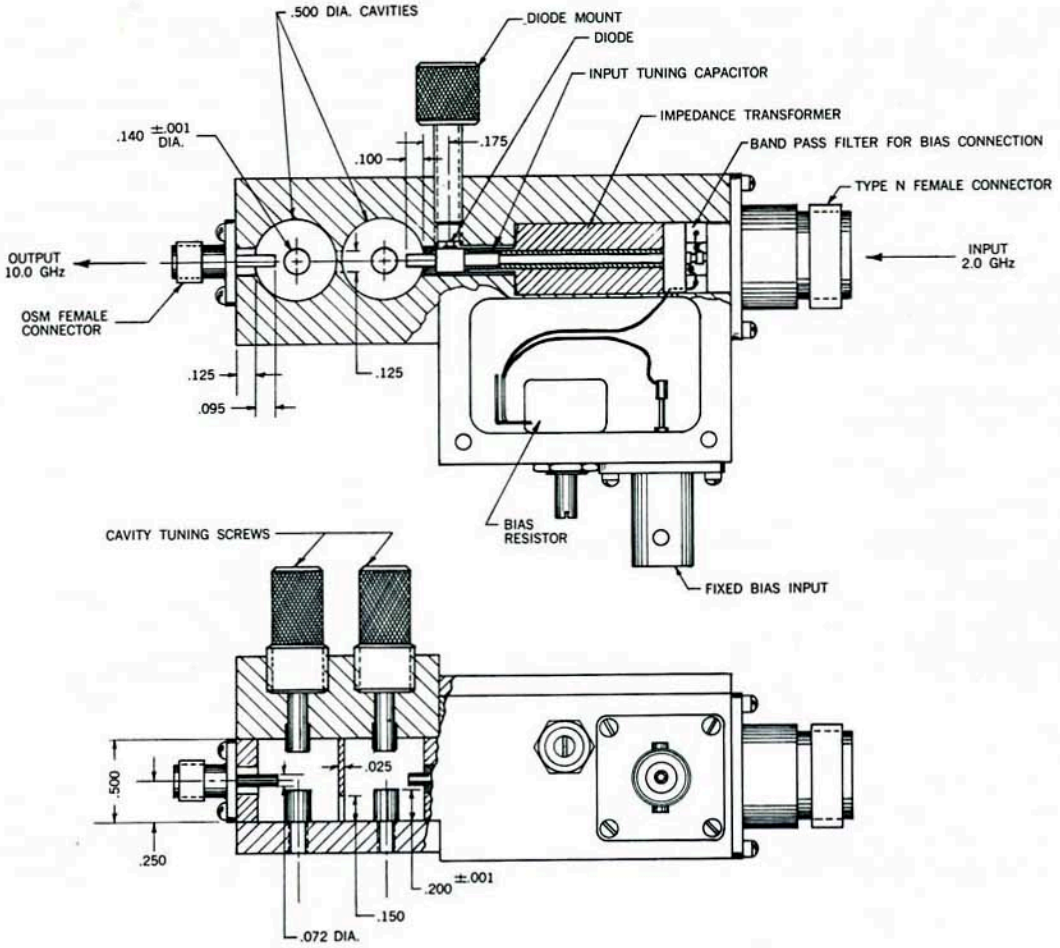


Figure 14. Mechanical and Electrical Layout of X-Band Multiplier.

II. X-Band Frequency Multiplier

The needs of the system designer for X-band solid state sources have been evident for many years. The design example will demonstrate that Step Recovery Diode solid state sources can meet requirements for local oscillator and low power transmitters in X-band and higher frequencies.

Requirements: $f_o = 10.0$ GHz
$P_o = 180$ mW

Design

1. Inspection of Figure 2 reveals that there are several HPA diodes that can do the job. The HPA 0320 diode is chosen because its low parasitic package design is better suited for very high frequencies.
2. The availability of a 2.0 GHz source dictated that $f_{IN} = 2.0$ GHz.
   $N = 5$
3. $\eta = \frac{100}{5} = 20\%$ by Equation (3).
4. $P_{IN} = 0.8$ watts
5. Figure 3 shows that HPA 0320 diode will satisfy Equation (5).
6. The reverse bias diode capacitance at $V_R = 10$ volts is typically 0.9 pF. Figure 5 shows that the drive inductance $L = 0.25$ nH.
7. From Figure 6, $C_T = 13$ pF
8. Equation (6) yields $Z_{IN} = R_{IN} = 3.54$ ohms
9. The input matching circuit is a distributed element circuit in the form of a transmission line. Refer to Figure 14 for the exact configuration.
10. The minimum bias resistance necessary is found from Figure 8.
    $(R_b)_{min} = 330$ ohms
    A variable bias resistance is used.
11. The effective resonator line length is a quarter wavelength at 10.0 GHz. The characteristic impedance is 27.9 ohms by Equation (9).

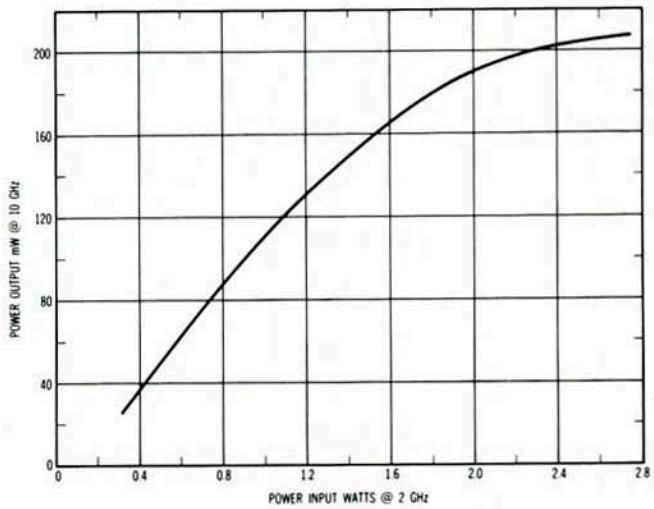


Figure 15. Typical Performance of HPA 0320 Diode.

12. The output filter is a simple, coupled cavity type. The input impedance to the filter is approximately 230 ohms by Equation (10).

The mechanical and electrical layout is shown in Figure 14. The bandpass filter is used to provide a dc return for the RF source, a biasing connection for the diode and dc isolation between source and multiplier. A typical power output versus power input curve is shown in Figure 15. The equipment set-up used in making the power tests is described in Figure 16. The performance of this multiplier is not as good as expected. One of the reasons for this is that the matching section does not match the impulse generator impedance to the source impedance as well as it should. Another possible reason lies in the difficulty of making a discrete capacitor for C_T. A third reason is that the resonating line, which also acts as a coupling probe into the input cavity, may not be of optimum length. The present multiplier length does not allow adjustments.

SUMMARY

The fundamental features of frequency multiplier design using HPA Step Recovery Diodes has been described. Examples of the design procedure have been stated and the results presented.

The interested reader will note that Figure 16 shows that the bias voltage may be swept over a voltage range of about 10 volts. This makes for easy RF alignment. More information on this technique is found in the HPA 0320 Data Sheet. The same technique can be applied to the equipment set-up shown in Figure 13.

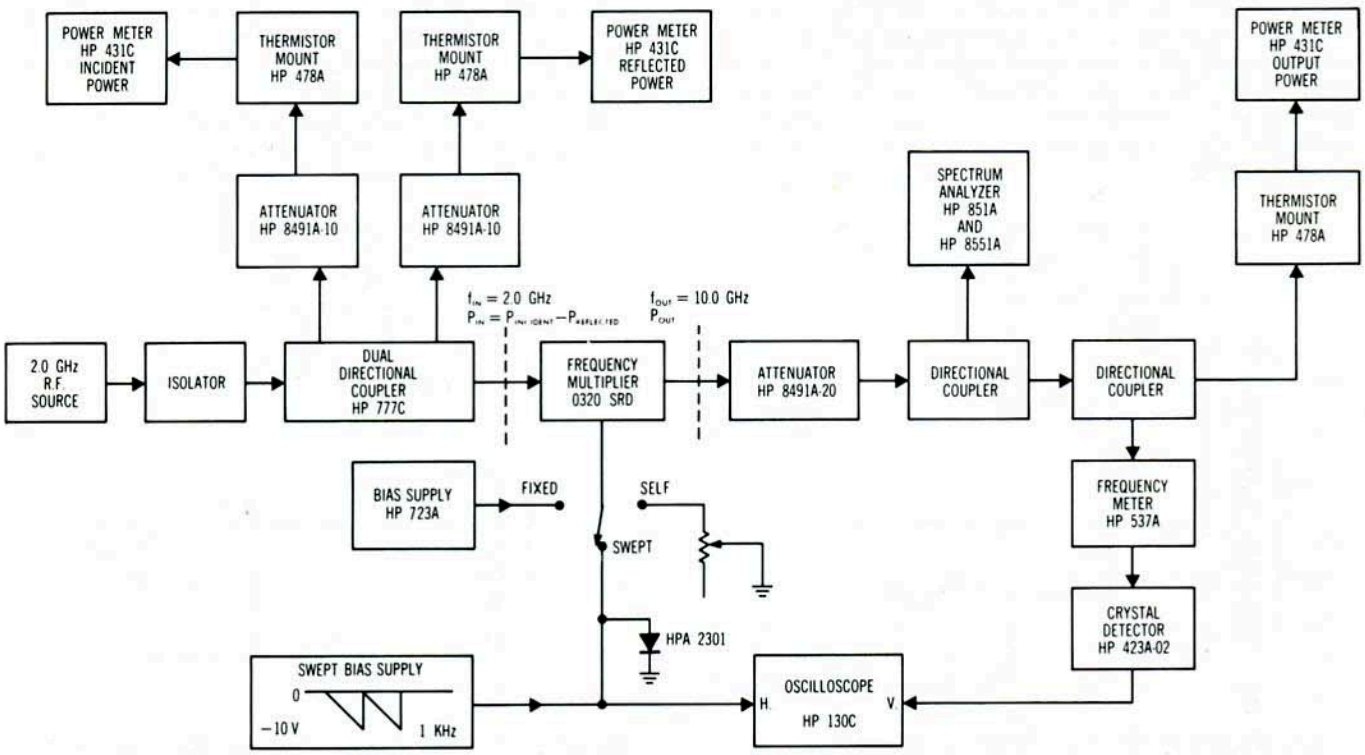


Figure 16. Block Diagram of Output Power Test.

APPENDIX

INTRODUCTION

The purpose of this article is to discuss the Step Recovery Diode and its use in harmonic generators and comb generators. A theory of operation of highly efficient harmonic generating and comb generating circuits will be given, with experimental results and practical circuitry in three frequency ranges: 30 MHz to 300 MHz, 200 MHz to 2000 MHz, and 2 GHz to 10 GHz.

The order of presentation will, of necessity, start with some preliminary description of diode behavior. After establishing the equivalent impedances of the diode as a function of the charge state, it will be incorporated into an "Impulse Generator" circuit. The impulse generator is the key element in the development of an efficient harmonic generator circuit. If the resistive output load of the impulse generator is replaced by a resonant tank circuit, the new spectrum at the output contains the same total energy as the impulse generator but is concentrated around the N^{th} harmonic where the resonating output circuit is tuned. The amount of energy in the N^{th} spectral line is of the order of 60 to 70 percent of the total, and, consequently, highly efficient harmonic generation is possible using that energy alone. Further filtering can be done to reduce the sideband level to the desired degree.

Two types of output resonators have been analyzed: the series L-C network lightly loaded (such that the loaded Q is greater than 3), and the quarter-wave transmission line terminated in an impedance large compared to the R_o of

the line. The latter will be discussed in detail here.

Since the impulse generator is of fundamental importance to this approach, it will be considered first. The analysis of the harmonic generator will then be a simple extension through changes in the form of the output network.

General Approach

The Step Recovery Diode is a highly nonlinear element in that forward stored charge results in low device impedance, while reverse stored charge gives high impedance. Thus, during a normal drive cycle, the impedance will be expected to vary as a function of time, depending on the charge. In the reverse direction, the diode capacitance is almost constant. In the forward direction, almost any amount of charge may be stored at constant voltage. The nonlinear or time varying circuit can, therefore, be replaced by two linear circuits, one with fixed reverse capacitance, the other with a very low, ideally zero impedance. In the time domain, boundary conditions are then applied at the time when the impedance of the diode switches from one state to the other. (Here, we use the current continuity requirement in an inductor.) Proper boundary conditions are necessary to assure that the linear piecewise smooth solutions match at the proper times.

It is assumed in this initial analysis that the diode changes from one impedance state to the other in zero time. This is, of course, not true in practical diodes. However, this analysis has been applied to the design of circuits using diodes having transition times in the 0.1 to 1 nanosecond range with good results when the transition time was less than half the required output pulse width.

IDEALIZATION OF SRD

The ideal Step Recovery Diode differs from the ideal varactor, since it behaves as a two-impedance state, charge controlled switch. Figures 1 and 2 show the ideal characteristics of the varactor and Step Recovery Diode.

The *ideal* varactor characteristic, Figure 1, would have a varying capacitance in the reverse voltage direction, due to the doping density. The movement of the potential wall across the center region uncovers charges continuously, and results in the capacitance change. This capacitance change in the reverse direction is used in varactor multipliers to obtain harmonic currents, which are related to the order of nonlinearity in this capacitance.

The *ideal* Step Recovery Diode characteristic is shown in Figure 2. Here, because of the intrinsic center region, the capacitance, as a function of reverse voltage, would be a

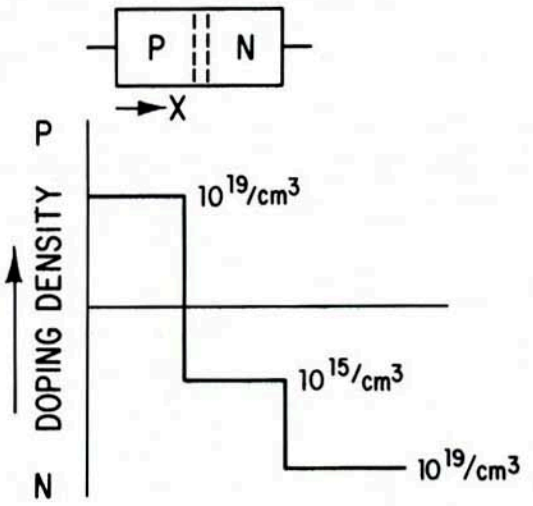


Figure 1a. Doping Profile, Ideal Varactor.

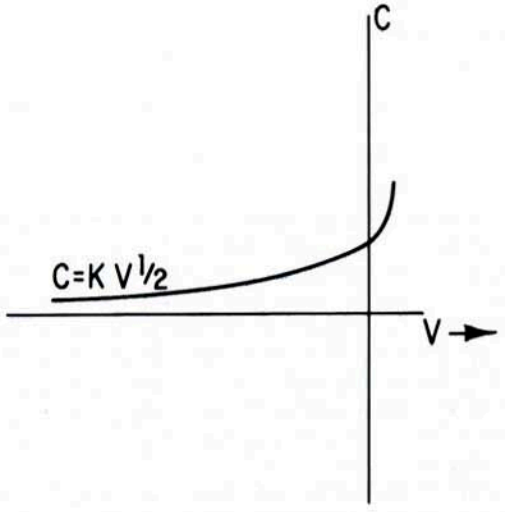


Figure 1b. Ideal Varactor Capacitance Characteristic—Reverse Voltage.

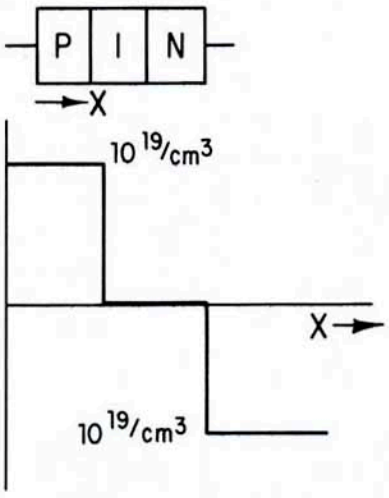


Figure 2a. Doping Profile, Ideal Step Recovery Diode.

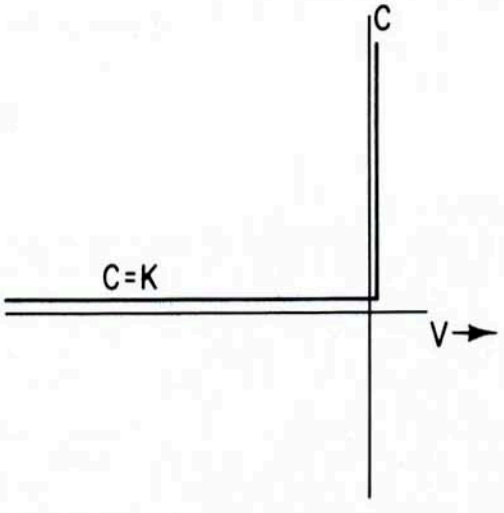


Figure 2b. SRD Ideal Capacitance Characteristic—Reverse Voltage.

constant, while diffusion capacitance in the forward direction is very large. The two well-defined states of the Step Recovery Diode permit a double linear analysis to replace the time varying analysis needed, if the capacitance changes continuously. Figure 3 shows the equivalent circuits used in the Step Recovery Diode analysis. The lossless circuits are used initially to obtain first order design data. Thus, the forward impedance is replaced by a short circuit, the reverse impedance by a fixed capacitor.

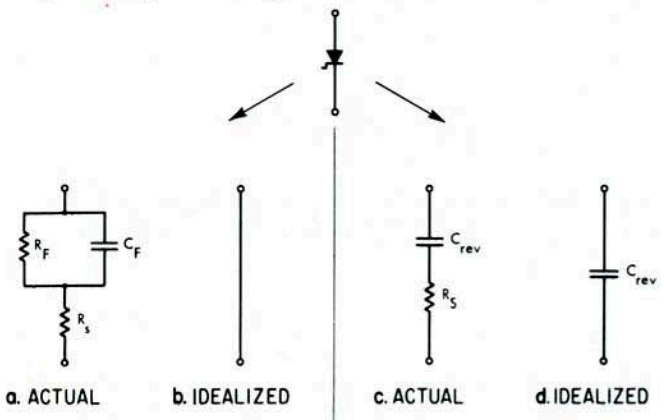


Figure 3a. Forward Conduction Equivalent.

Figure 3b. Depletion Equivalent.

IMPULSE GENERATOR CIRCUIT

The impulse generator circuit (Figure 4) consists of a voltage generator, a drive inductance, the SRD (the time varying element), a bias battery, and the load. There are two equivalent circuits of the impulse generator: one for the time during which the diode is in its low impedance state, and one for the time when the diode is in its high impedance state.

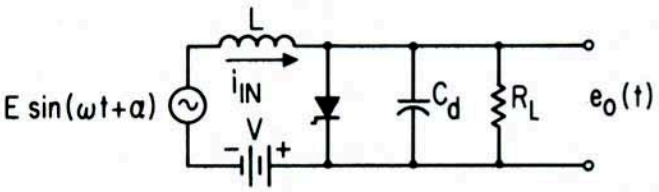


Figure 4a. Impulse Generator Circuit.

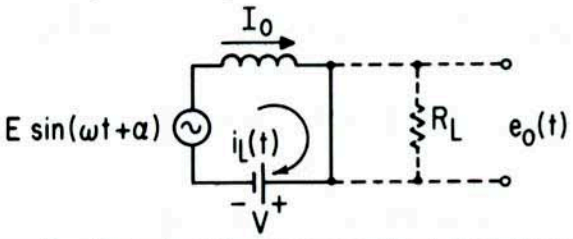


Figure 4b. Equivalent Circuit During Conduction Interval.

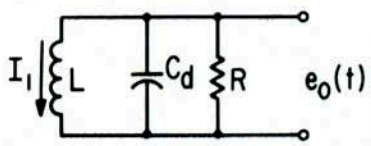


Figure 4c. Equivalent Circuit During Impulse Interval.

The operation of this circuit may be understood by referring to the time sequence shown in Figure 5. Time is represented as a top to bottom sequence going from one equivalent circuit to the other sequentially, starting with the conduction interval. Time is also represented horizontally to show the waveforms produced during the intervals. The first frame shows the conduction interval; the second, the depletion interval; and the third frame shows the second complete cycle.

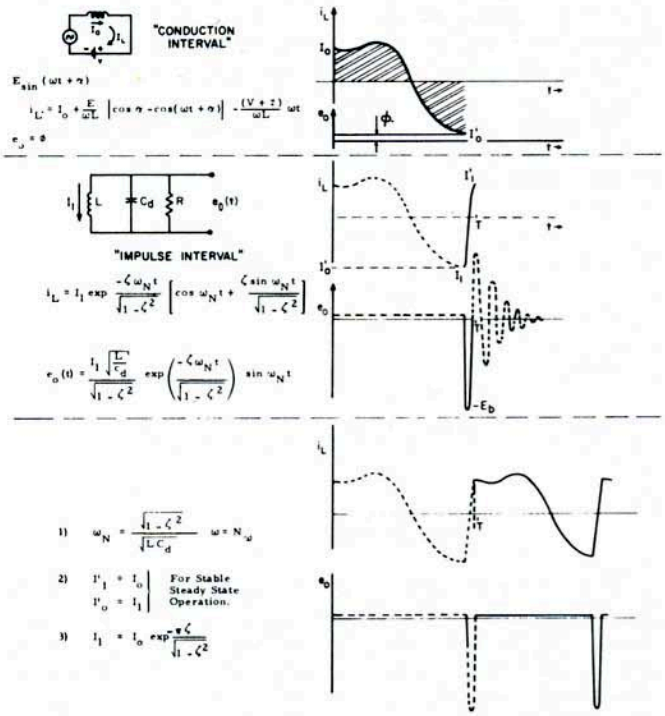


Figure 5. Impulse Generator Current and Voltage Waveforms.

Conduction Interval (Figure 5—1st frame)

During the conduction interval, the equivalent circuit [Figure 4(a)] is an inductance, a battery, and the generator whose voltage is E sin $(\omega t + \alpha)$. We are interested in the input current through the inductance L, and the output voltage appearing across the diode terminals. The network shown has a simple linear network solution for the input current during the conduction interval. It is

$$i(t)_{IN} = I_o + \frac{E}{\omega L}\left[\cos\alpha - \cos(\omega t + \alpha)\right] - \frac{(V + \phi)}{\omega L}\omega t \qquad (1)$$

This current consists of three terms. The first is an initial value, I_o, the second is a sinusoidal component of current, and the third is a linear ramp term due to the bias battery. This current is shown graphically in Figure 6. When the two areas, above and below the $i = 0$ axis, are equal, we can state that all the charge stored in the diode during forward current has been removed. At the instant that this is true, the equivalent circuit will change to the depleted I-layer equivalent, as shown in Figure 4(b).

The voltage across the diode during the conducting phase will simply be the contact potential of the diode (about 0.7 volt for silicon diodes), and subject to the assumption that $R_S = 0$, will not vary.

Depletion ("Impulse") Interval

We have found that by adjusting the bias voltage, V, the stored charge can be returned to zero at the time when the current has its maximum negative value, i.e., $\frac{di}{dt} = 0$.

The voltages across diode and inductor are then both zero. This in turn means that at the beginning of the depletion interval, the instantaneous value of the generator voltage is equal and opposite in sign to the battery voltage, V. We, therefore, neglect the generators during the "impulse" or depletion interval, as shown in the second frame of Figure 5. An initial current, I_1, in the inductor is the significant excitation.

The output voltage, e_o across R_L, and the current, I_L, in the inductor are found from linear circuit analysis with constant parameters R, L, and C.

$$e_O(t) = \frac{-I_1\sqrt{\frac{L}{C}}}{\sqrt{1-\zeta^2}}\, e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\beta t} \sin(\beta t) \tag{2}$$

where

$$\beta = \sqrt{\frac{1-\zeta^2}{LC}} = \omega_N$$

$$\zeta = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

Were it not for the diode, the circuit would ring until its energy was dissipated. However, because diode conduction begins when the diode voltage goes positive, only the first half cycle appears across R_L, as shown in Figure 5. The voltage across R_L is, therefore, half sine pulse during the depletion part of the cycle. The height of the pulse is limited to the breakdown voltage of the diode, and the width is controlled by the R, L, and C. The pulse width, t_o, is

$$t_O = \pi\sqrt{\frac{LC}{1-\zeta^2}} = \frac{\pi}{\beta} \tag{3}$$

and we define the compression ratio, N, by $N = \frac{\beta}{\omega}$.

The current i_L in the inductor, L, during the depletion interval is determined by integrating the voltage that appears across it. This integration results in the following expression for the inductor current

$$i_L(t) = I_1 \exp\left(\frac{-\zeta\omega_N t}{\sqrt{1-\zeta^2}}\right)\left[\cos\omega_N t + \frac{\zeta\sin\omega_N t}{\sqrt{1-\zeta^2}}\right] \tag{4}$$

This current is shown in the second frame of Figure 5.

We now have the input current (inductor current) and the output voltage described functionally over both parts of the drive cycle (Figure 6). For a stable cycle of operation, it is clear that the final current during the conduction phase (I_o') must be equal to the initial current during the impulse phase (I_1)

$$\begin{aligned} I_o' &= I_1 \\ I_1' &= I_o \end{aligned} \tag{5}$$

The relationship between I_1 and I_1' from simple substitution into (4) is

$$I_1' = -I_1 \exp\frac{\pi\zeta}{\sqrt{1-\zeta^2}} \tag{6}$$

It is also necessary that at the end of the conduction cycle, the charge in the diode equals zero. The expression for the charge is formed by integrating i(t) from (1). It is:

$$q(t) = \left(I_o + \frac{E}{\omega L}\cos\alpha\right)t - (V+\phi)\frac{t^2}{2L} - \frac{E}{\omega^2 L}\left[\sin(\omega t+\alpha) - \sin\alpha\right] \tag{7}$$

Since one conduction interval plus one impulse interval is one input period, the conduction interval ends at a time t_1, given by:

$$t_1 = 2\pi/\omega - \pi/N\omega = 2\pi/\omega\,(1 - 1/2N) \tag{8}$$

Evaluating $i(t_1) = I_1$ and $q(t_1) = 0$ gives two equations in E, V, I_o, and α. If it is stipulated that the current in L should be maximum at t_1 for maximum energy storage at the time of switching, we can eliminate V from the two equations. From (1):

$$L\frac{di}{dt} = E\sin(\alpha - \pi/N) - (V+\phi) = 0 \tag{9}$$

then

$$V + \phi = E\sin(\alpha - \pi/N) \quad \text{at } t_1 \tag{10}$$

When this relation is substituted into the expressions for $q(t_1)$ and $i(t_1)$, it is found that both E and I_o can be eliminated by division, and that the equations establish the required value of α. Solution of these equations for the required α gives

$$\tan\alpha = \frac{A_N G + B_N}{C_N G + D_N} \tag{11}$$

where

$$A_N = 2\sin\frac{\pi}{N} + \left(2\pi - \frac{\pi}{N}\right)^2 \sin\frac{\pi}{N} + 2\left(2\pi - \frac{\pi}{N}\right)$$

$$B_N = 2\sin\frac{\pi}{N} - \left(2\pi - \frac{\pi}{N}\right)^2 \sin\frac{\pi}{N} + 2\left(2\pi - \frac{\pi}{N}\right)\cos\frac{\pi}{N}$$

$$C_N = -2 + 2\cos\frac{\pi}{N} + \left(2\pi - \frac{\pi}{N}\right)^2 \cos\frac{\pi}{N}$$

$$D_N = -2 + 2\cos\frac{\pi}{N} - \left(2\pi - \frac{\pi}{N}\right)^2 \cos\frac{\pi}{N} - 2\left(2\pi - \frac{\pi}{N}\right)\sin\frac{\pi}{N}$$

$$G = \exp\left\{\frac{\pi\zeta}{\sqrt{1-\zeta^2}}\right\}$$

The angle, α, is plotted in Figure 7 for a range of N and several values of damping factor, ζ. It is a function of N, R, L, C and determines the bias voltage through the requirement that the total input voltage be zero at the beginning of the impulse interval.

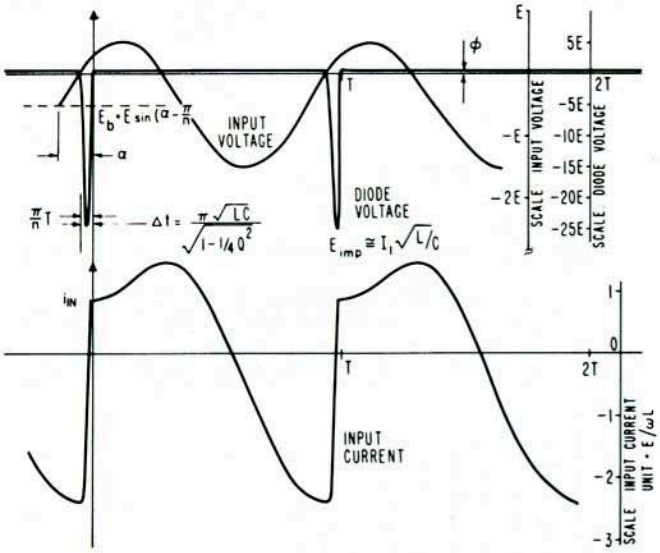


Figure 6. Typical Diode Waveforms.

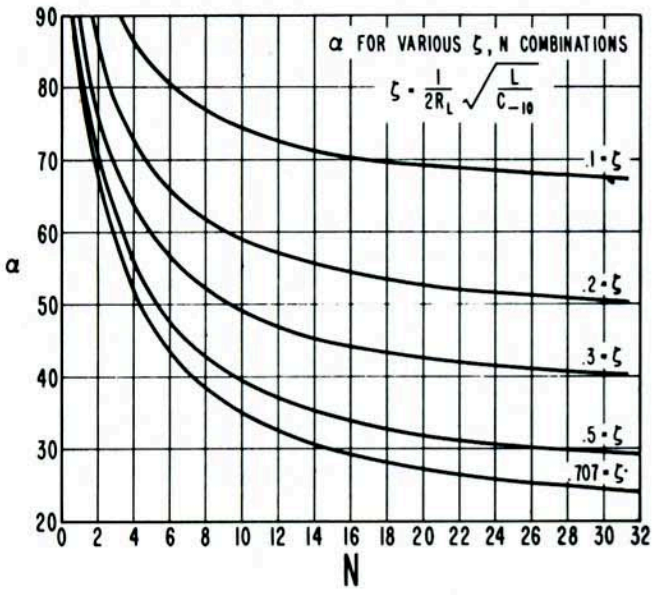


Figure 7. Multiplier Operation Angle.

Input Impedance

We define the input impedance at the input frequency using the equivalent circuit shown in Figure 8. The procedure is to resolve the fundamental component of input current into "in phase" and "quadrature" components and defines R_{in} and X_{in} as the ratios of the input voltage at the fundamental frequency to these currents.

The expressions for the input current are different for the conduction interval and the impulse interval. Consequently, each component must be broken into two integrals:

$$I_I = \frac{\pi}{\omega}\int_o^{m/\omega} i_{cond}(t)\sin(\omega t+\alpha)\,dt + \frac{\pi}{\omega}\int_{m/\omega}^{2\pi/\omega} i_{IMP}(t)\sin(\omega t+\alpha)\,dt = I_{condI} + I_{IMPI} \quad (12)$$

$$I_Q = \frac{\pi}{\omega}\int_o^{m/\omega} i_{cond}(t)\cos(\omega t+\alpha)\,dt + \frac{\pi}{\omega}\int_{m/\omega}^{2\pi/\omega} i_{IMP}(t)\cos(\omega t+\alpha)\,dt = I_{cond_Q} + I_{IMP_Q}$$

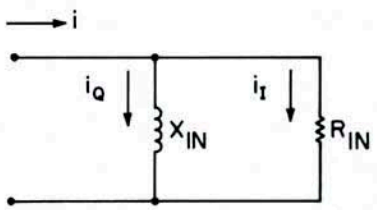
where $M = 2\pi - \pi/N$.

The input resistance and reactance are then defined as:

$$R_{in} = E/I_I \quad (13)$$

$$X_{in} = E/I_Q$$

Approximate solutions to the above integrations are shown in Figure 8.



EQUIVALENT INPUT IMPEDANCE

$$i_I = \frac{\omega}{\pi}\int_0^{\frac{2\pi}{\omega}} i\sin(\omega t+\alpha)\,dt$$

$$i_Q = \frac{\omega}{\pi}\int_0^{\frac{2\pi}{\omega}} i\cos(\omega t+\alpha)\,dt$$

$$R_{IN} = \frac{\omega L}{2\cos\alpha\,\sin(\alpha-\frac{\pi}{N})}$$

$$X_{IN} = \frac{\omega L}{1+2\sin(\alpha-\frac{\pi}{N})\sin\alpha}$$

Figure 8. Equivalent Circuit for Input Impedance Calculation.

In these approximations, the contributions to the integrals during the impulse interval have been ignored, leading to errors of the order of 1/N. The integration was carried out numerically. In either case, the input impedance is related to ωL,

$$\omega L = (1-\zeta^2)X_{di}/N^2 \qquad (14)$$

$$X_{di} = 1/\omega C$$

The input impedance is:

$$R_{in} = \frac{(1-\zeta^2)X_{di}}{N^2} R_1 \qquad (15)$$

$$X_{in} = \frac{(1-\zeta^2)X_{di}}{N^2} X_1$$

where, R_1 and X_1 are the results of the integrations above, and are plotted in Figure 9.

The input impedance, defined at the input to the drive inductance L, then consists of a resistance and an inductance in parallel. The inductance may be resonated at the input frequency by a simple capacitor, in the practical case, leaving a simple resistive input to be matched.

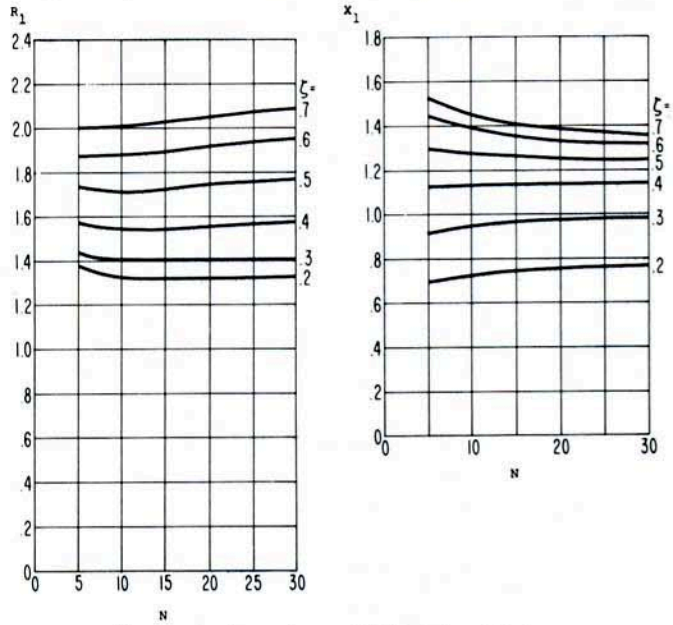


Figure 9. Impedance Multiplying Factors.

Power Output

The power output is found by determining the reduction of stored energy in L. It is

$$P_o = f_i \times \frac{L}{2}\left[I_1^2 - I_0^2\right] = \frac{f_i L I_1^2}{2}\left[1 - e^{-2\pi\zeta/\sqrt{1-\zeta^2}}\right] \qquad (16)$$

If the damping factor is chosen to be 0.5, which gives good power output without substantial pulse widening, the power output becomes

$$P_o \simeq 1.5\, E_b{}^2 f_i\, C \qquad (17)$$

This is the maximum useful power that can be put into the impulse generator; any additional power input supplies losses in the diode and network.

This result is independent of n and confirms the Manley-Rowe relation for nonlinear reactive devices.

Spectrum of Impulse Generator

The spectral content of the impulse can be found by Fourier analysis. Assuming that the impulse formed is a perfect half sine pulse, of loaded height equal to E_b, the amplitude, C_n, of the voltage in the frequency line, nf_{in}, can be found. It is:

$$C_n = C_o \frac{\cos\frac{\pi}{2}\left(\frac{n}{N}\right)}{1-\left(\frac{n}{N}\right)^2} \qquad (18)$$

$$\text{where} \quad C_o = \frac{2E_b}{\pi N}$$

A plot of $\frac{C_n}{C_o}$, the Fourier amplitude coefficients, is shown in Figure 10. The Fourier integral, which is the envelope of the lines shown, has its first zero at $3Nf_{in}$. Thus, frequency components of reasonable amplitude continue well beyond the frequency, Nf_{in}, where the pulse is one-half cycle long.

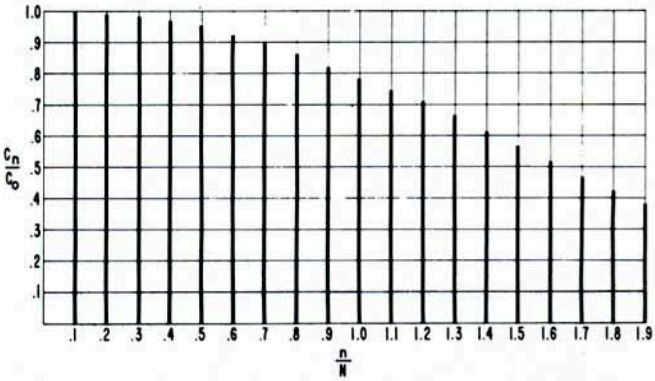


Figure 10. Fourier Coefficients for Impulse Waveforms.

DAMPED WAVEFORM CIRCUIT

The prototype circuit shown in Figure 11 can be used to shift the spectrum to peak at Nf_{in}. The operation of this circuit is similar to the impulse generator, except that the resistance across C_{diode} is now R_o, the characteristic impedance of the line. If the terminating resistance is equal to R_o, i.e., it is matched, then the impulse is generated as before and delayed by the propagation time down the line.

If $R_L > R_o$, some of the energy in the pulse is reflected to the diode and arrives after a time, t:

$$t = \frac{2l}{v} \qquad (19)$$

where

l - is line length

v - velocity of propagation.

If t is exactly equal to the pulse width, the diode will close just as the impulse returns from R_L, locking the energy of the impulse onto the line and making it resonant. This leads to the conclusion that $\ell = \frac{\lambda_N}{4}$. This circuit is shown in Figure 11.

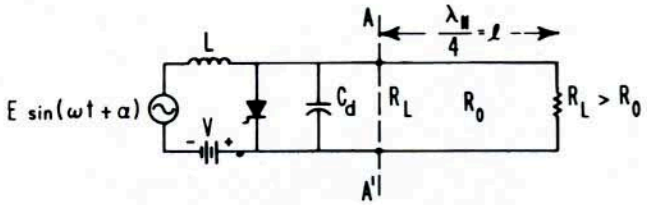


Figure 11a. Damped Ringing Waveform Circuit

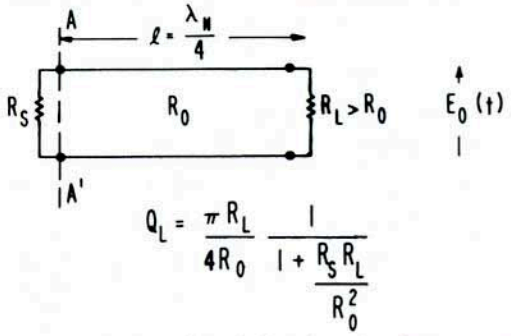


Figure 11b. Output Circuit During Conductance Phase.

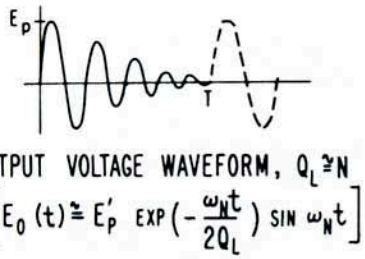


Figure 11c. Output Voltage Waveform.

When the traveling reflected pulse hits the closed diode, it will be reflected with inverted phase ($\Gamma = -1$ for short circuit). It travels toward load where it is partially dissipated, partly reflected without inversion. The process continues forming a damped wave at the termination. The functional form of this resulting wave is:

$$E_o(t) = (1 + \Gamma)E_p e^{-\alpha t} \sin \beta t \qquad (20)$$

where

$$\alpha = \frac{N\omega}{2Q}$$

$$\beta = N\omega$$

Γ = Reflection coefficient of R_L relative to R_o.

If $Q \simeq N$, the damped waveform just damps completely in one input period. Thus the impulse energy is delivered to the load in one input period rather than one pulse width. The same power reaches the load, but the spectral distribution is changed.

The spectral content of the damped waveform of Equation (20) may also be found using Fourier analysis. The amplitude, C_n, of the voltage in the N^{th} line is given by:

$$C_n = \frac{\left(\frac{1+\Gamma}{2}\right)\left(\frac{E_b Q}{\pi N}\right)}{\sqrt{\left(\frac{1}{2}\right)^2 + Q^2\left(1 - \frac{n^2}{N^2} + \left(\frac{n}{N}\right)^2\right.}} \qquad (21)$$

This function is plotted in Figure 12.

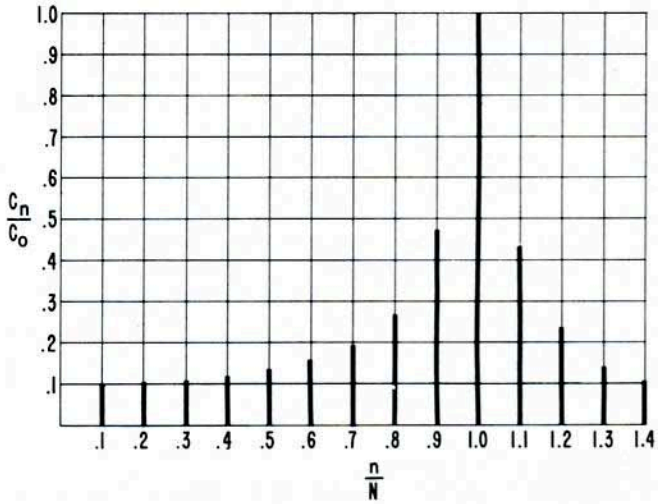


Figure 12. Fourier Coefficients for Damped Ringing Waveforms.

The maximum value of the envelope of the spectrum appears at the frequency, ω_M:

$$\omega_M = N\omega \sqrt{1 - \frac{1}{4Q^2}} \qquad (22)$$

For large Q, this would be at $N = n$. The amplitude of the C_N, maximum, line is:

$$C_N = \frac{E_p Q}{\pi N} \qquad (23)$$

The amplitude of this line has been increased by the factor $\frac{2}{\pi}Q$ over the amplitude of the N^{th} line in the impulse generator case. The energy, formerly spread over a wide spectrum, has now been concentrated in the vicinity of $N = n$.

HARMONIC GENERATION

The damped waveform may now be filtered conventionally to obtain a CW output at $N\omega_{in}$, with little loss due to rejected sideband energy. A harmonic generator, as shown in Figure 13, consists of an impulse generator and the quarter wave line coupling into the high electric field end of a bandpass filter. This establishes the damped ringing waveform at the end of the quarter wave line. The filter reflects the unwanted sidebands and this reflected energy goes back out the input, changing the input impedance slightly until a stable operating point has been reached.

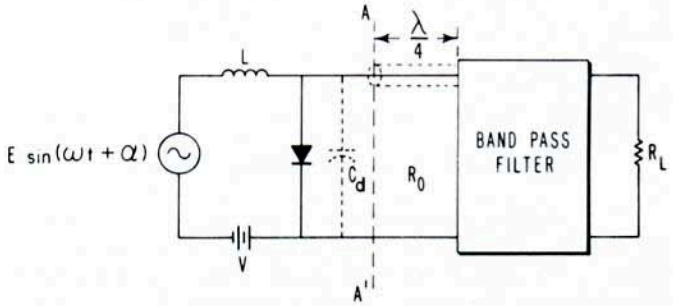


Figure 13. CW-Harmonic Generator Circuit.

PRACTICAL DESIGNS OF IMPULSE GENERATORS AND HARMONIC GENERATORS

In this section, we discuss the results achieved using the "Shunt Mode" theory of the Step Recovery Diode in three frequency ranges. The circuits discussed are tabulated in Table I.

TABLE I

Drive Frequency	Impulse Generator Pulse Width	Harmonic Generator Output Frequency
30 MHz	1.7 nanoseconds	300 MHz
200 MHz	250 picoseconds	2000 MHz
2000 MHz	<100 picoseconds	10,000 MHz

30 MHz Impulse Generator

An impulse generator, driven at 30 MHz with n = 10, was built using the circuit shown in Figure 14. It was expected that at this frequency the stray reactances and resistances of the circuit could be neglected, and that nearly ideal behavior, as described above, would result. This was the case. The overall efficiency of impulse production was 80%. The input resistance was calculated and measured and with agreement to within 10%. The input reactance was calculated, using the approximate expressions, and was different by a factor of two from the value found experimentally.

Figure 14 also shows the waveforms measured for the diode voltage and the input (inductor) current. The impulse generation is striking. The predicted current waveform has the shape B in Figure 14, rather than the observed dip at A. The reason is that the practical circuit has a finite generator resistance, rather than the zero impedance voltage generator assumed in the computation. Including the generator resistance in the computation makes the current agreement very close.

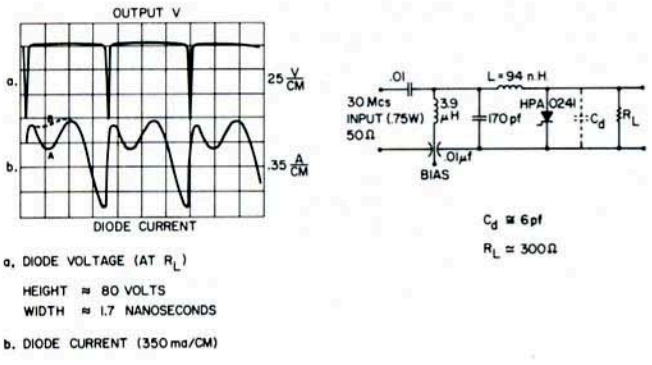
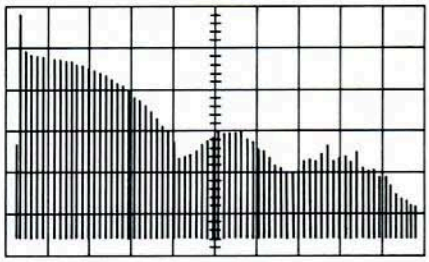


Figure 14. 30 MHz Impulse Generator.

The spectrum associated with the impulse train is shown in Figure 15. The first zero of the spectrum was at 860 MHz. This predicts that the pulse width would be 1.75 nanoseconds. The pulse width measured on a sampling scope was 1.8 nanoseconds.



Spectrum display of 30 mcs comb generator

Power in first line	= 50 mw
Total power output	= 570 mw
Power input	= 725 mw efficiency = 80%
First zero of spectrum	= 860 mcs. τ = 1.75 ns
Measured τ (direct)	= 1.8 ns
V_{bias}	= 2.1 volts
E(excitation peak amplitude)	= 6.25 volts
α(calculated)	= 48°
V(calculated) = V_{bias} + ϕ	= -E sin 30° = 3.13 volts
V_{bias}(calculated)	= 2.43 volts

Figure 15. Spectrum Display of 30 MHz Comb Generator.

200 MHz Impulse Generator

A cross-sectional drawing of an impulse generator (n = 10) driven at 200 MHz is shown in Figure 16. The diode is driven through an inductance formed by the short length of coax line. The input reactance is matched out by a capacitor, C_T. (See Figure 17.) Theoretically, the value of C_T is:

$$C_T = N^2 C_d \left[1 + 2 \sin\left(\alpha - \frac{\Pi}{N}\right) \sin \alpha\right] \qquad (24)$$

In practice, this predicted value has generally been off by a factor of about two. (Actual value, one-half C_T.) The dynamic input resistance is matched, using a low pass matching filter. Bias is obtained either by an external bias supply or by self bias. The self biasing problem will be discussed in more detail in the next section.

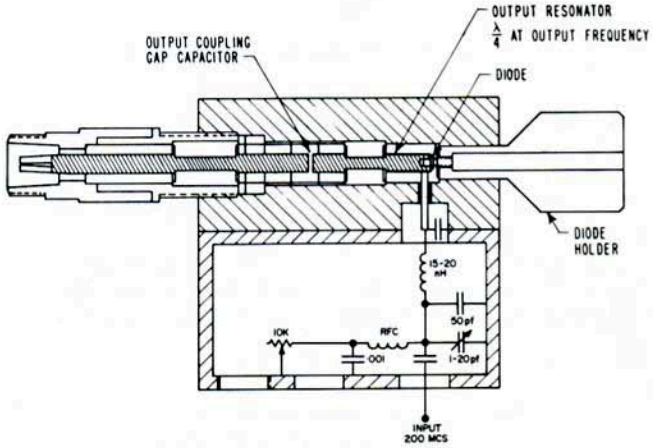


Figure 16. Physical Layout of a Damped Waveform Generator.

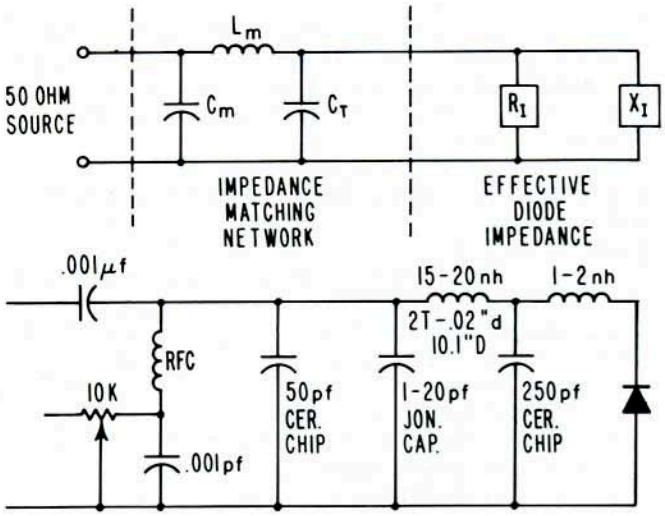


Figure 17. Input Matching Network—values shown are for 200 MHz drive frequency, 300-450 picosecond pulse width.

The 200 MHz impulse generator produces an impulse of about 80 volts amplitude and a width of 350-400 picoseconds. The conversion efficiency of this impulse production is of the order of 25%, as can be seen in Figure 18. The power output is seen in Figure 18 to be about 3.8 watts.

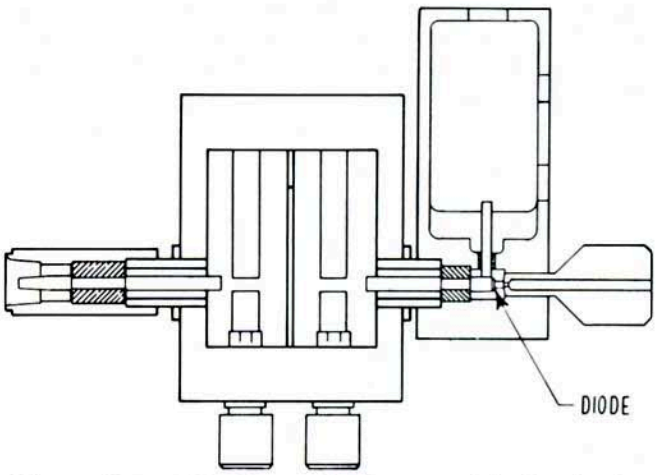


Figure 18. 2 GHz Harmonic Generator Circuit—the impulse generator is capacitively coupled, through the quarter wave line to the high E field point in the bandpass filter.

CW Harmonic Generation; 200 MHz to 2 GHz

Figure 18 is a cross-section of the harmonic generator built for n = 10, 200 MHz to 2 GHz. Coupling to the filter is accomplished by using the quarter wave line to lightly couple to the high E field end of the filter. (The high field end of the filter is also the high impedance end; this will result in the appropriate reflection for the impulse, as was described in the section on the damped ringing waveform.)

The output spectrum of the 2 GHz harmonic generator is controlled by the number of filter elements. Here, the rejection of the 1800 MHz and the 2200 MHz lines was greater than 55 dB.

The CW power output is shown in Figure 19, together with the measured power output for the impulse generator. The maximum output power achieved was 2.8 watts at 2 GHz. Note that the efficiency of converting the impulse into CW power (via the nonlinearity of the diode) is of the order of 60% to 70%. This is an excellent agreement with the theoretically estimated maximum of about 70%.

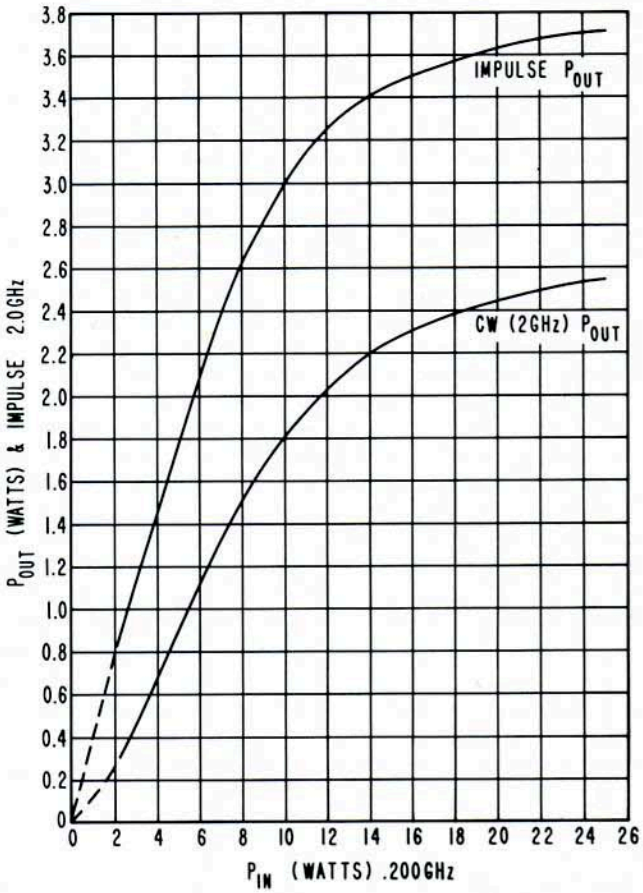


Figure 19. Measured Impulse and Harmonic Generator Efficiency Curves—when the impulse generator of Figure 16 is connected to a filter, as in Figure 18, approximately 70% of the total energy available in the impulse can be extracted as CW at N x f_{in}.

2 GHz to 10 GHz Harmonic Generator

A "times five" multiplier, going from 2 GHz to 10 GHz, is shown in Figure 20. The principle of operation of this circuit is the same as for the 200 MHz to 2 GHz multiplier, although slightly different in detail.

A quarter-wave matching section is used to match the generator impedance to the dynamic input resistance of

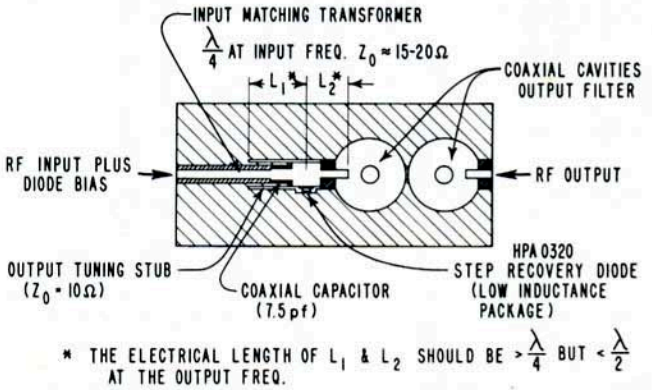


Figure 20. Cross Section of 10 GHz Multiplier (X5).

the multiplier. A coaxial capacitor of 7.5 picofarads is used to tune out the inductive reactance seen looking into the multiplier. The value of this capacitance was estimated using Equation (24). The diode used was an HPA 0320 diode. This diode has reduced inductance and is optimized for use in X-band (8-12 GHz).

Although the diode has a small lead inductance (of the order of a few hundred picohenries), it was still necessary to provide some compensation for it in the circuit in the form of a re-entrant stub resonant at the output frequency. The diode is coupled to the output cavity by means of the quarter-wave line, as was shown before. The quarter-wave line couples into the high E field point of the filter.

The maximum power output of the 10 GHz multiplier was 350 milliwatts when driven with 5 watts at 2 GHz. The multiplier can be tuned, at a reduced (100-125 mW output) power level, so that it has a broad, well controlled frequency response (Figure 21). In Figure 21, the response shown is the detected output of the multiplier when the input is swept. The response shown is virtually a duplication of the response of the bandpass filter when measured separately. This fact leads to the conclusion that the multiplication process might be a potentially broadband one. Figure 22 adds evidence to this conclusion. The output of the multiplier was adjusted over the wide frequency range shown by simply tuning the output bandpass filter.

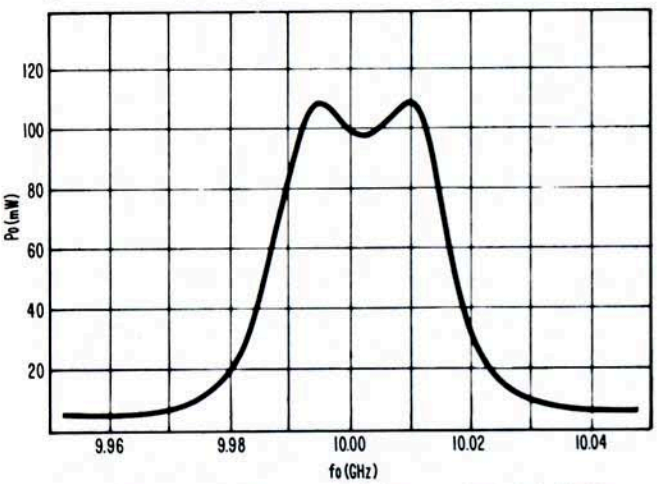


Figure 21. Swept Response of the 10 GHz Multiplier.

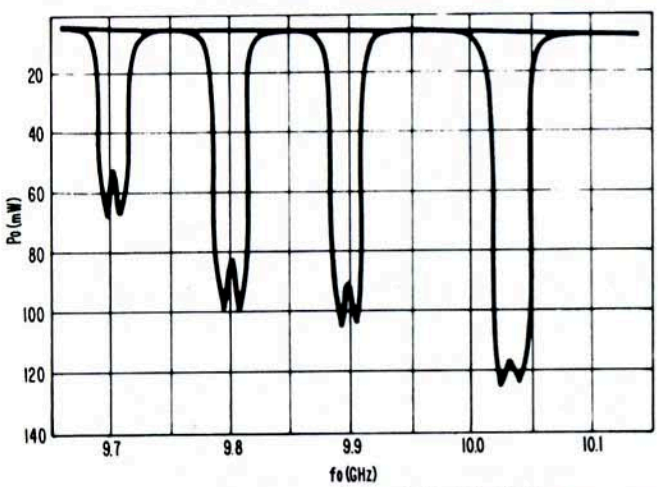


Figure 22. Swept Response of 10 GHz Multiplier—center frequency readjusted by changing tuning of filter along—multiple exposure.

The maximum tunable frequency of the filter was 10.05 GHz and no higher frequency data was taken. The output shown though indicates a half "tuning bandwidth" of 350 MHz. Hence, a total tuning bandwidth of 700 MHz has been assumed possible.

The variation of the output over the wide tuning range may be due to the reactances of the input matching network and the transformer.

Multiplier Stability

The X-band multiplier was particularly interesting in the stability data that resulted. As was mentioned earlier, the output could be adjusted to be very high power (350 milliwatts with 2.5 watts input—almost fully saturated), or lower power with broad bandwidth. When tuned to highest possible output power there was a tendency to oscillate off band (if input frequency was changed after optimizing).

At the lower power output, the output was stable and it was possible to temperature compensate the multiplier.

TEMPERATURE COMPENSATION

The temperature sensitive parameter in the SRD is the lifetime, τ, of the minority carriers in the I-layer. Since the lifetime determines the dc rectification efficiency, it is related to the bias resistance required.

Figure 23 shows the diode voltage. The *time average* of the voltage around the input loop (containing the battery, SRD, generator, and L) *must equal V*, the applied dc voltage. The average voltage across the generator and inductor must be zero, by definition, and the general shape of the diode voltage is known to be as in Figure 22. (An ideal half sine pulse is assumed.) The resulting relation between the impulse height and bias is:

$$V + \phi = \frac{E_{imp}}{\pi N} \tag{25}$$

This voltage can be generated by the rectification of the SRD.

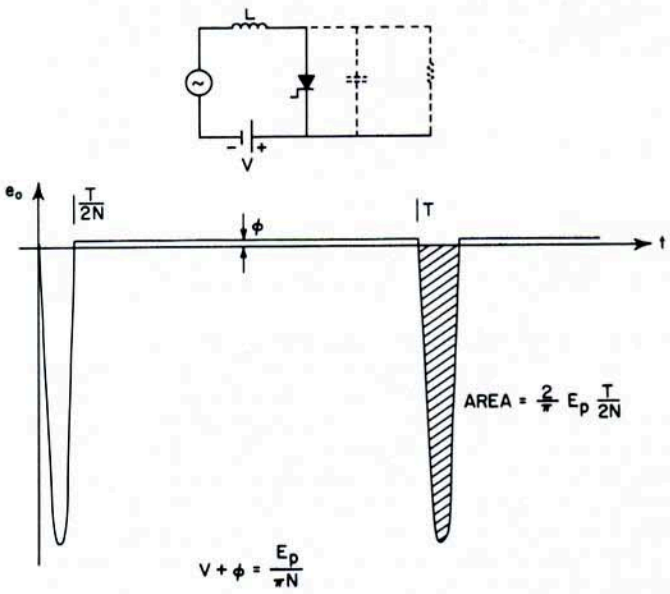


Figure 23. Simplified Bias Relationships.

The relation between the ac and dc current is derived in Figure 24. In a Step Recovery Diode driven by a sinusoidal current, the average storage time is $\frac{\pi}{\omega}$. That is, on the aver-

age, charge put into the diode will come back out a half cycle later (assuming recombination is relatively small). The recombined charge is then:

$$\Delta q = q_o \frac{t_s}{\omega} \tag{26}$$

Δq - recombined charge

q_o - average charge stored

t_s - storage time

The average charge is found by finding the area of the half sine wave.

$$q_o = \frac{I_{pac}}{\omega} \tag{27}$$

I_{pac} - peak ac current

The dc current, controlled by recombination, then is:

$$I_{dc} = \frac{q_o}{2\tau} = \frac{I_{pac}}{\omega\tau} \tag{28}$$

Having the dc current, we should be able to evaluate the resistance, R_b, to establish the required bias voltage. Figure 24 shows the derivation of R_b:

$$R_b = \frac{E_b\,\omega\tau}{\pi N\, I_{pac}} \tag{29}$$

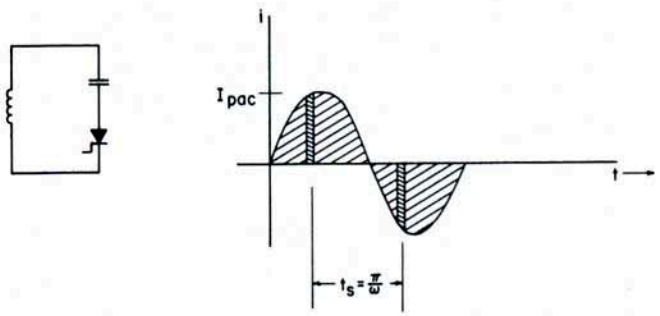
$$e_o(t) = -\frac{I_1\sqrt{\frac{L}{C}}}{\sqrt{1-\zeta^2}}\, e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\beta t} \sin \beta t \tag{30}$$

The peak voltage is not to exceed the breakdown of the diode. Approximately:

$$e_o(t)\,|_{max} = I_1\sqrt{\frac{L}{C}} = 2I_{pac}\sqrt{\frac{L}{C}} = E_{imp} \tag{31}$$

I_1 corresponds to approximately 2 I_{pac} (waveform of Figure 6). The bias resistance is then:

$$R_b = \frac{2\tau}{\pi N^2 C_{rev}} \tag{32}$$



$$\Delta q = q_o \frac{t_s}{\omega}$$

$$q_o = \frac{2\,I_{pac}}{\omega}$$

$$I_{DC} = \frac{q_o}{2\tau} = \frac{I_{pac}}{\omega\tau}$$

Figure 24. Lifetime Relationships.

The bias resistance is proportional to τ, so they should have the same temperature coefficient to make bias voltage independent of temperature. In Figure 25, lifetime is seen to be almost linearly increasing with temperature.

SELF BIAS RELATIONSHIPS

$$\phi + V = \frac{E_b}{\pi N} = I_{DC}\, R_b$$

$$R_b = \frac{E_b\,\omega t}{\pi N I_{pac}}$$

$$I_{pac} = \frac{E_b}{2X_{do}}$$

$$R_b = \frac{2t}{\pi N^2 C_{rev}}$$

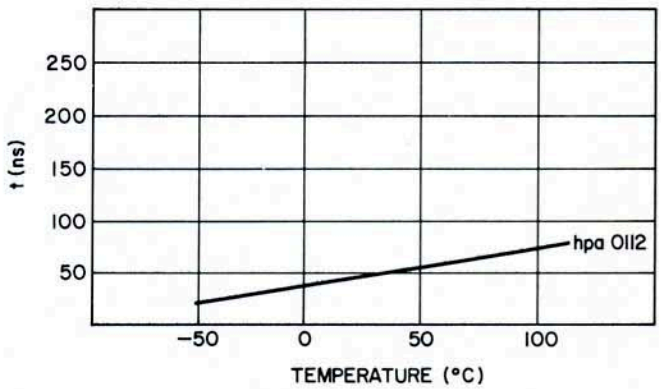


Figure 25. Self Bias Lifetime Relationships for Impulse Generator—the curve shows how the lifetime of a typical (HPA 0112) Step Recovery Diode behaves as a function of temperature.

Temperature Performance, X-Band Multiplier

Temperature data was taken on the X-band multiplier, plotting the optimum bias resistance needed as a function of the temperature. The resistance required is shown in Figure 26. A 900-ohm Sensitor was used to approximate this required behavior.

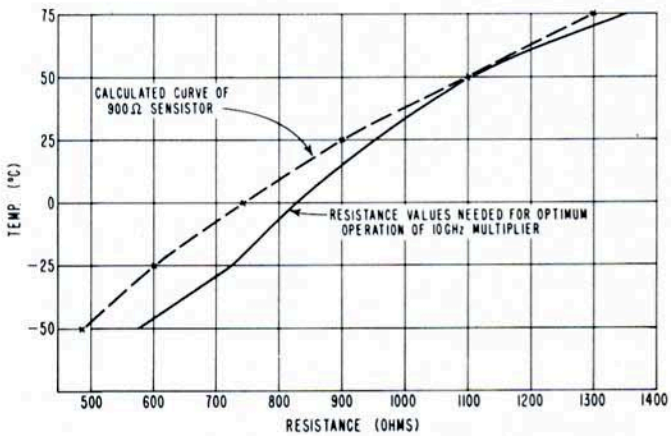


Figure 26. Measured Required Bias Resistance Versus Temperature.

The resulting performance of the multiplier is shown in Figure 27. At 100 milliwatts output, the power output was 100 milliwatts $\pm$ 0.2 dB from $-$ 50°C to $+$ 75°C (no retouching or tuning).

A comment on narrow band filtering is in order here. It

was necessary to temperature compensate the center conductors of the coaxial bandpass filter. It was found that the length of these conductors varied by 0.0003 inch over temperature. This corresponded, at 10 GHz, to 1.5 bandwidths! Invar center conductors, plated for low loss, solved this problem.

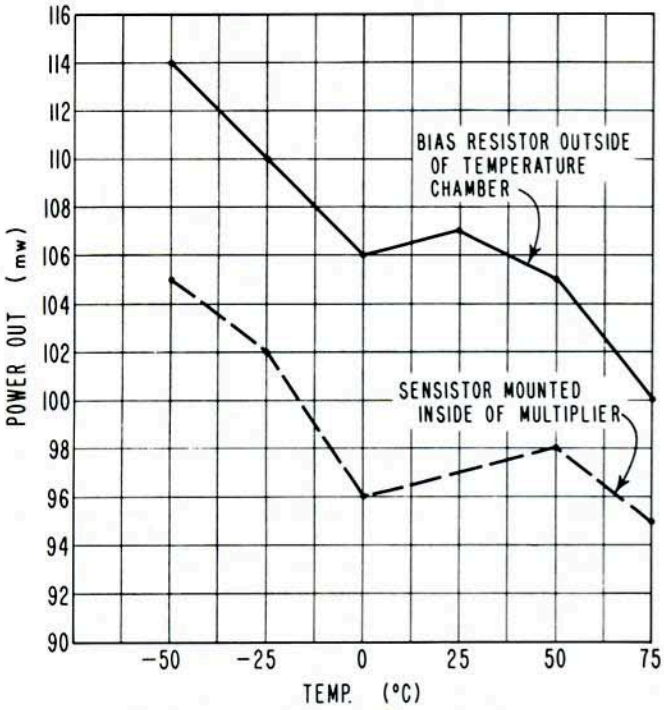


Figure 27. Power Output X-band Multiplier—(no readjustments) versus temperature when self biased with temperature compensating sensitor of Figure 26.

LOSSES IN THE MULTIPLIER

The basic loss mechanisms in multipliers are:

1. Input and output circuit losses (finite unloaded Q's).
2. Loss due to diode series resistance.
3. Recombination losses.
4. Transition losses.

Input and Output Circuit Losses

Input and output circuit losses are controlled by the Q's of the input and output networks. The input loaded Q can be quite low, as far as the multiplier is concerned. The output loaded Q is determined generally by spectral purity requirements. High unloaded Q's are often required to achieve low loss.

Diode capacitance partially determines output losses, since it determines the impedance level of the multiplier. We have found that in the quarter-wave coupled harmonic generator, the damping factor should be approximately 0.35. This means that

$$Z_o \cong 1.4\, X_{do} \tag{33}$$

where Z_o = quarter-wave coupling lines characteristic impedance

X_{do} = diodes capacitance reactance at output frequency

Extremely small values of Z_o, less than about 5 ohms, are to be avoided because of increased loss.

Loss Due to Diode Forward Resistance

The diode forward resistance under forward charge storage is a principal contributor to multiplier losses. The loss has been computed and takes the form (for $Q_L \simeq N$)

$$\alpha = -10 \log \left|1 + 2N^2 \frac{f_{in}}{f_c}\right| \text{ dB} \tag{34}$$

$$f_c = \frac{159}{R_f C_{-10}}$$

R_f - diode forward resistance

C_{-10} - diode capacitance at -10 volts

Losses Due to Finite Lifetime

Recombination effects are describable by an ordinary electronic Q, where:

$$Q = \omega\tau \tag{35}$$

τ — lifetime of minority carriers in I-layer

Since loss due to recombination decreased with increasing frequency, only the input frequency is important. Power loss per cycle is

$$P_{recomb} = 10 \log \left(1 + \frac{1}{f_{in}\tau}\right) \tag{36}$$

As discussed in Section VIII, this loss is often used to bias the diode.

Transition Losses

When the diode has been driven into the forward charge storing state, the device impedance is extremely low, as has been discussed. The time required for the device to change from that low impedance level to a very high impedance is the transition time. This subject is not thoroughly understood at this time. It is known that there are diodes which have transition times less than 100 picoseconds, but the ultimate speed capability has yet to be determined. The thicker the diode I-layer, the higher the breakdown voltage and the longer the transition time. This relation, empirically arrived at, requires that:

$$E_b < 140/\sqrt{f_o(\text{GHz})} \tag{37}$$

Thus, at 10 GHz, $E_b < 45$ volts and at 2 GHz, $E_b < 100$ volts. The smaller the breakdown voltage, the lower will be the losses due to finite transition time. This means that one can trade off power output (which is proportional to E_b^2) and efficiency to some extent. Since diode capacitance would increase for lower breakdown voltages, but we cannot permit very low impedances, the area must be reduced for higher frequency operation. Since this increases the reactance of the diode, it further reduces power handling.

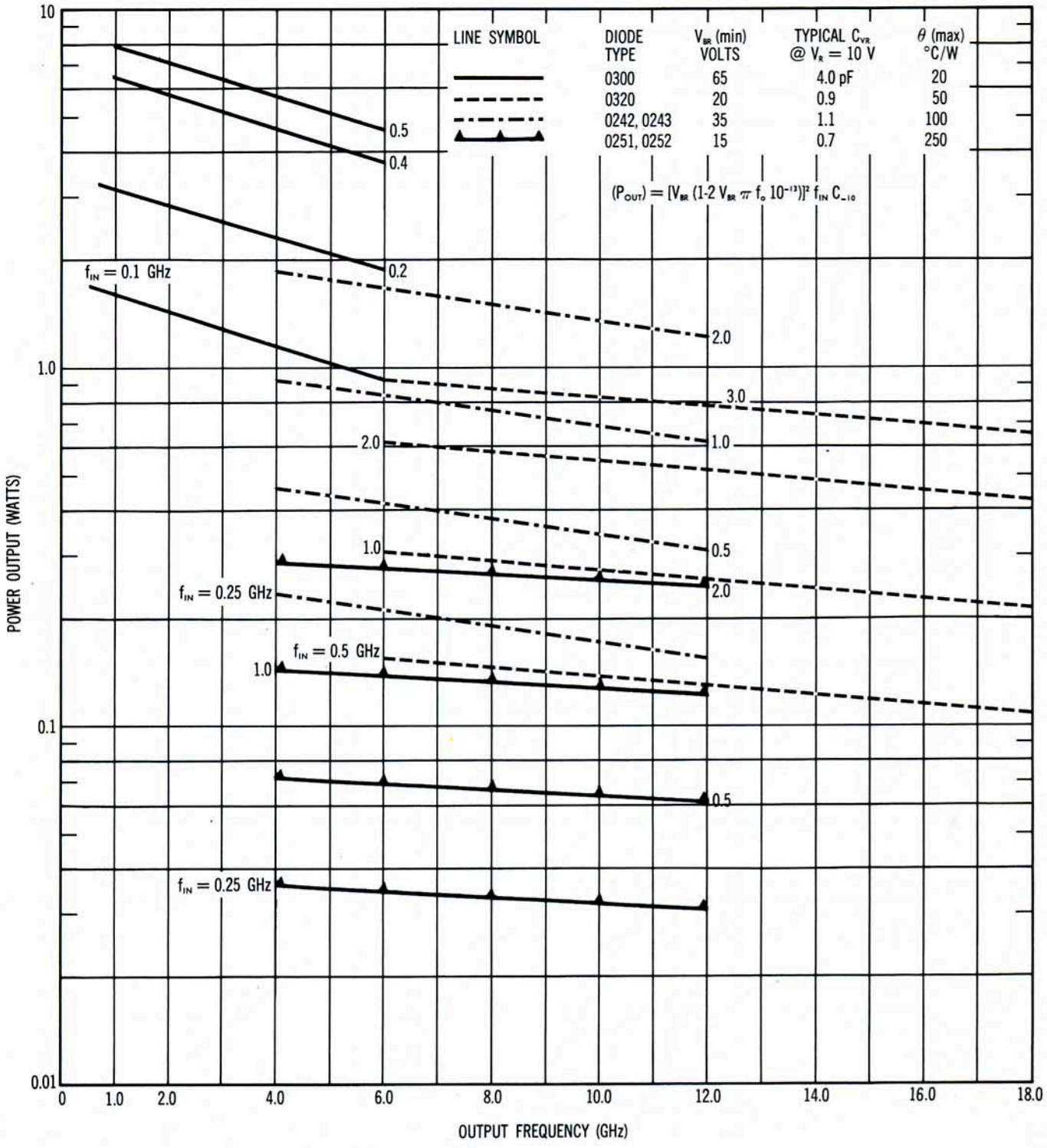


Figure 2. Theoretical Power Output Versus Output Frequency for HPA Step Recovery Diodes.

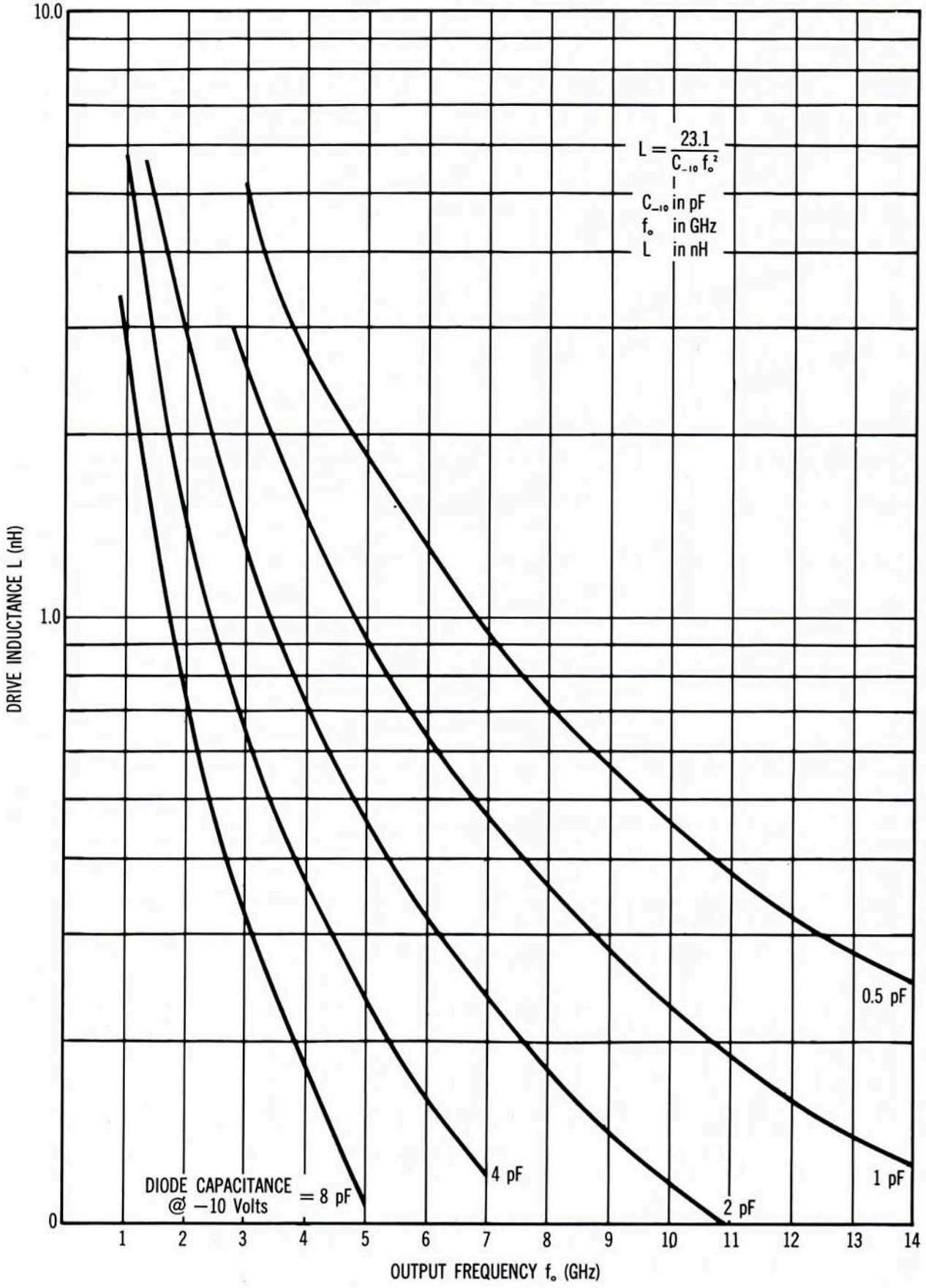


Figure 5. Drive Inductance L Versus Output Frequency f_o.

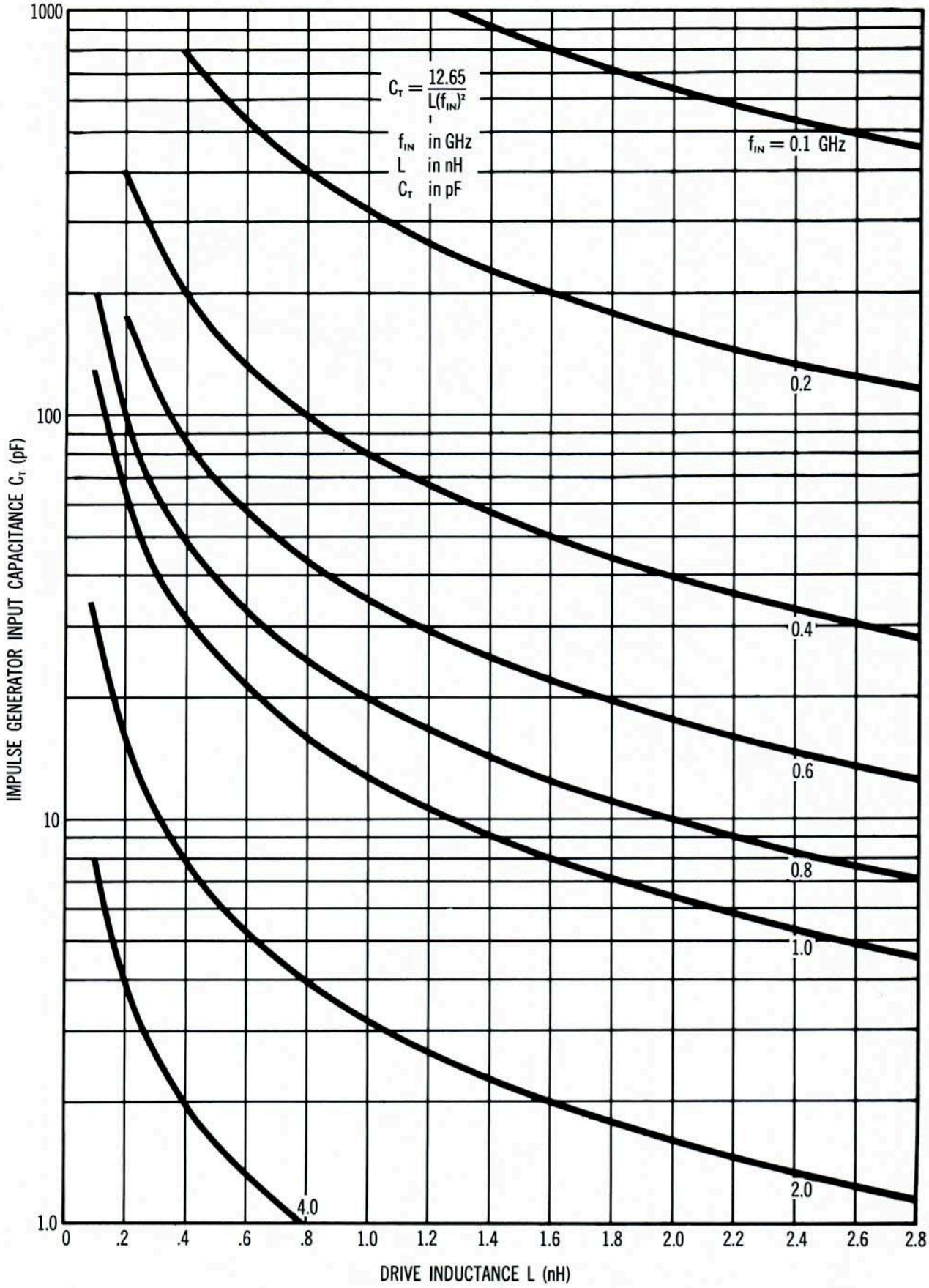


Figure 6. Impulse Generator Input Capacitance C_T Versus Drive Inductance L.

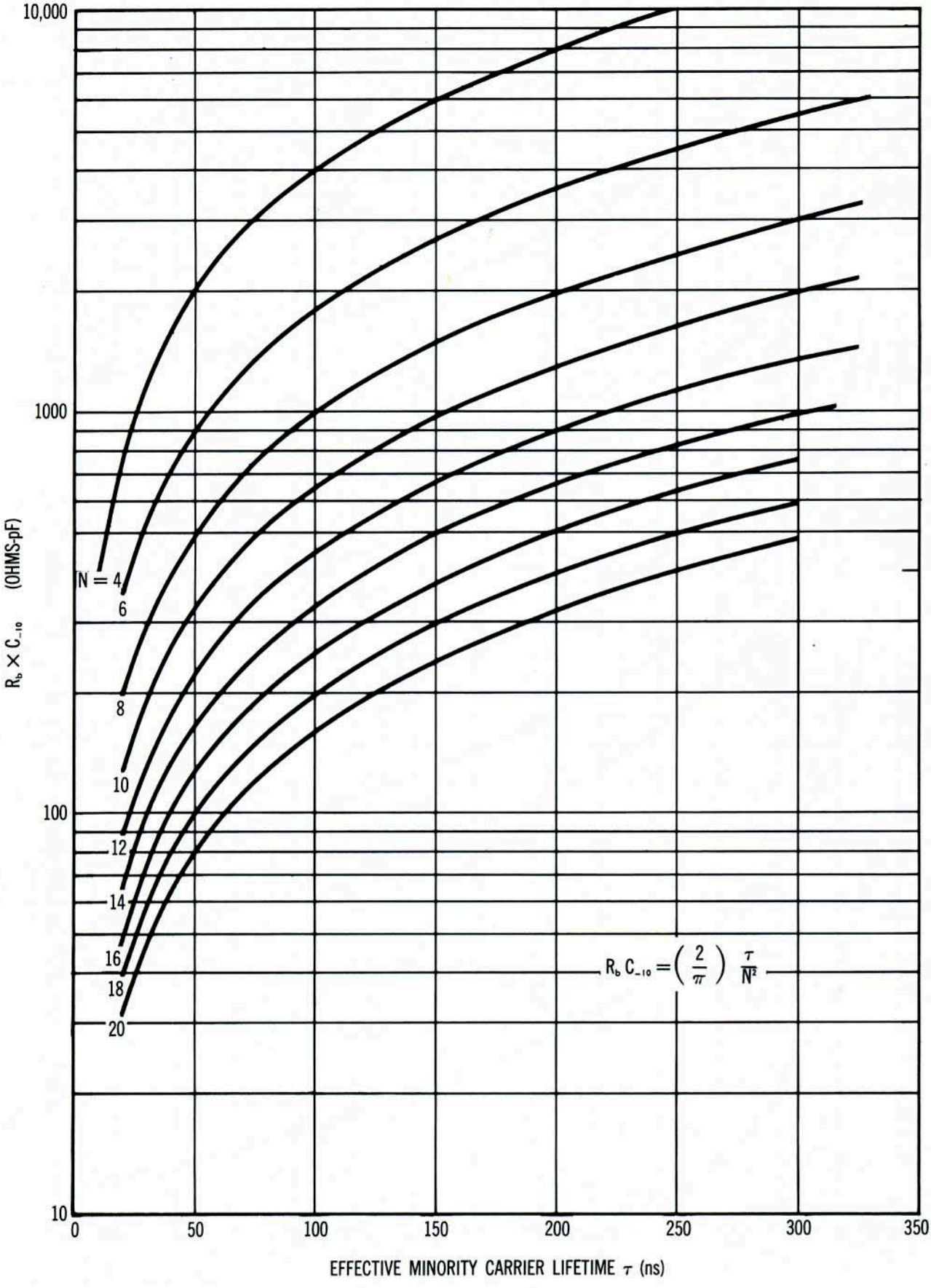


Figure 8. ($R_b \times C_{-10}$) Product Versus Effective Minority Carrier Lifetime τ.