

Application Note 218-5 Microwave Synthesizer Series

HEWLETT PACKARD

Obtaining Leveled Pulse-Modulated Microwave Signals From the HP 8672A

Introduction

Many radar and electronic warfare systems require pulse-modulated microwave signals for test, evaluation, and calibration. The HP 8672A Microwave Synthesized Signal Generator, used with the HP 11720A Pulse Modulator, delivers superior quality pulse-modulated microwave signals at carrier frequencies from 2 to 18.6 GHz.

In many test applications requiring pulsed power, it is desirable to have the peak power in the individual pulses remain constant with varying carrier frequency and duty cycle. With "leveled" pulsed power as the stimulus to a receiving system under test, all power measurements throughout the system can be made relative to the constant power level of the stimulus signal, regardless of carrier frequency. This is particularly useful in broadband surveillance and multi-receiver systems that require pulsed power in several frequency bands for complete test verification.

This application note describes a technique for obtaining leveled, pulsed microwave test signals using the 8672A/11720A combination. The technique described shows how pulsed microwave signals leveled to the peak power can be obtained, independent of the pulse modulation duty cycle.

The Leveling Technique

The 8672A is equipped with internal leveling circuitry that enables it to deliver power that is flat with frequency within ±1.25 dB, 2 to 18 GHz. When the 8672A is used with an 11720A Pulse Modulator, however, the peak pulsed power at the output of the 11720A varies with frequency as shown in Figure 1. Mismatch error and increasing insertion loss with frequency associated with the 11720A modulator and the interconnecting cable are the causes of the additional variation in pulsed power level. Any other devices, such as directional couplers or amplifiers, inserted into the microwave signal path add to the power variation with frequency.

The 8672A signal generator is capable of accepting external leveling inputs. In EXT ALC (external automatic leveling control) mode, the output level of the 8672A changes in direct proportion to the dc component of the signal present at its "EXT ALC INPUT". With this capability in the 8672A, it is possible to obtain leveled, pulsed microwave power by detecting part of the pulsed power and sending the detector output signal directly into the 8672A external ALC, as shown in Fig. 2. In response to this signal, the 8672A external leveling circuitry adjusts the power output to maintain a constant average power level at the input to the detector. The output level can be adjusted to a particular value by varying the ALC gain via the screwdriver potentiometer control labeled "CAL" on the 8672A front panel. Any change in power at the output port of the 11720A results in the output power of the

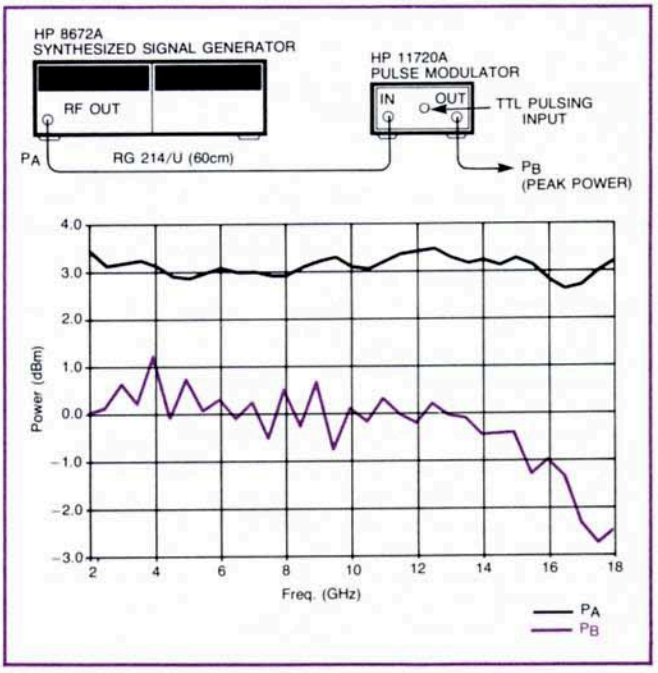


Figure 1. Typical Power Variation Without External Leveling, 8672A/11720A.

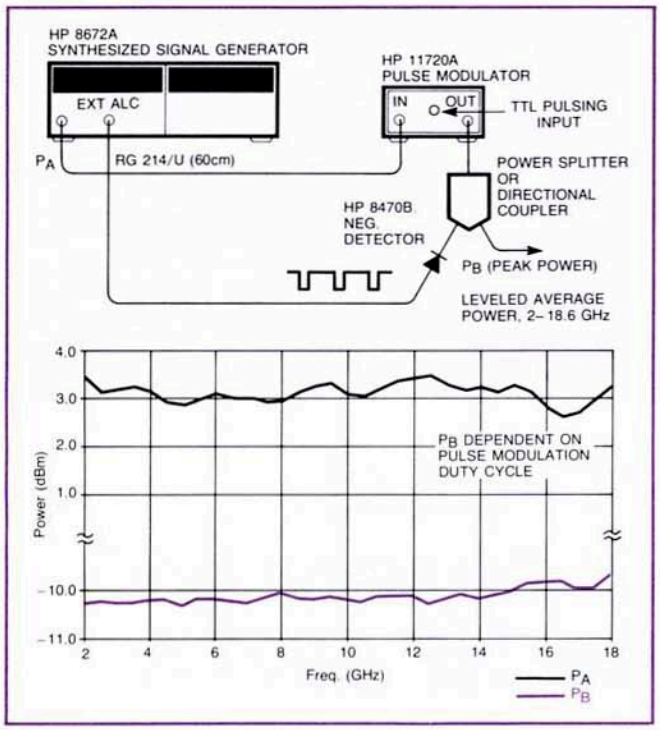


Figure 2. Typical Power Variation With External Leveling, 8672A/11720A.

8672A varying to compensate for the change. This feedback levels the average power in the pulsed microwave signal, and the peak power remains leveled as long as the modulation duty cycle remains constant.

With a variation in duty cycle, i.e., a change in pulse width or pulse rate, the average power in the pulsed microwave signal must change if the peak power is to remain constant. However, since the external leveling configuration of Fig. 2 holds the average power constant, the peak power in the microwave signal has to change proportionately with changing duty cycle. What is needed, then, to obtain constant peak power independent of carrier frequency *and* duty cycle, is a detected signal at the external leveling input of the 8672A that is proportional to the peak power in the microwave carrier rather than the average power.

The most direct way of accomplishing this is to use a peak-detecting circuit that delivers a constant voltage equal to the peak voltage of the detector output signal (Fig. 3). The peak voltage out of the detector is proportional to the peak power in the microwave pulses. The voltage out of the peak-detecting circuit is the signal that the 8672A external leveling circuitry attempts to keep constant, and thus the power out of the 8672A varies to maintain a constant peak power at the input to the detector.

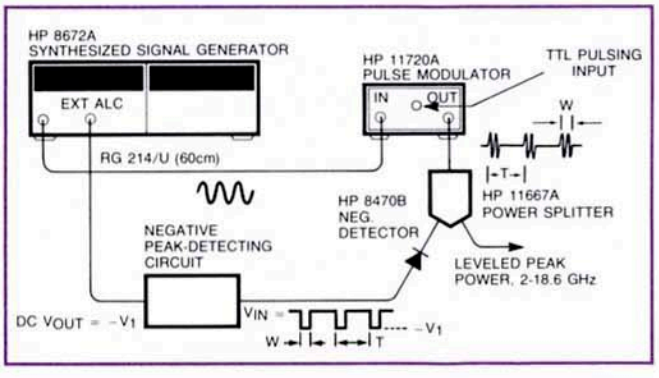


Figure 3. Setup for Peak Power Leveling with Peak-Detecting Circuit; Leveled, Pulsed Power Duty Cycle Independent.

The Peak-Detecting Circuit

Figure 4 shows the schematic diagram and parts list for a negative peak-detecting circuit that works well in this leveling application. The circuit is negative peak-detecting because most crystal detectors in microwave labs have negative output. The circuit has relatively few components and is inexpensive.

The circuit operates in a straightforward manner. When a negative pulse appears at the input of U1, the LM311 comparator, the comparator turns on essentially connecting C1 to the −5V supply through R0, the 196 ohm resistor. C1 charges with a time constant of R0C1 = (196)C1 seconds, but stops charging when the voltage across it equals the negative peak voltage of the input pulse. When the input pulse at the comparator returns to its off state, the comparator turns off, disconnecting C1 from the negative voltage supply and leaving it to discharge through R1. For R1 large, C1 discharges so slowly that the voltage across it hardly changes before it is recharged by the next pulse in the voltage pulse train. Thus, the voltage across C1, once buffered by the LM208 (U2) buffer stage, is essentially a dc value equal in magnitude to the peak negative voltages of the pulses in the pulse train entering the comparator. If the pulse train is the output voltage waveform from the crystal detector shown in Fig. 3, and if the output of the circuit is the signal reference for the external leveling control circuitry in the 8672A, then the feedback will maintain constant pulsed microwave power at the detector, independent of carrier frequency and duty cycle.

The critical components in the circuit are R1 and C1. Given the pulse modulation parameters of minimum pulse width in seconds, w, and minimum pulse rate in Hertz, PRF_{min} (equal to $1/T_{max}$, T_{max} being the maximum pulse repetition period), the equations for selecting R1 and C1 are

$$R1 \geq \frac{100\ T_{max}}{C1s}\ \text{ohms} \qquad (1\text{-}1)$$

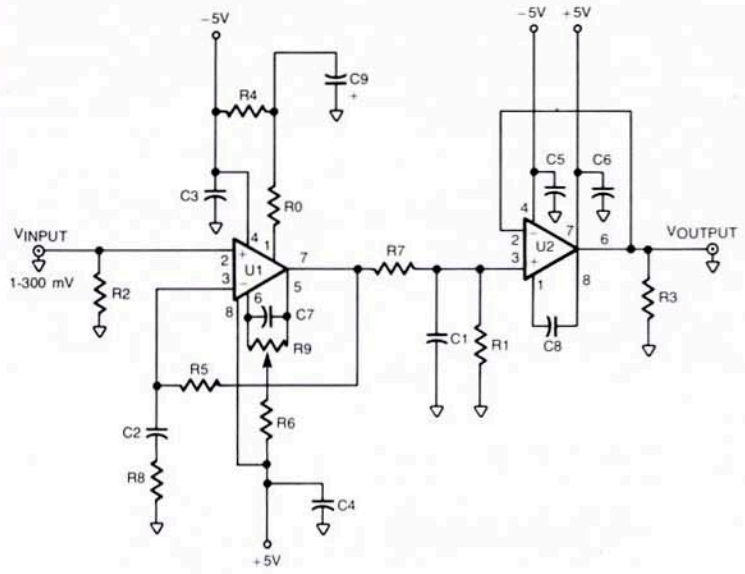
$$C1 \leq \frac{-100w(5)}{sV1R0}\ \text{farads} \qquad (1\text{-}2)$$

where V1 = the peak voltage into the comparator,
R0 = the 196 ohm resistor, and
s = the maximum allowable sag in the output voltage in percent (Fig. 5).

A 4 microfarad TRW metalized polycarbonate capacitor is suggested for C1 to ensure circuit stability. Another capacitor type may cause oscillations in the comparator feedback loop. As indicated by equation 1-1, R1 should be kept as small as possible to ensure that the leveling loop stabilizes as fast as possible after a carrier frequency change.

The circuit works reliably on all pulse widths from 150 nanoseconds to CW. PRF's as low as 50Hz are possible with R1 being the determining factor as shown in equation 1-1. The 422 ohm resistor at the comparator input loads the typical microwave detector to ensure the optimum rise/fall-time response. The circuit responds to pulse amplitudes as small as 1mV and as large as 300mV. If a drive level greater than 300mV is present, it should be attenuated or resistor R3 should be made larger to reduce the current drawn from the LM 208.

When operating on narrow pulses, the circuit may require a number of pulse periods to deliver its final output voltage. This means that a number of pulse cycles have to pass after the 8672A's RF output is turned on before the peak power of the pulse-modulated microwave signal is leveled. Using previously defined symbols, the number of cycles, n, that must pass before leveled peak power can be ensured is determined by the following equation:



PARTS LIST

C1 = 4 μF, 50V, Metalized Polycarbonate, TRW Capacitor Div.
C2 = 0.047 μF, 200V, Mylar
C3 C4 C5 C6 = 0.01 μF, 100V, Disc Ceramic
C7 = 0.1 μF, 50V, Dipped Ceramic
C8 = 30 pF, 200V, Dipped Ceramic
C9 = 33 μF, 10V, Electrolytic
U1 = Voltage Comparator, National Semiconductor LM311
U2 = OP AMP, National Semiconductor LM 208
R0 = 196 Ω, 1/8 Watt, 1%
R1 = 1 MΩ, 1/8 Watt, 1%
R2 = 422 Ω, 1/8 Watt, 1%
R3 = 46.4 Ω, 1/8 Watt, 1%
R4 R5 = 100 Ω, 1/8 Watt, 1%
R6 = 3.16 kΩ, 1/8 Watt, 1%
R7 = 1.47 Ω, 1/8 Watt, 1%
R8 = 4.64 Ω, 1/8 Watt, 1%
R9 = Potentiometer, 2-5 kΩ, 1/2 Watt, Cermet Type H

Figure 4. Schematic Diagram and Parts List for a Negative Peak-Detecting Circuit.

$$n = \frac{\ln\left[1-\left(\frac{V1(1-c)}{cd}\right)\right]}{\ln c} \qquad (1\text{-}3)$$

where $c = 1 - \frac{s}{100}$, and

$$d = \frac{-0.027w}{C1}.$$

For example, suppose V1 = -20 mV,
C1 = 4μF,
w = 400 ns, and
s = 0.5%.

Then $d = \frac{-0.027(400\ ns)}{4\mu F} = -2.7mV,$

$$c = 1 - \frac{0.5}{100} = 0.995, \text{ and}$$

$$n = \frac{\ln\left[1-\left(\frac{-20mV\ (1-0.995)}{0.995\ (-2.7mV)}\right)\right]}{\ln 0.995}$$

$$= 7.6 \text{ cycles.}$$

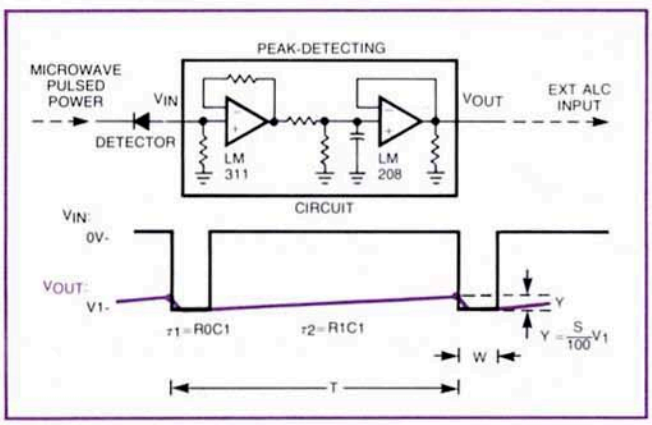


Figure 5. Peak-Detecting Circuit Input and Output Voltage Waveforms.

If the PRF is 100Hz, T is 1/100 or 10 milliseconds and 7.6 cycles x 10 milliseconds/cycle is 76 milliseconds. Therefore, in this example, 76 milliseconds must pass after RF power is applied to the diode detector before leveled power can be attained.

It is important to note that allowing time for C1 to charge fully is required only when input signal to the circuit has been removed for relatively long periods of time, such as when RF power is turned off and then on again more than a second or two later. Switching frequencies or varying the duty cycle does not constitute removing the signal from the circuit long enough to require the waiting time discussed above.

If the leveling configuration of Fig. 3 is used in an HP-IB controlled system, the status byte of the 8672A can be polled to determine when a leveled power condition exists. Bits 6 and 2 of the 0 through 7 bit status byte are high when output power is unleveled.

Leveling Performance

Leveling performance is determined by tracking variations associated with the power splitter or coupling factor variations associated with the directional coupler, the frequency response of the diode detector, and how well the peak-detecting circuit can deliver a voltage level proportional to the signal entering it.

An HP 8470B Crystal Detector, HP 11667A Power Splitter, and peak-detecting circuit with C1 = 4μF and R1 = 1 Megohm (s = 0.5%, T_{max} = 20 ms) in the configuration of Fig. 3 yield the typical leveling performance shown in Fig. 6 at duty cycles of 1.0, 0.1, 0.03, and 0.003%. Leveling errors are ±0.25 dB power splitter tracking, ±0.6 dB detector frequency response, and +10log[1/(1-s/100)] = +0.02 dB peak-detecting circuit output voltage variance. Worst-case summing of the leveling errors implies the peak pulsed power out of the 11720A should be flat within +0.87/-0.85 dB irrespective of varying frequency and duty cycle. Leveling on this order is more than adequate for most tests and measurements requiring leveled, pulsed power.

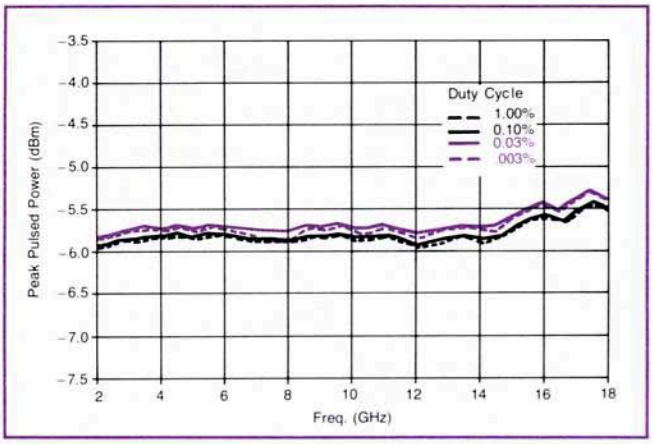


Figure 6. Typical Leveling Performance for Various Duty Cycles.

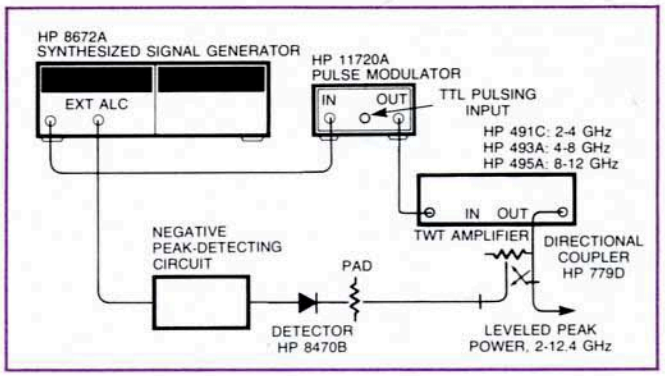


Figure 7. Setup for Obtaining High-Power Leveled Pulses.

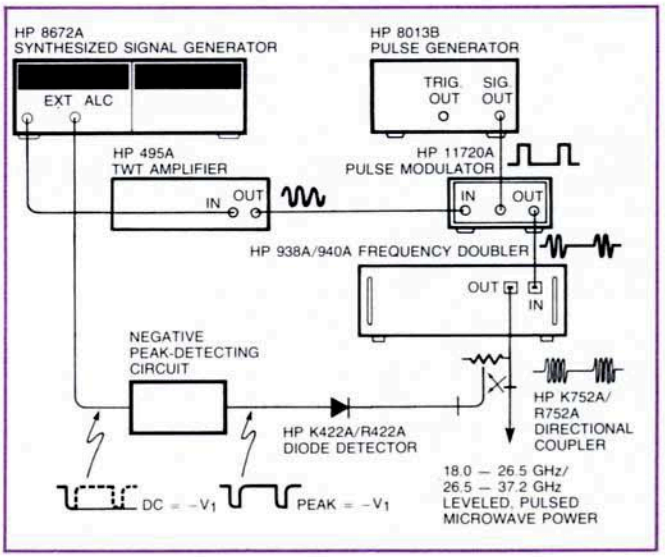


Figure 8. Setup for Obtaining 18-37.2 GHz Leveled, Pulsed Microwave Power.

Extended Configurations

Two typical extensions of the peak power leveling technique described in this application note are adding a TWT amplifier to obtain higher leveled, pulsed power and adding frequency doublers to obtain leveled, pulsed power at frequencies from 18 to 37.2 GHz.

Fig. 7 shows how a TWT amplifier can be configured into the leveling loop to provide higher leveled, pulsed power. The resulting microwave signal can be used for any application requiring higher peak power than can be delivered by the 8672A/11720A alone. The amplifier output may be low-pass filtered to prevent out-of-band harmonic content from entering the directional coupler and causing power drops in spite of the external leveling impetus. The frequency range and rise/fall times of the microwave pulses are constrained by the TWT parameters. However, complete flexibility in controlling pulse width and pulse rate without affecting peak power level is maintained.

Fig. 8 shows how an HP 938A or 940A Frequency Doubler can be combined with an 8672A and an 11720A to generate leveled, pulsed microwave signals at carrier frequencies up to 37.2 GHz. The amplifier shown in the leveling loop may or may not be required, depending upon the magnitude of the doubled-frequency signal desired. The conversion loss of the 938A or 940A Frequency Doublers increases rapidly with decreasing input signal. If the amplifier is required to compensate for the losses in the microwave path, it will have to cover the frequency range equal to one-half of the doubler output frequency range for the full capability of the system to be realized. With appropriate use of programmable switches and HP-IB control, a system including the 8672A, 11720A, 938A, and 940A could be assembled that would deliver leveled, pulsed microwave signals at frequencies from 2 to 37.2 GHz. For more information on use of the 8672A with the 938A and 940A Frequency Doublers, see HP Application Note 218-4, "Synthesized Signals from 18 to 37.2 GHz Using the 8672A".

Summary

The HP 8672A Synthesized Signal Generator and HP 11720A Pulse Modulator can together deliver pulsed microwave signals from 2 to 18.6 GHz with superior performance. The peak-detecting circuit detailed in this application note extends the capability of the 8672A/11720A in that peak-leveled, pulsed power can be delivered independent of changing carrier frequency or changing pulse modulation duty cycle.

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