

# FUNCTIONAL DIGITAL ANALYSIS

HEWLETT  PACKARD

APPLICATION NOTE 167-3

## FUNCTIONAL DIGITAL ANALYSIS

Data flow in digital machines is seldom repetitive and must be captured on the first pass or lost. By operating the 1601L Logic State Analyzer in its single-sample mode, events that occur only once are captured and displayed for analysis. The Analyzer's digital memory makes it ideal for monitoring the turn-on sequences of microprocessors in algorithmic state machines.

The displayed 12 bit words (8 bit words plus 4 qualifiers) are referenced to a front panel selectable trigger word. The analyzer can be set to display the trigger word and the 15 words that follow it (Start Display) or it can be set to display the trigger word and the 15 words that precede it (End Display). The trigger word can also start a digital delay generator so that the analyzer captures and displays the 16 words that follow a preset number of clock cycles which makes it possible to page through sequences as long as 100,000 words.

The trigger word, which can be brightened to show its position in the data stream, is selected with 12 front panel switches that correspond to the 12 data inputs. The three position switches can be set to HI, OFF, or LO. When analyzing positive logic, HI corresponds to "1" and LO to "0". With negative logic, a logic POS/NEG pushbutton prevents ambiguity by maintaining logic sense. OFF corresponds to "don't care".

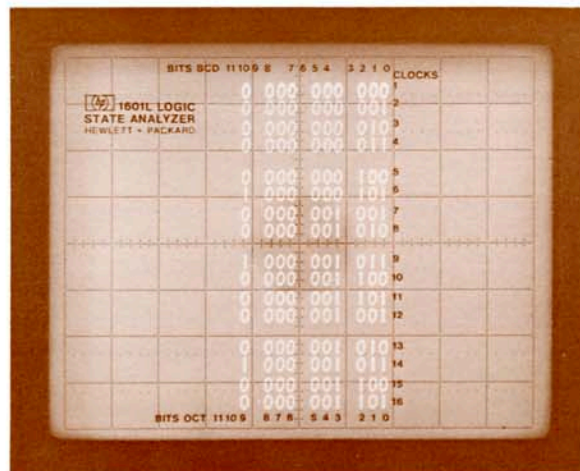


Figure 1. Logic Analyzer functional display of the single-shot turn-on sequence of the 3490A DMM.

An example of how the Analyzer is used to monitor a turn-on sequence is shown in figure 1. This shows the state flow, in octal format, of a HP Model 3490A digital multimeter. Seven data probes corresponding to bits 0 through 6 are attached to the 3490A State Counter outputs with the corresponding trigger switches set to "0" (all other switches are set to OFF). Probes for bits 7 and 8 are not connected and bit 9 is connected to the Qualifier Select which separates the display of the qualifier status from the state counter display for easier interpretation. By comparing the algorithm in figure 2 and the display, it is easy to see that the DMM followed the proper turn-on sequence to the wait loop at states  $11_8$  through  $15_8$ .



To check other functions, qualifiers can be set in various Ranges or Function command states. The Analyzer is set to single sample and end display to capture a sequence and display the 15 words preceding the trigger word.

Another check using the turn on sequence shows how the the DMM arrived at state  $25_8$  with end display mode and a range select command, qualifier of 1, selected at state  $25_8$ . The display in figure 3 now shows that the DMM arrived at state  $25_8$  with two cycles through states  $11_8$ ,  $16_8$ , and  $21_8$ . To determine if the two cycles through states  $11_8$ ,  $16_8$ , and  $21_8$  are valid, another data probe can be connected to the Flag Signal at the Inguard/Outguard interface (figure 4). By recycling the DMM, the Analyzer display will show if the qualifier at state  $16_8$  set properly or if the Flag Signal inhibited it. Further checks in the Outguard circuit will determine if the machine was busy prior to setting the flag or if a malfunction occurred.

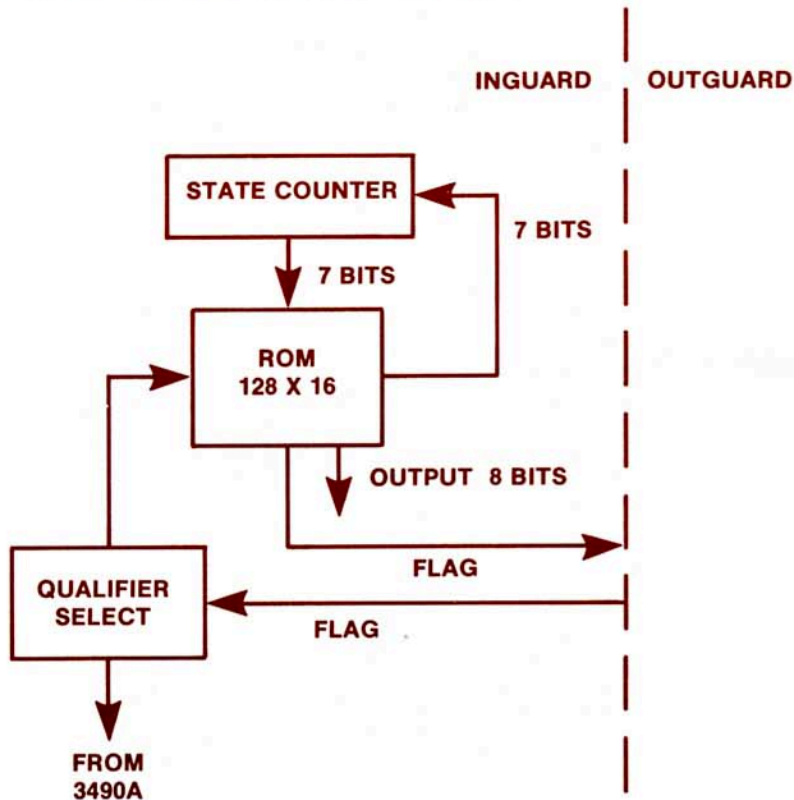


Figure 4. Partial block diagram of the 3490A DMM.

This application note should give you some basic ideas about how the HP Model 1601L Logic State Analyzer can aid in troubleshooting during the initial turn-on of digital machines. The functional single sample and repetitive modes of operation can be used to follow an algorithm to show where a machine has stopped or incorrectly branched, allowing you to quickly pinpoint the problem with electrical measurements.

