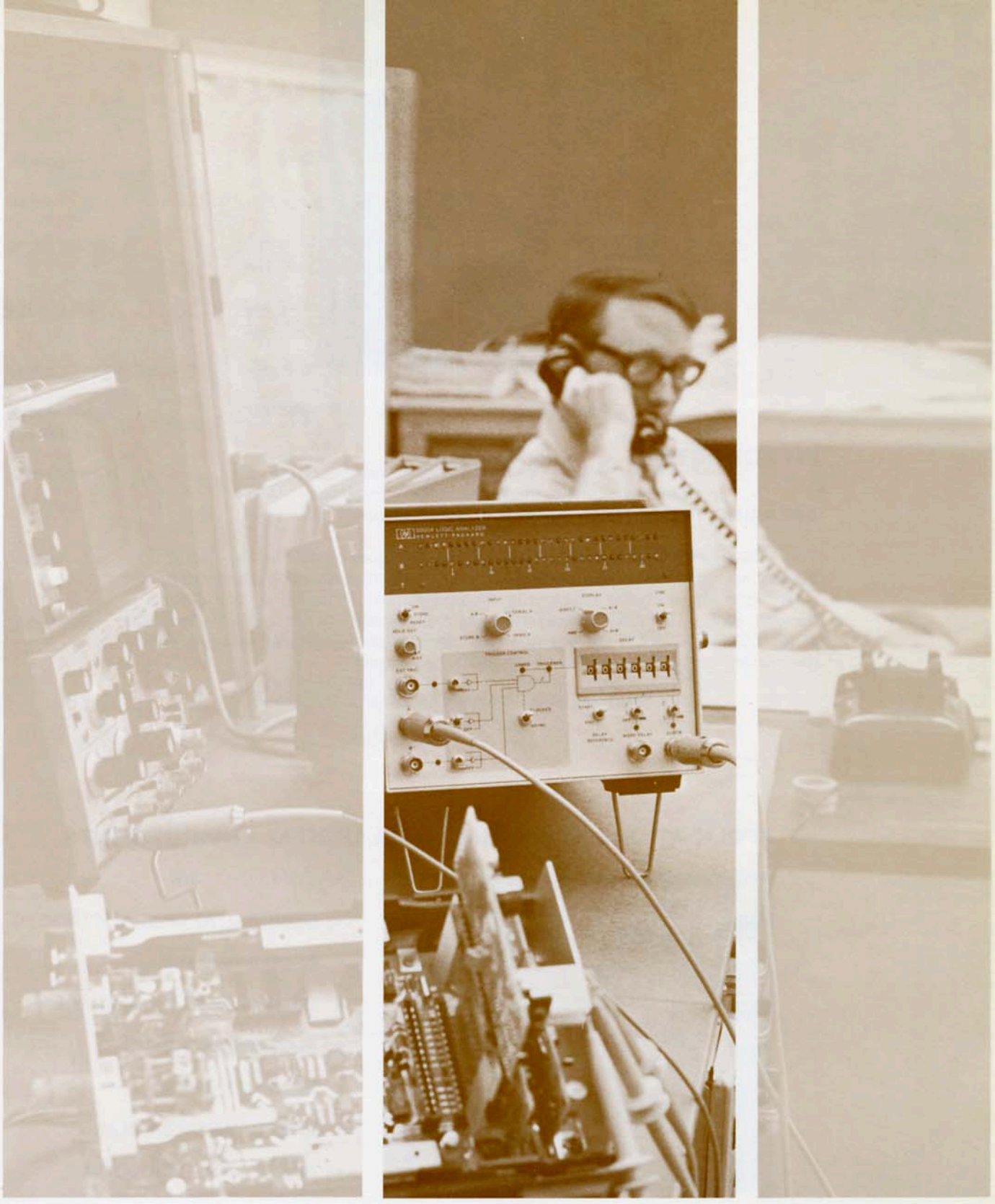


THE LOGIC ANALYZER

APPLICATION NOTE 167-1

HEWLETT hp PACKARD



THE LOGIC ANALYZER —

INTRODUCTION

BREAKING THE DIGITAL BARRIER

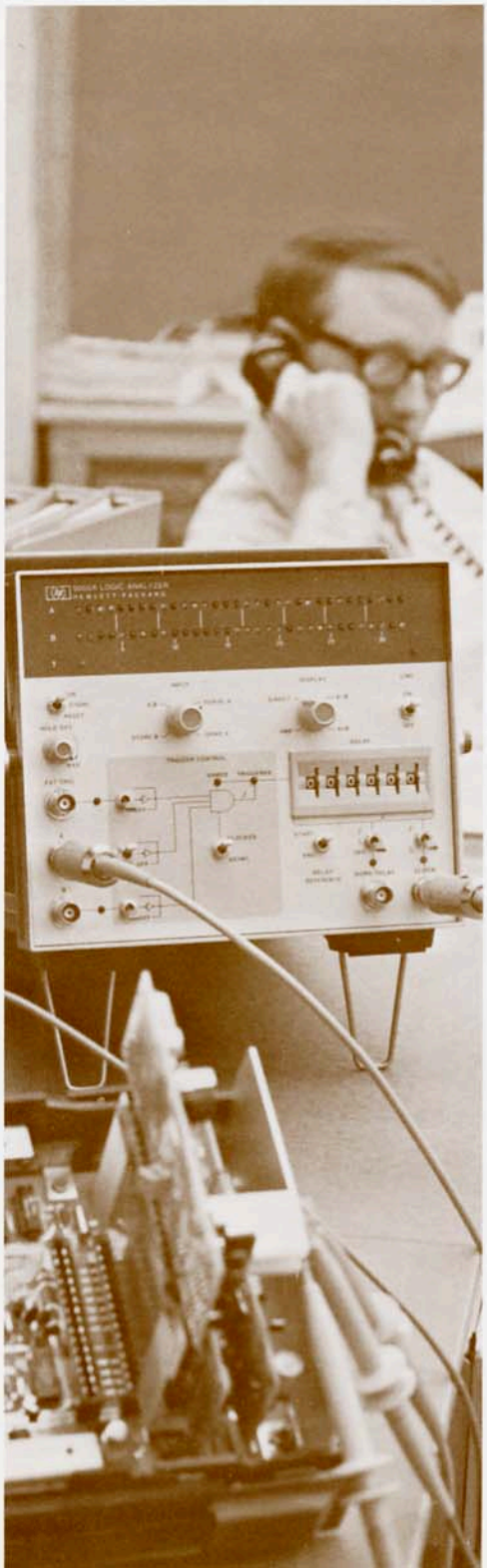
The 5000A LOGIC ANALYZER is a digital test instrument that is used for the display and analysis of LOGIC STATE VS. TIME. Its total digital nature enables us to approach a digital problem in its own domain. The key to this domain is the **utilization of the time base of the system under test**, its clock, for the timebase of the LOGIC ANALYZER display. With this display quantized in terms of bits, the content of the data can now be intuitively grasped.

APPLICATIONS IN VIRTUALLY ALL DIGITAL ENVIRONMENTS



- CALCULATORS
- GENERAL ALGORITHM DESIGN
- ASCII SYSTEMS
- DIGITAL MAG TAPE READERS
- MAG DISC SYSTEMS
- DRUM MEMORIES
- PAPER TAPE READERS
- POINT OF SALE READERS
- MARK/SENSE CARD READERS
- MINI-COMPUTERS
- MICRO-PROGRAMMED INSTRUMENTS
- PRN GENERATORS

A STEP TO EASIER DIGITAL TROUBLESHOOTING



UNIQUE CAPABILITIES IN DIGITAL ANALYSIS

- CLOCKED DISPLAY
- TRIGGER ON COMBINATION OF SIGNALS
- DIGITAL DELAY—JITTER-FREE DELAYED SWEEP
- SEE DATA BEFORE TRIGGER POINT
- TROUBLE-FREE DATA CAPTURE AND STORAGE
- FIND SPIKES AND NOISE GLITCHES IN YOUR SYSTEM

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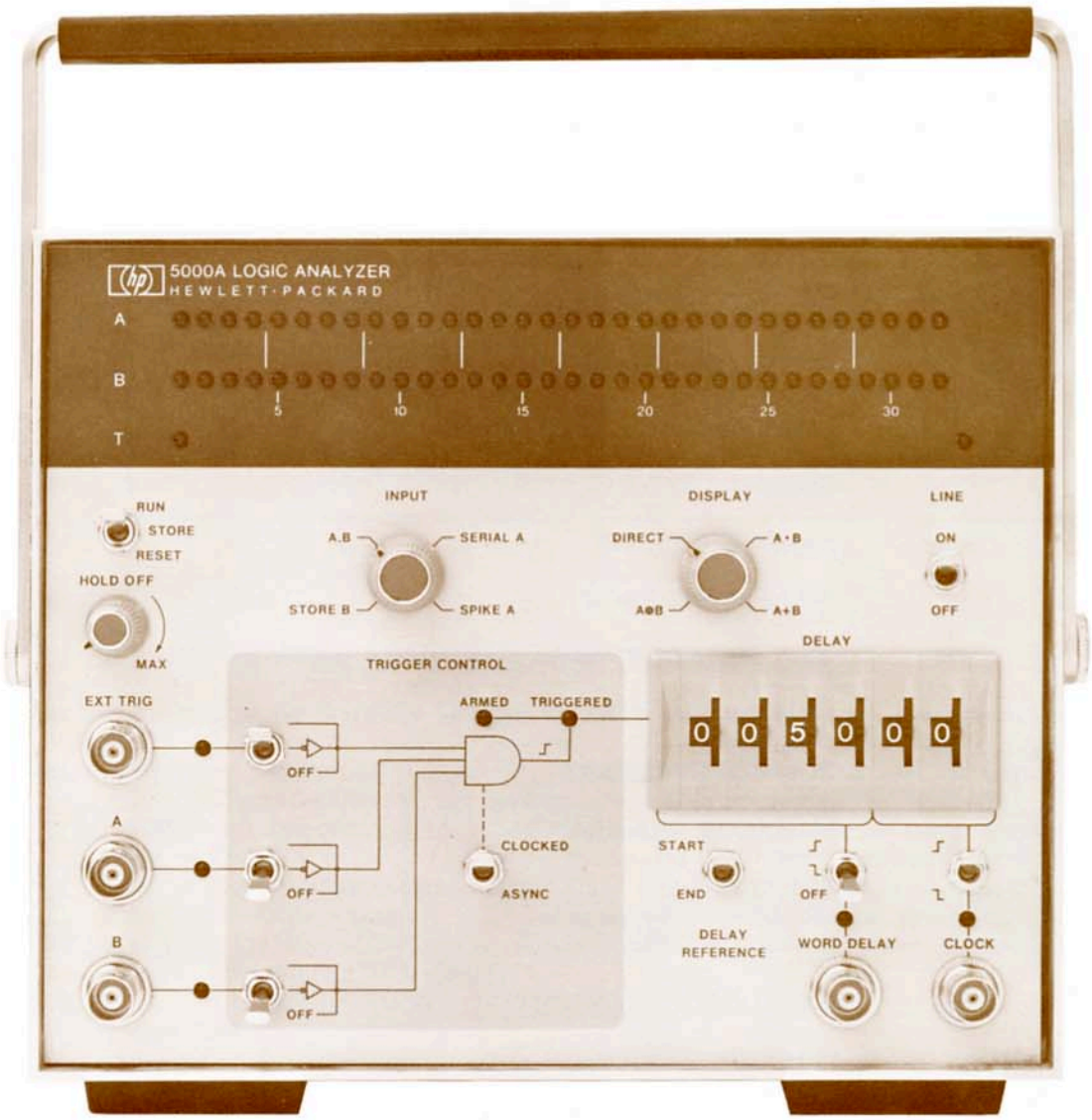


5000A Logic Analyzer. Switches and modes discussed in the text of this Application Note may be referenced in the above front panel photograph.

I. THE NEW TOOLS OF DIGITAL ANALYSIS

THE CLOCKED DISPLAY

The existence of a clock in the hardware of a digital system is almost certain. The omnipresence of this clock has its roots in several basic ideas. By allowing a particular system to change its condition or state only at the end of a regular time period, we can be certain, that just before this change, all transient conditions have died out and the circuit condition is stable. The most stable point in time to look at the circuit condition is, therefore, just prior to the occurrence of another clock. To take advantage of this fact, sequential circuits such as flip-flops and shift registers sample only on command from the clock. The data that is sampled by these devices is, of course, the data that was present just before the clock. In fact, the requirement that the data be present for a short time before the clock is called SET-UP TIME.

The idea of sampling information or data at the most stable point is also vital in any kind of data transmission. In fact, most bus structures have a 'data valid' line which functions as a data sampler or clock. In some cases, Teletypes* and moving head disc memories* (HP 7900) for example, this clock is derived from or initiated by the data itself and is therefore present only at the computer interface card where the data is received. But the important thing to note is that it is nonetheless present.

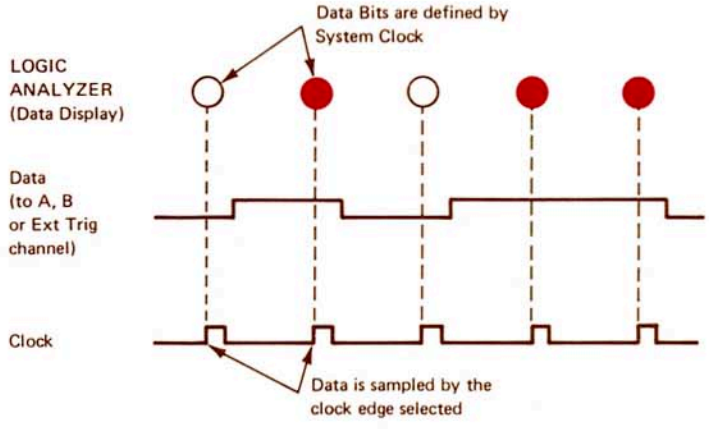


Figure 1. The "By-Bit" Display of the Logic Analyzer

The data inputs to the LOGIC ANALYZER are designed to accept data exactly the way a device such as a 'D' flip-flop or shift register does: in a clocked manner. The ANALYZER, therefore, reacts the way a clocked flip-flop would and displays data in terms of bits referenced to the clock of the system under test. These 1's and 0's can be exactly compared to the timing diagram of that node on the circuit.

Using a display device with the same time base as the system under test has many advantages. For instance, in any system that relies on a mechanical device for the generation of the clock, a large amount of instability is present in the

*See Section II for further discussion of this measurement problem.

clock. This is present in tape systems (paper and magnetic), disc and drum memories, card readers (optical and magnetic) and similar devices. The LOGIC ANALYZER is not affected by these instabilities since its display is in terms of 'bits' referenced to this clock.

The ultimate clock instability occurs when the data and clock are present only in bursts. This common occurrence in many data transmission systems is easily handled by the LOGIC ANALYZER, because its time base is that of the data.

With its data inputs (A, B, EXT TRIG) analogous to the "D" input of a standard flip-flop and the utilization of the system clock for a time base, the LOGIC ANALYZER operates in exactly the same domain as the digital circuit on which it is used. The LOGIC ANALYZER is, therefore, easy to understand and use because it behaves in a manner similar to the devices it tests.

COMBINATORIAL TRIGGERING

In any display of information with respect to time or events, there must exist some unique sync or starting point. The simplest case of this requirement is, of course, triggering or starting the display upon the occurrence of an event on one line. This type of triggering is the familiar negative or positive slope triggering. In many cases, this simple form of triggering is sufficient, and, in fact, people have been limited to this type of triggering for many years. In the digital world, however, it is often necessary to trigger on the simultaneous occurrence of several events. This added flexibility often makes the investigation of a particular data stream much easier. This need is answered by allowing the ANALYZER to trigger on a simultaneous event at the A, B and EXT TRIG inputs. Typical trigger conditions might include events such as A•$\overline{B}$•(EXT TRIG), $\overline{A}$•B ($\overline{\text{EXT TRIG}}$) or A•B•(EXT TRIG). See Figure 2. These

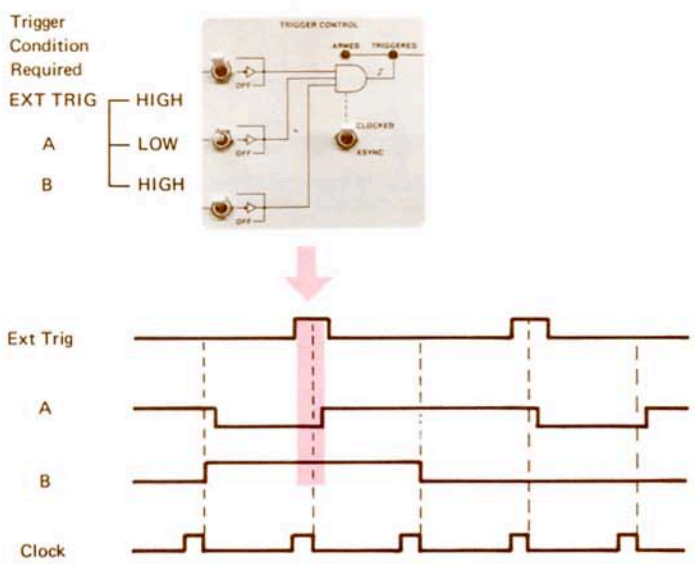


Figure 2. Trigger on a *Combination* of the Three Input Signals

conditions are selected by the polarity switches in the "TRIGGER CONTROL" region (shaded on the front panel) which control the inputs to the symbolic AND gate.

It is important to note that the triggering described is still edge (slope) sensitive as indicated by the edge symbol (⌐) on the output of the AND gate. This historic triggering method, when translated to the digital domain, simply means that for triggering to occur (after arming), the present data must not only satisfy the trigger condition (AND gate on front panel), but must also differ from the data sampled by the previous clock. Therefore, in a series of consecutive data bits which all represent the trigger condition, only the first bit qualifies to start the display. See Figure 3. The edge triggering, as defined, somewhat alleviates the necessity of AND-ing many channels together in an attempt to define a unique sync point. Triggering in the 5000A LOGIC ANALYZER is, therefore, often possible on only one channel.

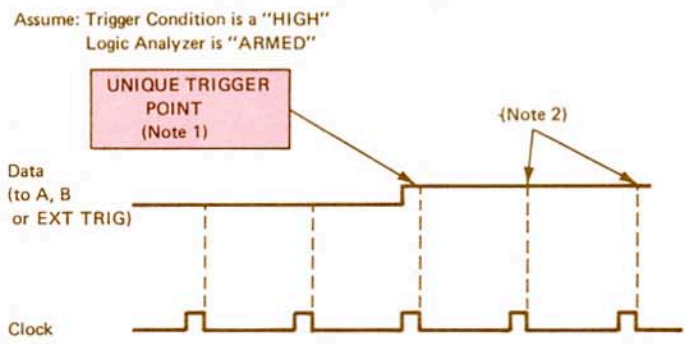


Figure 3. "Edge Triggering" Helps Give a Stable Display When Triggering on a Single Line

Triggering in the ANALYZER affords one further degree of freedom by offering either "CLOCKED" (synchronous) triggering or "ASYNC" (asynchronous) triggering. The "CLOCKED" mode of operation offers the sure-footed triggering that is characteristic of synchronous circuits. In this mode, *the inputs are only tested for the trigger condition on command from the clock.* Any transient or false trigger condition will not effect triggering since the inputs are now sampled for the existence of a trigger condition at the most stable part of the data stream, i.e., just before the next data change.

The "ASYNC" mode of triggering captures trigger conditions that are not accessible to synchronous (sampled) triggering. This feature allows the user to *initiate the display sequence on a signal that is not present when the clock samples the inputs.* This event could be a spike or perhaps a signal that occurs prior to the burst of clock pulses (clock is not available to sample the trigger).

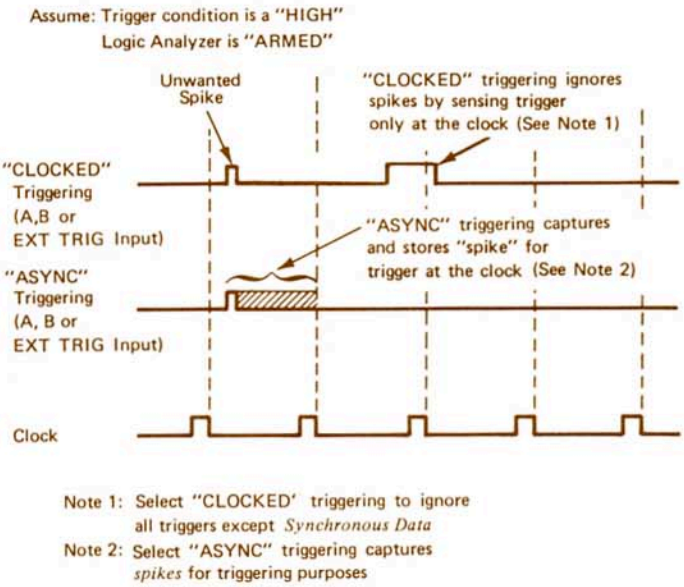


Figure 4. "CLOCKED" or "ASYNC" Triggering

In the "ASYNC" mode, a trigger event is detected and stored in a way that is analogous to the operation of the "set" or "preset" input to a flip-flop. A short spike could therefore be used as a trigger since it would be stored until the clock could sample it. The stored trigger condition is then cleared at the next clock pulse.

If the digital delay is set to zero, the trigger condition initiates the simultaneous display of the A and B channels. For "CLOCKED" triggering, the first bit displayed is the trigger condition; for "ASYNC" triggering, the first bit displayed is that sampled by the first clock that follows the asynchronous condition.

DIGITAL DELAY

Delayed Sweep for the Digital World

If it is desired to display a window of data that occurs some time after the trigger condition, the appropriate number of clock periods is entered into the thumbwheel switches as digital DELAY. The first bit of the display, therefore, is loaded after the LOGIC ANALYZER receives the trigger and enough clock pulses to count down the DELAY. This adjustable DELAY is analogous to the delayed sweep on an oscilloscope.

In the past, it has been very hard to display data in a long bit stream. If conditions are ideal, a fast storage oscilloscope with delayed sweep can display portions of a waveform several thousand clock periods long. Unfortunately, even after this elusive stream of data is captured, it is difficult to know what part of the data stream is being displayed. Is it bit number 2540 or 2630? More often than not, this particular measurement is avoided just because it is so difficult and meaningless.

The LOGIC ANALYZER has a delay capability that extends up to $10^6 - 1$ clock periods. With the ANALYZER, it is as easy to display the 900,000th bit as it is the 2nd. The only control to adjust in making this measurement is the thumbwheel switch that controls the length of the delay. The implication of this precise digital delay is that it is now easy to ascertain exactly which bit is being observed. This digital delay combined with the inherent storage capabilities of the ANALYZER makes possible the single-shot capture of any portion of a data stream, even one million clock periods after the trigger.

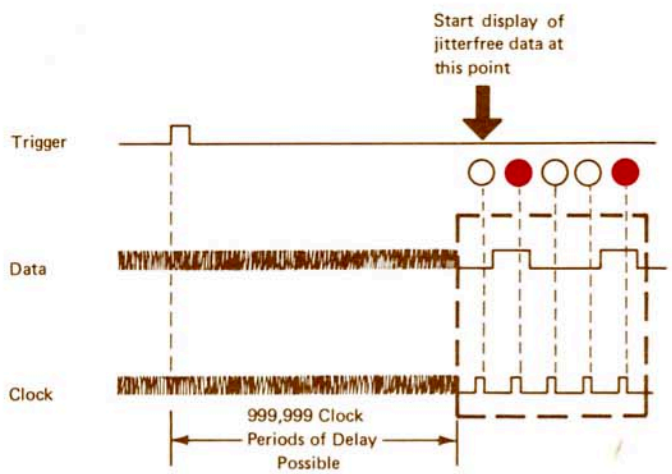


Figure 5. Access Data Anywhere in a Data Stream with DIGITAL DELAY

In some cases, it may be desirable to delay in terms of some signal other than the clock. This requirement is fulfilled in the LOGIC ANALYZER by the WORD DELAY. Engaging the WORD DELAY switch in either the positive (⌐) or nega-

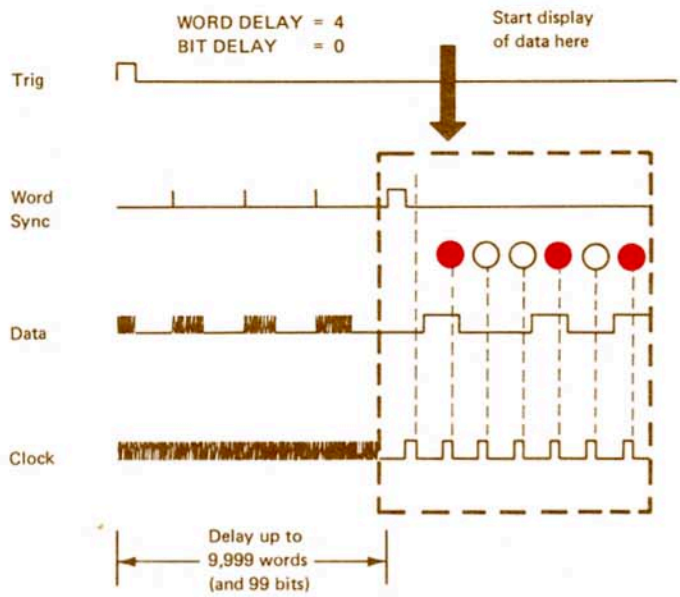


Figure 6. Move in a Data Stream in Terms of *Words and Bits*

tive (⌐) slope position divides the thumbwheel switch into two sections corresponding to the brackets beneath it. In the WORD DELAY mode, the left four digits of the thumbwheel are counted down by the positive or negative edges of pulses occurring at the WORD DELAY input. The occurrence of this pulse is stored and synchronized to the clock; therefore, a WORD DELAY of 1 would be counted down when a WORD DELAY pulse is received and it is synchronized by the following clock. See Figure 6.

The WORD DELAY feature, when combined with the standard delay in terms of clock periods, provides a coarse and fine adjustment within a serial data stream. The coarse steps may be in terms of sync pulses or word markers, the fine steps are in terms of the system clock. The display sequence with delay included is therefore:

1) ARM (5000A is initially waiting for a trigger)
2) TRIGGER
3) COUNT DOWN WORD DELAY (Sync Pulses)
4) COUNT DOWN BIT DELAY (Clock Pulses)
5) LOAD DISPLAY*
6) PAUSE (HOLD-OFF)
7) (REPEAT)

*Note: Data is displayed as it is loaded; i.e., it is not necessary to load the full display before viewing.

NEGATIVE DELAY

View Data Before Triggering

In many cases, the only information available concerning a sequence of data bits is the event at the end of the sequence. In this case, it would be desirable to trigger on this event and see what led up to the trigger instead of what followed it. By placing the ANALYZER in the END mode, the user can view this pre-trigger data either 32 or 64 bits before the trigger depending on whether the "A, B" or "SERIAL A" input mode is selected. This capability is especially useful in determining what conditions lead up to a particular error condition.

"Negative Delay" or pretrigger storage is further enhanced when used with the storage capabilities of the ANALYZER. Thus data occurring before an error condition can be stored even on a single-shot basis. If the error condition occurred when the user was absent, the information would reliably be there when he returned, one week or one year later. False triggering or missing a trigger is not a problem because of the drift free, digital triggering utilized by the ANALYZER.

The "Negative Delay" is engaged by setting the DELAY REFERENCE switch to the "END" position. Selection of this mode of operation places a 32* bit shift register between the input and the display; therefore, when a trigger is received, the first bit of data displayed is that which was loaded 32* clock periods prior to the trigger. When using the DELAY REFERENCE "END" mode on a single shot data stream, it is necessary that at least 32* clock pulses be received after the trigger to load the contents of this "Negative Delay" shift register into the display.

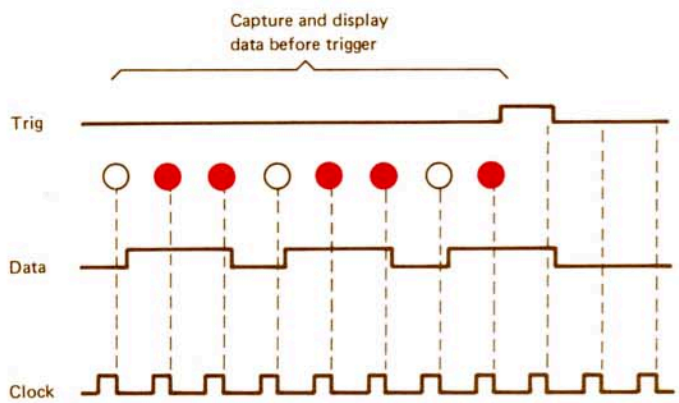


Figure 7. "Negative Delay" Displays Data *Preceding* the Trigger

*64 bits in "SERIAL A" mode.

DISPLAY STORAGE

The digital nature of the ANALYZER makes storage an inherent capability. It is no longer necessary to adjust a myriad of controls if storage is required. By simply placing the ANALYZER in the "STORE" position, the display is frozen. This is accomplished by preventing the ANALYZER from rearming; thus, the information last displayed will not be changed or lost.

If it is desired to store only one channel of data, the "STORE B" mode can be selected. In this mode, Channel B is locked in as Channel A continuously accepts new data. This mode can be used for storing a reference of good data to which succeeding data may be compared.

II. USING THE LOGIC ANALYZER IN YOUR SYSTEM

BASICS

In Section I, it was mentioned that the existence of a clock in a digital system is almost certain. The few basic examples that follow should give an understanding of the nature of this clock as it appears in different ways, and also suggest some typical applications for the LOGIC ANALYZER.

By reflecting for a moment on how the LOGIC ANALYZER works, the user will get a clue to where in a particular digital system to connect it for data display. The ANALYZER's clocked data entry makes its operation analogous to a clocked flip-flop or shift register. Therefore, if the data of interest goes into a flip-flop or shift register, this is the ideal place to pick up the necessary clock and data channels. See Figure 8. With these two channels available, the only remaining consideration is that of finding a trigger or 'sync' signal as with any display device. This signal consists of some unique signal to which the data can be referenced. If the data is uniform and repetitive, the data can also be used as a trigger; if not, a sync signal must be connected to one of the input channels and used as a trigger. For connection to a shift register, the same rules apply.

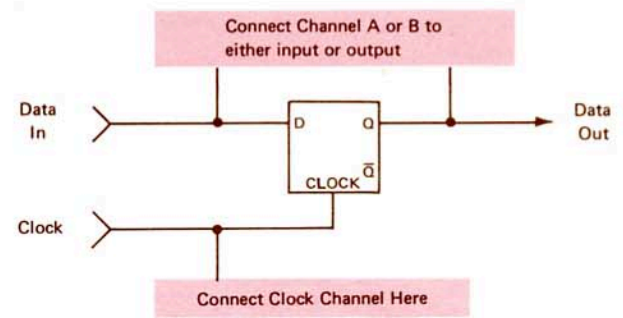
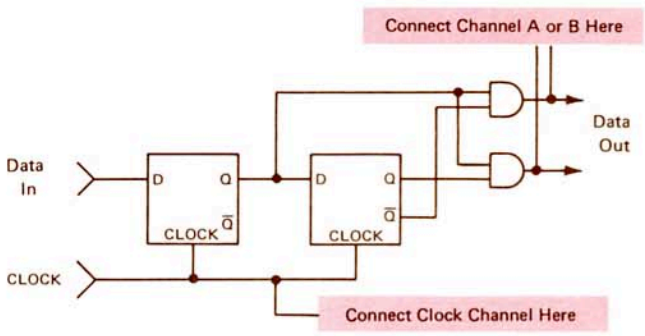


Figure 8. Logic Analyzer can be Connected to a Flip-flop.



Circuit condition changes only on occurrence of the clock. The clock serves as the Time Reference for the system.

Figure 9. Simple Clocked Circuit

The next level of complexity is that of looking at circuits whose operation directly depends on the state of the flip-flop we are considering. See Figure 9. It can be

seen in this case, that, since the AND gate is dependent on the flip-flops and the flip-flops are dependent on the clock, the output of the AND gate can, indeed, be referenced to the clock. This same theory extends to very complex circuits whose operation can usually be traced to the highest frequency clock in the system. Using this clock as the time base or clock input to the LOGIC ANALYZER enables the ANALYZER to display data at most of the nodes in the circuit. If a different time scale is desired, a slower (divided down clock) can often be found.

ROM SEQUENCER

The LOGIC ANALYZER can be put to good use in troubleshooting a ROM sequencer. These ROM sequencers form the basis of the control circuitry in many instruments and computers in use today. The microprograms from these ROM sequencers can be long, high frequency data streams that occur only once for each cycle of the machine. Under these conditions, it is very difficult to see meaningful information on an oscilloscope. The LOGIC ANALYZER, by virtue of its clocked nature, is ideally suited to looking at any part of the data stream that is desired while the system is operating normally. A trigger or sync for this application can be derived from a control line such as "Start Program" or "Reset." An alternative method of investigating this data is single stepping through the output sequence and observing each individual state. This measurement is, needless to say, especially tedious if no simple mechanism for single stepping the clock is provided.

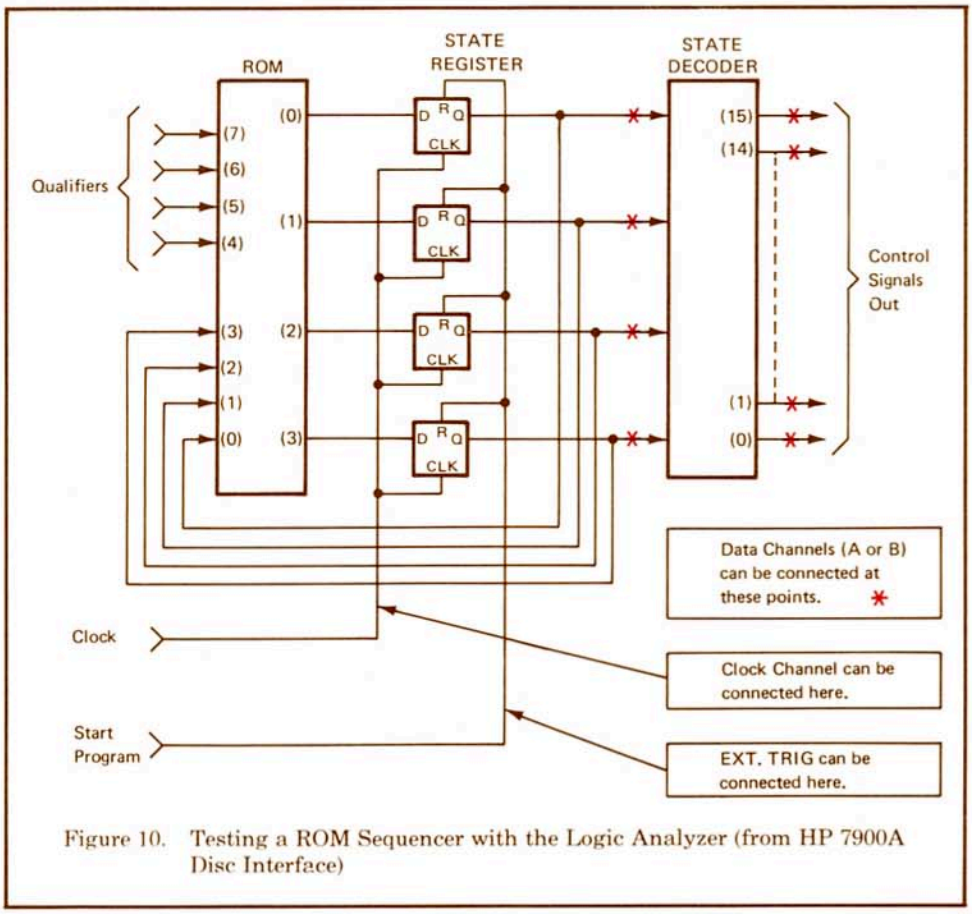


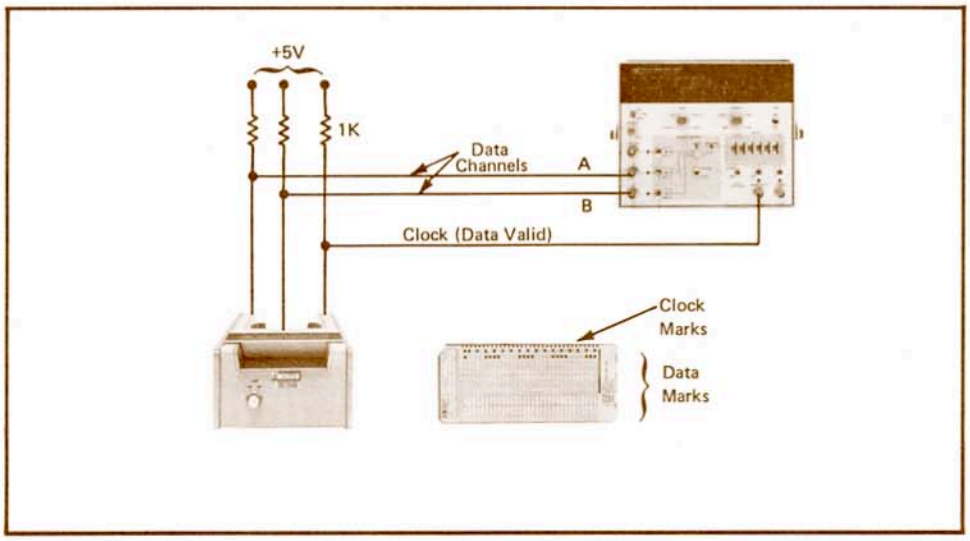
Figure 10. Testing a ROM Sequencer with the Logic Analyzer (from HP 7900A Disc Interface)

MARKED CARD READER

The Marked Card Reader or Optical Mark Reader such as the HP 3260A is a relatively simple data entry device that nevertheless presents a troublesome measurement problem: that of capturing and displaying the serial data output as the marked card is read. The storage and by-bit display of the ANALYZER make it a good solution to this problem.

The clock of the reader is derived from the black marks that are located on the edge of the card. These clock marks follow each one of the data positions on the card and therefore serve to sample the content of the data channels.

The LOGIC ANALYZER takes advantage of the clock channel of the card reader and uses it for the display time base. Therefore, the data is displayed exactly as it appears on the paper card—in bits. The storage capability of the ANALYZER keeps the data stored for display as long as desired. Reloading another card refreshes the display with new data and this data is also automatically stored.



Procedure for HP 3260A:

NOTE

The open collector output of this device requires that a dummy load be connected to each output (a 1K resistor from each output to +5 volts will suffice) if it is not connected to the device it is programming.

Connect as shown in Figure 11.

On 5000A set:

INPUT Mode to "A, B"

DISPLAY Mode to "DIRECT"

DELAY REFERENCE to "START"

WORD DELAY to "OFF"

Clock Polarity to "(⌐)"

RUN-STORE-RESET to "STORE"

ASYNC-CLOCKED to "CLOCKED"

DELAY to "000000"

Trigger as desired [Example: Set A channel trigger control to "◁▷" and trigger when the first mark (low) appears on the card].

To Operate:

1) "RESET" 5000A and return to "STORE".

2) Load Card.

3) Repeat 1) and 2) as desired.

TELETYPE

The Teletype typifies the type of peripheral that does not transmit the clock as a separate line to the computer or controller. The clock, of course, is still necessary to sample the data; however, it exists only on the interface board of the controller. This clock is initiated by the interface board on receipt of the first bit of the character which goes low for 9.09 ms. This negative transition starts a counter which counts to the middle of the data bit (4.54 ms) and initiates a clock pulse to sample the data. Every 9.09 ms thereafter another clock pulse occurs until the whole character is clocked in.

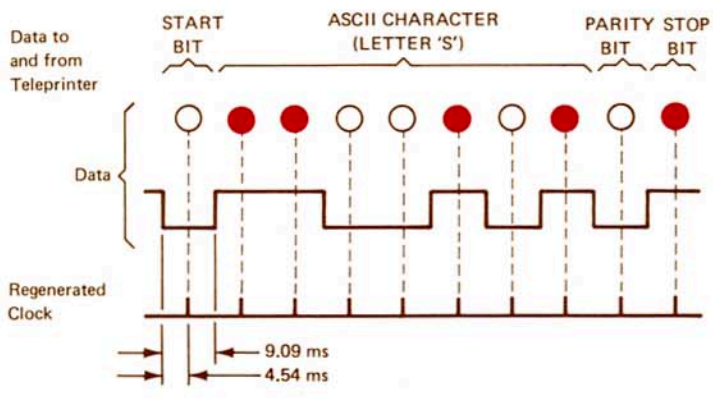


Figure 12. Typical Serial Character from a Teleprinter

This serial character is typically 10 or 11 bits long and consists of a start bit, 7 data bits, a parity bit and 1 or 2 stop bits. This serial character is loaded into a shift register on the interface board to convert it into the parallel format understood by the computer. Since all the data must flow into the shift register where both data and clock are available, this is the ideal place to connect the LOGIC ANALYZER for data display. Since the start bit always precedes the

information of interest as a '0' or low, it provides a good trigger to start the display of the individual character. Therefore, to display the serial character, it is only necessary to connect one of the data channels (A or B) of the LOGIC ANALYZER to the input of this shift register and connect the clock of the LOGIC ANALYZER to the clock of the Shift Register.

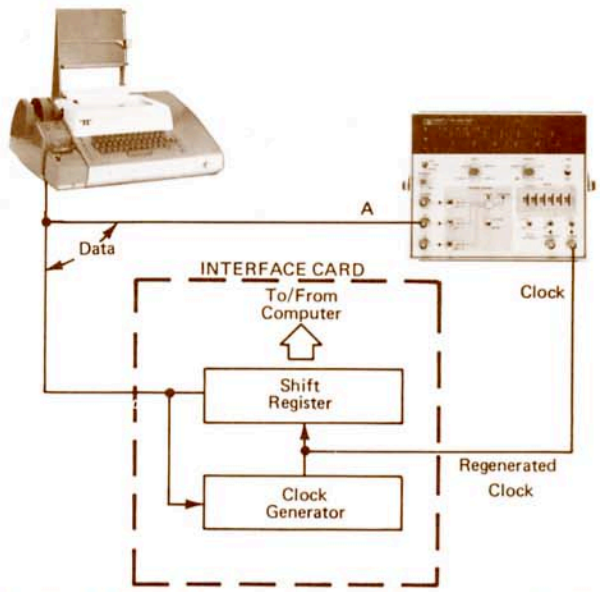


Figure 13. Individual ASCII Characters from a Teleprinter can be Displayed and Stored Using the Logic Analyzer

Procedure:

On 5000A set:

INPUT Mode to "A, B"

DISPLAY Mode to "DIRECT"

DELAY REFERENCE to "START"

WORD DELAY to "OFF"

Clock Polarity to "⌐"

RUN-STORE-RESET to "RESET" then release to "STORE"

ASYNC-CLOCKED to "CLOCKED"

DELAY as desired

Trigger to "◁" (A)

On Teleprinter:

Press key

Sequence:

1) Reset LOGIC ANALYZER as desired.

2) Press key on teleprinter.

3) Repeat 1) and 2) as desired.

This same shift register is used on the parallel-to-serial converter for data transmission from the computer to the teleprinter. The LOGIC ANALYZER can also be used to monitor data flow in this direction by attaching the A input of the LOGIC ANALYZER to the output of the shift register instead of the input. In this case, it is, however, necessary to find a trigger point as a data reference, since the character output is now controlled by the computer instead of directly by the operator. This trigger could be, for instance, the clearing of the "In/Out" flip-flop by the computer or a transition on the "Flag" flip-flop.

MOVING HEAD DISC

Data from a moving head disc such as the HP 7900A is very difficult to investigate using standard techniques because of its non-repetitive nature. The combination of digital delay and storage present in the LOGIC ANALYZER, makes it a natural for capturing this data stream. The example of the moving head disc is presented as the most difficult measuring problem in the disc family; however, the fixed head disc is also a very good application of the LOGIC ANALYZER. The fixed head disc has a clock generated directly by the disc whereas the moving head disc must regenerate its clock on the computer interface card.

On a moving head disc system such as the HP 7900A, both the clock and data are derived from a single channel. The clock is derived from this channel with

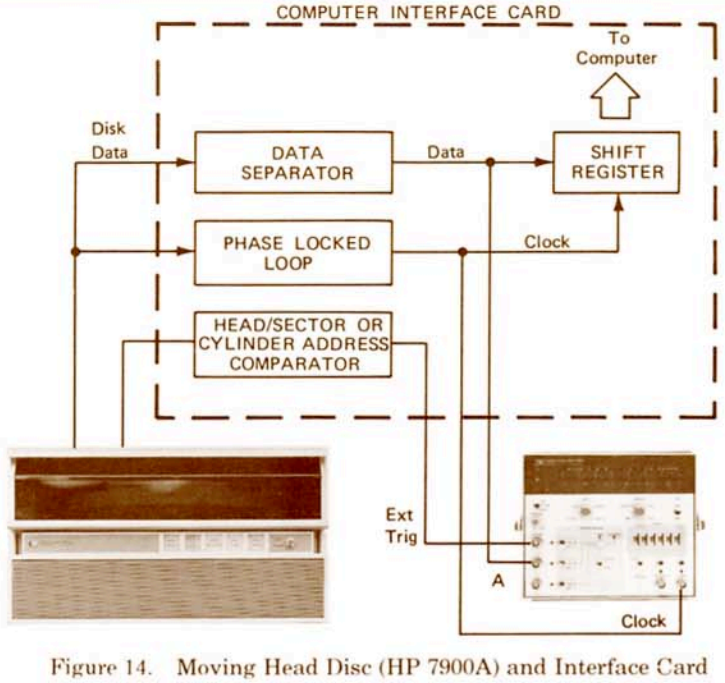


Figure 14. Moving Head Disc (HP 7900A) and Interface Card

a phase-locked-loop. If all 0's are transmitted the single channel contains a signal the same frequency as the clock. For a 1, however, an extra pulse is inserted between the clock pulses. The data separator detects these extra pulses and produces a data bit that can be clocked into a shift register by the regenerated clock. This shift register is the serial-to-parallel converter necessary to interface the serial nature of the disc to the parallel nature of the computer. The input of the shift register is an ideal place to connect the LOGIC ANALYZER by virtue of the fact that both clock and data are readily available.

A sync signal or trigger may be derived in many ways. One simple way is to repetitively read the same track on the disc and trigger on the output of the data address comparator. This pulse occurs on head/sector or cylinder address comparator and signifies the point on the disk where the data address is exactly that indicated by the controller. If this pulse is asynchronous with respect to the clock chosen for the LOGIC ANALYZER or not present when the clock occurs, switching to "ASYNC" triggering will capture the trigger event and store it until the clock occurs. With the trigger point established, the digital DELAY can access any data on the sector by delaying the proper number of clock pulses from the trigger event. If it is desired to observe the sector/head/cylinder address, the DELAY REFERENCE "END" mode is selected and the address leading up to the trigger is displayed.

Procedure:

Connect 5000A per diagram.

INPUT mode to "A, B"

DISPLAY mode to "DIRECT"

DELAY REFERENCE to "START"

WORD DELAY to "OFF"

Clock polarity to "⌐" (or as desired)

RUN-STORE-RESET to "RUN"

ASYNC-CLOCKED:

1) "CLOCKED" if pulse is coincident with the clock

2) "ASYNC" if no coincidence exists between clock and trigger pulses

DELAY as desired

Trigger to: " — " if trigger pulse is ⎍

" ◇ " if trigger pulse is ⌐⎍

On Disc System:

Select one track to be read repetitively.

Observe: Data window as selected by digital delay with reference to the trigger pulse.

III. SPECIAL TROUBLESHOOTING TECHNIQUES

Logic analysis involves, in many cases, problems that go beyond simple display of data. The LOGIC ANALYZER has several capabilities that tailor it to solving these problems.

SPIKE DETECTION

One of these special troubleshooting capabilities consists of being able to detect narrow spikes between clock pulses in a data stream. When placed in the "SPIKE A" mode, the LOGIC ANALYZER ignores synchronous data and only indicates the location of spikes. These spikes may be caused by race conditions, ringing, noise, or design and are defined as more than one transition of the data on the A channel within one clock period. If the high to low transition occurs first, then the spike is defined as negative and displayed on the B channel. If the low to high transition occurs first the spike is positive and displayed on the A channel.

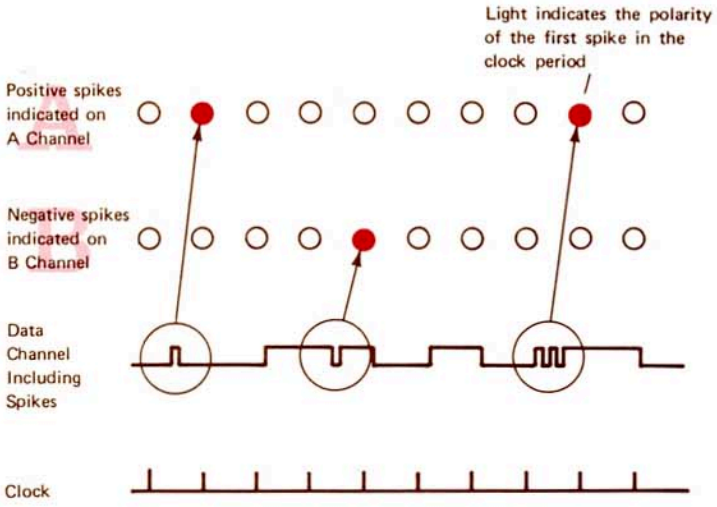


Figure 15. Spikes can be Detected and Located Within Synchronous Data

The "SPIKE A" mode, used in conjunction with the digital DELAY, can be used to look for spikes anywhere in a long serial data stream even on a single shot basis. The triggering and clocking of the ANALYZER take place exactly as before to provide a display reference and time base for the displayed spikes. The "SPIKE A" mode, therefore, not only detects spikes but also shows their position in the data stream.

TRIGGER OSCILLOSCOPE FROM LOGIC ANALYZER

In measurements where analog considerations such as risetime, ringing, voltage level or asychronous timing are of interest, an oscilloscope is an invaluable instrument. The combinatorial triggering and digital delay available in the LOGIC ANALYZER can be utilized to trigger an oscilloscope and therefore extend the triggering flexibility of the ANALYZER to an oscilloscope.

The TRIG OUT signal, available on the back panel of the LOGIC ANALYZER is used as the external trigger input to the oscilloscope. The TRIG OUT signal goes from TTL low to high at a point that corresponds to the loading of the ANALYZER display. TRIG OUT stays high until the display is loaded at which time a hold-off period (minimum 50 ms) is entered. During this 50 ms , the trigger is inhibited. This hold-off provides pulse stretching for any transient display and is necessary for the proper display of data.

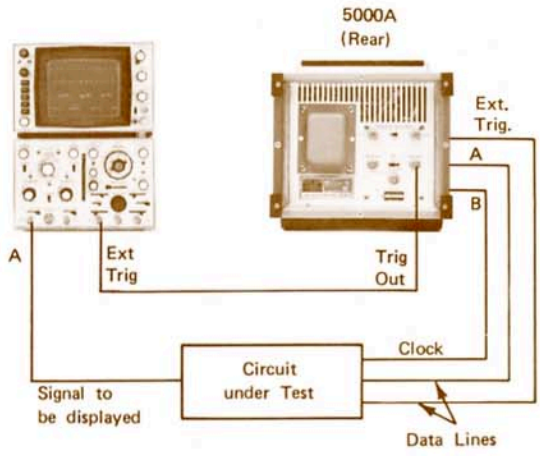


Figure 16. Triggering and Digital Delay Functions of the Logic Analyzer can Expand the Usefulness of an Oscilloscope

Under some conditions, the maximum trigger rate permitted by this 50 ms delay is not great enough to provide a bright trace on the oscilloscope. This condition is accentuated by any digital delay that is entered. If this is a problem, a storage oscilloscope can be used to capture the dim waveform. If a storage oscilloscope is not available, the ANALYZER can be operated in a hybrid mode that reduces the hold-off to 3 microseconds. This mode is selected internally on the "Control A" board by placing the programming plug in the "TEST" position. In this mode, however, the display cannot be used and must be disregarded. This mode of operation can be used whenever it is desired to use the LOGIC ANALYZER only as a trigger and digital delay generator. This mode is also useful when the ANALYZER is used as a serial-to-parallel converter (parallel data is available on the top connectors of the register boards).

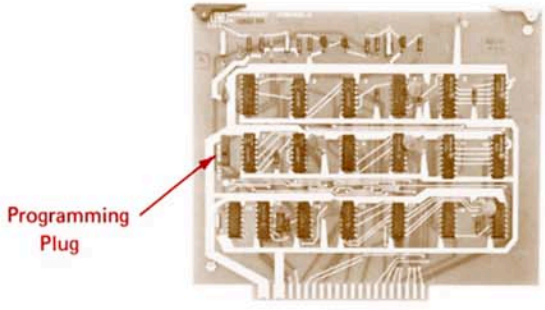


Figure 17. "Control A" Board

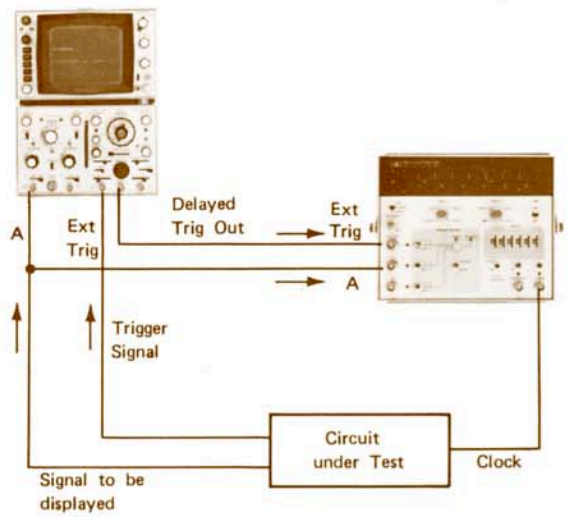


Figure 18. Analog Delay of an OSCILLOSCOPE Positions the Display of the LOGIC ANALYZER

TRIGGER LOGIC ANALYZER FROM OSCILLOSCOPE

An interesting marriage between a LOGIC ANALYZER and a delayed sweep oscilloscope can be made by connecting the oscilloscope to the data and sync source in the normal manner; the ANALYZER is then triggered from the delayed trigger output of the oscilloscope. This triggering scheme starts the display window of the ANALYZER at the same point the delayed sweep starts on the oscilloscope. Thus, by adjusting the analog delay control on the oscilloscope, the display window of the ANALYZER is smoothly moved along any portion of the oscilloscope waveform to be interrogated for data content or spikes. The start of the intensified region of the oscilloscope trace indicates the starting point of the ANALYZER display.

Procedure

Connect test set-up as shown.

On 5000A set:

INPUT Mode to "SPIKE A"

DISPLAY Mode to "DIRECT"

DELAY REFERENCE to "START"

WORD DELAY to "OFF"

Clock Slope as desired

RUN-STORE-RESET to "RUN"

CLOCKED-ASYNC to "ASYNC"*

DELAY to "000000"

Trigger: EXT TRIG to "—"

A to "OFF"

B to "OFF"

On Oscilloscope:

Adjust delay to interrogate desired portion of oscilloscope waveform for spikes.

*Note: The spike nature of the trigger pulse requires the use of Async Mode. The threshold of the ANALYZER must be set to a level that is compatible with this pulse.

IV. GLOSSARY OF TERMS

Analog Delay: Delay period, whose length is determined by time.

Armed: Logic Analyzer is ready to accept a trigger. In "RUN", Armed occurs after a display is loaded and the HOLD-OFF delay is completed.

Async Triggering: Used only to trigger on conditions that cannot be sampled by clock (e.g. spikes).

Bit: Smallest piece of binary information, either a logic ONE or ZERO at a given point in time.

Clock: Most basic signal in a digital system. Often free-running, derived from a crystal, the prime-mover of the system.

Clocked Flip-Flop: Digital storage device whose input is transferred to the output and stored only on signal from a clock (strobe).

Clocked Triggering: Trigger condition is sampled by clock. Spikes or transients will not be detected as triggers. Should be used in most cases.

Delay: Period between trigger event and start of data input. May be analog or digital.

Digital Delay: Delay interval whose length is an integral number of pulses (usually clock pulses).

Edge Sensitive (Logic Analyzer Triggering): "CLOCKED" Mode—LOGIC ANALYZER triggers only on the first of a group of consecutive data bits that all satisfy the trigger condition.

"ASYNC" Mode—LOGIC ANALYZER triggers only on the first *spike or data bit* of a group that satisfies the trigger condition.

Hold-Off (Rearming Time): For the LOGIC ANALYZER, the interval between the end of a display sweep and the point at which the ANALYZER will accept a new trigger.

"Negative Delay" (pre-trigger storage): LOGIC ANALYZER function selected by DELAY REFERENCE "END". Permits display of *data preceding the trigger* by loading the display with data that is delayed by 32 clock periods (64 in "SERIAL A") through a shift register.

Parallel: Occurring simultaneously in time.

Parallel Word: N bits of information occurring on N different data lines or nodes at the same time.

Register:	A data storage device.
Serial:	Occurring consecutively in time.
Serial Word:	N bits of information occurring one at-a-time on one data line during N consecutive clock cycles.
Setup Time:	The time before clock pulse edge when data inputs must be steady.
Spike:	More than a single transition between clock pulses.
Synchronous System:	Controlled by a clock.
Threshold Voltage:	The voltage that determines logic HIGH and LOW for the Analyzer. Voltages above threshold voltage are HIGH. Voltages below are LOW.
Trigger:	An event from which other events (data input, display, or delay countdown) are referenced.
Triggered:	Trigger conditions set up by TRIGGER CONTROL were met while LOGIC ANALYZER was ARMED.
Word:	A group of bits forming a functional unit in which information is encoded and which is processed as a unit.



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