
Low Cost Surface Mount Power Limiters

Application Note 1050

Abstract

Many receivers are often at risk of having their front ends burned out by high power RF and microwave stray signals. This paper presents practical design techniques for low cost power limiters operating at frequencies below 2 GHz. Both circuit techniques and Surface Mount Devices (SMD) diode trade-offs are covered. Measured data on several different prototype limiters are presented.

Introduction

Microwave and RF receivers, as well as many instruments, are susceptible to damage from input signals having amplitudes which exceed some danger level. For some instruments, such as counters, this danger level may be as high as one watt. The front end of some receivers can be destroyed or degraded by power levels substantially less than one watt. Furthermore, the danger may come from signals which are out of the normal operating band of the device. Thus, for example, a GPS or mobile telephone receiver, operating at L-Band, could be damaged by a nearby X-

Band airport radar or the C-Band radar of a nearby ship. Such sensitive instruments and receivers are traditionally protected by a power limiter circuit.

The limiter should have the following characteristics:

- It should provide very low insertion loss to in-band small signals (the desired signals) in order to keep receiver noise figure as low as possible.
- It should provide very high loss to incoming signals which exceed the danger threshold.
- It should be very fast, providing protection within nanoseconds of the arrival of a damaging signal.
- Unlike a fuse, it must survive exposure to the high power signal and it must return to its low loss (small signal) behavior within nanoseconds after the high power signal has disappeared.

In the microwave frequency range, such limiters have

traditionally been designed around a special type of PIN diode called a limiter diode. However, the price of such diodes is prohibitively high for consumer and commercial applications. This paper will describe the application of a low cost SMD PIN diode to the design of a limiter circuit operating up to 2 GHz.

Limiter Diode Basics

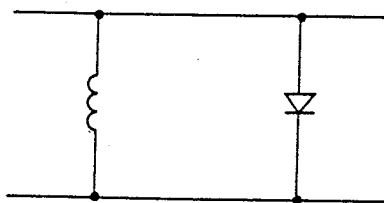
The limiter diode is a special type of PIN diode. A thin epitaxial I-layer is formed on a heavily N⁺ doped substrate, after which P⁺ top contacts are added by diffusion. Typical limiter diodes have I-layer thicknesses between 2 μm and 7 μm, with corresponding values of breakdown voltage. The diode is mounted in shunt across the transmission line which leads to the receiver front end, and is provided with a DC bias return, as shown in Figure 1. For incoming signals which are below the threshold level in amplitude, the diode acts as an ordinary unbiased PIN diode¹, which is to say that it appears to be a capacitor of

¹Hewlett-Packard Application Note 922, "Applications of PIN Diodes"

relatively small value. When the incident signal exceeds the threshold power level, the diode's I-layer is flooded with carriers during the positive half-cycle of the incoming RF signal. Most of these carriers persist through the negative half cycle, DC current begins to flow in the loop formed by the diode and the bias return choke, and the diode biases itself to a low value of resistance in a matter of nanoseconds. Under the influence of this self-generated bias current, the diode's junction resistance falls to a very low value, shorting out the transmission line. The limiter circuit then acts as a reflective switch, reflecting the large signal back to its source and protecting the circuitry which is "downstream" from the limiter. When the large amplitude incoming signal has disappeared, the carriers in the diode's I-region recombine in a matter of nanoseconds, the circulating bias current stops and the diode's junction resistance once again becomes very high, allowing small signals to pass.

Limiter Diode Design Tradeoffs

Several trade-offs exist in the design and selection of epi PIN diodes for limiter applications. For example, diodes with thick I-layers turn on "late" (at high levels of input power), while those with thin I-layers turn on "early." However, those with thin I-layers are easily damaged by high power, since they lack the breakdown voltage and thermal conductivity of the thicker diodes. The behavior of three different limiter diodes, having I-layers of 2 to 15 μm , is illustrated in Figure 2.



$$35 < V_{br} < 70V$$

$$2\mu < W < 7\mu$$

Figure 1. Basic Limiter Circuit.

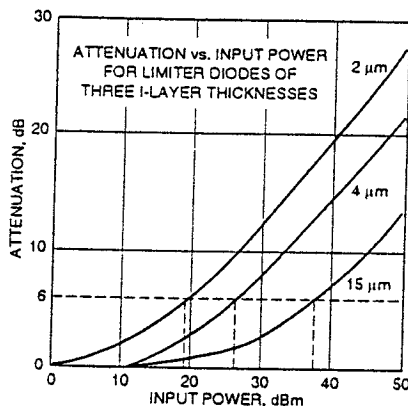


Figure 2. Comparison of Three Limiter Diodes.

When a transmission line is shunted by a resistor (such as a self-biasing PIN diode), some of the incident power is reflected back to the source, some passes the resistor and is received in the load, and some is dissipated in the resistor (in the form of heat). The percent of incident power which is actually dissipated in the shunt device is a function of its resistance, as shown in Figure 5. At a value of 25 Ω (in a 50 Ω system), this fraction reaches a maximum of 50%. This 25 Ω shunt resistance corresponds to an attenuation of 6 dB. Thus, a thick limiter diode which turns on late (see Figure 2) may pass through this (6 dB) point of maximum dissipation at a sufficiently high power level that it will itself burn out (as well as being too "slow" to protect a receiver front end). Thus, a diode with a 2 μm I-layer thickness

may be too fragile to make a good limiter while one which is 15 μm thick is too slow. Clearly, there is a narrow range of optimum I-layer thickness for an effective limiter diode.

In the design of low current, low R_S PIN diodes for switching applications, the use of a thin epitaxial I-layer offers a low cost approach to meeting these design goals. Hewlett-Packard's HSMP-4820 surface mount PIN diode was evaluated in a series of limiter configurations. These PIN diodes were found to perform quite well as limiters, as described below.

Package Considerations

The performance of the limiter is governed by the characteristic of the PIN diode, the package and the circuit in which it is contained.

Continuous wave power handling capability is set by the maximum junction temperature and the thermal resistance between junction and ambient. One major contributor is the thermal resistance of the package (θ_{package}) and the kind of heatsink. The maximum power dissipation of the diode can be estimated by using the following formula:

$$P_d = \frac{T_{j\text{max}} - T_a}{\theta_{j-a}}$$

$$\theta_{j-a} = \theta_{\text{chip}} + \theta_{\text{solder}} + \theta_{\text{package}} + \theta_{\text{heatsink}}$$

j-a: junction to ambient

P_d : maximum power dissipation

$T_{j\text{max}}$: maximum junction temperature

T_a : ambient temperature

There are large differences in the value of package thermal resistance from one package type to another. For example, the thermal resistance of the bolt channel package (e.g., the HP package outline 61) is $\approx 25\%$ of the value for the SOT-23 package.

Insertion loss, isolation and maximum frequency range are not only determined by the diode's capacitance and resistance. Package inductance (due to bondwires and package leads) and the specific circuit layout degrade the high frequency performance of the limiter as well.

The ideal limiter package should meet the following major requirements:

- Broadband
- Low thermal resistance
- Easy to assemble
- Inexpensive

The bolt channel package (HP outline 61) is an ideal package for broadband, high frequency and high power applications. Internal bondwires add the proper amount of series inductance to resonate the junction capacitance of the diode chip, forming a low pass filter with $f_c > 12$ GHz. The limiter chip in the bolt channel package can be functionally integrated into a 50Ω balanced strip line or microstrip transmission line² and can be used up to X-band applications. Insertion loss and isolation are specified at 9.4 GHz in the data sheet.

The gold plated copper body and the gold plated kovar leads of the bolt channel package achieve an

excellent thermal conductivity and give high power handling capabilities as high as 50Ω peak.

The HP bolt channel limiter 5082-3071 is successfully used in many military systems like radars, EW equipment, radios, telemetry equipment and many others. It's an excellent limiter but too costly for high volume commercial applications such as the 1.5 GHz Global Positioning System (GPS) receivers. To achieve the price targets for consumer and commercial applications semiconductor manufacturers have to offer surface mount components such as the Hewlett-Packard HSMP-382X SMD PIN diode series, available in the SOT-23 package.

The SOT-23 is a plastic package with tin/lead plated leads suitable for various soldering processes such as wave soldering,

infrared reflow soldering and vapor phase reflow soldering. In high volume low cost commercial applications, surface mount technology is widely accepted. The JEDEC standard Surface Mount Packages (SOT-23 and SOT-143) are excellent packages with respect to automatic SMD pick and place assembly and are therefore well accepted by the industry.

Many diode configurations, such as singles, series pairs, common anode and cathode pairs and others, are available in a single SOT package for specific applications. This enables the design engineer to minimize his circuit and manufacturing costs. However, the disadvantage of this package is the inherently long bondwire inside the package, and the bent leads, as shown in the top of Figure 3. This

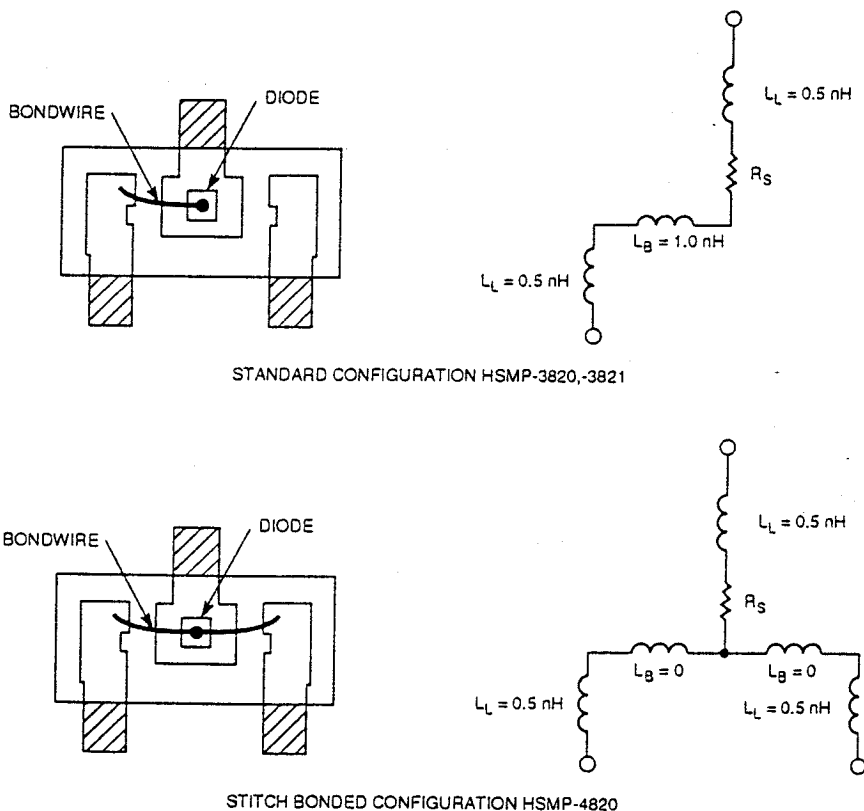


Figure 3. Bondwire Configuration in the SOT-23 Package.

²Hewlett-Packard Application Note 957-2, "Reducing the Insertion Loss of a Shunt PIN Diode"

bondwire ($L_B = 1.0$ nH) with the two bent leads ($L_L = 0.5$ nH each) create a total series inductance of 2 nH. This high value of parasitic inductance will result in a high reactance at frequencies above a few hundred MHz. The result, in a shunt-mounted diode, is a reduced value of isolation as shown in Figure 4. Another important parasitic is the package capacitance, typically 0.08 pF between opposite leads. It has a minor impact on isolation performance in comparison to the high inductance over the frequencies under discussion.

The PIN diode chips are die attached on the Alloy 42 (Fe/Ni) leadframe using conductive epoxy. After wirebonding, a molding process takes place and in the next step the leads become tin/lead plated. Most of the heat generated at the diode's junction due to high power signals can only dissipate through the silicon, epoxy and leadframe into the heatsink or PCB. The thermal resistance, measured from the diode junction to an infinite heatsink, is approximately 500 °C/W. It should be kept in mind that the application-specific circuit layout and PCB material will raise the thermal resistance from diode junction to ambient air. How-

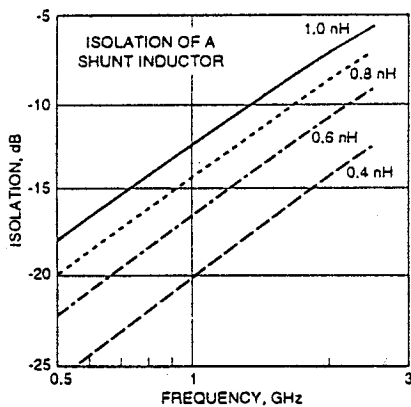


Figure 4. Effect on Isolation of Excessive Parasitic Inductance.

ever, during informal testing, the HSMP-4820 diode has shown the ability to stand off 8 to 10 watts of CW input power at 25°C when used as a limiter. To calculate power handling at high temperatures, derate this value linearly from 10 watts at 25°C to zero watts at 150°C. To calculate the approximate pulse power handling capability, multiply this CW power rating by the factor shown in the curve given in Figure 6, keeping in mind that the pulse duty factor must be such that the average incident power must be less than half the CW power rating. Note that all of these thermal calculations are estimates.

Up to this point, the discussion has focussed on two standard packages, the bolt channel (with its superior performance) and the standard SOT-23 (with its low cost). We will now turn to a discussion of solutions to the problem of extending the limiter's bandwidth. All solutions use a "stitch bonded" PIN diode in a SOT-23, as shown on the bottom of Figure 3. This special product is a standard surface mount diode with an additional bondwire "stitch bonded" from the die's bond pad to the normally unconnected package lead.

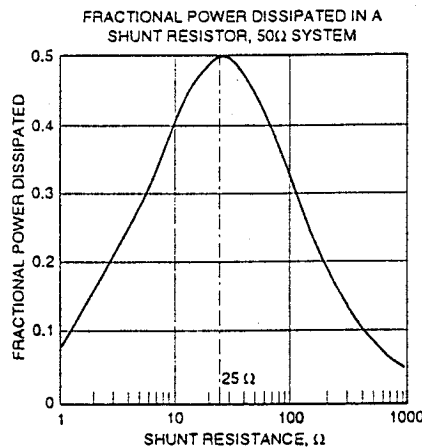


Figure 5. Power Absorbed in a Limiter Diode.

Two bondwires, electrically in parallel, exhibit only half the inductance of a single bondwire. However, because of their very close proximity, the two parallel bondwires are coupled resulting in a cancellation of the inductance L_B , as shown in the schematic at the bottom of Figure 3.

To examine the effect of parasitics upon limiter performance, consider a HSMP-3820 SMD PIN in a microstrip shunt application. Two effects of parasitics reduce the bandwidth of the limiter. One is the parasitic inductance of the package, the other is the inductance of the via holes which bring ground potential up from the microstrip groundplane. The package inductance is nearly constant, tightly controlled by the diode manufacturer due to automatic wire bonders, where the via hole inductance depends on several factors such as the PCB material, metallization, thickness and hole diameter.

In a shunt configuration, lead and bondwire inductance of the surface mount package prevents higher frequency signals from being shorted by the diode's low resistance. The reactance due to the parasitic inductance is much higher (approximately 19.Ω at

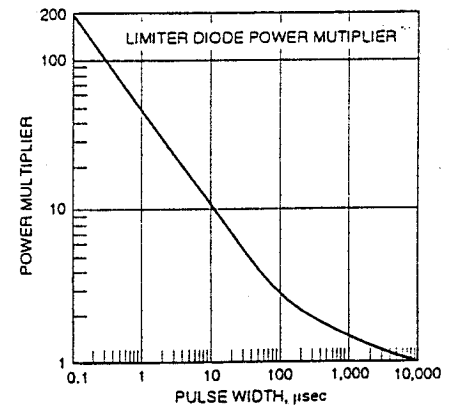


Figure 6. Power Multiplier For Operation With Short Pulses.

1.5 GHz) than the RF resistance (approximately 1Ω). This behavior is illustrated in more detail in Figure 4. This set of curves shows isolation for different values of inductance versus frequency for an ideal diode with $R_s = 0 \Omega$. It can easily be seen that the standard HSMP-3820, with its 2 nH lead inductance, can only be recommended as a limiter at frequencies below 500 MHz.

Transmission Line Considerations

When a SMD is mounted in shunt in a microstrip line, some complication is introduced. Plated-through via holes must be used to bring ground up to the top surface of the board. Not only do these via holes introduce some additional expense, but

they also insert a small amount of parasitic inductance which appears (electrically) between the SMD and ground, reducing the amount of available isolation. This is treated in more detail in the following section. CoPlanar Waveguide (CPW) is a type of transmission line in which some of these problems are eliminated. The following treatment of CPW is taken from Waugh and Waugh³.

The configuration of CPW is shown in Figures 7 (plan view) and 8 (cross section). CoPlanar Waveguide is a transmission line having ground and center conductor on the same plane of a circuit board. The underside of a CPW board is blank, with no copper traces and no ground-plane. Transmission line imped-

ance is set by the dimensions shown in Figure 8. Note that both the linewidth and gapwidth control Z_0 . In order to calculate the characteristic impedance from these dimensions, one can use a computer program such as AppCAD⁴ or MWTL⁵. However, a simplification is possible. In order to allow a SOT-23 diode to straddle the CPW as shown in Figure 7, the sum of linewidth plus 2 times gapwidth (dimension $2b$) must be maintained a constant equal to 0.055 inch. When this design restriction is applied, the computation of characteristic impedance is reduced to the simple graph given in Figure 9 (shown for two different board materials).

Like microstrip, CPW is sensitive to effects from the top and bottom covers of the housing in which the board is mounted, as well as coupling between transmission lines. See Figure 10. Some good rules of thumb when using CPW are as follows: If $D > 2b$, Z_0 is independent of substrate thickness. Keep $S_1 > 3b$. If $H_1 > 4b$ and $H_2 > 3b$, the covers can be ignored in all calculations of Z_0 . Maintain $S_2 > 5b$ to avoid coupling between adjacent lines.

In order to obtain good performance from a circuit realized in CPW, the potential of the groundplanes on either side of the center conductor must be kept equal at all points along the line. This is illustrated in Figure

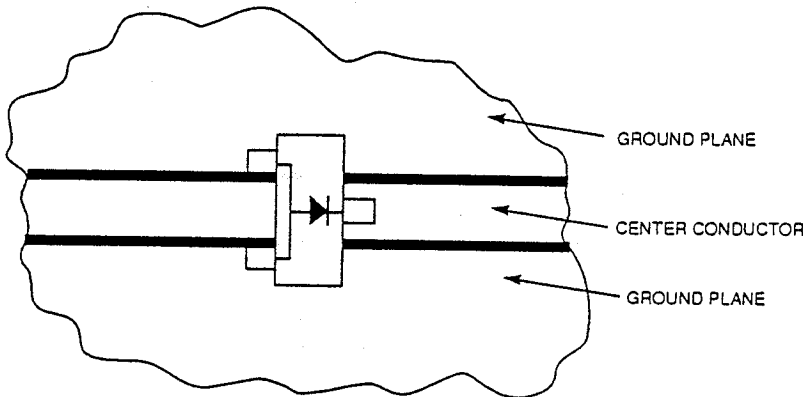


Figure 7. Plan View of a CoPlanar Waveguide With SOT-23 Shunt Diode.

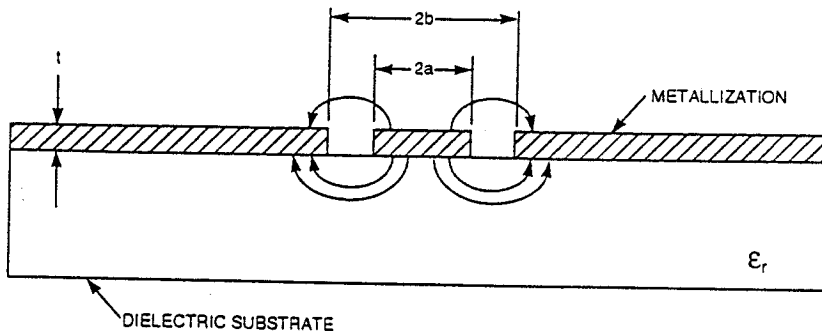


Figure 8. Cross Section of a CoPlanar Waveguide.

³R. W. Waugh and R. M. Waugh, "A Shunt PIN Diode T/R Switch for PCN Applications," to be published in the near future.

⁴Hewlett-Packard, "RF and Microwave AppCAD," HP part number HAPP-0001.

⁵Daniel Swanson, "A Transmission Line Calculation Program," *RF Design*, August, 1991, pp 66-67.

11, in which it is shown that conductive bridges, spaced every $\lambda/4$ to $\lambda/2$, will maintain ground planes at the same potential.

Shunt stubs or transmission line intersections in CPW can lead to problems. Refer to Figure 12. Currents flowing along the ground planes are equal (in phase) at plane I, but unequal at plane II because of the longer length of the path taken by I_1 . A conductive bridge, as shown in Figure 13, solves the problem. If one is using surface mount technology, an interconnecting line on the backside of the board, with two via holes connecting it to the two ground-planes, reduces pick and place

operations and gives the same electrical results as the topside conductive bridge.

At frequencies higher than those reported here, similar problems can occur at bends in transmission lines. Conductive bridges interconnecting the ground planes are required, or one can maintain the ground plane intact and bridge the line as shown in Figure 14.

Finally, the question of a transition between CPW and microstrip must be discussed, since any CPW component will eventually have to interface with a conventional microstrip circuit. In Figure 15 such a transition is shown. This transition works well to frequencies as high as 3 GHz.

Several of the circuits were realized in CPW, fitted with SMA connectors (E.F. Johnson 142-0701-801) which are designed for use with CPW.

The circuits were fabricated on HT-2 PCB (Printed Circuit

Board) material. HT-2 is a new PCB material offered by Hewlett-Packard's Printed Circuit Board Division. Based upon cyanate ester resin chemistry, it has superior thermal and mechanical properties when compared to conventional FR-4. Dielectric constant is better controlled, and somewhat lower in value.

Loss tangent of HT-2 is lower than that of FR-4, resulting in a board material which is practical to use at microwave frequencies. In both microstrip and CPW circuits on 0.032" material, losses are about 0.6 dB/λ through 6 GHz. The characteristics of HT-2 are compared to those of FR-4 in Figures 16 and 17.

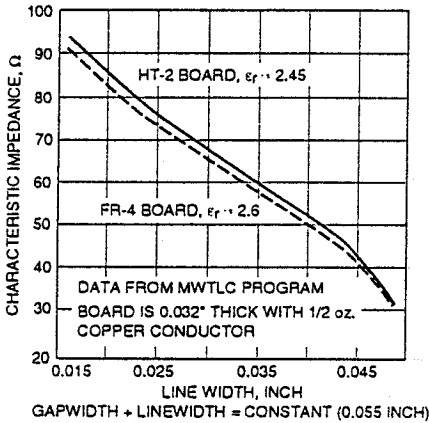


Figure 9. Characteristic Impedance of a CPW Line.

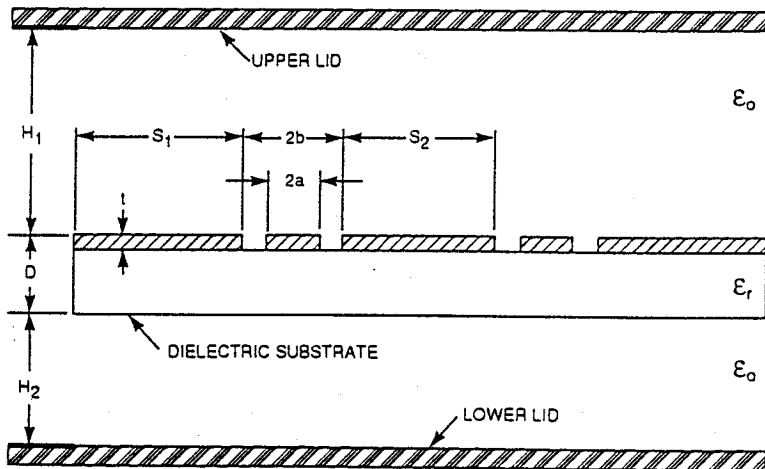


Figure 10. CPW Mounted in a Housing.

Single Diode Test Circuits

Throughout the sections that follow, the terms "insertion loss" and "isolation" will be used. While both apply to the attenuation produced by a shunt mounted limiter diode and its associated circuitry, it is understood that "insertion loss" refers to the undesirable loss under small signal conditions, when the diode's junction resistance is very high. "Isolation," on the other hand, will be used to describe the protective attenuation provided by the diode and circuit under the application of high power signals, when R_j is low.

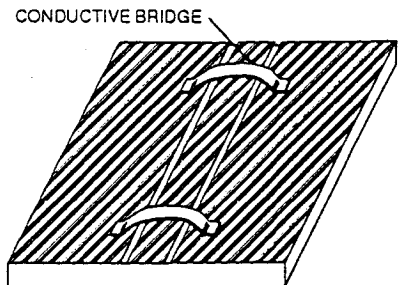
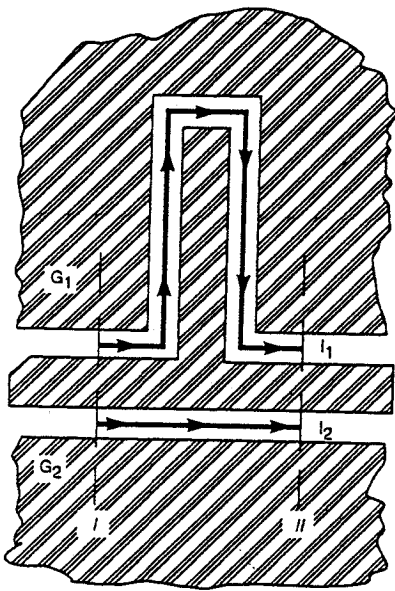
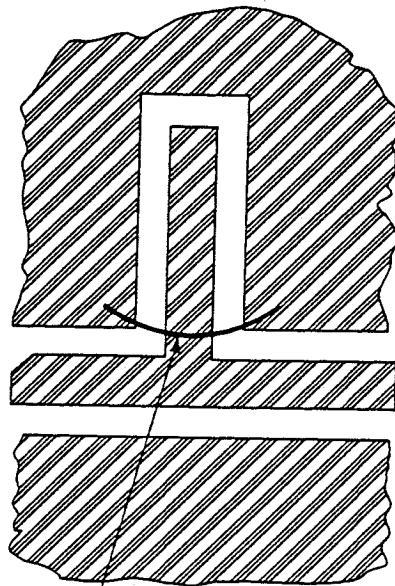


Figure 11. Maintaining Groundplanes at Equal Potentials.



$l_1 = \frac{1}{2} \text{ AT } I$
 $l_1 \neq \frac{1}{2} \text{ AT } II Z$



CONDUCTIVE BRIDGE

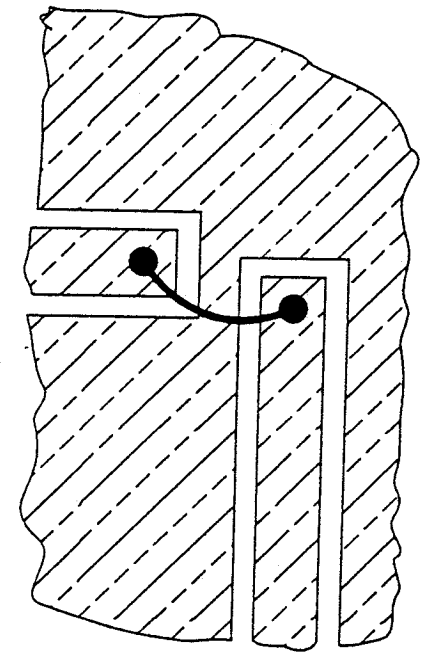





Figure 12. Uncompensated Shunt Stub in CPW.

Figure 13. Compensated Shunt Stub in CPW.

Figure 14. Compensated CPW Bend.

-  0.030 INCH DIAMETER PLATED THROUGH VIA HOLE
-  TOP SIDE (CPW) GROUNDPLANE
-  UNDERSIDE (MICROSTRIP) GROUND

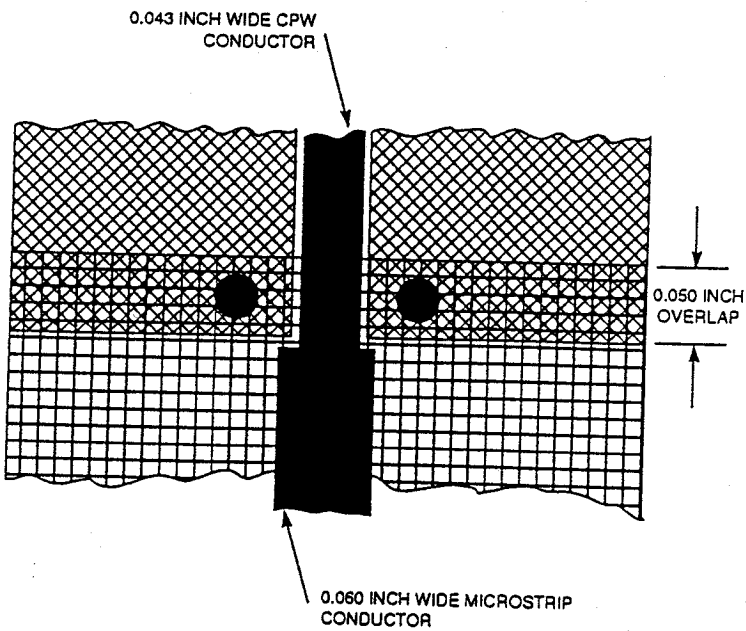


Figure 15. Microstrip to CPW Transition.

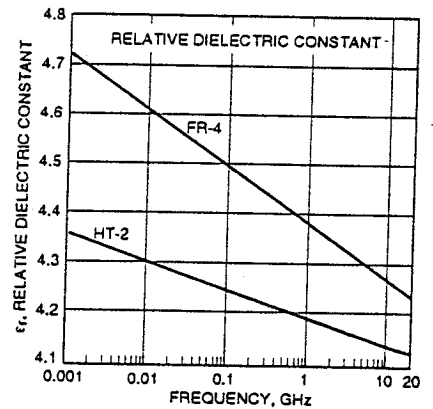


Figure 16. Comparison of Dielectric Constant.

The most obvious way in which to mount a SOT-23 packaged limiter diode in shunt across a microstrip line is shown in Figure 18. Two leads of the SOT-23 package are mounted in parallel on the 50 Ω transmission line and the third lead is soldered on the ground pad as shown. Using the stitch-bonded HSMP-4820, this approach simply takes advantage of the additional parallel bondwire which reduces the package inductance to $L_p = 0.75\text{nH}$. Adding the via hole inductance of $\approx 0.3\text{nH}$ resulting from the use of 0.032" thick HT-2 substrate, the total parasitic inductance is 1.05 nH.

Referring to Figure 4, isolation of this limiter is estimated to be about 9 dB in the GPS frequency range, a value of protection which will not be considered sufficient in many applications. Moreover, under small signal operating conditions, the 50 Ω microstrip transmission line is shunted by a series L-C combination of 1 nH and 0.8 pF. A quick analysis on AppCAD⁴ shows that this combination forms a resonant circuit at $\approx 5\text{ GHz}$, a very undesirable characteristic (see Figure 19). Even at lower frequencies, such as those used in GPS systems, the losses are unacceptably high as can be

seen from the AppCAD analysis shown in Figure 20. However the next section describes a more efficient circuit approach, yielding higher values of isolation and lower insertion loss, which does not entail any additional expense.

This improved design approach integrates the bondwire inductance into the 50 Ω microstrip transmission line by cutting a gap in the line and bridging the gap with lead #1 and #2 of the stitch bonded limiter diode. Lead #3 must be grounded as shown in

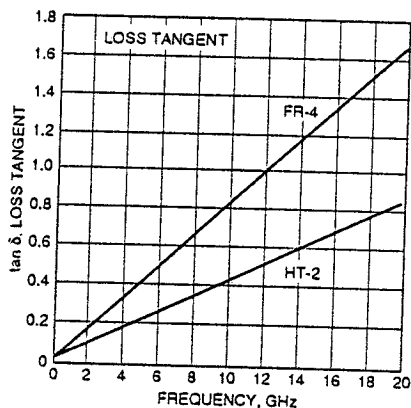


Figure 17. Comparison of Loss Tangent.

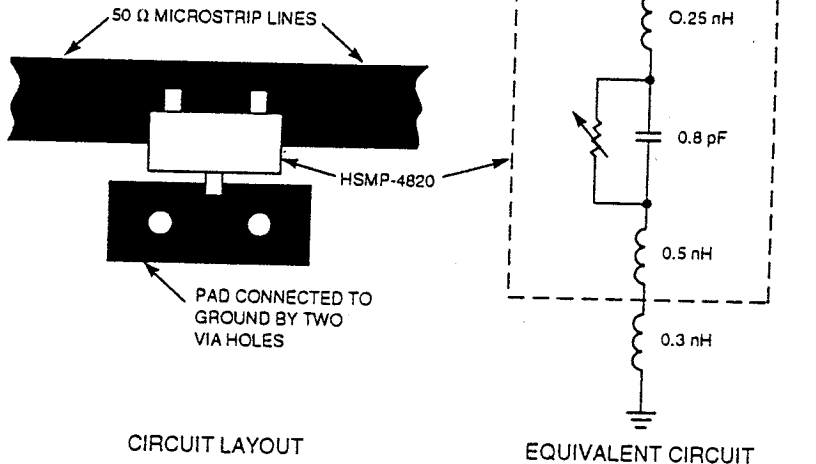


Figure 18. Shunt Mounted SOT-23 Limiter Diode.

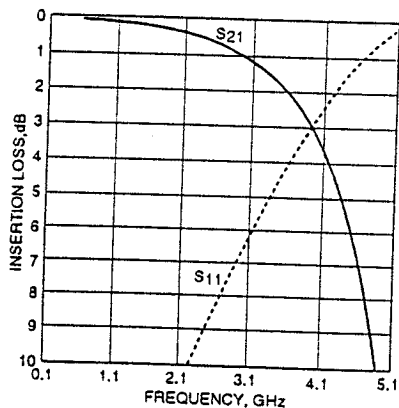


Figure 19. Small Signal Insertion Loss of the Shunt Mounted Limiter.

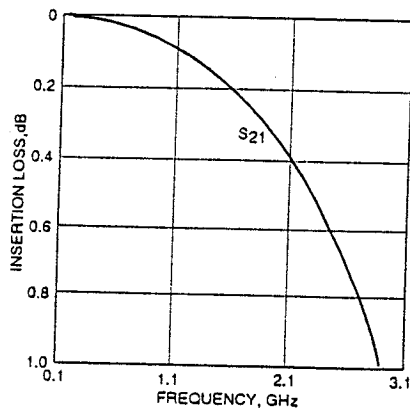


Figure 20. Detail of Small Signal Insertion Loss of the Shunt Mounted Limiter.

Figure 21. The result is a circuit which, under small signal operating conditions, looks like a low pass filter structure with a higher cutoff frequency than observed in first approach. As described in AN 957-2², this helps to reduce the small signal insertion loss in the pass band. Under high power signal conditions, the resistance of the diode is reduced to an ohm or so. Under these conditions, the lead

inductance plus via hole inductance ($L = L_L + L_V = 0.5 \text{ nH} + 0.3 \text{ nH}$) becomes the dominant factor in total shunt impedance. This total shunt inductance of 0.8 nH is less than the 1.05 nH of the first circuit approach. Reference to Figure 4 will show that a 2 dB improvement in isolation results.

A test circuit was built to verify the simulations by actual mea-

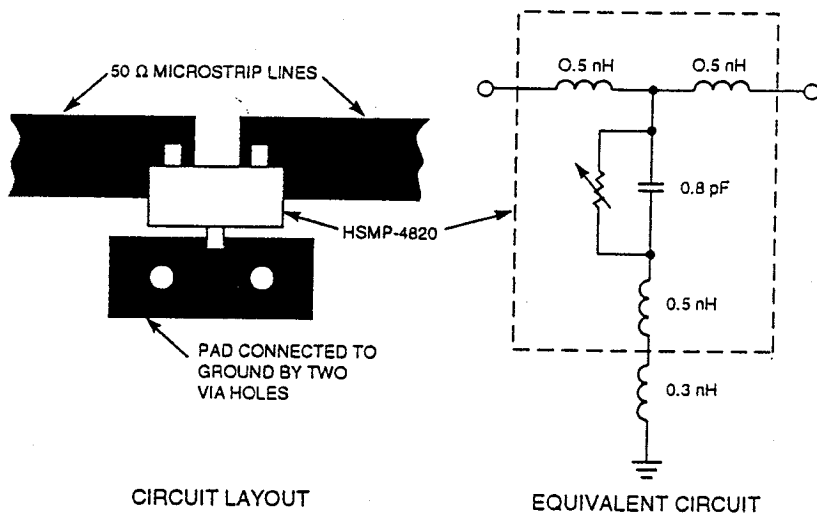


Figure 21. Improved Shunt Mounting Technique.

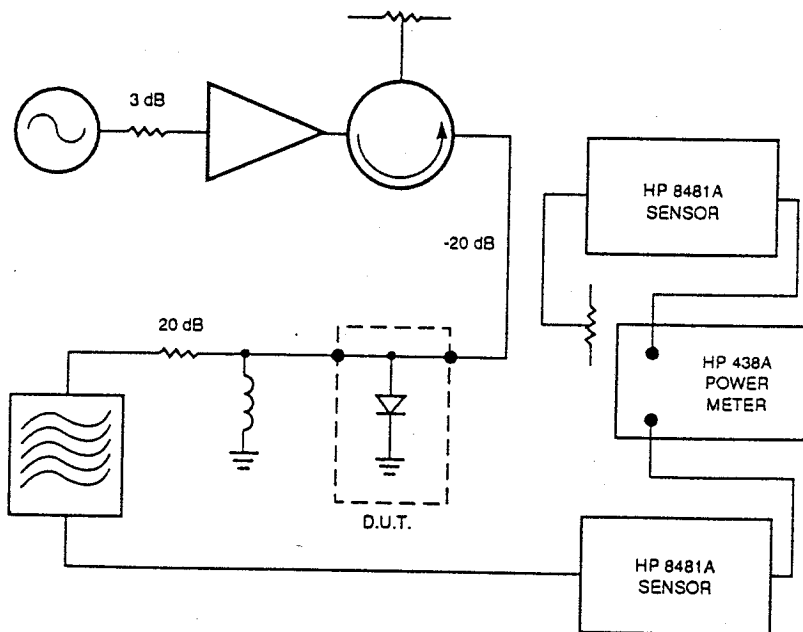


Figure 22. Apparatus Used For High Power Measurements.

surements. Small signal measurements such as insertion loss were made with a scalar network analyzer. The high power measurement test setup for 1 GHz and 1.5 GHz tests is shown in Figure 22. Limiter diodes share many of their characteristics with step recovery diodes. Therefore, under high power conditions the limiter diode generates a comb of harmonic outputs. Specifically the second harmonic output power level can be close to that of the fundamental. Therefore a low pass filter is necessary to reduce the second harmonic at the power meter to get a proper reading. To prevent damage to the power amplifier by high power reflections a circulator was used to terminate the reflections. Notice that the limiter circuit DC return is provided by an external bias network.

Small signal insertion and return loss for the improved circuit of Figure 21 were measured over frequency at low power levels (-10 dBm) and displayed in Figure 23. This and all other insertion loss measurements were made with respect to a 50Ω reference line of the same physical length as the limiter

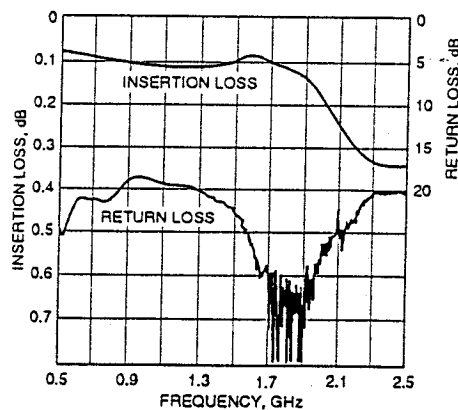


Figure 23. Small Signal Performance, Improved Limiter Circuit.

test circuit. Insertion loss of the improved limiter circuit is 0.1 dB all the way up to 1.7 GHz and increases to about 0.35 dB at 2.5 GHz. In the GPS band (1.5 GHz) return loss is better than 20 dB. These measured results agree well with the simulated values.

Limiter isolation performance under high power conditions was simulated by small signal measurements using an externally applied DC bias to reduce the diode junction resistance R_j to its minimum value. The results are shown in Figure 24. At 1.5 GHz the reading of isolation is 11.5 dB, which is close to the value of 11 dB calculated using Figure 4. The effect of the parasitic inductance can be seen in the decrease in isolation from 21 dB at 500 MHz to 9 dB at 2.5 GHz. Finally, the improved limiter was tested under high real power conditions at 1 GHz and 1.5 GHz. The maximum applied CW power was 10 watts at 1 GHz and 1 watt at the higher frequency. Results are shown in Figure 25; note that the threshold level is in the range of $P_{in} = 8$ dBm. Above this threshold level the limiting effect takes place and reaches its maximum isolation of 17 dB at 35 dBm input power at 1 GHz. However, at 1.5

GHz the limiter reaches a maximum insertion loss of 10 dB at 27 dBm input power. The different characteristics of the 1 GHz and 1.5 GHz curves correspond to the variation in externally biased isolation as shown in Figure 24.

Figure 26 shows the large signal transfer curve of P_{out} versus P_{in} , the same data of Figure 25 displayed in a different format. From it one can easily see that the circuit maintains output leakage power to less than 100 mW for input power levels of 1 watt at 1.5 GHz and up to 5 watt at 1 GHz input power.

Up to this point, the tests and measurements described have highlighted the performance of the stitch bonded PIN diode mounted in microstrip transmission lines. As described above, a major contributor to the lack of isolation performance is the via hole inductance to ground. This fact led us to consider CoPlanar Waveguide technology, bypassing the problem of parasitic via hole inductance.

Based on the same idea of integrating the lead inductance into a 50 Ω transmission line to form a low pass filter structure, a co-

planar waveguide test circuit shown in Figure 27 was fabricated using HT-2 substrate material. As can be seen from the equivalent circuit in Figure 27, the elimination of via hole inductance reduces the total parasitic inductance to 0.5 nH, offering the possibility of higher isolation than the improved microstrip limiter described above.

Insertion loss at low input power levels was measured on the CPW test circuit, with the results as shown in Figure 28. Insertion PIN diode is mounted with the two interconnected leads straddling the transmission line, as loss is quite good below 1 GHz and rolls off badly around 1.3 GHz. High input power levels were simulated by externally biasing the diode to display isolation performance versus frequency (Figure 29). Compared to the microstrip approach an improvement of 4 dB is demonstrated, as expected. Nevertheless this version is more complicated to fabricate due to the conductive bridges. Also the insertion loss roll off is another disadvantage which will become a noise figure problem above 1.5 GHz in receiver front ends.

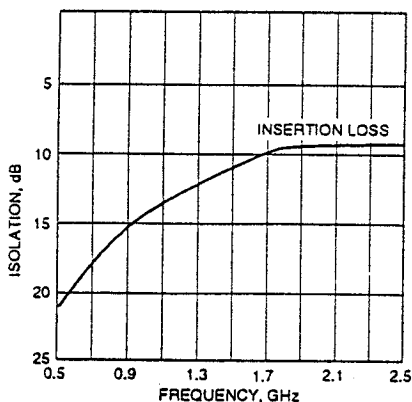


Figure 24. Isolation With Externally Applied DC Bias, Improved Limiter.

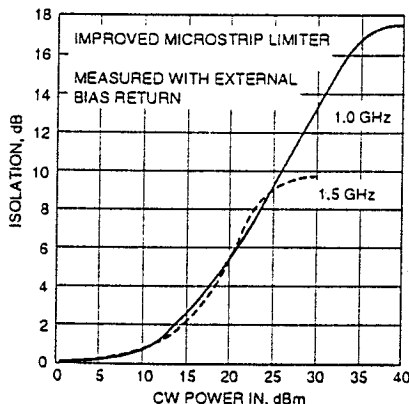


Figure 25. Large Signal Isolation of the Improved Limiter.

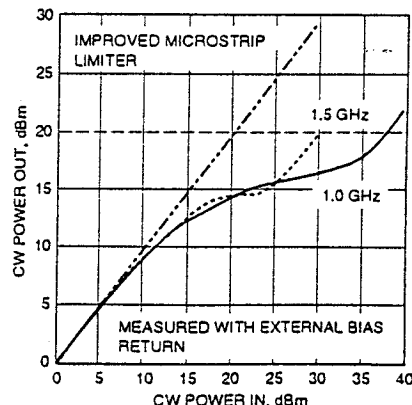


Figure 26. Large Signal Transfer Curve of the Improved Limiter.

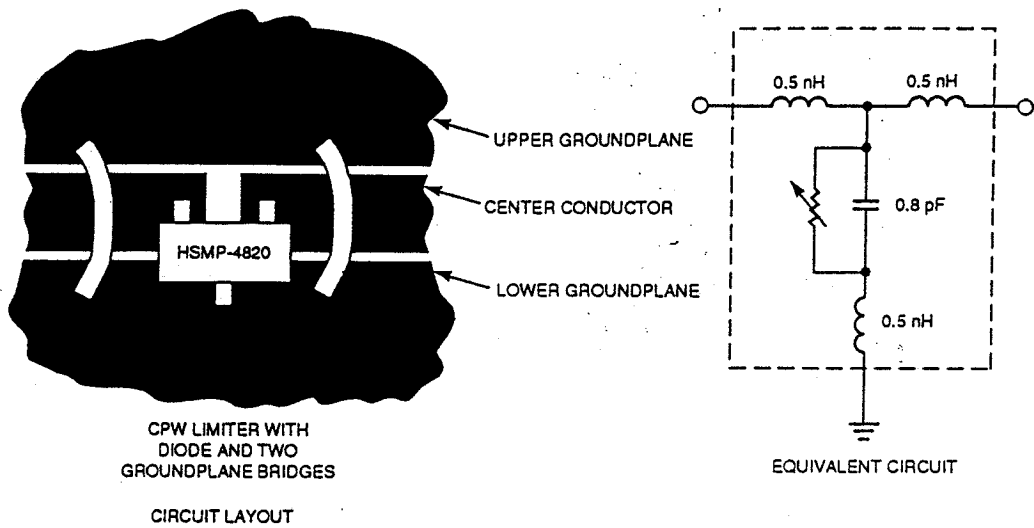


Figure 27. CoPlanar Waveguide Limiter Circuit.

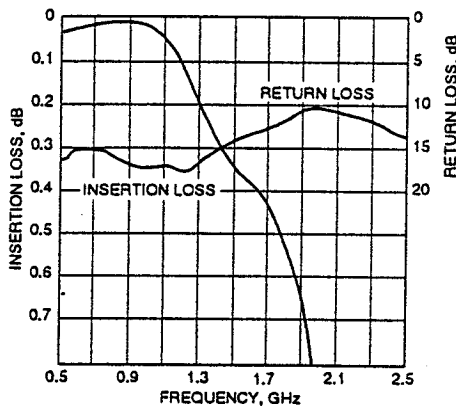


Figure 28. Small Signal Performance, CPW Limiter.

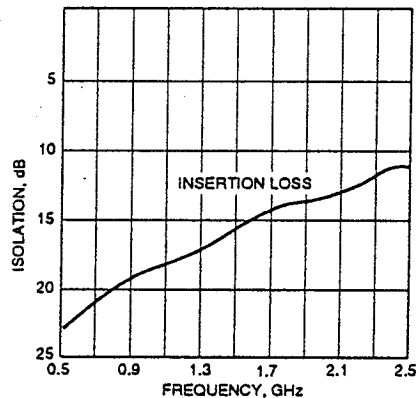


Figure 29. Isolation With Externally Applied DC Bias, CPW Limiter.

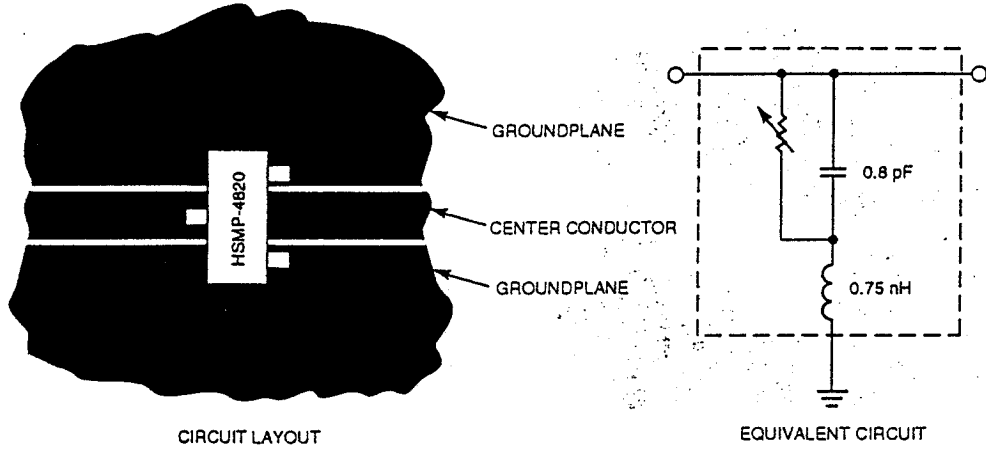
In the next section a more convenient and lower cost coplanar waveguide approach will be presented. The stitch bonded PIN diode is mounted with the two interconnected leads straddling the transmission line, as shown in Figure 30, eliminating the conductive bridges. The package inductance to ground is reduced to 0.75 nH. Unfortunately, the low pass filter structure is lost in this mounting. Low input power measurements show an excellent insertion loss performance below 1 GHz, with a bad roll off above 1.3 GHz.

Isolation performance was simulated by forward biasing the diode. At 1.5 GHz the isolation is around 13dB, 1.5dB better than the improved microstrip approach of Figure 21. Next, measurements were made of the limiting performance under high power conditions. At 1 GHz the maximum achieved isolation was around 17 dB and the maximum isolation at 1.5 GHz is close to 13 dB - the best result we achieved with a single limiter diode. The improvement of 3 dB compared to the improved microstrip design can be explained by the low total parasitic

inductance to ground. Output power leakage (Figure 31) is well below 15 dBm for frequencies up to 1.5 GHz and input power levels up to 25 dBm. Only above 5 watt input power will the leakage be higher than 100 mW at 1 GHz.

Transmission Lines and $\lambda/4$ Spacing

If a shunt attenuating element produces X dB of isolation, two of them spaced very closely together (compared to a wavelength) will produce X + 3 dB of isolation. However, if they are spaced $\lambda/4$ (a quarter wavelength) apart, the pair will produce appro-



CIRCUIT LAYOUT

EQUIVALENT CIRCUIT

Figure 30. CoPlanar Waveguide Limiter.

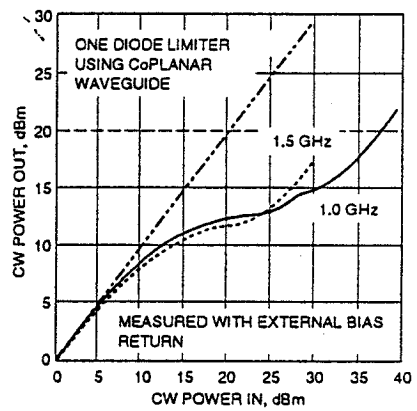


Figure 31. Large Signal Transfer Curve, CPW Limiter.

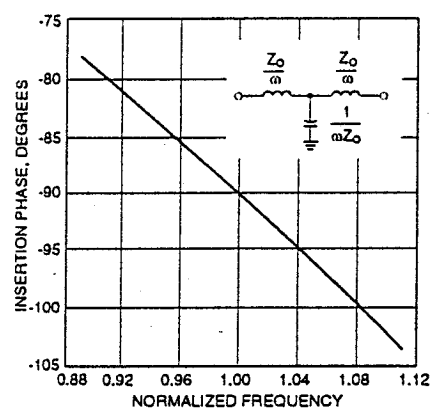


Figure 32. Lumped Element Version of a $\lambda/4$ Line.

HEWLETT-PACKARD TWO-PORT ANALYSIS APPCAD

UNITS	SWEEP	TERM	OUTPUT
DEG OHMS MIL nH GHz pF	START: 1.0 STOP: 2.0 STEP: 0.10	$Z_0: 50$ FILENAME NONE	DB[S11] & DB[S21] X: 1.0 TO 2.0 BY 0.50 Y: -35.0 TO -20.0 BY 5.00

0.70 50.00 0.70
90.00
1.50

[F1] = HELP [F5] = INSERT [F8] = SAVE FILE
 [F2] = ANALYZE [F6] = DELETE [F9] = WINDOW
 [F3] = TOGGLE [F7] = READ FILE [ESC] = QUIT
 [F4] = ADD

ENTER REFERENCE FREQUENCY FOR ELECTRICAL LENGTH

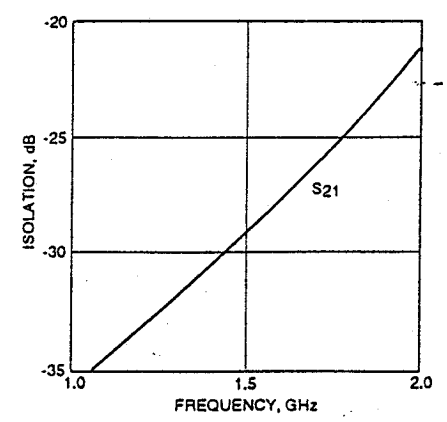


Figure 34. AppCAD Performance Calculation.

Figure 33. AppCAD Network Description.

ximately $2X + 6$ dB of isolation. Moreover, this enhancement occurs over a substantial bandwidth, with little loss of isolation over most of an octave. Thus, two limiter diodes spaced $\lambda/4$ apart should demonstrate much higher levels of protection than a single diode. That this is indeed

the case will be seen in the next section.

While a 90° segment of line is not large at 1.5 GHz (being about 1.25 inches long), it can be prohibitively large at lower frequencies. In these cases, one can substitute the lumped element

equivalent to a $\lambda/4$ line which is shown in Figure 32.

Two Diode Test Circuits

In Figure 7 a stitch-bonded HSMP-4820 PIN diode is shown mounted on a CPW line, straddling the upper and lower groundplanes. Discussed earlier in the paper, this limiter produced about 12 dB of isolation at 1.5 GHz (see Figure 31). Two such limiters, separated by $\lambda/4$, could reasonably be expected to exhibit approximately $12 + 12 + 6 = 30$ dB of isolation. In fact, the AppCAD analysis shown in Figures 33 and 34 predict an isolation of 29 dB from two shunt inductors of 0.7 nH, separated by 90° at 1.5 GHz. A test circuit was fabricated on a 2.0" length of CPW, using two diodes separated by 0.680" of line. As can be seen from the AppCAD analysis of Figure 35, this physical length corresponds to an electrical length of 50° at 1.5 GHz. When the circuit shown in Figure 33 is modified to reduce the separation between shunt inductors to 50° , the result is as shown in Figure 37. Predicted isolation is 28 dB, a sacrifice of only 1 dB of isolation in exchange for a 50% savings in space.

When small signal measurements were made on this circuit, the results were as shown in Figures 38 and 39. Return loss was acceptable at frequencies up to 1.7 GHz, and insertion loss was reasonable (less than 0.5 dB) to 1.5 GHz. When the diodes were externally biased at 25 mA each, measured isolation (Figure 39) was 32 dB, slightly higher than predicted.

The experimental board was then high power tested at 1.0 and 1.5 GHz, as shown in Figures 40 and 41. Attenuation vs.

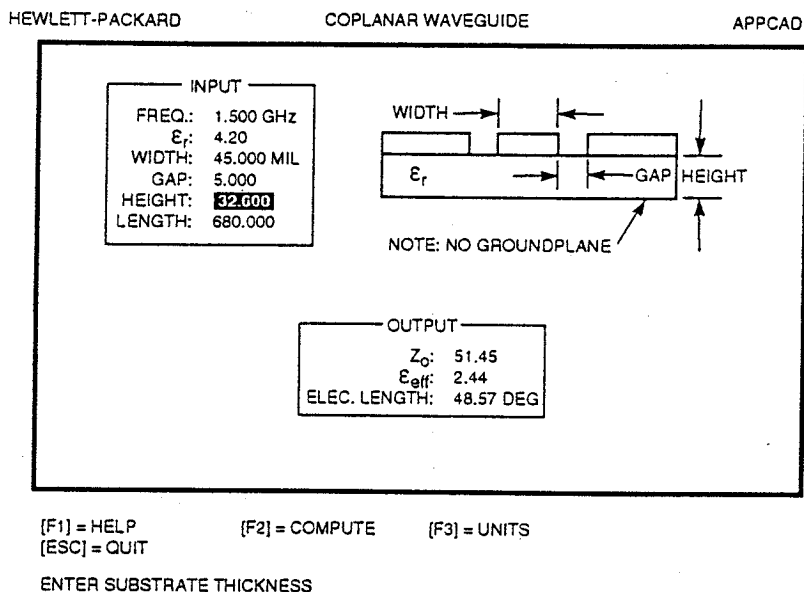


Figure 35. Analysis of CPW Line.

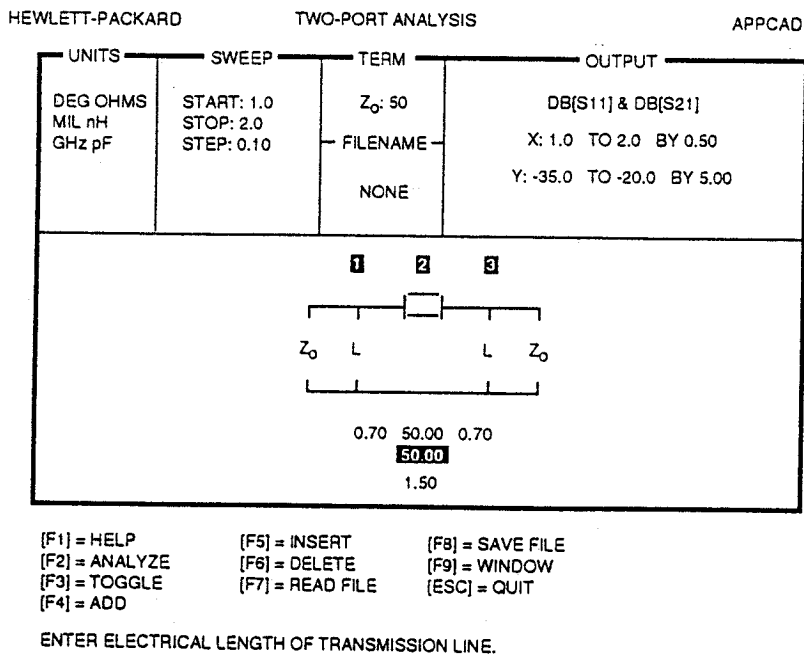


Figure 36. AppCAD Network Description.

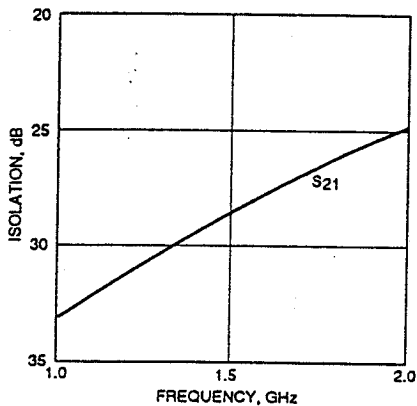


Figure 37. AppCAD Performance Calculation.

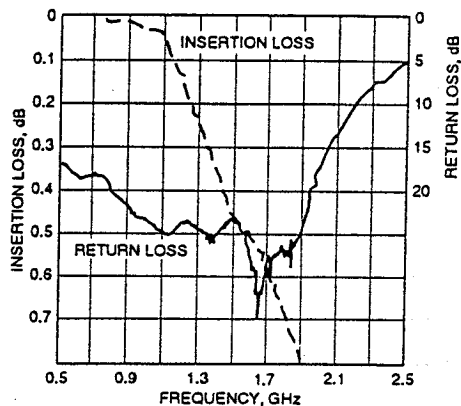


Figure 38. Small Signal Performance, Zero Bias, Two Diode Limiter.

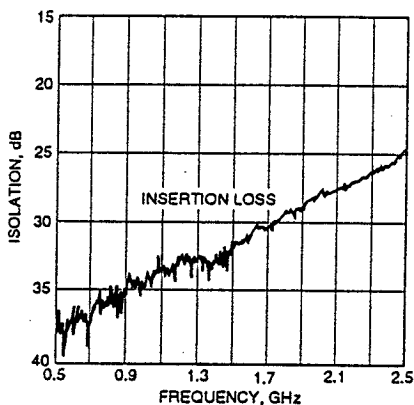


Figure 39. Small Signal Performance, +50mA Bias, Two Diode Limiter..

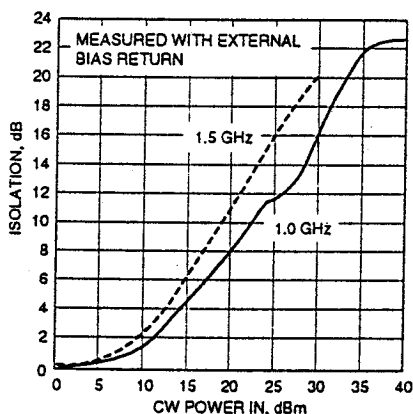


Figure 40. Attenuation vs. Pin, Two Diode Limiter Using CoPlanar Waveguide SOT-23 Diode.

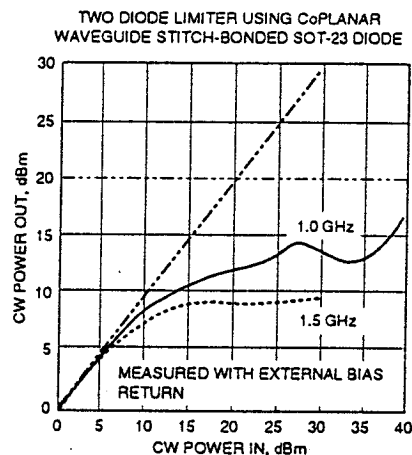
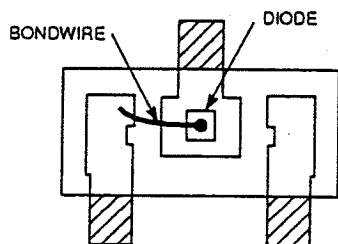
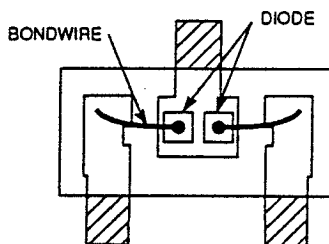


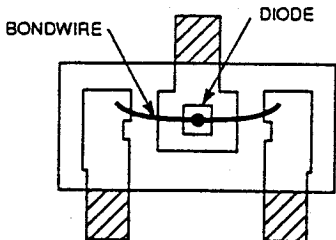
Figure 41 Pout vs. Pin, Two Diode Limiter.



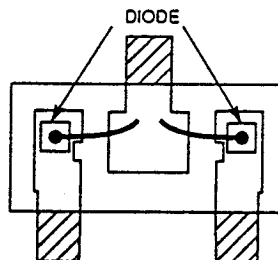
STANDARD CONFIGURATION HSM-3820, -3821



COMMON CATHODE CONFIGURATION HSM-3824



STITCH BONDED CONFIGURATION HSM-4820



COMMON ANODE CONFIGURATION HSM-3823

Figure 42. Some Members of the HSM-382X Family.

input power is shown in Figure 40. Unlike the single diode limiter, performance at 1.0 GHz is markedly different from that at 1.5 GHz. Because the diodes are only 33° apart at 1.0 GHz, there is less enhancement due to diode separation, and the result is a lower level of attenuation than measured at 1.5 GHz (where the separation is 50°). Interestingly enough, one can see the two diodes working in cascade in the 1.0 GHz curve. Around $P_{in} = +24$ dBm, the attenuation begins to show signs of leveling off. However, when $P_{in} \approx +27$ dBm, the RF power leaking past the first diode

(about +16 dBm) begins to "turn on" the second diode, and the curve of attenuation begins to climb once again.

Figure 41 is a transfer curve of P_{out} vs. P_{in} , one which shows the same data as Figure 40, but in a more meaningful way. From it one can easily see that this circuit maintains output leakage power well below +20 dBm for input power levels up to 10 watts. This is extremely useful performance for a power limiter.

Four Diode Test Circuit

In the two diode limiter described above, both diodes are of the

same polarity (anode grounded, cathode connected to the transmission line center conductor) and both use a common ground return to complete their bias loops. Thus, the "front" diode turns on first, almost reaching its full value of isolation before leakage past it is sufficient to turn on the "back" diode. If diodes of opposite polarity were available, each could serve as the ground return for the other, eliminating the need for an external choke and forcing both diodes to turn on at the same point in the transfer curve.

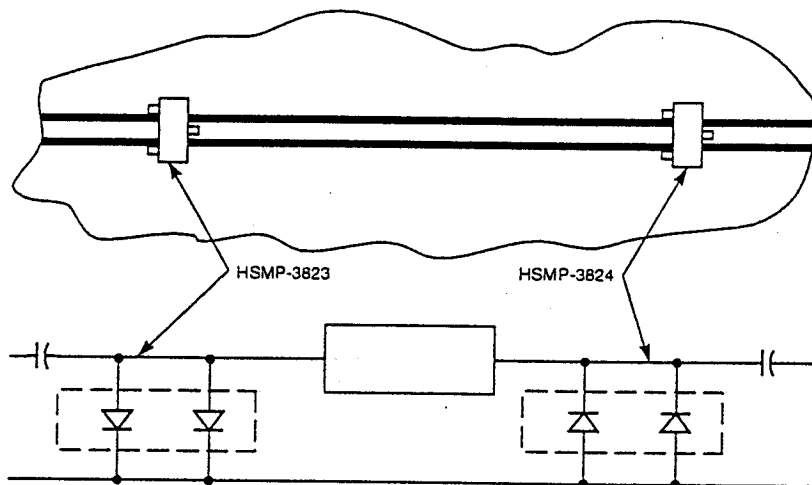


Figure 43. Four Diode Limiter.

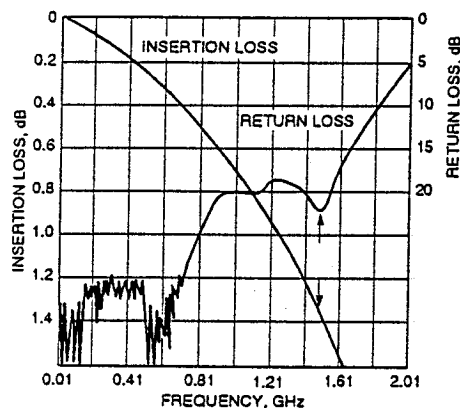


Figure 44. Small Signal Performance, Four Diode Limiter.

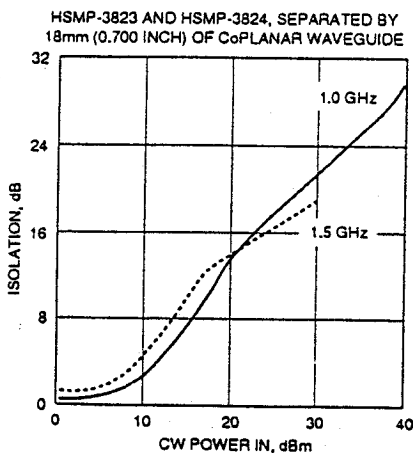


Figure 45. Loss vs. P_{in} , Four Diode Limiter.

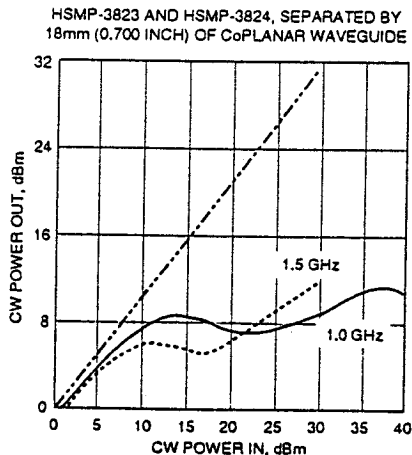


Figure 46. P_o vs. P_{in} , Four Diode Limiter.

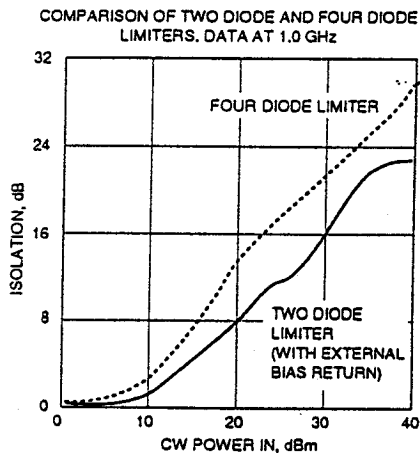


Figure 47. Comparison of Two and Four Diode Limiters.

Unfortunately, only one polarity is available for the PIN diode chip used in the HSMP-4820. However, diode pairs are available in both polarities, as shown in Figure 42. Of course, a pair such as the HSMP-3823 and the HSMP-3824 have two diodes in RF parallel when they are mounted straddling a CPW (as shown in Figure 7). The good news is that this cuts the effective value of R_s in half, improving isolation. The bad news is that it doubles the effective capacitance from center conductor to ground, lowering the upper limit of the practical frequency range.

A four diode limiter was constructed as shown in Figure 43. Spacing between the front and rear diode pairs was 0.700 inch. Small signal, zero bias insertion loss and return loss are shown in Figure 44. Insertion loss is about 0.7 dB at 1.0 GHz, a marginally high value of loss. At 1.5 GHz (see the marker on Figure 44), the loss is 1.3 dB, too high to be of practical value. Clearly, the high capacitance resulting from the use of two diodes in parallel has restricted this circuit to operation at relatively low frequencies. Return loss is reasonable out to 1.6 GHz or so. No small signal isolation with forward biased diodes was obtained, since the diode arrangement made it impossible to apply an external DC current to all four diodes simultaneously. Figure 45 gives the insertion loss vs. input power for the network. The effect of having two diodes in parallel in each location can be seen in the very high level (30 dB) of isolation which is achieved. The fact that the forward diode pair is biasing the rear pair leads to a very steep slope of attenuation vs. Pin. While this can be seen from a careful comparison of Figures 17

and 40, it can be more easily seen from the plots in Figure 47. In Figure 46, the transfer curve of the four diode limiter is given. Output leakage barely exceeds +10 dBm for input power levels up to 10 watts, making this circuit suitable for the protection of very sensitive receivers.

Conclusions

Sensitive receiver front-ends in commercial applications such as Global Positioning Systems (GPS) can be protected against excessive RF and microwave power levels up to 8 to 10 watts through the use of a limiter circuit and special surface mount plastic package PIN diode. Single limiter diode circuits for L-Band applications, with insertion loss on the order of 0.1 dB and a reasonable leakage power of 100 mW for input signals of 1 watt, have been demonstrated using the "stitch bonded" HSMP-4820 on microstrip transmission line. A type of transmission line new to the commercial market, CoPlanar Waveguide, has been shown to eliminate parasitic inductance caused by via holes to ground, extending the bandwidth of limiter circuits and reducing high power leakage. Two and four diode limiter circuits were demonstrated providing isolation as high as 30 dB for UHF applications.

It must be noted that good limiter performance is highly dependent upon the thickness of the I-layer and the lifetime of the diode. These characteristics are not tightly controlled in the production of low cost, high volume switching PIN diodes. Therefore, the user must take one of several precautions to insure that diodes do not vary in their limiter characteristics from one lot

to the next. First, one can test sample diodes from several lots, buying all of each lot which meets the limiter performance parameters. Second, one can ask the manufacturer to guarantee limiter performance, transferring the burden of testing to him. Obviously, the first alternative is the cheapest while the second is the most convenient.

It has been shown previously that diode capacitance is a major contributor to the noise figure of a receiver which is protected by a limiter. Careful process control and testing provides for tight control of the PIN diode capacitance and allows a maximum value to be guaranteed. This permits the design engineer to specify his receiver for minimum noise figure.

Of course, limiters do not help to improve the signal reception of the system, but they do protect a receiver from severe EMF conditions. For the manufacturer of commercial systems, this could present a sales advantage as well as a performance benefit. Long used exclusively to protect expensive electronic warfare equipment, low cost limiters are now available for commercial applications.

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