

Seven Segment LED Display Applications

INTRODUCTION

Hewlett-Packard's line of seven segment LED display products can be divided into two broad categories. The first product family is the large seven segment display which is constructed using individual LEDs for each segment. These large single digit LED display devices have become common in instruments throughout the industry. The other standard type of seven segment device is known as the monolithic display. Monolithic displays are constructed by diffusing several LED junctions in a single GaAsP die. This type of display is characterized by its small size, low cost, and low power requirements. The monolithic display typically has several digits per package and is often found in calculators and hand held or portable instruments.

This application note begins with a detailed explanation of the two basic product lines that Hewlett-Packard offers in the seven segment display market. This discussion includes mechanical construction techniques, character heights, and typical areas of application. The two major display drive techniques, dc and strobed, are covered. The resultant tradeoffs of cost, power, and ease of use are discussed. This is followed by several typical instrument applications including counters, digital voltmeters, and microprocessor interface applications. Several different microprocessor based drive techniques are presented incorporating both the monolithic and the large seven segment LED displays.

The application note contains a discussion of intensity and color considerations made necessary if the devices are to be end stacked. Hewlett-Packard has made several advances in the area of sunlight viewability of LED displays. The basic theory is discussed and recommendations made for achieving viewability in direct sunlight. Information concerning display mounting, soldering, and cleaning is presented. Finally, an extensive set of tables has been compiled to aid the designer in choosing the correct hardware to match a particular application. These tables include seven segment decoder/drivers, digit drivers, LSI chips designed for use with LEDs, printed circuit board edge connectors, and filtering materials.

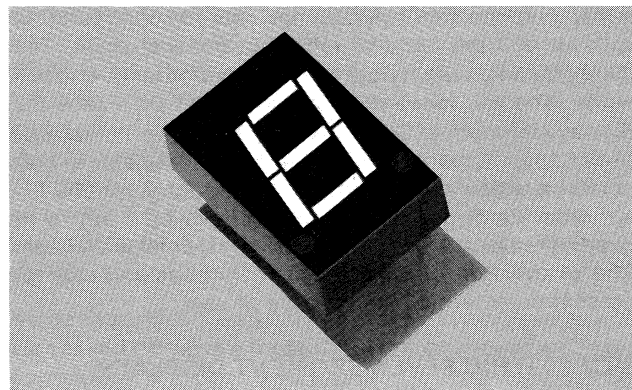


Figure 1. Large Seven Segment Display

LARGE SEVEN SEGMENT DISPLAYS

The large seven segment displays are designed to be easy to read single digit LED devices (Figure 1). They are typically used in electronic instruments, point-of-sale terminals, weighing scales, digital clocks, televisions, and appliances. The colors available are standard red, high efficiency red, yellow, and green. The standard red product is made from Gallium Arsenide Phosphide (GaAsP) on a GaAsP substrate. Both the high efficiency red and yellow seven segment displays are made from GaAsP on a Gallium Phosphide (GaP) substrate. The green seven segment displays are made from GaP on a GaP substrate. The increased efficiency of the GaP material results in the high efficiency red, yellow, and green displays having 3 to 5 times the minimum luminous intensity of the standard red displays.

A wide range of character heights varying from 7.6 mm (0.3 inch) to 20.3 mm (0.8 inch) allow the designer to choose the correct size display for the desired viewing range. The information in Figure 2 can be used to determine which character size display should be used for easy readability. The information has been compiled for a standard viewer (20/20 eyesight) in typical office ambient condition (100-1000 lux) with the displays driven at recommended data sheet values.

Character Size	Maximum Viewing Distance
7.6 mm (0.3 inch)	5 metres
10.9 mm (0.43 inch)	6 metres
14.1 mm (0.56 inch)	7.5 metres
20.3 mm (0.8 inch)	9 metres

Figure 2. Large Seven Segment Display Viewing Distances

The large LED display devices are manufactured using the concept of stretching the light from an LED by diffusion and reflection. The LED chips are mechanically supported and electrically connected by a lead frame. A cone shaped reflecting cavity is cast inside a rectangular package above each LED. This is done using glass filled epoxy with the top of this cavity forming the stretched segment. The plastic housing, called a "scrambler," forms the display package and contains the segment cavities. The stretched segment displays offer a variety of colors, sizes, and good on/off contrast.

These seven segment display products are available in either common anode or common cathode configuration with either right hand or left hand decimal point. The displays can be either dc driven or operated in the strobed mode. The low forward voltage of the LEDs makes the displays inherently IC compatible. The ± 1 overflow digit in the 14.1 mm (0.56 inch) package style is available in both common anode and common cathode configurations. For all other large seven segment displays, a universal overflow ± 1 digit with right hand decimal point is available. The ± 1 overflow digit has each LED anode and cathode present on external pins for ease of use.

MONOLITHIC SEVEN SEGMENT DISPLAYS

The monolithic seven segment displays are small, low cost, low power, multi-digit LED devices. They are typically used in desktop calculators, hand held instruments, metering devices, and various consumer products. With character heights ranging from 2.5 mm (0.1 inch) to 4.4 mm (0.175 inch), the monolithic products provide a flexible family of seven segment displays. The 2.5 mm (0.1 inch) character height displays are designed for hand held applications, whereas the 4.4 mm (0.175 inch) displays can be easily read at distances up to 2 metres.

Monolithic displays differ from other types of LED displays in that the individual light emitting segments are formed by diffusing separate LED junctions on a single chip of GaAsP. Because GaAsP is relatively expensive, most monolithic displays are magnified to keep chip sizes small. In most cases, the monolithic display is magnified by an external lens to attain a viewable character size.

Monolithic displays can be classified into two basic categories according to whether the lens is of the immersion or non-immersion type. Immersion lenses are formed by molding a lens directly over the LED chip. Non-immersion lenses have at least one layer of air between the LED chip and the lens assembly. Monolithic displays constructed with immersion lenses (Figure 3a) are manufactured by die attaching the monolithic GaAsP chips to the lead frame. The die attach pad also forms the common cathode electrical connection to the monolithic chip. The aluminum contact for each segment on the monolithic chip is then wire bonded to the appropriate anode contact. The

completed device is then fully encapsulated in epoxy. The magnifying lens is formed during encapsulation.

Monolithic displays with non-immersion lenses (Figure 3b) are usually constructed by epoxy die attaching the monolithic GaAsP chips to a special high temperature printed circuit board. The electrical contact for each segment on the monolithic chip is wire bonded to the appropriate anode trace on the printed circuit board. A precision injection molded lens is then aligned and attached to the printed circuit board. This attachment is done using holes that were drilled during fabrication of the printed circuit board to ensure alignment.

Hewlett-Packard's monolithic displays are of common cathode configuration since the GaAsP substrate is n doped material and each LED junction is formed by a P+ diffusion. Due to the monolithic display's low dynamic resistance in the forward region, multiplexing at relatively high peak current is possible while keeping forward voltage typically less than 1.8 volts. For this reason, long strings can be easily strobed.

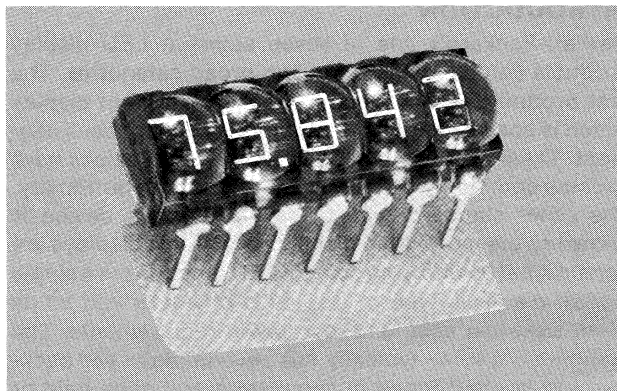


Figure 3a. Immersion Lens Monolithic Display

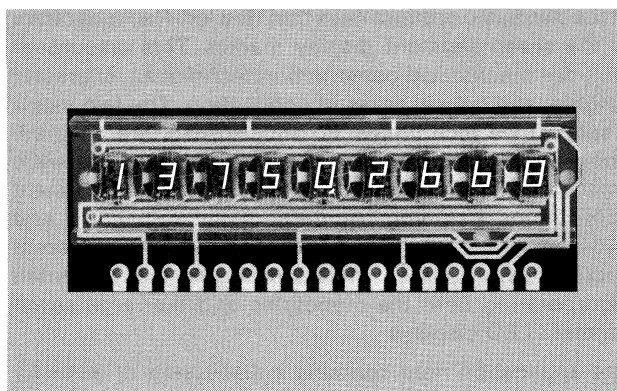


Figure 3b. Non-Immersion Lens Monolithic Display

DC DRIVE TECHNIQUES (Large Seven Segment Displays Only)

When seven segment displays are dc driven, each character is continuously illuminated. This is usually done with one decoder/driver per character and is commonly used for short display strings. If the display length is sufficiently short, the cost of dc decoding may be less than that of strobing circuitry. The fact that the drivers need not handle high current levels is a distinct advantage of dc operation.

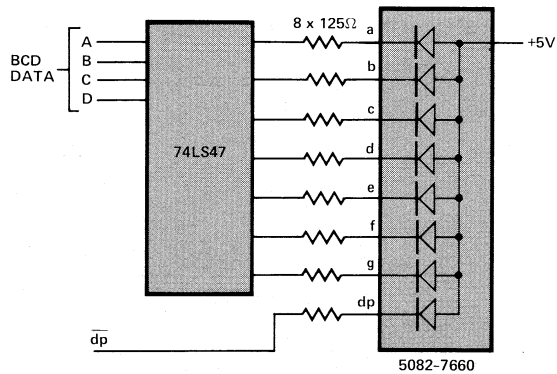


Figure 4a. DC Drive Circuit for the 5082-7660 Common Anode Display

Figure 4a shows the standard configuration for a common anode display. The current level, set here at 20 mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_F - V_{0(ON)}}{I_F} = \frac{5.0V - 2.2V - 0.35V}{20 \text{ mA}} = 125\Omega$$

where

- V_{CC} = voltage supply potential
- V_F = forward voltage of LED at desired I_F
- $V_{0(ON)}$ = ON state output voltage of display driver (74LS47)
- I_F = desired forward current (20 mA)

An analogous circuit is shown in Figure 4b for a common cathode display. The Fairchild 9368 is a seven segment decoder/driver incorporating input latches and constant 15 mA current outputs to directly drive common cathode LED displays.

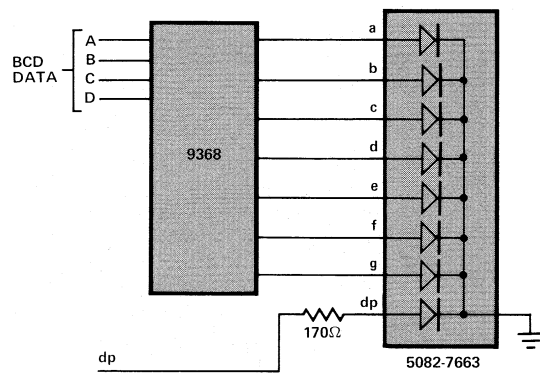


Figure 4b. DC Drive Circuit for the 5082-7663 Common Cathode Display

MULTIPLEXED DRIVE TECHNIQUES

When multiplexing drive circuitry is used, the decoder is timeshared among digits in the display. The digits are electrically connected with like segments wired in parallel. This forms a seven (seven segments) by N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. Simultaneously, a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position. Figure 5 contains a block diagram of a typical five digit multiplexed LED display.

Since the eye is a relatively slow time average sensor, a viewer will perceive a repetitive visual phenomenon to be continuous if it occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read.

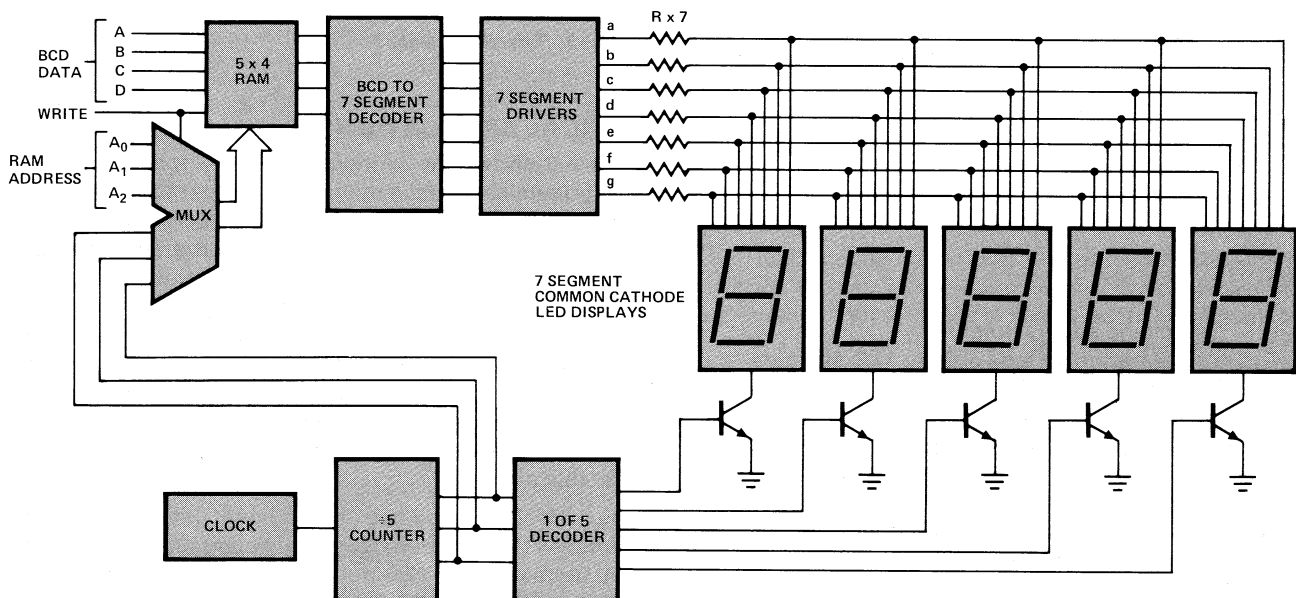


Figure 5. Block Diagram of a Multiplexed Five Digit LED Display

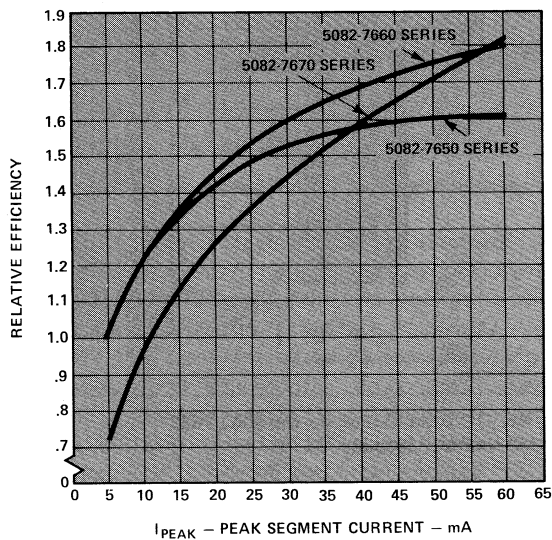


Figure 6a. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

In displays subject to vibration, a minimum strobe rate of five times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than dc drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 6a). Thus, for the same average current, the use of lower duty cycles and higher peak current levels results in increased light output. This phenomenon is illustrated in Figure 6b. Notice that the graph is normalized to one at a forward current of 5 mA dc. If this same device were operated at 25 mA peak, 20% duty factor (as if in a five digit strobed display) the time averaged luminous intensity would increase 40%.

For common decoder/driver circuits, a series resistor is placed in each segment line to limit the LED current. This is done to prevent uneven current distribution among segments. Referring to Figure 7, the current limiting resistor values may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{CE (SEG)} - V_F - V_{CE (DIG)}}{I_{PEAK}}$$

where

- V_{CC} = voltage supply potential
 - $V_{CE (SEG)}$ = saturation voltage drop across segment driver at I_{PEAK}
 - V_F = LED forward voltage at I_{PEAK}
 - $V_{CE (DIG)}$ = saturation voltage drop across digit driver at [$I_{PEAK} \times 8$ (worst case number of segments ON)]
 - I_{PEAK} = $I_{AVERAGE} \times \text{number of digits} = \text{peak LED segment current}$
- OR

$$I_{PEAK} = \frac{I_{AVG}}{D.F.}$$

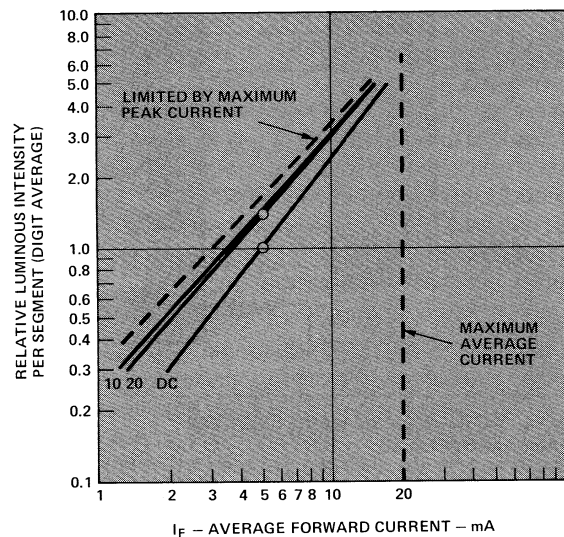


Figure 6b. Relative Luminous Intensity per Segment vs. Average Current (5082-7650)

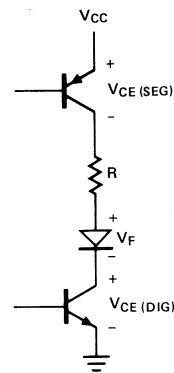


Figure 7. Typical Segment

TYPICAL APPLICATIONS

Figure 8 shows the complete circuitry for a minimum component universal counter. The Intersil ICM7226B is a fully integrated universal counter and LED display driver. It combines a high frequency oscillator, a decade time-base counter, an eight decade data counter with latches, a seven segment decoder, a digit multiplexer, and eight segment and eight digit drivers that drive monolithic LEDs directly. If the designer wishes to use the ICM7226A or B (common anode or cathode) to drive large seven segment products, he should consider his application carefully because higher drive currents are required to produce a readable display.

The ICM7226B updates the segment information and refreshes the common cathode displays at an I_{PEAK} of 15 mA/segment on a 12% duty cycle. This drive current is ideal for the monolithic seven segment family. The circuit in Figure 8 employs two 5082-7414 monolithic devices as the display portion of the counter. Typical devices will exhibit a 30 μ cd time averaged luminous intensity, thus

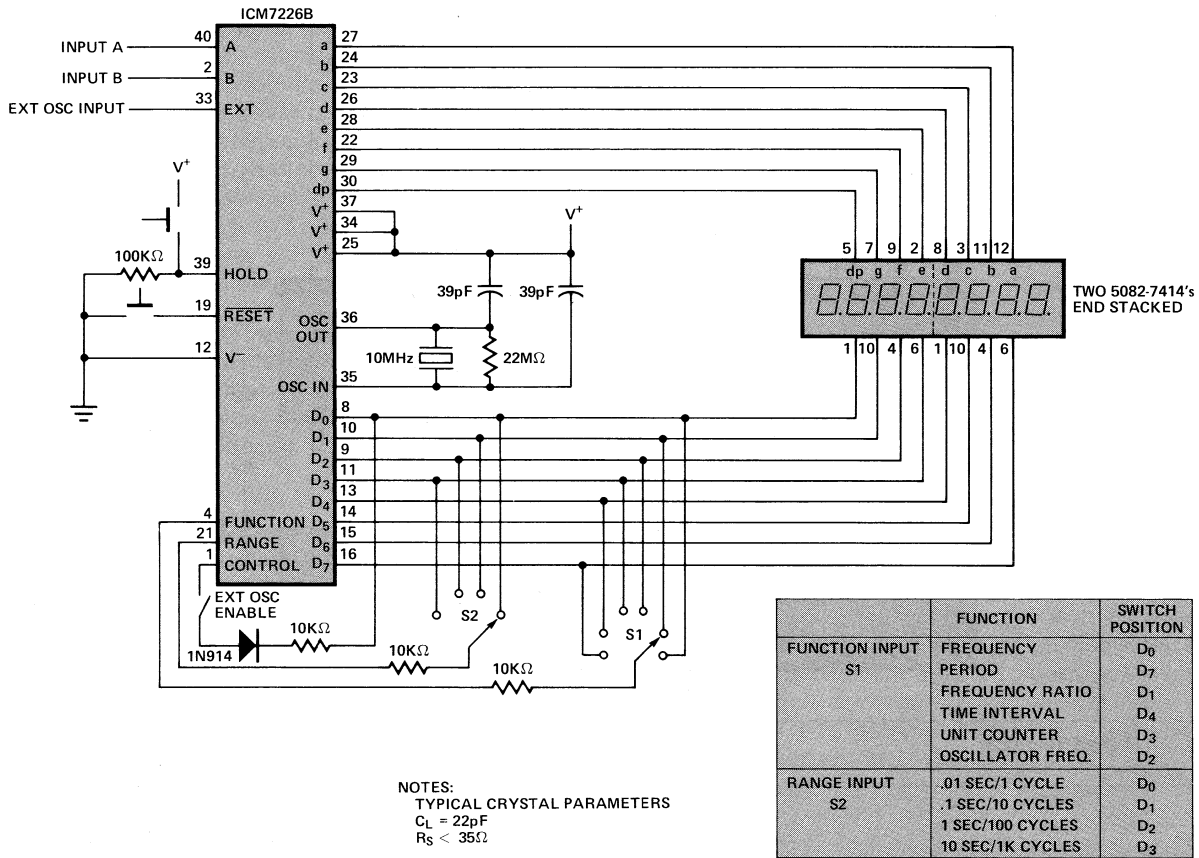


Figure 8. 10 MHz Universal Counter

providing excellent readability. Combining the compactness of the monolithic displays and the complexity of the single chip universal counter system, an extremely powerful hand held instrument can be realized.

Figure 9 shows the circuitry necessary for a high performance, low power 3-1/2 digit panel meter. The circuit utilizes the Intersil ICL7107 (CMOS) A/D converter, seven passive components, and four large seven segment displays. All necessary active devices are contained on the chip. This includes seven segment decoders, display drivers, a reference voltage, and a clock.

The ICL7107 is designed to dc drive 3 seven segment displays and one overflow digit at a typical forward current of 8 mA per segment. The segment information is decoded and updated continuously by the control logic within the chip. The 7.6mm (0.3 inch) standard red displays (5082-7736/-7740) provide an attractive display for this low cost digital panel meter. For higher light output, the high efficiency red, yellow, or green displays can be used.

MICROPROCESSOR DISPLAY INTERFACE TECHNIQUES

The four basic techniques for interfacing microprocessors to seven segment displays are listed below:

1. The DC Driven Controller statically drives an LED

seven segment display from a microprocessor output port. In the standard configuration, each display is assigned a different address so that a Memory or I/O Write to that address changes the contents of the corresponding display digit.

2. The Refresh Controller interfaces the microprocessor to a multiplexed LED display. The controller periodically interrupts the microprocessor and after each interrupt, the microprocessor supplies new display data for the next refresh cycle of the display.
3. The Decoded Data Controller refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores decoded display data. This data is continuously read from the RAM and then used to refresh the display. Whenever the display message is changed, the microprocessor decodes each character in software and writes the decoded data into the local RAM.
4. The Coded Data Controller also refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores BCD data which is continuously read, decoded, and used to refresh the display. The display message is changed by writing new BCD characters into the local RAM.

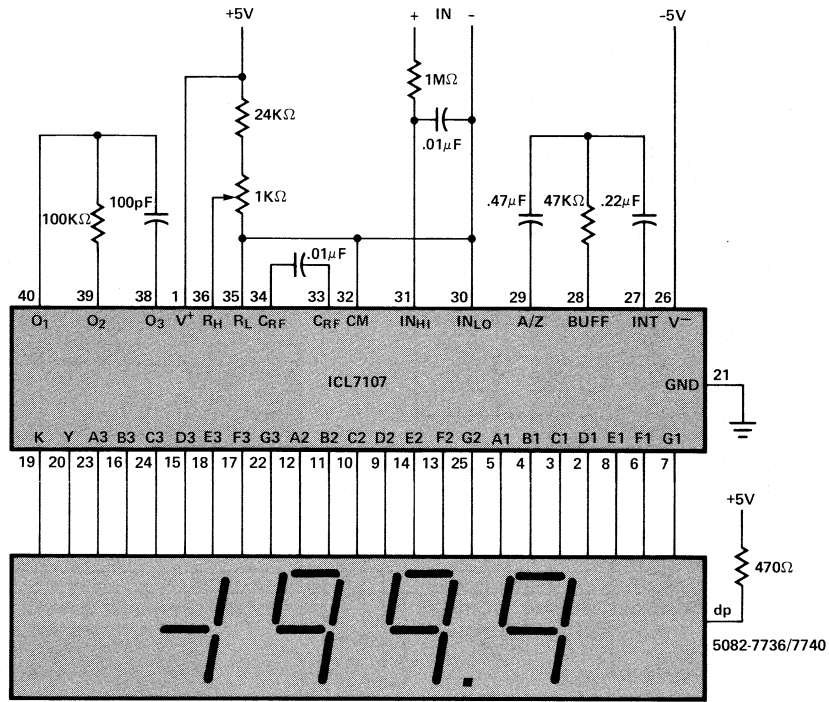
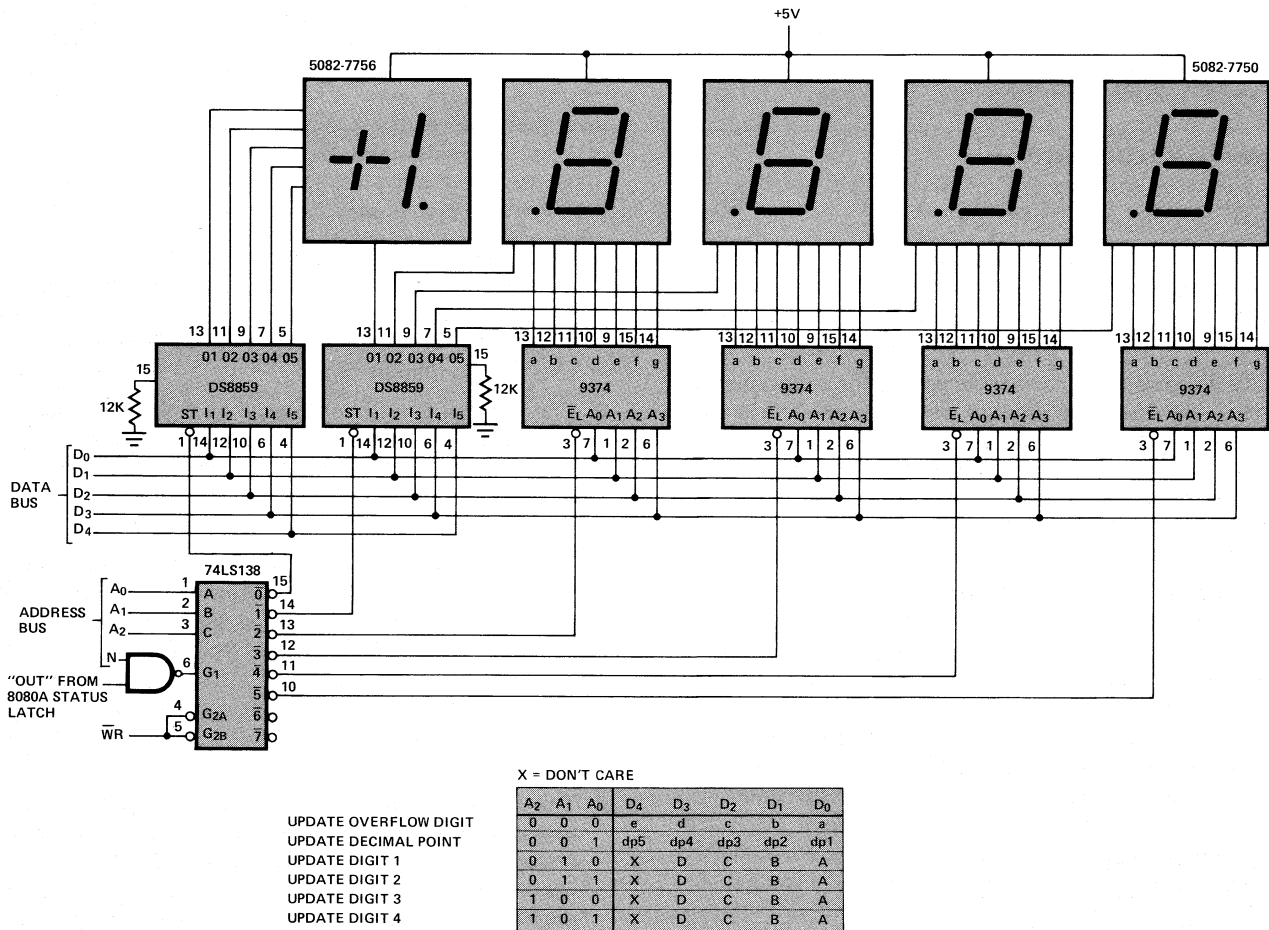


Figure 9. 3-1/2 Digit Voltmeter



X = DON'T CARE

A ₂	A ₁	A ₀	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	e	d	c	b	a
0	0	1	dp5	dp4	dp3	dp2	dp1
0	1	0	X	D	C	B	A
0	1	1	X	D	C	B	A
1	0	0	X	D	C	B	A
1	0	1	X	D	C	B	A

UPDATE OVERFLOW DIGIT
 UPDATE DECIMAL POINT
 UPDATE DIGIT 1
 UPDATE DIGIT 2
 UPDATE DIGIT 3
 UPDATE DIGIT 4

Figure 10. DC Driven Controller

DC DRIVEN CONTROLLERS

When the seven segment display is driven on a dc basis, a seven segment decoder/driver or latch is required for each display. Figure 10 shows an example of a seven segment display to microprocessor interface. Each display is driven by its own seven segment driver. The Fairchild 9374 has current sink outputs that drive each LED segment at 15 mA dc. The decimal points and overflow digit are driven by two National DS 8859's. These hex latches have programmable current sink outputs. The Intel 8080A microprocessor updates each display with an OUTput instruction which accesses up to 256 output devices and ports.

Upon execution of the OUTput instruction, the lower five bits of the accumulator are loaded into the DS8859 associated with the overflow digit. Next, the decimal point is updated in a similar fashion. Finally, the four decoder/drivers are successively loaded with the correct BCD information.

Figure 11 shows a DC Driven Controller utilizing the National MM5450 LED Display Driver. The MM5450 is a serial in-parallel out shift register with 34 output pins that can sink up to 15 mA each. It is specifically designed to operate with common anode displays and minimal interface with the source of data. Serial data transfer from the data source, in this case the microprocessor, to the display driver is accomplished with two signals. These signals are SERIAL DATA and CLOCK. By using a format of a leading "1" bit followed by the 35 data bits, data transfer

is allowed without any additional handshaking signals. The 35 data bits are latched after the 36th bit is complete. This provides non-multiplexed, direct drive to the seven segment displays.

Figures 12a and 12b contain the software necessary to interface the MM5450 to the 6800 and 8080A microprocessors respectively. The serial display data is transferred to the microprocessor via bit 7 of the Data Bus. The data is clocked in each time the microprocessor writes to the MM5450. In the case of the 8080A, this is done with the I/O WRITE signal and a combination of lower ordered addresses. The 6800 accomplishes this task with the VMA signal and a combination of higher address bits. The decoded segment data is assumed to be in four successive memory bytes starting at location \$0006. The format of the decoded segment data for all microprocessor interfaces in this note is shown in Figure 13.

The software first outputs a start bit to the MM5450. Next, the first digit's segment information is clocked into MM5450. The segment information is then rotated left eight times with this data being clocked into the display after each shift. This procedure is repeated for each digit, thus providing 33 clock pulses (the start bit plus (4x8) segment bits). In order for the segment data to be latched to the display, a complete set of 36 clocks must occur. For this reason, there are three dummy clocks at the end of the program. The term "dummy" is used because the data that is being clocked into MM5450 never appears on the seven segment display.

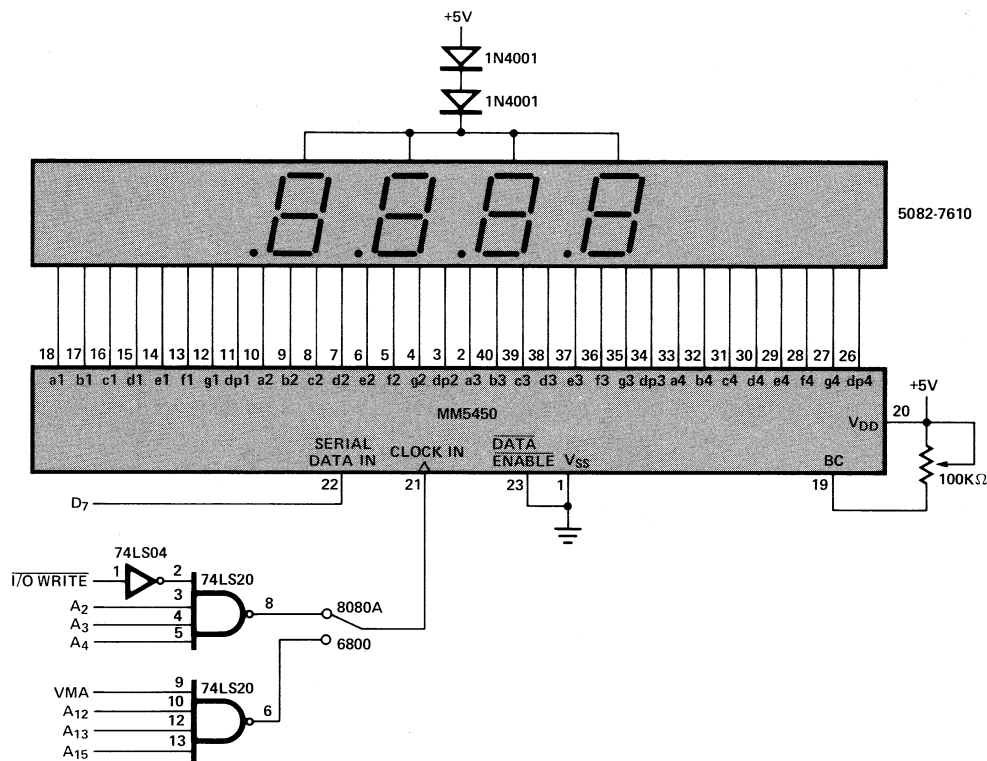


Figure 11. DC Driven Controller with Serial Data Interface to 6800 and 8080A

```

        B0 00  DSPLY  EQU  $B000
0006          ORG  $0006
0006          DATA  RMB  $4

0400          ORG  $0400
0400  CE 00 06  LOAD  LDX  I,DATA
0403  86 80          LDA  A I,$80      LOAD START BIT
0405  B7 B0 00          STA  A E,DSPLY  OUTPUT START BIT
0408  C6 08          START  LDA  B I,8      INITIALIZE COUNTER
040A  A6 00          LDA  A X,0      LOAD DATA
040C  B7 B0 00  LOOP  STA  A E,DSPLY  OUTPUT DATA TO DISPLAY
040F  49          ROL  A      ROTATE TO NEXT BIT
0410  5A          DEC  B      DECREMENT COUNTER
0411  26 F9          BNE  LOOP      BRANCH IF NOT DONE, ELSE CONTINUE
0413  08          INX          LAST WORD?
0414  8C 00 04          CPX  I,$04      BRANCH IF NOT LAST WORD, ELSE CONTINUE
0417  26 EF          BNE  START
0419  B7 B0 00          STA  A E,DSPLY  DUMMY CLOCK 1
041C  B7 B0 00          STA  A E,DSPLY  DUMMY CLOCK 2
041F  B7 B0 00          STA  A E,DSPLY  DUMMY CLOCK 3, SEG DATA LATCHED
0422  39          RTS

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**Figure 12a. 6800 Interface to DC Drive Controller
Shown in Figure 11**

```

E000          DSPLY  EQU  001CH
E000          ORG  0E006H
E006          DATA  DS  4

E00A          ORG  0E400H
E400  3E 80  LOAD  MVI  A,80H      LOAD START BIT
E402  D3 1C  OUT   DSWLY  OUTPUT START BIT
E404  21 06 E0  LXI  H,DATA  GET ADDRESS OF SEG DATA
E407  06 08  START  MVI  B,08H  INITIALIZE COUNTER
E409  7E          MOV  A,M      LOAD SEG DATA
E40A  D3 1C  LOOP  OUT   DSWLY  OUTPUT SEG DATA TO DISPLAY
E400  07          RLC          ROTATE TO NEXT BIT
E40D  05          DCR  B      DECREMENT COUNTER
E40E  02 0A E4  JNZ  LOOP      JUMP IF NOT DONE, ELSE CONTINUE
E411  2C          INR  L
E412  7D          MOV  A,L
E413  FE 0A          CPI  0AH      LAST WORD?
E415  C2 07 E4  JNZ  START  JUMP IF NOT LAST WORD, ELSE CONTINUE
E418  D3 1C  OUT   DSWLY  DUMMY CLOCK 1
E419  D3 1C  OUT   DSWLY  DUMMY CLOCK 2
E41C  D3 1C  OUT   DSWLY  DUMMYCLOCK 3, SEG DATA LATCHED
E41E  C9          RET

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**Figure 12b. 8080A Interface to DC Driven Controller
Shown in Figure 11**

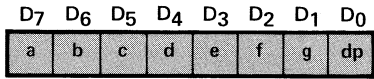


Figure 13. Format for Decoded Segment Data

The 5082-7610 7.6mm (0.3 inch) high efficiency red displays driven at 15 mA/segment dc provide a large, easy to read, four digit display. The 100 KΩ potentiometer sets a reference current for the LEDs and provides brightness control for applications in varying ambients.

REFRESH CONTROLLER

The Refresh Controller uses the microprocessor to actively strobe the display. This strobing is accomplished via an interrupt that causes the microprocessor to service the refresh subroutine. The refresh program provides new segment and digit information for the display. This application note shows two types of Refresh Controllers. The basic difference between the controllers is the nature of data that is transferred from the microprocessor to the controller. The first type (Figure 14) requires eight data lines to transfer the decoded segment and decimal point information. The second type of Refresh Controller (Figure 15) requires only five data lines to interface to the microprocessor. The data is transferred using BCD data and a decimal point bit. The technique for digit strobing also is slightly different due to the difference in display length.

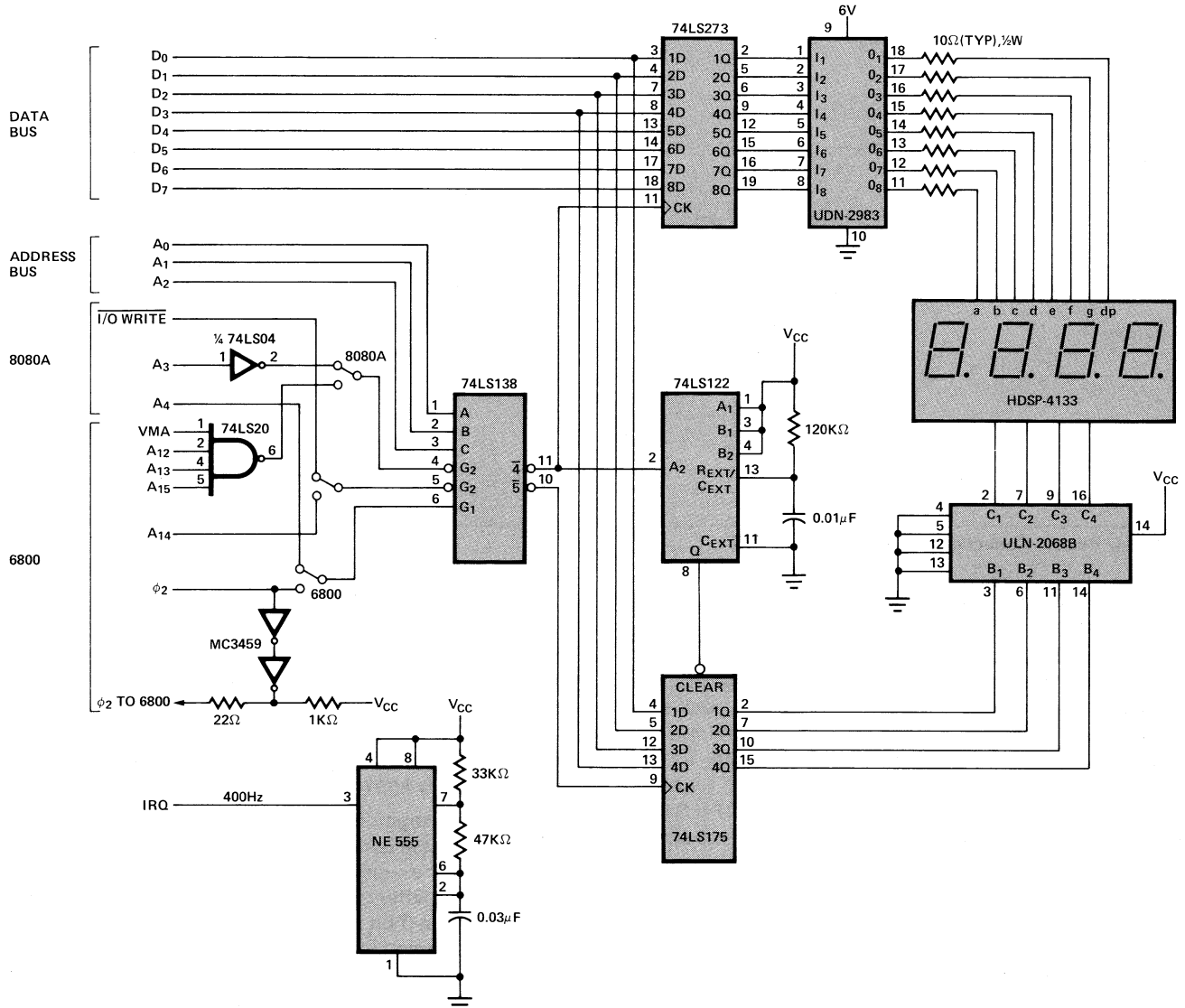


Figure 14. Sunlight Viewable Refresh Controller

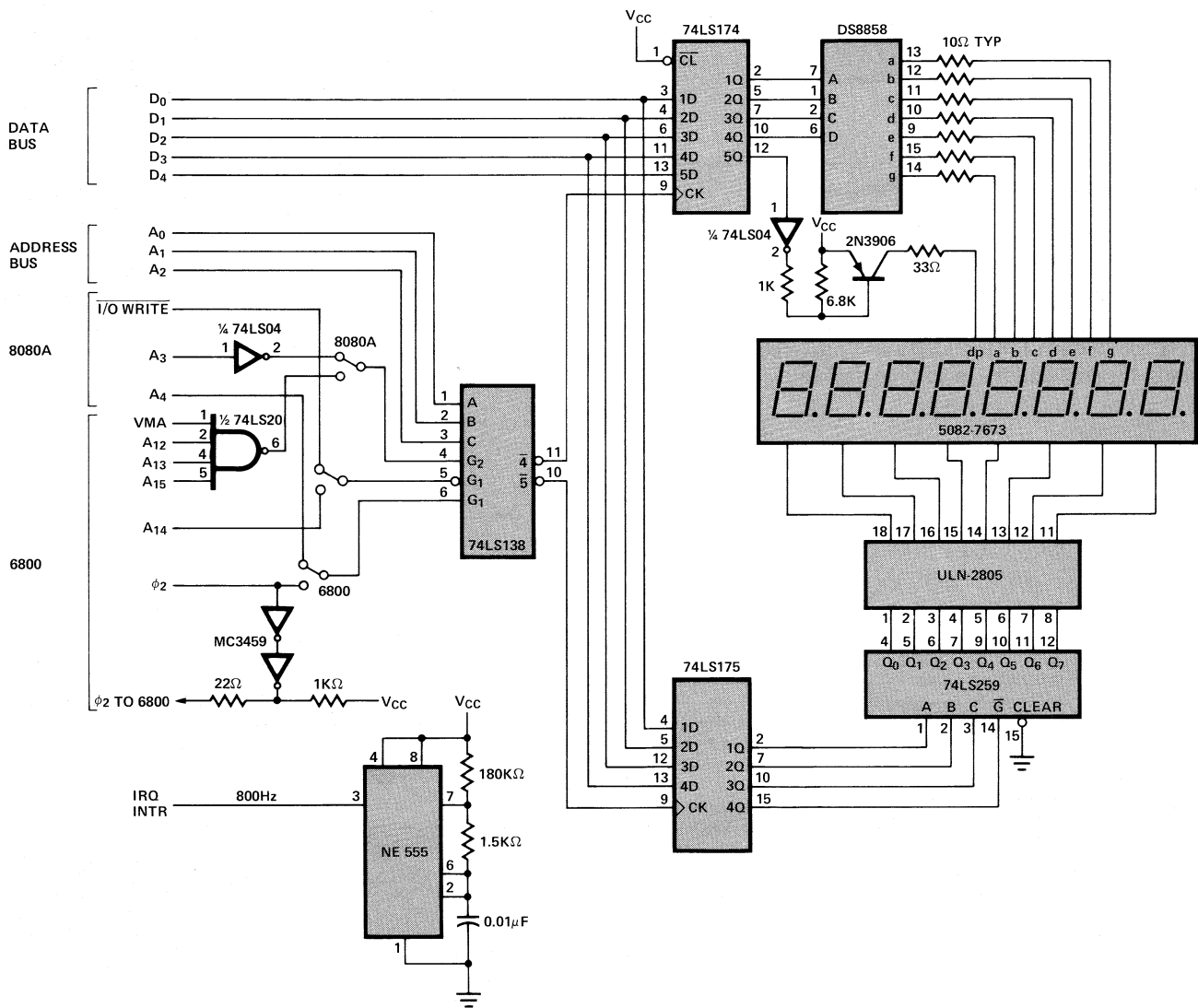


Figure 15. Refresh Controller

The circuit in Figure 14 utilizes the 10.9mm (0.43 inch) yellow HDSP-4133 seven segment displays. These displays are readable in direct sunlight when driven near the data sheet maximums as they are in Figure 14. The Sprague segment drivers are sourcing 120 mA peak on a 1/4 duty factor. The ULN-2068B can sink a maximum of 1.75A and therefore is an excellent digit driver as the maximum digit current is (120 mA) (8 segments) \approx 1 Amp. The retriggerable monostable multivibrator (74LS122) senses strobing activity on the segment lines. If the strobing stops for any reason (microprocessor crash, etc.), the digit drivers are turned off immediately. This protects the displays from the 120 mA dc they would pass if the strobing ceased.

Figure 16a and 16b contain the software necessary to interface the Refresh Controller in Figure 14 to the 6800 and the 8080A microprocessors respectively. The programs consist of two subroutines. The first subroutine LOAD is called by the user's main program. LOAD should

be called the first time data is to be displayed and any time when new display data is desired. This subroutine assumes the user has stored three consecutive bytes of BCD data and decimal point information in locations WORD1, WORD2, and DP. The subroutine unpacks the coded data stored in these locations, decodes it into segment data, and stores it in locations DD1, DD2, DD3, and DD4. Figure 16c graphically shows the effect of the subroutine LOAD.

LOAD uses a segment data lookup table located in ROM. The lookup table consists of sixteen successive locations that contain the segment information for displaying numbers 0-9 and letters A-F. A 1 bit corresponds to an ON segment and a 0 bit to an OFF segment. All dp bits have been programmed to a logical 0 in the lookup table. Subroutine LOAD assumes that only one decimal point will be ON in the four digit string. The code beginning with label DCPT determines which digit should display a decimal point and changes the dp bit to a logical 1. The subroutine is now complete and control returns to the main program.

```

BF 04 SEG EQU $BF04
BF 05 DIG EQU $BF05
0000 POINT RMB 2
0002 DIGIT RMB 1
0003 WORD1 RMB 1
0004 WORD2 RMB 1
0005 DP RMB 1
0006 DD1 RMB 1
0007 DD2 RMB 1
0008 DD3 RMB 1
0009 DD4 RMB 1

0400 ORG $0400
0400 CE 06 00 LOAD LDX 1,$0600
0403 DF 00 STX D,POINT INITIALIZE POINTER
0405 86 01 LDA A 1,$01
0407 97 02 STA A D,DIGIT INITIALIZE DIGIT
0409 96 03 LDA A D,WORD1 LOAD 2 BCD WORDS
040B 16 TAB MAKE A COPY
040C 54 LSR B RIGHT JUSTIFY BCD1
040D 54 LSR B
040E 54 LSR B
040F 54 LSR B
0410 D7 01 STA B D,POINT +1
0412 DE 00 LDX D,POINT POINT TO DIGIT 1 SEG. DATA
0414 E6 00 LDA B X,0 LOAD DIGIT 1 SEG. DATA
0416 D7 06 STA B D,DD1 STORE DIGIT 1 SEG. DATA
0418 84 0F AND A 1,$0F MASK LEAVING BCD2
041A 97 01 STA A D,POINT +1
041C DE 00 LDX D,POINT POINT TO DIGIT 2 SEG. DATA
041E A6 00 LDA A X,0 LOAD DIGIT 2 SEG. DATA
0420 97 07 STA A D,DD2 STORE DIGIT 2 SEG. DATA
0422 96 04 LDA A D,WORD2 LOAD NEXT 2 BCD WORDS
0424 16 TAB MAKE A COPY
0425 54 LSR B RIGHT JUSTIFY BCD3
0426 54 LSR B
0427 54 LSR B
0428 54 LSR B
0429 D7 01 STA B D,POINT +1
042B DE 00 LDX D,POINT POINT TO DIGIT 3 SEG. DATA
042D E6 00 LDA B X,0 LOAD DIGIT 3 SEG. DATA
042F D7 08 STA B D,DD3 STORE DIGIT 3 SEG. DATA
0431 84 0F AND A 1,$0F MASK LEAVING BCD4
0433 97 01 STA A D,POINT +1
0435 DE 00 LDX D,POINT POINT TO DIGIT 4 SEG. DATA
0437 A6 00 LDA A X,0 LOAD DIGIT 4 SEG. DATA
0439 97 09 STA A D,DD4 STORE DIGIT 4 SEG. DATA
043B 96 05 DCPT LDA A D,DP LOAD DIGIT THAT NEEDS DP (1, 2, 3, 4)
043D CE 00 00 LDX 1,$0000 CLEAR INDEX REG
0440 08 INCR INX
0441 4A DEC A
0442 26 FC BNE INCR LOOP TRANSFERS DP DATA TO INDEX REG
0444 A6 05 LDA A X,DP LOAD THE SEG. DATA NEEDING DP
0446 8B 01 ADD A 1,$01 GIVE IT A DP
0448 A7 05 STA A X,DP STORE IT BACK
044A 39 RTS

044B 0F RFRSH SEI DISABLE INTERRUPTS DURING REFRESH
044C D6 02 LDA B D,DIGIT FIND OUT WHICH DIGIT
044E C1 01 CMP B 1,$01 IS IT DIGIT 1?
0450 26 05 BNE NFST BRANCH IF NOT FIRST. ELSE CONTINUE
0452 CE 00 06 LDX 1,$0006
0455 DF 00 STX D,POINT INITIALIZE POINTER TO DD1
0457 86 00 NFST LDA A 1,$00 CLEAR A
0459 B7 BF 05 STA A E,DIG BLANK DISPLAY
045C DE 00 LDX D,POINT POINT TO SEG. DATA
045E A6 00 LDA A X,0 LOAD SEG. DATA
0460 B7 BF 04 STA A E,SEG. OUTPUT SEG. DATA TO DISPLAY
0463 F7 BF 05 STA B E,DIG OUTPUT DIGIT DATA TO DISPLAY
0466 C1 08 CMP B 1,$08 IS IT THE LAST DIGIT?
0468 27 08 BEQ LOOP1 BRANCH IF LAST. ELSE CONTINUE
046A 78 00 02 ASL E,DIGIT SHIFT TO NEXT DIGIT
046D 7C 00 01 INC E,POINT +1 POINT TO NEXT SEG. DATA
0470 0E CLI RE-ENABLE INTERRUPTS
0471 3B RTI RETURN
0472 86 01 LOOP1 LDA A 1,$01 RE-INITIALIZE TO DIGIT 1
0474 97 02 STA A D,DIGIT
0476 0E CLI RE-ENABLE INTERRUPTS
0477 3B RTI RETURN

0600 ORG $0600
0600 FC FCB $FC 0
0601 60 FCB $60 1
0602 DA FCB $DA 2
0603 F2 FCB $F2 3
0604 66 FCB $66 4
0605 B6 FCB $B6 5
0606 3E FCB $3E 6
0607 E0 FCB $E0 7
0608 FE FCB $FE 8
0609 E6 FCB $E6 9
060A EE FCB $EE A
060B 3E FCB $3E B
060C 9C FCB $9C C
060D 7A FCB $7A D
060E 9E FCB $9E E
060F BE FCB $BE F

```

Figure 16a. 6800 Interface to Refresh Controller in Figure 14

E000		SEG	EQU	001CH	
E000		DIG	EQU	001DH	
E000			ORG	0E000H	
E000		POINT	DS	2	
E002		DIGIT	DS	1	
E003		WORD1	DS	1	
E004		WORD2	DS	1	
E005		DP	DS	1	
E006		DD1	DS	1	
E007		DD2	DS	1	
E008		DD3	DS	1	
E009		DD4	DS	1	
E00A			ORG	0E400H	
E400	21 00 E6	LOAD	LXI	H,0E600H	
E403	22 00 E0		SHLD	POINT	INITIALIZE POINTER
E406	3E 01		MVI	A,01H	
E408	32 02 E0		STA	DIGIT	INITIALIZE DIGIT
E40B	3A 03 E0		LDA	WORD1	LOAD 2 BCD WORDS (BCD1, BCD2)
E40E	E6 F0		ANI	0F0H	MASK OUT LOWER NIBBLE
E410	0F		RRC		RIGHT JUSTIFY BCD1
E411	0F		RRC		
E412	0F		RRC		
E413	0F		RRC		
E414	6F		MOV	L, A	POINT TO DIGIT 1 SEG. DATA
E415	7E		MOV	A, M	LOAD DIGIT 1 SEG. DATA
E416	32 06 E0		STA	DD1	STORE DIGIT 1 SEG. DATA
E419	3A 03 E0		LDA	WORD1	LOAD SAME 2 BCD WORDS (BCD1, BCD2)
E41C	E6 0F		ANI	0FH	MASK OUT UPPER NIBBLE
E41E	6F		MOV	L, A	POINT TO DIGIT 2 SEG. DATA
E41F	7E		MOV	A, M	LOAD DIGIT 2 SEG. DATA
E420	32 07 E0		STA	DD2	STORE DIGIT 2 SEG. DATA
E423	3A 04 E0		LDA	WORD2	LOAD NEXT 2 BCD WORDS (BCD3, BCD4)
E426	E6 F0		ANI	0F0H	MASK OUT LOWER NIBBLE
E428	0F		RRC		RIGHT JUSTIFY BCD3
E429	0F		RRC		
E42A	0F		RRC		
E42B	0F		RRC		
E42C	6F		MOV	L, A	POINT TO DIGIT 3 SEG. DATA
E42D	7E		MOV	A, M	LOAD DIGIT 3 SEG. DATA
E42E	32 08 E0		STA	DD3	STORE DIGIT 3 SEG. DATA
E431	3A 04 E0		LDA	WORD2	LOAD SAME 2 BCD WORDS (BCD3, BCD4)
E434	E6 0F		ANI	0FH	MASK OUT UPPER NIBBLE
E436	6F		MOV	L, A	POINT TO DIGIT 4 SEG. DATA
E437	7E		MOV	A, M	LOAD DIGIT 4 SEG. DATA
E438	32 09 E0		STA	DD4	STORE DIGIT 4 SEG. DATA
E43B	3A 05 E0	DCPT	LDA	DP	LOAD DIGIT NEEDING DP
E43E	01 05 E0		LXI	B,0E005H	SET BC REG PAIR AS A POINTER
E441	03	INCR	INX	B	LOOP TRANSFERS DP DATA TO BC
E442	3D		DCR	A	
E443	C2 41 E4		JNZ	INCR	
E446	0A		LDAX	B	LOAD SEG. DATA NEEDING DP
E447	C6 01		ADI	01H	GIVE IT A DP
E449	02		STAX	B	STORE IT BACK
E44A	C9		RET		
E44B	F3	RFRSH	DI		DISABLE INTERRUPTS
E44C	F5		PUSH	PSW	SAVE ON STACK
E44D	E5		PUSH	H	
E44E	D5		PUSH	D	
E44F	3A 02 E0		LDA	DIGIT	FIND OUT WHICH DIGIT
E452	FE 01		CPI	01H	LAST DIGIT?
E454	C2 5D E4		JNZ	NFST	JUMP IF NOT FIRST, ELSE CONTINUE
E457	21 06 E0		LXI	H,0E006H	HL REG RE-INITIALIZED
E45A	22 00 E0		SHLD	POINT	POINT POINTS TO DD1
E45D	3E 00	NFST	MVI	A, 00H	
E45F	D3 1D		OUT	DIG	BLANK DISPLAY
E461	2A 00 E0		LHLD	POINT	POINT POINTS TO SEG. DATA
E464	EB		XCHG		SWAP
E465	1A		LDAX	D	LOAD SEG. DATA VIA DE PAIR
E466	EB		XCHG		SWAP BACK
E467	D3 1C		OUT	SEG	OUTPUT SEG. DATA TO DISPLAY
E469	3A 02 E0		LDA	DIGIT	LOAD DIGIT DATA
E46C	D3 1D		OUT	DIG	OUTPUT DIGIT DATA TO DISPLAY
E46E	FE 08		CPI	08H	LAST DIGIT?
E470	CA E4 80		JZ	LOOP1	JUMP IF LAST, ELSE CONTINUE
E473	07		RLC		ROTATE TO NEXT DIGIT
E474	32 02 E0		STA	DIGIT	STORE FOR NEXT DIGIT
E477	23		INX	H	INCREMENT
E478	22 00 E0	LOOP2	SHLD	POINT	POINT POINTS TO NEXT SEG. DATA
E47B	D1		POP	D	SAVE IT
E47C	E1		POP	H	
E47D	F1		POP	PSW	
E47E	FB		EI		ENABLE INTERRUPTS
E47F	C9		RET		RETURN
E480	3F 01	LOOP1	MVI	A, 01H	
E482	32 02 E0		STA	DIGIT	DIGIT POINTS TO DIGIT 1
E485	C3 78 E4		JMP	LOOP2	
E600	FC		ORG	0E600	0
E601	60		DB	0FCH	1
E602	DA		DB	0DAH	2
E603	F2		DB	0F2H	3
E604	66		DB	066H	4
E605	B6		DB	0B6H	5
E606	3E		DB	03EH	6
E607	E0		DB	0E0H	7
E608	FE		DB	0FEH	8
E609	E6		DB	0E6H	9
E60A	EE		DB	0EEH	A
E60B	3E		DB	03EH	B
E60C	9C		DB	09CH	C
E60D	7A		DB	07AH	D
E60E	9E		DB	09EH	E
E60F	8E		DB	08EH	F

Figure 16b. 8080A Interface to Refresh Controller in Figure 14

Upon interruption by the 555 timer, the microprocessor is vectored to service the routine RFRSH. This routine uses the register POINT to locate segment information (DD1, DD2, DD3 and DD4) to be output to the display. Label SEG is the address to which segment data is to be written. The label DIG is used in a similar manner to identify the address where digit data is to be written. RFRSH updates the display by first blanking all segments. This interdigit blanking eliminates the phenomenon of partially illuminated segments known as ghosting. Next, segment information is written to the octal latch (74LS273). Finally, the digit information is written to the quad latch (74LS175). Control is then returned to the main program. This process is repeated with the correct segment information for each of the four digits.

With proper display filtering, the circuit in Figure 12 controlled by either the 6800 or 8080A programs provides an excellent four digit, sunlight viewable display.

The Refresh Controller shown in Figure 15 is quite similar to the circuit in Figure 14. However, there are a few minor differences that should be pointed out. The Refresh Controller in Figure 15 utilizes the National DS8858 BCD-to-seven segment decoder driver. This enables the user to write BCD data to the Refresh Controller without utilizing the LOAD subroutine. This saves both RAM space and microprocessor time. The software to interface this Refresh Controller to the 6800 and the 8080A microprocessors is shown in Figures 17a and 17b respectively. The circuit uses the green 5082-7673 large seven segment common cathode displays.

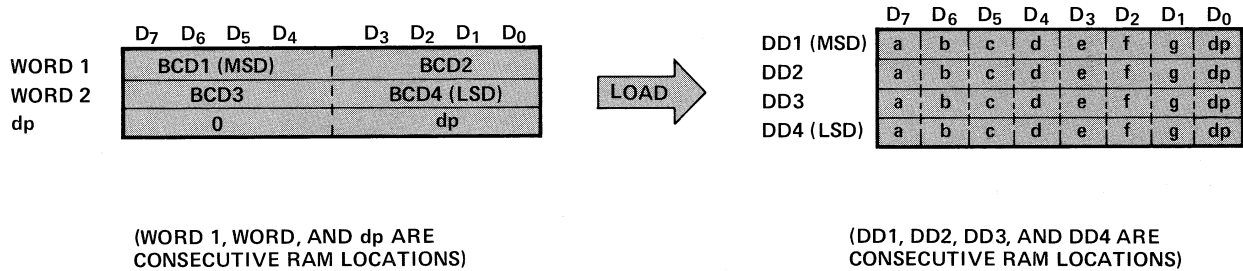


Figure 16c. Subroutine LOAD

	BF 04	SEG	EQU	\$BF04	
	BF 05	DIG	EQU	\$BF04	
0000		POINT	RMB	2	
0002		DIGIT	RMB	1	
0003		DATA	RMB	8	
0400			ORG	\$0400	
0400	CE 00 03	INIT	LDX	I,\$0003	
0403	DF 00		STX	D,POINT	INITIALIZE POINT
0405	7F 00 02		CLR	E,DIGIT	INITIALIZE DIGIT
0408	0F	RFRSH	SEI		DISABLE INTERRUPTS
0409	DE 00		LDX	D,POINT	GET POINT
040B	E6 00		LDA	B X,0	
040D	86 08		LDA	A I,\$08	
040F	B7 BF 05		STA	A E,DIG	BLANK DISPLAY
0412	F7 BF 04		STA	B E,SEG	OUTPUT SEG. DATA TO DISPLAY
0415	96 02		LDA	A D,DIGIT	GET DIGIT
0417	81 07		CMP	A I,\$07	
0419	27 0B		BEQ	LOOP1	BRANCH IF LAST DIGIT, ELSE CONTINUE
041B	7C 00 02		INC	E,DIGIT	INCREMENT TO NEXT DIGIT
041E	B7 BF 05		STA	A E,DIG	OUTPUT DIGIT DATA TO DISPLAY
0421	7C 00 01		INC	E,POINT+1	POINT POINTS TO NEXT BCD WORD
0424	0E		CLI		
0425	3B		RTI		
0426	B7 BF 05	LOOP1	STA	A E,DIG	OUTPUT DIGIT DATA TO DISPLAY
0429	CE 00 03		LDX	I,\$0003	
042C	DF 00		STX	D,POINT	RE-INITIALIZE POINT
042E	7F 00 02		CLR	E,DIGIT	RE-INITIALIZE DIGIT
0431	0E		CLI		
0432	3B		RTI		

Figure 17a. 6800 Interface to Refresh Controller Shown in Figure 15

E000		SEG	EQU	001CH	
E000		DIG	EQU	001DH	
E000			ORG	0E000H	
E000	03 E0	POINT	DW	DATA	
E002		DIGIT	DS	01H	
E003		DATA	DS	08H	
E00B			ORG	0E400H	
E400	21 03 E0	INIT	LXI	H,\$0E003H	
E403	22 00 E0		SHLD	POINT	INITIALIZE POINT
E406	3E 00		MVI	A,0	
E408	32 02 E0		STA	DIGIT	INITIALIZE DIGIT
E40B	F3	RFRSH	DI		DISABLE INTERRUPTS
E40C	F5		PUSH	PSW	SAVE
E40D	E5		PUSH	H	SAVE
E40E	2A 00 E0		LHLD	POINT	GET POINT
E411	3E 08		MVI	A,\$08H	
E413	D3 1D		OUT	DIG	BLANK DISPLAY
E415	7E		MOV	A,M	
E416	D3 1C		OUT	SEG	OUTPUT SEG. DATA TO DISPLAY
E418	3A 02 E0		LDA	DIGIT	GET DIGIT
E41B	D3 1D		OUT	DIG	OUTPUT DIGIT DATA TO DISPLAY
E41D	FE 07		CPI	07H	
E41F	CA 2E E4		JZ	LOOP1	BRANCH IF LAST, ELSE CONTINUE
E422	3C		INR	A	
E423	32 02 E0		STA	DIGIT	INCREMENT TO NEXT DIGIT
E426	23		INX	H	
E427	22 00 E0	LOOP2	SHLD	POINT	POINT POINTS TO NEXT BCD WORD
E42A	E1		POP	H	
E42B	F1		POP	PSW	
E42C	FB		EI		ENABLE INTERRUPTS
E42D	C9		RET		
E42E	3E 00	LOOP1	MVI	A,0	
E430	32 02 E0		STA	DIGIT	RE-INITIALIZE DIGIT
E433	21 03 E0		LXI	H,\$0E003H	RE-INITIALIZE POINT
E436	C3 27 E4		JMP	LOOP2	

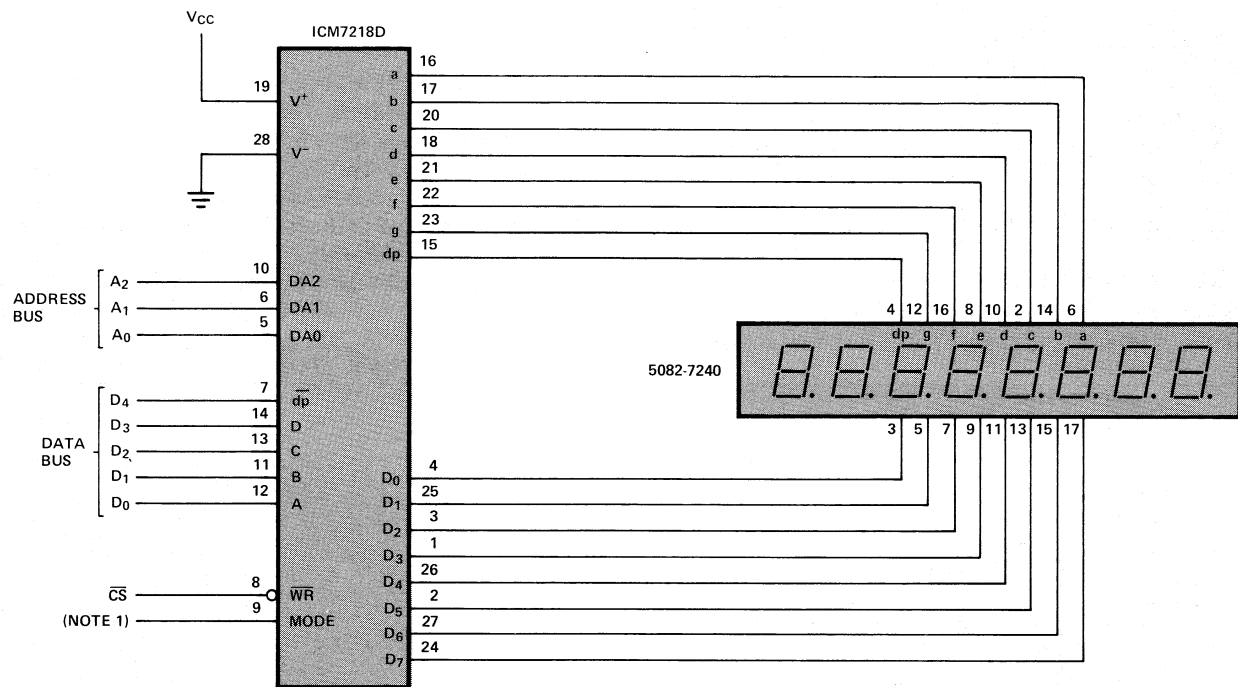
Figure 17b. 8080A Interface to Refresh Controller Shown in Figure 15

CODED DATA CONTROLLER

Figure 18 shows a Coded Data Controller designed for an eight character monolithic seven segment display. The circuit uses the Intersil ICM7218D to provide BCD data storage and display multiplexing. The ICM7218D is designed to drive common cathode LED displays at 10 mA I_{PEAK}/segment (minimum) on a 12% duty cycle.

The circuit illustrated in Figure 18 uses the ICM7218D to drive an eight digit 5082-7240 monolithic LED display. The common anode version (ICM7218C) is rated at 20 mA I_{PEAK}/segment (minimum). If higher drive currents are needed and a four digit display is acceptable, the eight

digit lines on the ICM7218D can be paralleled to drive four digits at twice the minimum current. The microprocessor interfaces to the ICM7218D through five Data Inputs (BCD and \overline{dp}), three digit address lines (DA0, DA1, and DA2), a MODE input, and a \overline{WRITE} input. Data can be written in to the eight memory locations in the static memory of the ICM7218D via a three bit binary code on the digit address inputs. When the digit address lines are valid, a negative going \overline{WRITE} pulse clocks the BCD and \overline{dp} data into the RAM. This method of memory addressing allows the user to update the display information only where it is necessary.



(NOTE 1) MODE IS A TRISTATE INPUT SUCH THAT WHEN MODE = HIGH, THE 7218 PROVIDES HEXIDECIMAL DECODING; WHEN MODE = FLOATING, THE 7218 PROVIDES CODE B DECODING; AND WHEN MODE = LOW, THE 7218 BLANKS THE DISPLAY.

Figure 18. Coded Data Controller

DECODED DATA CONTROLLER

Figure 19 shows a Decoded Data Controller designed for use with 20.3mm (0.8 inch) seven segment displays. The circuit utilizes the National MM74C911 to directly drive four of the large seven segment displays. The MM74C911 is used to provide segment data storage and display multiplexing. The MM74C911 is designed to drive common cathode displays at 100 mA I_{PEAK}/segment on a 25% duty cycle. The circuit illustrated in Figure 17 uses the MM74C911 to drive four HDSP-3403 20.3 mm (0.8 inch) standard red common cathode displays.

The microprocessor interfaces to the MM74C911 through eight data lines (a, b, c, d, e, f, g, dp), two address inputs K₁ and K₂, $\overline{\text{CHIP ENABLE}}$, and $\overline{\text{WRITE ENABLE}}$. The desired segment data is written into the register selected by the address information when $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are low. This data is latched when either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ return high. Data hold time is not required.

An internal oscillator sequentially presents the stored data to the output drivers which directly drive the LED display. The drivers are active when the control pin labelled $\overline{\text{SEGMENT OUTPUT ENABLE}}$ (SOE) is low, and are tri-stated when SOE is high. This feature allows duty cycle brightness control for varying ambient light conditions. Also, $\overline{\text{SOE}}$ can be used to disable the output drivers for power conservation. The digit outputs directly drive the base of the digit transistor when the control pin labelled $\overline{\text{DIGIT INPUT OUTPUT}}$ (DIO) is low.

INTENSITY MATCHING

All Hewlett-Packard seven segment displays are tested for luminous intensity to ensure that data sheet values are

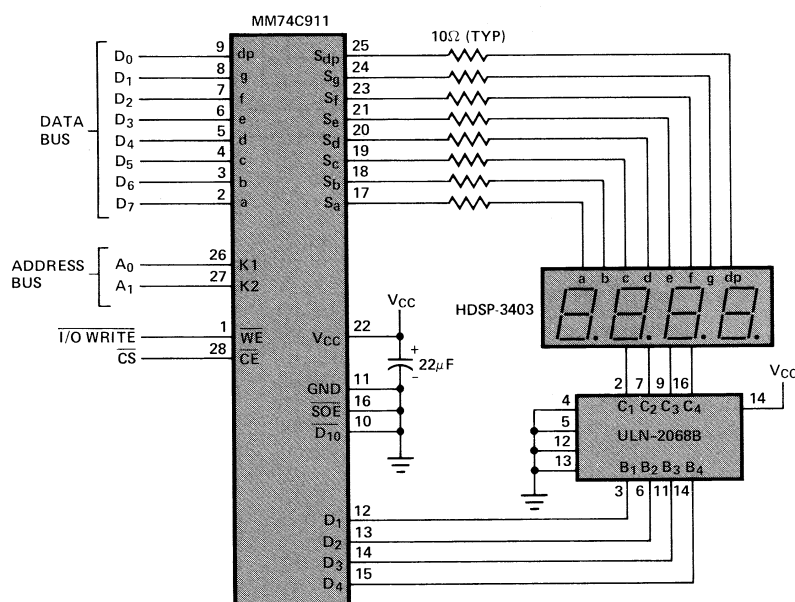
met. All displays which can be end stacked are categorized according to their intensity levels. The eye can detect roughly a 2:1 change in luminous intensity and, therefore, this is the criterion for intensity categories. This categorization allows end stacking of the displays, thereby providing a panel with a pleasing, uniform appearance.

The large seven segment displays are individually tested and categorized for luminous intensity. The intensity category is designated by a single or double letter located on the right hand side of the package. When end stacking, it is preferable that the user choose devices from a single category to provide uniform intensity across the display panel.

The monolithic seven segment display clusters are inherently intensity matched digit to digit in one display package. The immersion type monolithic displays which are designed for end stacking are categorized for intensity. The category is designated by a letter on the back side of the package. The user should choose devices from a single category when end stacking the displays.

COLOR MATCHING

Color uniformity of the large seven segment displays is an important consideration. The standard red and high efficiency red displays have inherent color uniformity and need not be categorized. However, the eye is more sensitive to color differences in the yellow and green regions. Therefore, displays of these color types are categorized by dominant wavelength. This category is denoted by a number on the right hand side of the package. The user should choose units from a single category to achieve a display panel with optimal color uniformity.



INPUT CONTROL				OPERATION
CE	DIGIT ADDRESS		WE	
	K2	K1		
0	0	0	0	WRITE DIGIT 1
0	0	0	1	LATCH DIGIT 1
0	0	1	0	WRITE DIGIT 2
0	0	1	1	LATCH DIGIT 2
0	1	0	0	WRITE DIGIT 3
0	1	0	1	LATCH DIGIT 3
0	1	1	0	WRITE DIGIT 4
0	1	1	1	LATCH DIGIT 4
1	X	X	X	DISABLE WRITING

X = DON'T CARE

DIO	SOE	DIGIT LINES				OPERATION
		D4	D3	D2	D1	
0	0	R	R	R	R	REFRESH DISPLAY
0	1	R	R	R	R	DISABLE SEGMENTS
1	0	0	0	0	0	DIGITS ARE INPUTS
1	0	0	0	0	1	DISPLAY DIGIT 1
1	0	0	0	1	0	DISPLAY DIGIT 2
1	0	0	1	0	0	DISPLAY DIGIT 3
1	0	1	0	0	0	DISPLAY DIGIT 4
1	1	0	0	0	0	POWER SAVER MODE

R = REFRESH (DIGIT LINES SEQUENTIALLY PULSED)

Figure 19. Decoded Data Controller

SUNLIGHT VIEWABILITY

The rapid growth of sophisticated electronic systems for use in avionic, automotive, machine, and military equipment has created the need for an electronic information display that is viewable in bright sunlight. By combining the newest LED product design technology and the most recent techniques for contrast enhancement, Hewlett-Packard can now provide the display system designer with devices that are useable in direct 107,000 lumens per square meter (10,000 foot candle) sunlight.

The HDSP-3530/-3730/-4030/-4130 series of large seven segment displays optimize the following parameters that contribute to the readability of the LED display in bright sunlight:

- a. LED Color
- b. Luminance Contrast
- c. Chrominance Contrast (color difference)
- d. Front Surface Reflections

These sunlight viewable display devices are assembled with Gallium Arsenide Phosphide (GaAsP) LED chips on a Gallium Phosphide (GaP) substrate. These materials produce the needed light output when driven with peak currents up to 120 mA. High current LED chips are used to allow high peak and average current in the display. The high efficiency red and yellow displays provide the most light output for a given input current and can easily be made visible in bright sunlight. The package configuration uses a neutral gray body and untinted segments to allow the display system designer to achieve readability by obtaining an optimum combination of both luminous and chrominance contrast. When placed behind a 20% to 25% neutral density gray filter, the illuminated segments provide a distinctly visible chrominance contrast with respect to the gray package.

MOUNTING CONSIDERATIONS

The large segment display devices are constructed utilizing a lead frame in a standard DIP package. All 7.6mm (0.3 inch) and 10.9mm (0.43 inch) displays are manufactured with leads on 2.54mm (0.10 inch) centers with a row-to-row spacing of 7.6mm (0.3 inch). The 20.3mm (0.8 inch) displays are also on 2.54mm (0.10 inch) centers but the row-to-row spacing is 15.2mm (0.6 inch). The 14.1mm (0.56 inch) displays are on 2.54mm (0.10 inch) centers with row-to-row spacing of 15.2mm (0.6 inch). However, the leads are aligned along the top and bottom of the package rather than down the sides. Both the 14.1mm (0.56 inch) and 20.3mm (0.8 inch) displays can be socketed using a standard 24 pin IC socket or strip sockets. All large seven segment devices are end stackable and are designed for PC board mounting and wave soldering.

If the large segment devices are to be wave soldered, Sn60 or Sn63 solder is recommended. The solder wave is

recommended to be at 245°C with a dwell time of 1-1/2 to 2 seconds. The 20.3mm (0.8 inch) displays have a small tab at each corner to establish a 1mm (0.040 inch) seating plane above the printed circuit board. The other large seven segment displays have a shoulder on the lead frame to achieve a similar seating plane above the printed circuit board.

The non-immersion type monolithic displays may be mounted either by use of pins which may be soldered into the plated holes at the connector edge of the PC board or by insertion into a standard PC board connector (Table IV). The devices may be soldered for up to three seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the lens. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid wire be used in soldering operations.

The immersion type monolithic displays are designed for insertion into 12 or 14 pin DIP sockets or soldering into PC boards. All of these type of displays are manufactured on 2.54mm (0.100 inch) centers with a row-to-row spacing of 7.6mm (0.300 inch). If the displays are to be soldered into a PC board, the solder temperature must be kept at or below 245°C, 1/16 inch below the seating plane, for a maximum of five seconds. The shoulders of the lead frame pins are intentionally raised above the bottom of the package so that the display can be mounted at an angle to the PC board. Mounting angles up to 20° are often necessary in hand held or desk top applications and are easily attainable with immersion type monolithic displays. Refer to Application Note 937 for further instructions concerning installation of these devices.

LED displays, as well as all electronic components, operate more reliably at lower temperatures. Thermal considerations are important, and any method of cooling or heat sinking the displays will result in more reliable operation. Under no conditions should the absolute maximum temperature ratings be exceeded.

To optimize device optical performance, specially developed plastics are used in all display products. These plastics restrict the solvents that may be used for cleaning. Tests have demonstrated that the only fluorocarbon cleaner that is compatible with plastic LED devices is trichloro-fluoroethane (F113). This cleaner is sold commercially under the trade names Freon, Genesolv D, and Arkalone. Water can be used to clean both large seven segment displays and the immersion lens type monolithic displays. Water can also be used for hand cleaning the non-immersion type monolithic seven segment displays if care is taken to prevent water from collecting under the lens.

TABLE I. BCD to Seven Segment Decoder/Drivers

Part Number	Vendor*	Output Structure	Output Current	Output Active State	Features
74LS47	TI, Fairchild, National	Open Collector	24 mA	Low	Auto Zero-Blanking, Lamp Test, 0-9
74LS48	TI, Fairchild, National	2K Pull-Up	6 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
74LS49	TI, National	Open Collector	8 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
8T04	Signetics	Open Collector	40 mA	Low	Auto Zero-Blanking, Lamp Test, 0-9
8T06	Signetics	Open Collector	40 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
9368	Fairchild	Open Emitter	-19 mA	High	Constant Current, Latch, Auto Zero-Blanking, 0-9, A-F
9370	Fairchild	Open Collector	40 mA	Low	Latch, Auto Zero-Blanking, 0-9, A-F
9384	Fairchild	Current Mirror	15 mA	Low	Constant Current, Latch, Auto Zero-Blanking, 0-9, E,H,C,D
DS8669	National	Open Collector	25 mA	Low	2 Digit (14 Outputs), 0-9, C,A,P,E,H,J,L,F,-
MC14511	Motorola	NPN Bipolar Emitter	-25 mA	High	Latch, Lamp Test, Blanking Input, 0-9
MC14547	Motorola	NPN Bipolar Emitter	-65 mA	High	Latch, Blanking Input, 0-9

*This is a partial list of vendors. Other suppliers for the same part may exist.

TABLE II. Display Drivers

Part Number	Vendor*	Number of Drivers	Input Compatibility	Output Current (mA)	Features
DS8859	National	6	TTL	0-40 (Max)	Programmable Constant Current
DS8867	National	8	7V MOS	-14 (Typ)	Constant Current
DS8877	National	6	MOS, TTL	50 (Typ)	Low Current Version of 75492
DS8874/76/79	National	9	9V MOS	50 (Min)	Serial Input, Low Battery Indicator
ULN-2031/33	Sprague	7	TTL, 5V-15V CMOS	±80 (Max)	NPN or PNP Darlington Pair
75497/498	TI	7	MOS, TTL	125 (Max)	
75492	TI, Fairchild, Motorola, National	6	9 MOS	250 (Max)	Darlington Pair
DS8870	National	6	9V MOS	350 (Max)	
DS8863/8963	National	8	9V MOS	500 (Max)	
ULN-2003A (MC1413)	Sprague, TI, Motorola	7	TTL, 5V CMOS	500 (Max)	2.7 kΩ Series Resistance to Darlington Pair
ULN-2981A	Sprague	8	TTL, 5V CMOS	-500 (Max)	
ULN-2068B	Sprague	4	TTL, 5V CMOS	1500 (Max)	Predriver Stage to Darlington Pair

1 OF N DECODERS

Part Number	Vendor*	Number of Drivers	Input Compatibility	Output Current (mA)	Features
74LS259	TI, Signetics	8	TTL	8 (Max)	Active High, Four Mode Operation
DS8665	National	14	9V MOS	-20 (Max)	Active Low, Oscillator Output
NE590	Signetics	8	TTL	250 (Max)	Active Low, Four Mode Operation

*This is a partial list of vendors. Other suppliers for the same part may exist.

TABLE III. Multifunction Display Drivers

COUNTERS

Part Number	Vendor	Function	Drive Conditions
MM74C925/6/7/8	National	CMOS counter with internal output latch and self-contained internal oscillator and scanning circuitry	4 Digit Common Cathode 40 mA pk (typ) 1 of 4 D.F.
MK50395-9	MOSTEK	Six decade counter/display decoder; look ahead carry or borrow, loadable counter	6 Digit Common Anode segment and digit drivers required
MK5002/517	MOSTEK	Four decade counter, latch, decoder with leading zero blanking	4 Digit Common Anode or Common Cathode segment and digit drivers required
ICM7217 ICM7227	Intersil	CMOS up/down counter; presettable start/count and compare register; for hard-wired microprocessor control applications; cascadable	4 Digit Common Cathode (A,C) 12.5 mA pk (typ), 10 mA pk (min) 1 of 4 D.F. Four Digit Common Anode (B) 40 mA pk (typ), 25 mA pk (min) 1 of 4 D.F.
ICM7208	Intersil	Seven decade counter with scanning circuitry, display blanking, reset	7 Digit Common Cathode 15 mA pk (typ) 1 of 8 D.F.
ICM7225	Intersil	High speed (25 MHz typ) counter/decoder/driver	4-1/2 Digit Common Anode 8 mA dc (typ), 5 mA dc (min)
ICM7216 ICM7226	Intersil	Universal Counter that measures frequency, period, frequency ratio, time interval, units	8 Digit Common Anode (A/C) 35 mA pk (typ), 25 mA pk (min) 1 of 8 D.F. 8 Digit Common Cathode (B/D) 15 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ZN1040E	Ferranti Packard	Universal Up/Down Synchronous Counter, with separate memory latches, look ahead or borrow, internal oscillator, and scanning circuitry	4 Digit Common Anode or Common Cathode 80 mA pk (typ), 50 mA pk (min) 1 of 4 D.F.

DISPLAY CONTROLLERS

Part Number	Vendor	Function	Drive Conditions
8279 8279-5	Intel	Programmable Keyboard/Display Interface; scanned keyboard, sensor mode, strobed input mode, right or left entry mode	16 Digit Common Anode or Common Cathode segment and digit drivers required
MM74C912 (BCD-7 Segment) MM74C917 (Binary-Hex)	National	Display Controller Driver with 6 x 8 RAM, internal oscillator and scanning circuit, internal segment decoder	6 Digit Common Cathode 100 mA pk (typ), 60 mA pk (min) 1 of 4 D.F.
MM74C911	National	Expandable Segment Display Controller with 4 x 8 RAM, self-contained internal oscillator and scanning circuit	4 Digit Common Cathode 100 mA pk (typ), 60 mA pk (min) 1 of 4 D.F.
MM5450 MM5451	National	Serial Input Display Driver; two line interface to microprocessor, continuous brightness control, data enable	39 or 35 Segment Common Cathode 25 mA dc (max), 15 mA dc (min)
ICM7218	Intersil	Display driver system with 8 x 8 memory; Hex decode, code B, or no decode	8 Digit Common Anode (A, C, E) 25 mA pk (typ), 20 mA pk (min) 1 of 8 D.F. 8 Digit Common Cathode (B) 25 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ICM7212	Intersil	Display Decoder Driver	4 Digit Common Anode 8 mA dc (typ), 5 mA dc (min)

CLOCKS AND STOPWATCHES

Part Number	Vendor	Function	Drive Conditions
ICM7045A	Intersil	Complete industrial stopwatch, precision decade timer to count seconds, minutes or hours by relation of suitable oscillatory frequencies	7 Digit Common Cathode 15 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ICM7215	Intersil	Split and Taylor time stopwatch circuit	6 Digit Common Cathode 13.2 mA pk (typ), 9 mA pk (min) 1 of 8 D.F.
S1998A1B	AMI	Digital Alarm Clock with snooze and sleep timer	4 Digit Common Anode 16 mA dc (typ)
MSM5523	OKI	Multifunction clock and radio, frequency counter; five time modes, four frequency modes, AM/FM indicator	4-1/2 Digit Common Anode or Common Cathode segment and digit drivers required
MSM5929	OKI	Auto Clock; 12 or 24 hour format, blinking colon, leading zero blanking	4 Digit Common Anode or Common Cathode segment and digit drivers required

TABLE III. Multifunction Display Drivers (Continued)

A/D CONVERTERS

Part Number	Vendor	Function	Drive Conditions
ICL7107	Intersil	A/D Converter with decoder/drivers and clock	3-1/2 Digit Common Cathode 8 mA dc (typ), 5 mA dc (min)
ADD3501/3701	National	DVM with pulse modulation A-D conversion, internal or external clock overflow displayed	3-1/2 Digit Common Cathode 50 mA pk (typ) 1 of 4 D.F. digit drivers required
LD130	Siliconix	CMOS A/D Converter; BCD outputs	3-1/2 Digit Common Anode or Common Cathode required BCD-7 segment decoder and digit drivers

TABLE IV. Connectors for Non-Immersion Lens Monolithic Seven Segment Displays

Vendor	Part Number	Description
Teledyne Kinetics 410 South Cedros Avenue P.O. Box 427 Solano Beach, CA 92075 (714) 755-1181	Model S4050 Model S4200	Glass filled thermoplastic polyester with spring contacts. Parallel and 90° mounting as well as high and low profile available. Model S4200 is available with up to 40 contacts.
Precision Concepts, Inc. 1595B Ocean Avenue Bohemia, NY 11716 (516) 567-0995	1255 90-1255	Snapper connector. Any number of contacts can be supplied on a strip with any of the following angles from horizontal (0°, 45°, 60°, 90°). Solder plug pins also available.
William Prym-Werke KG 519 Stolberg/Rheinland (02402) 14331/14465	Specify Contact Pin	Contact pin with knurling. Standard dimensions with special designs done on request.
J.A.V. Manufacturing, Inc. 125 Wilbur Place Bohemia, NY 11716 (516) 567-9030	Series 022-002	Snap in friction fit. Available in 30° angle from horizontal. Up to 17 contacts. Solder plug pins also available.

TABLE V. Filter Materials

LED Color	Panelgraphic	SGL Homalite	3M Company	Glarecheq	Rohm and Haas	Schott	OCLI	Polaroid
Standard Red	Ruby Red 60 Dark Red 63 Purple 90	H100-1600 H100-1605 H100-1804 (Purple)	R6510 P7710	Spectrafilter 112 Spectrafilter 118	Plexiglass 2423 Oroglass 2414	RG-645 RG-630		
High Efficiency Red	Scarlet Red 65 Neutral Gray 10	H100-1670	R6310 N0220 (Neutral Gray)	Spectrafilter 110 Spectrafilter 105 (Neutral Gray)		RG-610	Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)
Yellow	Yellow 27 Neutral Gray 10	H100-1720	A5910 N0220 (Neutral Gray)	Spectrafilter 106 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)
Green	Green 48 Neutral Gray 10	H100-1440	G5610 N0220 (Neutral Gray)	Spectrafilter 107 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)

Addresses for companies listed above.

Panelgraphic Corporation
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

3M Company
Visual Products Division
3M Center, Bldg. 220-10W
St. Paul, MN 55101
(612) 733-0128

Rohm and Haas
Independence Mall West
Philadelphia, PA 19105
(215) 592-3000

Optical Coating Labs, Inc. (OCLI)
2789 Griffen Avenue
Santa Rosa, CA 95401
(707) 545-6440

SGL Homalite
11 Brookside Drive
Wilmington, DE 19804
(302) 652-3686

Glarecheq
Chequers Engraving Ltd.
1-4 Christina Street
London EC2A P4A
England
(01) 739-6964

Schott Optical Glass
Duryea, PA 13642
(717) 457-7485

Polaroid Corporation
Polarizer Division
20 Ames Street
Cambridge, MA
(617) 577-2000/3655

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