High-Frequency Transistor Primer

Part I

Silicon Bipolar Electrical Characteristics

Table of Contents

I. Transistor Structure Types 2
- A. Bipolar 2
- B. NPN 2
- C. Silicon 2
- D. Planar 2
- E. Epitaxial 2

II. Maximum Ratings 3
- A. Voltage Ratings 3
- B. Current Ratings 3
- C. Dissipation Ratings 3
- D. Junction Temperature Rating 4
- E. Storage Temperature Rating 5

III. Electrical and Performance Ratings 5
- A. Performance (Operating) Characteristics 5
  - 1. Power Gain 5
    - a. G_{max} 5
    - b. $|S_{21}|^2$ 5
  - 2. Noise Figure 6
  - 3. Power Output 6
  - 4. Efficiency 6
- B. Electrical Characteristics 6
  - 1. DC Characteristics 6
    - a. Collector-Base Junction, $V_{(BR)\ CBO}$, I_{CBO} 6
    - b. Emitter-Base Junction, $V_{(BR)\ EBO}$, I_{EBO} 7
    - c. Collector-Emitter Terminal, $V_{(BR)\ CEO}$, I_{CEO} 7
    - d. DC Current Gain, h_{FE} 8
  - 2. AC Characteristics 8
    - a. S-Parameters 8
    - b. Transition Frequency, f_T 9
    - c. Collector-Base Time Constant, $r_b'C_c$ 10
    - d. Collector-Base Capacitance, C_{cb} 10
    - e. Maximum Frequency of Oscillation, f_{max} 10

IV. Glossary of Microwave Terminology 11

Preface

Transistors have been used at frequencies above 1 GHz since about 1960. The technology has increased such that both circuit and project engineers look to transistors for new system requirements at frequencies up to millimeter wave. The purpose of this primer series is to introduce microwave designers to the terminology used in describing the characteristics of high-frequency transistors. An understanding of the capabilities and limitations of these transistors should result in better performing, more reliable circuits.

This volume, Part I, covers general device electrical characteristics for silicon bipolar transistors. Volume II covers general noise and S-parameter characterization. Part III covers device thermal properties and Part IV covers GaAs FET device parameters and measurements.

Introduction

This primer is a short glossary and brief explanation of transistor terms commonly used in Hewlett-Packard transistor data sheets, advertisements and other technical communications. Some of these terms are simple, virtually self-explanatory and are included here primarily for the sake of completeness. Others are more specialized and potentially ambiguous due to a lack of terminology standardization in the high-frequency transistor area. These latter types receive more treatment here.

I. Transistor Structure Types

All current Hewlett-Packard silicon transistors are of the bipolar NPN planar epitaxial type. Briefly, the significance of each of these terms is as follows:

A. Bipolar

In its broadest sense it is the basic structure shown schematically in Figure 1, i.e., the familiar three semiconductor-region structure. Bipolar specifically means that the charge carriers of both negative (electrons) and positive (holes) polarities are involved in the transistor action. In way of contrast, unipolar types include the junction-gate and insulated-gate field-effect transistors which are basically one- or two-semiconductor-region structures in which carriers of a single polarity dominate.

B. NPN

An abbreviation for *negative-positive-negative* which identifies the regions of the structure as to polarity of the dominant or majority carrier in each region. The other polarity type is PNP. (See Figure 1.)

C. Silicon

Silicon is one of two elements from the fourth column of the periodic table which are in widespread use for transistor fabrication (the other is germanium). Other materials used include the compound gallium arsenide. Silicon is in predominant use because it results in the most favorable compromise among high-frequency, high-temperature, high-reliability and ease of use attributes of the usable semiconductor materials.

D. Planar

A term which denotes that both emitter-base and base-collector junctions of the transistor intersect the device surface in a common plane (hence, a better term might be co-planar). However, the real significance of the so-called planar structure is that the technique of diffusing dopants through an oxide mask, used in fabricating such a structure, results in junctions being formed beneath a protective oxide layer. These protected junctions are less prone to surface problems sometimes associated with other types of structures, such as the mesa.

E. Epitaxial

This term, as it is commonly used, is actually a shortening of the term epitaxial-collector. That is, the collector region of the transistor is formed by the epitaxial technique rather than by diffusion which is commonly used to form the base and emitter regions. The epitaxial layer is formed by condensing a single-crystal film of semiconductor material upon a wafer or substrate which is usually of the same material. Thus, an epitaxial (collector) transistor is one in

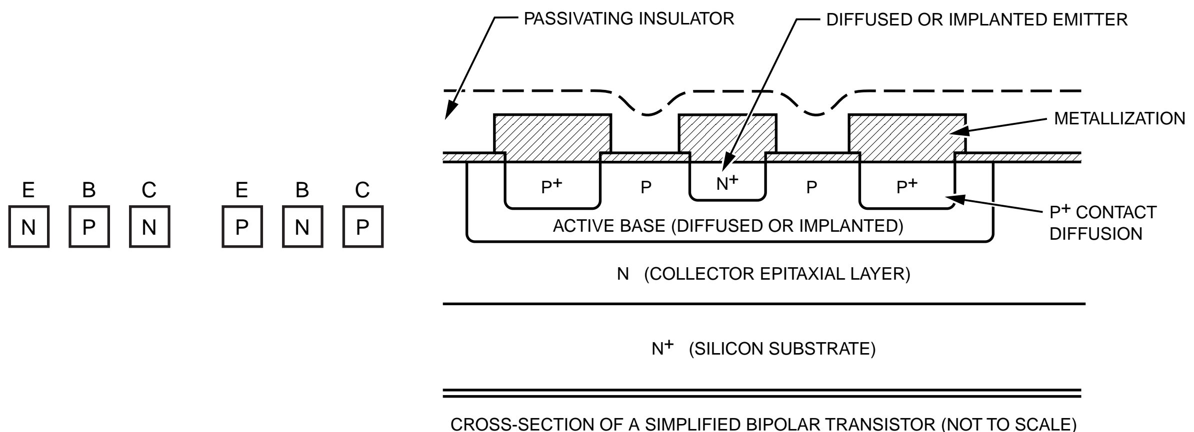


Figure 1. Transistor Structure Schematics

which the collector region is formed upon a low-resistivity silicon substrate. Subsequently, the base and emitter regions are diffused into the "epi" layer. The epitaxial technique lends itself to precise tailoring of collector-region thickness and resistivity with consequent improved device performance and uniformity.

II. Maximum Ratings

Maximum ratings may be defined as limiting values of externally applied stresses (voltage, current, temperature, etc.) normally under control of the user which if exceeded may result in irreversible damage to the device. The user who exceeds the maximum ratings does so necessarily at his own risk. These ratings are set by the manufacturer on the basis of many considerations such as life tests, breakdown voltages, etc., in order to define to the user certain operating conditions which are safe for each and every transistor of a given type.

Unfortunately, due to the cost of establishing certain ratings (which must eventually be reflected in product prices) the ratings given do not always encompass all conceivable operating conditions. For example, device dissipation ratings typically are complete only for the case of continuous dissipation (as opposed to peak dissipation in pulse applications). In practice, the ratings given should be sufficient for the majority of applications of a particular device. In certain applications, more information must be obtained by the user himself and/or through applications assistance from the manufacturer. The following ratings typically appear on Hewlett-Packard transistor data sheets and provide adequate information for most applications of these devices.

A. Voltage Ratings

These ratings are usually derived from and usually coincide with the minimum device breakdown voltages. However, since this coincidence does not necessarily occur, it has become common practice to include both maximum voltage ratings and minimum breakdown voltages on data sheets.

It can be argued that such practice erodes the meaning of maximum ratings. Since, strictly speaking, maximum ratings should not be exceeded under any circumstances, strict adherence to voltage ratings would preclude measurement of breakdown voltage of any but marginal devices. In practice, voltage ratings are usually maximum operating voltages and no damage results if they are exceeded only to measure the breakdown voltages provided that care is taken to ensure that the specified low currents for these measurements are not exceeded.

B. Current Ratings

Maximum current ratings are arrived at from various considerations such as bonding-wire current-carrying ability, overall transistor performance degradation, etc. Maximum ratings are usually given only for collector current (except, in some cases for switching devices) since safely limiting collector current usually ensures that base and emitter currents are also safely limited.

C. Dissipation Ratings

In addition to the individual ratings on voltage and current discussed above, there is also a limit to the voltage-current products which can be safely handled by a transistor. That is, there is a power dissipation rating which must also be adhered to. Since the dissipation capabilities of a device are a function of the temperature of the external environment, this rating is a function of that temperature. For the DC case, this temperature dependence is usually the only significant functional dependence of this rating. In the AC case, that is when device dissipation varies significantly with time, dissipation capabilities become a generally complex function of waveshape. In the latter case, in addition to an average dissipation rating (which coincides with the DC rating) there exists a peak dissipation rating which is a function of waveshape (e.g., a function of pulse width and pulse period in the case of rectangular waveforms). Due to the complexity of the general AC case, transistors are seldom characterized completely enough to include complete AC rating information. Most transistors are rated only in terms of maximum continuous dissipation (i.e., the maximum DC and the maximum average dissipation). This rating is typically specified in terms of a maximum continuous dissipation at or below some stated reference temperature (usually 25°C) and a linear derating factor to be applied at higher temperatures. These two quantities define the maximum continuous dissipation rating curve shown graphically in Figure 2, or expressed analytically as shown in Equation 1.

Equation 1 :

$P_{T(max)}\,T_X = P_{T(max)}\,T_{XI}\,; T_X \le T_{XI}$

$P_{T(max)}\,T_X = P_{T(max)}\,T_{XI} - K_{JX}\,\Delta T_X\,; T_{XI} < T_X < T_{X(max)}$

Where

T_X = Temperature of the external reference point

$P_{T(max)}$ = Maximum Total Dissipation, a function of T_X

T_{XI} = Reference temperature below which $P_{T(max)}$ is constant

K_{JX} = Linear Derating Factor

$T_{X(max)}$ = Maximum Junction Temperature

ΔT_X = $T_X - T_{XI}$

Two external temperature reference points are commonly used:

1. Air ambient, T_A (or free-air; i.e., no forced air cooling), which is the air temperature in proximity to the transistor case as mounted in its "normal" manner and,

2. Case ambient, T_C, which is the temperature at the point on the transistor package at which it is most effective to heat sink the transistor.

Which reference point is used depends on the application.

In summary, the continuous dissipation rating (usually based on a V x I product), and the collector voltage and current ratings define a DC safe operating area as sketched in Figure 3.

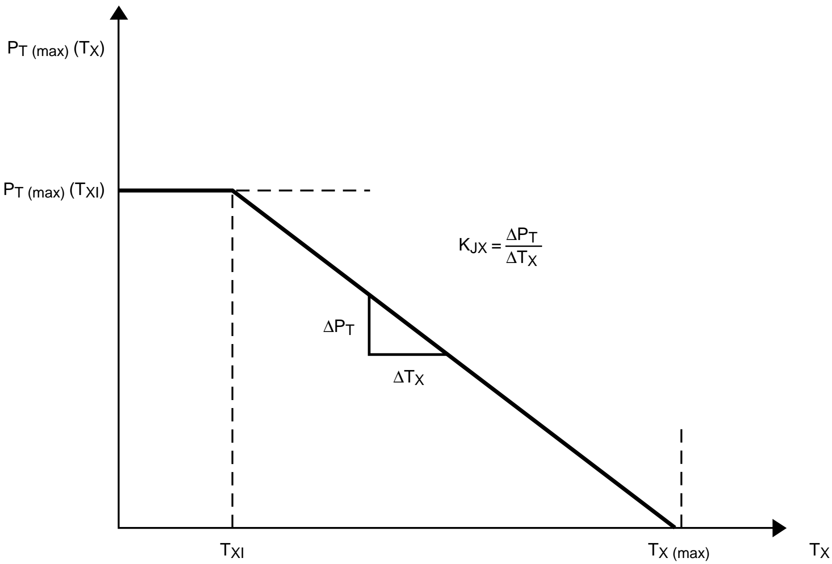


Figure 2. Continuous Dissipation Rating Curve

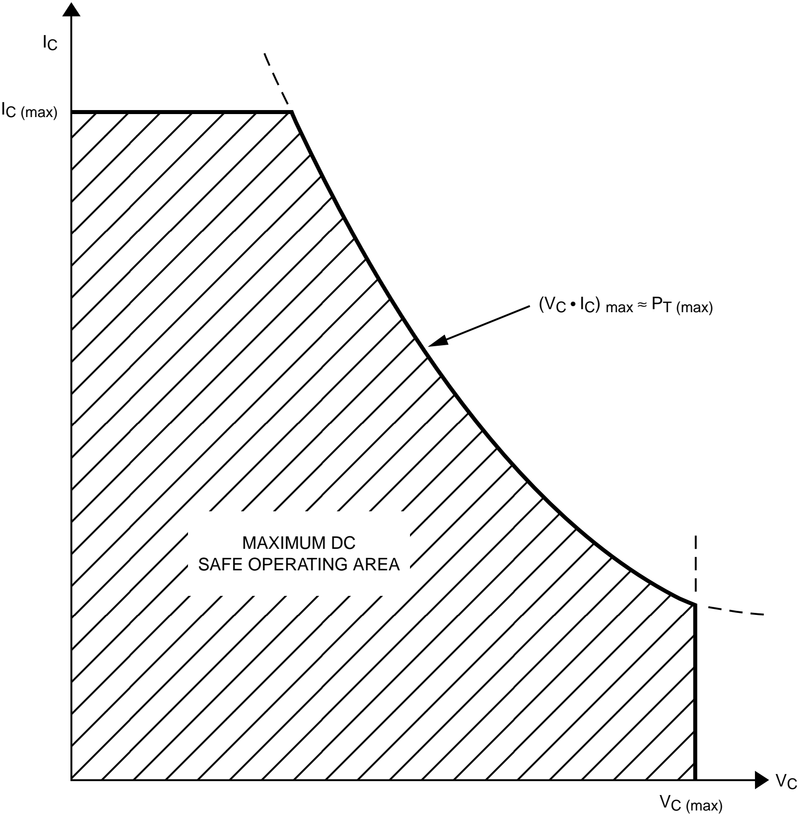


Figure 3. Maximum DC Safe Operating Area

D. Junction Temperature Rating

Another temperature reference point implicit in the above discussion of dissipation ratings is transistor junction temperature. The maximum external reference-temperature, $T_{X(max)}$, corresponds to the maximum internal junction

temperature, since at $T_{X(max)}$ the power dissipation must be derated to zero. Strictly speaking, junction temperature does not properly classify as a maximum rating since it is not an external stress under direct control of the user (as opposed to power dissipation and external operating temperature which are). Thus, a more appropriate terminology for this rating would be maximum operating temperature. However, since it is a limiting factor in transistor dissipation capabilities and its use simplifies time-varying thermal analysis, the rating still appears on many transistor data sheets as a junction temperature rating.

E. Storage Temperature Rating

This rating defines the range of temperature over which the transistor may be stored (in the non-operating state) without damage. Because of possible electrical-temperature interactions, storage temperature range and operating temperature range do not necessarily coincide. However, in practice, they usually do coincide and in the absence of stated restrictions on operating range, storage temperature range may be taken as operating range also.

III. Electrical and Performance Characteristics

Electrical characteristics may be described as uniquely defined, measurable electrical properties of the transistor which are not a function of the measuring circuit or apparatus (except insofar as standard terminations and measurement accuracy are concerned). Performance, or operating characteristics are also electrical properties but they are, in general, not unique because their values depend upon the measuring circuit (in particular, the source and load impedance, which may be arbitrary). As might be expected, the terms are often used somewhat loosely (and sometimes interchangeably), especially in some cases where there are only subtle differences involved. The terms are generally used on transistor data sheets to segregate (for emphasis) under performance or operating characteristics those properties most directly applicable for the primary intended application.

A. Performance (Operating) Characteristics

Of the numerous performance characteristics which can be specified for high-frequency transistors, perhaps the most fundamental and pertinent characteristics are:

1. Power gain and noise figure, for small-signal applications;

2. Power gain, power output and efficiency, for large signal applications.

All of these characteristics are, of course, functions of frequency, bias temperature, etc., and to completely characterize a transistor over its full frequency, bias, and temperature ranges would be prohibitively costly. Consequently, characterization data is given only for restricted ranges of these variables. This data should portray sufficiently the capabilities of a particular device for its intended applications. As in the case of maximum ratings, some applications may require additional characterization by the user himself or through applications assistance from the manufacturer.

1. Power Gain

a. G_{max}

Of the various definitions for the measure of power flow in an active two-port device, such as a transistor, two are unique enough to allow specification without recourse to specifying the complete measuring circuit in detail. One of these definitions is termed Maximum Available Gain, G_{max}, and is the power gain obtained when the input and output ports are simultaneously conjugately matched to source and load impedances, respectively. Implicit in this definition is the assumption that the two-port is unconditionally stable, i.e., no combinations of input/output tuning can result in increasing gain to the point of oscillation.

b. $|S_{21}|^2$

The other unique power gain is the gain realized when the transistor is inserted between a source and a load with identical impedances (in practice usually 50 + j0 ohms). This particular insertion or transducer gain happens to coincide with the usual definition of the two-port forward scattering parameter, S_{21}. More precisely, it is equal to the magnitude squared of this parameter and is therefore often identified by the symbol

$|S_{21}|^2$.

For wideband applications,

$|S_{21}|^2$ is important since

wideband terminations “ not-too-different” from 50 ohms are more easily realized than are wideband transforming networks which provide the matching required for G_{max}.

2. Noise Figure
A common measure of the noise generated by an active two-port device, noise which sets a lower limit on amplifier sensitivity, is the noise factor, F. This is defined as:

$$F = \frac{\text{Input signal-noise ratio}}{\text{Output signal-noise ratio}} \quad (2)$$

or more generally as:

$$F = \frac{\text{Total output noise power}}{\text{Output noise power due to source resistance}} \quad (3)$$

At high frequencies, spot noise factor or noise factor for a small fractional bandwidth (say 1%) is used and is usually expressed as noise figure, NF, in decibels, i.e.,

$$NF = 10 \log F$$

As already discussed, noise figure is a function of source impedance (as well as functions of frequency, bias, etc.) and hence, there is an infinity of noise figures associated with a given device corresponding to the infinity of possible impedances which may be presented to the device input. The only unique one, in the sense that it does not involve arbitrary source impedances, is NF_{min}, the minimum noise figure obtained (at given bias and frequency) when the input is tuned to optimize this parameter. It is this noise figure which is usually given on Hewlett-Packard data sheets.

In practical amplifiers, involving more than one stage, overall noise factor F_O is given by:

$$F_0 = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_n - 1}{G_{(n-1)}} \quad (4)$$

where
n = number of stages
G_n = gain of the nth stage
F_n = noise factor of the nth stage.

This expression emphasizes the important fact that for low noise amplifiers, the first stage must be designed for the lowest noise figure and highest gain possible. (Note that the noise contribution of the second stage is divided [reduced] by the gain of the first stage). Since the optimum source impedance and bias currents for optimum gain and noise figure do not often coincide, very careful circuit design is required to minimize overall noise figure.

3. Power Output
This characteristic is important for both amplifier and oscillator transistors. In both cases, it is extremely circuit sensitive. For amplifiers, maximum useful output is often limited to that power output level at which gain has compressed 1 dB, an indicator of the upper limit on the linearity range. For oscillators, it is merely a quantitative measure of RF power for a given DC input power.

4. Efficiency
In the most general sense, this characteristic expresses as a percentage, the ratio of RF power output to the total circuit input power, both DC and RF. That expression is total efficiency, η_t , defined as:

$$\eta_t = \frac{P_O}{P_i + P_{DC}} \times 100 \quad (5)$$

where
P_O = RF output power
P_i = RF input power
P_{DC} = total DC power input

Power transistors are often characterized in terms of power added efficiency, η_{add} , defined as:

$$\eta_{add} = \frac{P_O - P_i}{P_{DC}} \times 100 \quad (6)$$

Since for oscillator transistors there is no RF power input, and for amplifier transistors the maximum input RF power is calculable from the power gain and power output specifications, the inclusion of P_i in efficiency is redundant. Moreover, since the major portion of the DC power is dissipated by the transistor collector, a more restricted definition of efficiency is pertinent. This parameter, termed collector efficiency, η_c, is given by:

$$\eta_c = \frac{P_O}{P_{CC}} \times 100 \quad (7)$$

where
P_{CC} = V_{CC} x I_{CC}
V_{CC} = collector supply voltage
I_{CC} = collector supply current

B. Electrical Characteristics
Electrical characteristics may be conveniently classified into two main types, DC and AC.

1. DC Characteristics
The importance of DC characteristics of high frequency transistors lies primarily in biasing and reliability considerations. However, certain DC characteristics are also directly related to high-frequency performance. For example, high-frequency noise figure is affected by the DC current gain. The DC characteristics which are discussed here are those usually found on high frequency transistor data sheets.

a. $V_{(BR)CBO}$, I_{CBO}
These two parameters serve to characterize the reverse-biased collector-base p-n junction and are defined as follows (with the aid of Figure 4a). The collector-base breakdown voltage, $V_{(BR)CBO}$, identifies the voltage at which collector current tends to increase without limit, usually due to the high electric field developed across the junction. This voltage sets a limit on the maximum transistor operating voltage and, as mentioned before under maximum ratings, usually is the basis for the collector-base maximum voltage rating. $V_{(BR)CBO}$ should be specified at a value of $I_C = I_{C1}$ in the figure, which is within the avalanche (or high slope) region of the reverse characteristic. Typical values of I_{C1} are in the 1 – 10 μA region for high frequency transistors.

To further define the quality of the reverse V-I characteristic a specification is usually placed on collector cutoff current, I_{CBO}, measured at some value of collector-base voltage less than $V_{(BR)CBO}$. For a good quality silicon junction (“sharp” instead of soft, see Figure 4a), I_{CBO} is in the nano-ampere range.

b. $V_{(BR)EBO}$, I_{EBO}
These two parameters characterize the reverse-biased emitter-base p-n junction in an analogous manner to the collector-base junction parameters $V_{(BR)CBO}$, and I_{CBO}, given above and are shown in Figure 4b. No further discussion will be given here.

c. $V_{(BR)CEO}$, I_{CEO}
The collector-emitter breakdown voltage and cutoff current are somewhat more complex in nature than either the collector-base or emitter-base parameters. In the

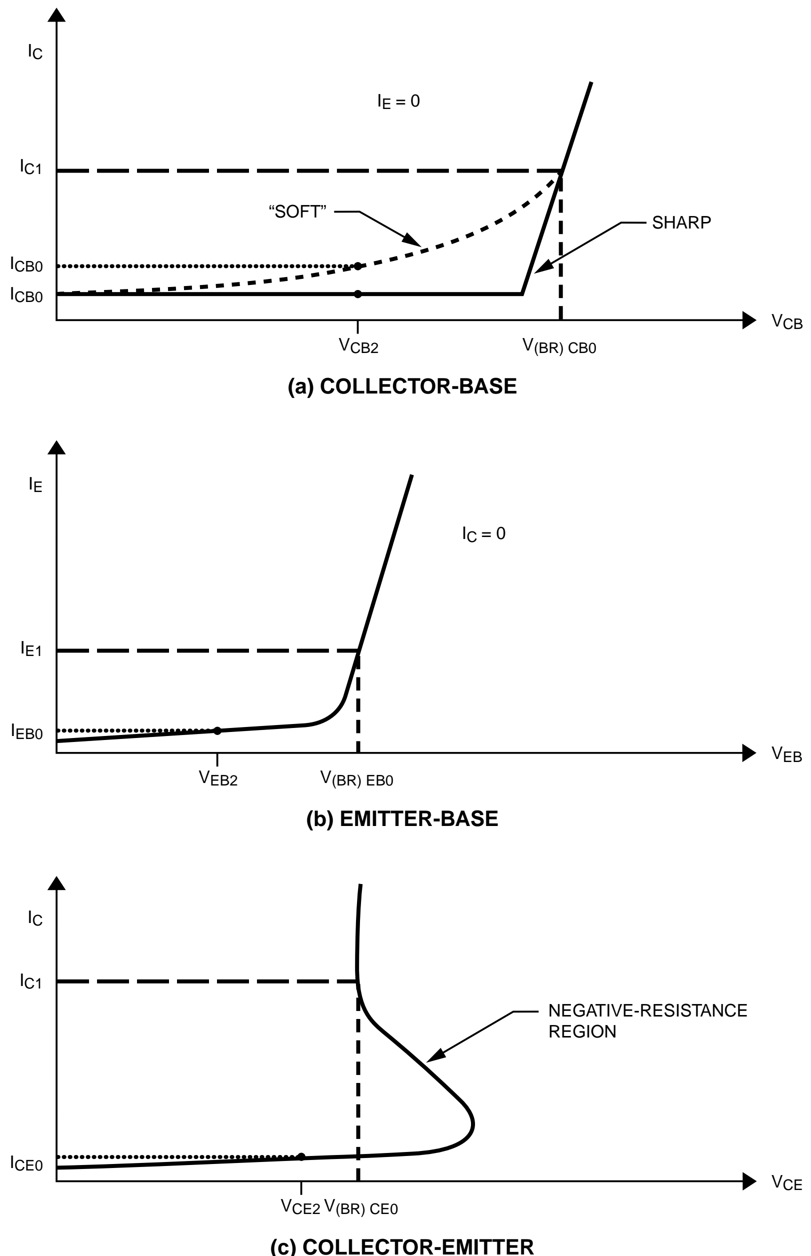


Figure 4. Transistor Reverse V-I Characteristics

latter two, only a single p-n diode is involved. In the collector-emitter case, two diodes are involved. Moreover, each is influenced by the other through transistor action, since the reverse current of the collector-base diode flows through the emitter-base junction as forward current. Thus the collector-base reverse current is amplified by the DC current gain of the transistor resulting in:

1) I_{CEO} being greater than I_{CBO} (for a given voltage).

2) Typically the familiar negative-resistance region in the V-I characteristic as shown in Figure 4c.

Consequently, $V_{(BR)CEO}$ is typically specified at collector currents one to three orders of magnitude higher than in the case of $V_{(BR)CBO}$ and $V_{(BR)EBO}$ in order to establish the minimum value of this characteristic.

d. h_{FE}
This parameter is simply the DC common-emitter current gain; i.e., the ratio of collector current to base current at some specified collector voltage and current.

2. AC Characteristics
Of the numerous AC characteristics which are defined for transistors, only relatively few are commonly used in characterizing high-frequency transistors. Some of the more pertinent parameters are briefly covered here.

a. S-Parameters
By far the most useful and conveniently measured set of two-port parameters for transistor high frequency (roughly 100 MHz and above) characterization is the S-parameter or scattering-matrix set. These parameters completely and uniquely define the small-signal gain and input/output immitance properties of any linear "black box". (By definition, a transistor or any active device is linear under small-signal conditions). However, these parameters reveal nothing (except possibly indirectly and approximately) about large-signal behavior or about noise behavior. Simply interpreted (more general definitions and other interpretations abound in the technical literature), the S-parameters are merely insertion gains, forward and reverse; and reflection coeffecients, input and output, with driven and non-driven ports both terminated in equal impedances, usually 50 ohms, real. Such an interpretation tends to make S-parameters very attractive, once some familiarity is gained, at high (especially microwave) frequencies, since the power flow or gain and reflection-coefficient concepts are more intuitively meaningful than voltage and current conceptual schemes. It should also be mentioned that S-parameters can be converted through straight-forward matrix transformations to other two-port parameter sets; e.g., h-, y-, or z-parameters.

Proceeding with more specific definitions, the S-parameters are defined analytically by:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \qquad (8)$$

or, in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (9)$$

where, referring to Figure 5:

a_1 = (incoming power at port 1) $^{1/2}$

b_1 = (outgoing power at port 1) $^{1/2}$

a_2 = (incoming power at port 2) $^{1/2}$

b_2 = (outgoing power at port 2) $^{1/2}$

E_1, E_2 = Electrical stimuli at port 1, port 2

From the figure and defining linear equations, for $E_2 = 0$, then $a_2 = 0$, and (skipping numerous rigorous steps) refer to Equation 10 below.

Equation 10 :

$$S_{11} = \frac{b_1}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{1/2}$$

$$= \frac{\text{Reflected Voltage}}{\text{Incident Voltage}} = \text{Input Reflection Coefficient}$$

$$S_{21} = \frac{b_2}{a_1} = \left[\frac{\text{Outgoing Output Power}}{\text{Incoming Input Power}}\right]^{1/2}$$

$$= \left[\frac{\text{Output Power}}{\text{Available Input Power}}\right]^{1/2} = \left[\text{Forward Transducer Gain}\right]^{1/2}$$

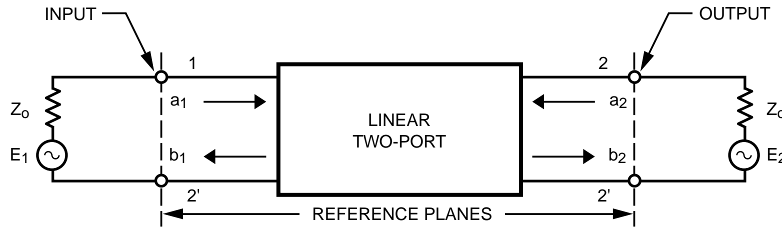


Figure 5. Two-port S-parameter Definition Schematic

or more precisely in the case of S_{21}:

Equation 11:

$$\text{Forward Transducer Gain} = G_{TF} = |S_{21}|^2$$
$$Z_i = Z_o$$

Similarly at Port 2 for $E_1 = 0$, then $a_1 = 0$, and

Equation 12:

$$S_{22} = \frac{b_2}{a_2} = \text{Output Reflection Coefficient}$$
$$S_{12} = \frac{b_1}{a_2} = \text{Reverse Transducer Gain}^{1/2}$$
$$G_{TR} = |S_{12}|^2$$

Since many measurement systems actually "read out" the magnitude of S-parameters in decibels, the following relationships are particularly useful:

Equation 13:

$$|S_{11}|_{db} = 10\log|S_{11}|^2 = 20\log|S_{11}|$$
$$|S_{22}|_{db} = 20\log|S_{22}|$$
$$|S_{21}|_{db} = 10\log|S_{21}|^2 = 20\log|S_{21}| = 10\log|G_{TF}| = |G_{TF}|_{db}$$
$$|S_{12}|_{db} = 10\log|S_{12}|^2 = 20\log|S_{12}| = 10\log|G_{TR}| = |G_{TR}|_{db}$$

b. Transition Frequency

One of the better known, but perhaps least understood, figures-of-merit for high-frequency transistors is the so-called transition frequency, f_T. Part of the misunderstanding which appears to exist is due to the use of a misleading (but common, for historical reasons) terminology of "short-circuit gain-bandwidth product" for this parameter.

By definition, f_T is that characteristic frequency described by the equation:

$$f_T = h_{fe} \times f_{meas} \quad (14)$$

where

h_{fe} = magnitude of small-signal common-emitter short-circuit current gain, h_{fe}

f_{meas} = Frequency of measurement, chosen such that:

$$2 \le h_{fe} \le \frac{h_{feo}}{2} \quad (15)$$

h_{fe} = the low frequency value of h_{fe}

To varying degrees of approximation, depending on transistor type, f_T is the frequency at which h_{fe} approximates unity. It is not, in general, the frequency at which h_{fe} is precisely equal to unity. To clarify these points further, consider the plot of h_{fe} against frequency sketched in Figure 6.

At low frequencies, $f \ll f_B$, h_{fe} is constant and equal to h_{feo}.

At f_B, h_{fe} has decreased to 0.707 h_{feo}; i.e., f_B is the 3 dB cutoff frequency for common-emitter short-circuit current gain, h_{fe}.

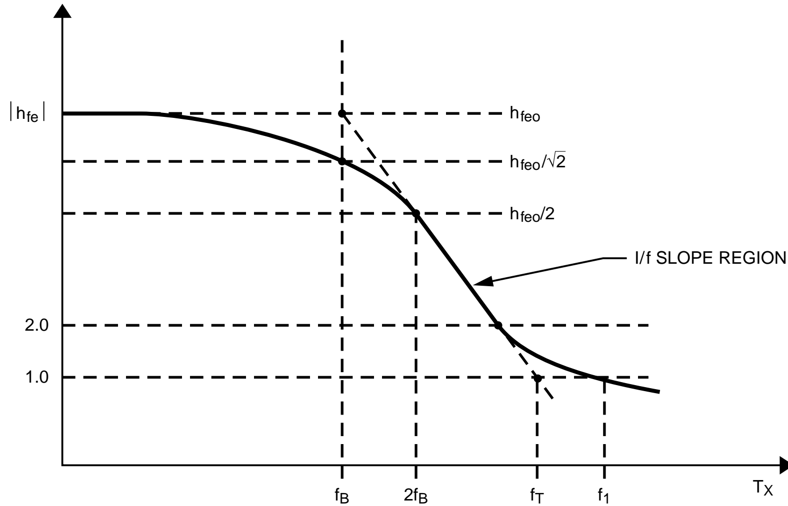


Figure 6. |hfe| Frequency Characteristics

For frequencies such that

$$2f_B < f < f_T$$

h_{fe} varies inversely proportional to frequency. That is, the f_T defining relationship holds:

$$h_{fe} \times f_{meas} = \text{constant} = f_t \qquad (16)$$

At frequencies approaching f_T, other parameters, especially package parasitics, can cause $|h_{fe}|$ to depart significantly from this 1/f variation. Therefore, the frequency, f_1, at which $|h_{fe}|$ actually equals unity can be somewhat different from f_T.

Applying this frequency-gain characteristic to common-emitter wide-band, low-pass amplifiers gives rise to the terminology of f_T being a "gain-bandwidth product". However, this is an optimistic approximation at best, since the product of low frequency circuit gain and the 3 dB cutoff frequency is reduced from f_T by an amount depending on circuit impedances.

The real significance of f_T lies in the fact that it is a measure of certain internal transistor parameters which do, in fact, affect high-frequency performance; for example, gain (though not in the convenient quantitative manner implied by the gain-bandwidth product terminology). In particular, good high-frequency noise performance requires that f_T be high. Thus, f_T is included on transistor data sheets as a figure of merit primarily, not as a parameter to be used directly in design.

c. Collector-Base Time Constant, $r_b'C_c$

This is an internal device parameter which relates only indirectly to high frequency performance. It is primarily a measure of internal feedback within the transistor. It also relates to transistor high-frequency impedance. As the name says (in symbols), it is a measure of transistor base resistance and collector capacitance in combination; however, except for certain low-frequency transistors, it cannot be considered the simple two-element lumped R-C time constant implied by the terminology. (In high frequency transistors, both base resistance and collector capacitance must be considered distributed when considered in detail). As a figure of merit, it is included on transistor data sheets to indicate how well base resistance and collector capacitance have been minimized. It also allows the estimation of certain gain properties of the transistor (see f_{max} parameter, following).

d. Collector-Base Capacitance, C_{cb}

This parameter is simply the total collector-base p-n junction capacitance measured at a low frequency (typically, 1 MHz) where it can be considered a single lumped element. For high-frequency transistors it is, of course, desirable that C_{cb} be small from bandwidth and stability considerations as well as from gain considerations alone.

e. Maximum frequency of Oscillation, f_{max}

This is another figure-of-merit parameter, as opposed to measurable parameters directly usable in the applications of transistors. Its importance stems from the following approximate relationships (which will not be derived here):

$$f_{max} \approx \left(\frac{f_T}{8\pi r_b' C_c}\right)^{1/2} \qquad (17)$$

$$G_{max} \approx \left(\frac{f_{max}}{f_{oper}}\right)^2 \qquad (18)$$

These expressions illustrate in a quantitative way the importance and the interrelationship between high f_T and low $r_b'C_c$ insofar as high frequency gain is concerned. However, since they are approximations and since their derivation

involves several assumptions not always valid, they must be interpreted with caution. For example, the expression for G_{max} is obviously not applicable at low frequencies since as $f \to 0$, $G_{max} \to \infty$, according to this expression. As a rule of thumb, the G_{max} expression is a reasonable approximation for frequencies such that,

$$5 > \frac{f_{max}}{f_{oper}} > 1 \qquad (19)$$

For accurate analysis of transistor gain and stability, a complete set of two-port parameters must be employed in exact expressions, such as those from which the approximations shown above were derived.

IV. Glossary of Microwave Transistor Terminology

$V_{(BR)CBO}$
Breakdown voltage of a reverse biased collector-base junction measured with the emitter open.

$V_{(BR)EBO}$
Breakdown voltage of a reverse biased emitter-base junction measured with the collector open.

$V_{(BR)CBO}$
Breakdown voltage between the collector and emitter terminals measured with the base open.

I_{CBO}
Leakage current of a reverse biased collector-base junction measured with the emitter open.

I_{EBO}
Leakage current of a reverse biased emitter-base junction measured with the collector open.

h_{fe}
DC common-emitter current gain.

C_{cb}
Collector-base junction capacitance measured with the emitter connected to the guarded terminal of a three terminal measurement system.

f_T
Transition Frequency. The frequency at which the magnitude of the small-signal common-emitter short-circuit current gain approximates unity.

$r_b'C_c$
The collector-base time constant.

f_{max}
Maximum frequency of oscillation. The frequency at which G_{max} approaches unity.

$P_{T(max)}$
Maximum continuous power dissipation below a reference temperature (usually 25°C).

$T_{J(max)}$
Maximum allowable transistor junction temperature.

$I_{C(max)}$
Maximum allowable collector current without destruction or degradation of the transistor.

NF
A measure of the noise generated by the transistor.

G_{max}
The maximum available power gain (MAG) when the transistor is unconditionally stable and input and output ports are sumultaneously conjugately matched.

S_{11}
Input reflection coefficient.

S_{12}
Reverse transfer coefficient.

S_{21}
Forward transfer coefficient.

S_{22}
Output reflection coefficient.

P_O
Amplifier – The power output at the one (1) db gain compression point.
Oscillator – A measure of the RF power output.

www.hp.com/go/rf
For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Copyright © 1998 Hewlett-Packard Co.

Obsoletes 300120

Printed in U.S.A. 5966-3085E (3/98)

HEWLETT® PACKARD

High-Frequency Transistor Primer

Part II

Noise and S-parameter Characterization

This is the second part of the Hewlett-Packard High Frequency Transistor Primer series. It is an introduction to the noise and S-parameter characterization of GaAs FET and silicon bipolar transistors for the microwave engineer. The contents are based on questions often received by HP application engineers.

The other parts of the High Frequency Transistor Primer series currently available are: Part I, *Electrical Characteristics* (of bipolar microwave transistors); Part III, *Thermal Properties* (of silicon bipolar and GaAs FET transistors); Part III-A, *Thermal Resistance* (of power FETs) and Part IV, *GaAs FET Characteristics*.

Copies of the Hewlett-Packard High Frequency Transistor Primer volumes are located on the world wide web at <http://www.hp.com/go/rf> under "Application Notes", or by calling one of the telephone numbers listed on the back page of this publication.

Table of Contents

Introduction 2
I. S-parameters 2
II. Functional Relationships 4
III. Stability 6
IV. Gain Contours 7
V. Noise Characterization 8
VI. Noise Contours 11
VII. Noise and Gain Contours 12
Summary 13
References 13

Introduction

This Primer is a short summary of the S-parameter and noise parameters commonly used on Hewlett-Packard transistor data sheets and their functional relationships to noise figure, gain, stability, impedance matching and other parameters necessary for high frequency circuit design. Much of this information has been published in various journals over the years. The intent of this primer is to provide a short, concise booklet containing the key functional relationships necessary for circuit design.

I. S-parameters

By far the most accurate and conveniently measured microwave two-port parameters are the scattering parameters. These parameters completely and uniquely define the small signal gain and the input/output emittance properties of any linear two-port network. Simply interpreted, the scattering parameters are merely insertion gains, forward and reverse, and reflection coefficients, input and output, with the driven and non-driven ports both terminated in equal impedances; usually 50 ohms, real. This type of measurement system is particularly attractive because of the relative ease in obtaining highly accurate 50 ohm measurement hardware at microwave frequencies.

Proceeding more specifically, S-parameters are defined analytically by:

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

or, in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where (referring to Figure 1):

a_1 = (Incoming power at Port 1)$^{1/2}$

b_1 = (Outgoing power at Port 1)$^{1/2}$

a_2 = (Incoming power at Port 2)$^{1/2}$

b_2 = (Outgoing power at Port 2)$^{1/2}$

E_1, E_2 = Electrical Stimuli at Port 1, Port 2

z_o = Characteristic Impedance = (50 + j0) Ohms

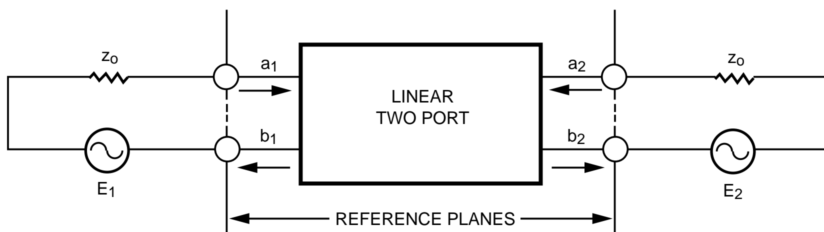


Figure 1. S-Parameters Definition Schematic

From Figure 1 and defining linear equations for $E_2 = 0$, then $a_2 = 0$, and:

$$S_{11} = \frac{b_1}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{1/2} \quad (1)$$

$$= \frac{\text{Reflected Voltage}}{\text{Incident Voltage}}$$

$$= \text{Input Reflection Coefficient}$$

$$S_{21} = \frac{b_2}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{1/2} \quad (2)$$

$$= [\text{Forward Transducer Gain}]^{1/2}$$

or in the case of S_{21}:

$$\text{Forward Transducer Gain} = |S_{21}{}^2| \quad (3)$$

Similarly at Port 2 for $E_1 = 0$, $a_1 = 0$:

$$S_{12} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Output Power}}\right]^{1/2} \quad (4)$$

$$= \frac{b_1}{a_2}$$

$$= \text{Reverse Transducer Gain}$$

$$S_{22} = \left[\frac{\text{Outgoing Output Power}}{\text{Incoming Output Power}}\right]^{1/2} \quad (5)$$

$$= \frac{b_2}{a_2}$$

$$= \text{Output Reflection Coefficient}$$

Since many measurement systems actually “read out” the magnitude of S-parameters in decibels, the following relationships are particularly useful:

$$|S_{11}|_{dB} = 10 \log |S_{11}|^2 = 20 \log |S_{11}| \quad (6)$$

$$|S_{22}|_{dB} = 20 \log |S_{22}| \quad (7)$$

$$|S_{21}|_{dB} = 20 \log |S_{21}| \quad (8)$$

$$|S_{12}|_{dB} = 20 \log |S_{12}| \quad (9)$$

Using scattering parameters, it is possible to calculate the reflection coefficients and transducer gains for arbitrary load and source impedance where the load and source impedances are described by their reflection coefficients Γ_L and Γ_S respectively:

$$S'_{11} = \frac{b_1}{a_1} = \frac{S_{11}(1-S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{1-S_{22}\Gamma_L}$$

$$= S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1-S_{22}\Gamma_L} \quad (10)$$

$$S'_{22} = \frac{b_2}{a_2} = \frac{S_{22}(1-S_{11}\Gamma_S) + S_{21}S_{12}\Gamma_S}{1-S_{11}\Gamma_S}$$

$$= S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1-S_{11}\Gamma_S} \quad (11)$$

$$\text{Transducer Power Gain} = \frac{\text{Power Delivered to Load}}{\text{Power Available from Source}}$$

$$= \left|\frac{b_2}{b_S}\right|^2 (1-|\Gamma_S|^2)(1-|\Gamma_L|^2)$$

$$= \frac{|S_{21}|^2 (1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|^2} \quad (12)$$

II. Functional Relationships

With this information, the functional relationships to gain, stability, input and output matching impedance can be readily derived from S-parameters. Since much of the literature[1, 2, 3] gives the complete derivation of these relationships, the mathematics of their derivation is omitted. Table 1 lists the most useful relationships required for circuit design.

Table 1.

1. Available Power Gain = $\dfrac{\text{Power Available from Network}}{\text{Power Available from Generator}}$

$$G_A = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{(1-|S_{22}|^2) + |\Gamma_S|^2(|S_{11}|^2 - |D|^2 - 2\,\text{Re}\,(\Gamma_S C_1)}$$

2. Stability

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}$$

3. Maximum Stable Gain

$$G_{msg} = \left| \frac{S_{21}}{S_{12}} \right|$$

4. Maximum Available Gain (for K>1)

$$G_{max} = \left| \frac{S_{21}}{S_{12}} (K \pm \sqrt{K^2 - 1}) \right|$$

5. Maximum Unilateral Power Gain

$$U = \frac{|S_{21}|^2}{(1 - |S_{11}|)^2 \ (1 - |S_{22}|)^2}$$

6. Source and Load Match for Maximum Available Power Gain

$$\Gamma_{ms} = C_1^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2|C_1|^2} \right]$$

$$\Gamma_{mL} = C_2^* \left[\frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2|C_2|^2} \right]$$

Use minus sign when B_1 or B_2 is positive, plus sign when B_1 or B_2 is negative.

where:

$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |D|^2$

$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D|^2$

$C_1 = S_{11} - D(S_{22}^*)$

$C_2 = S_{22} - D(S_{11}^*)$

$D = \det [s] = S_{11} S_{22} - S_{12} S_{21}$

Table 2. y and h Parameters in Terms of S-Parameters

$$y_{11} = \frac{S_{12}S_{21} + (1 - S_{11})(1 + S_{22})}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{22} = \frac{S_{21}S_{12} + (1 + S_{11})(1 + S_{22})}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Z_o^{-1}$$

$$h_{11} = \frac{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} Z_o$$

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$h_{12} = \frac{+2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$h_{22} = \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} Z_o^{-1}$$

III. Stability

A two port network is unconditionally stable if there exists no combination of passive load or source impedances which will allow the circuit to oscillate. In terms of S-parameters, unconditional stability is assured if the following equations are simultaneously satisfied:

$$| S_{11} | < 1 \tag{13}$$

$$| S_{22} | < 1 \tag{14}$$

$$\left| \frac{|S_{12}S_{21}| - |C_1^*|}{|S_{11}|^2 - |D|^2} \right| > 1 \tag{15}$$

$$\left| \frac{|S_{12}S_{21}| - |C_2^*|}{|S_{22}|^2 - |D|^2} \right| > 1 \tag{16}$$

Under these conditions, Rollett's Stability Factor, K > 1 and Maximum Available Gain is real and defined (Equation 4, Table 1):

When K < 1, the 2 port network is potentially unstable, but there may exist areas of the Γ_s and Γ_L plan in which the real part of the total

impedance in the input (or output) loop is positive and the network is conditionally stable. The regions of instability occur within the stability circles, the centers and radii of which are defined by,

rS_1 = Center of the stability circle on the input plane

$$= \frac{C_1^*}{|S_{11}|^2 - |D|^2} \quad (17)$$

RS_1 = Radius of stability circle on the input plane

$$= \left[\frac{|S_{12}S_{21}|}{|S_{11}|^2 - |D|^2}\right] \quad (18)$$

rS_2 = Center of the stability circle on the output plane

$$= \frac{C_2^*}{|S_{22}|^2 - |D|^2} \quad (19)$$

RS_2 = Radius of the stability circle on the output plane

$$= \left[\frac{|S_{12}S_{21}|}{|S_{22}|^2 - |D|^2}\right] \quad (20)$$

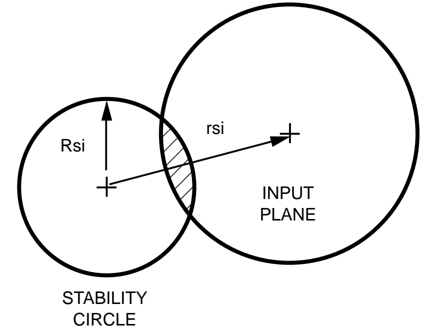


Figure 2.

Figure 2 is a typical example of the input plane of a conditionally stable network and the location of the stability circle. The shaded area represents the area of the input plane in which instability (or oscillation) occurs.

IV. Gain Contours

By manipulating Equation 1, Table 1, circles of constant power gain can be generated in the Γ_s plane.

Equation 1, Table 1, may be expressed as:

$$G_A = |S_{21}|^2 \, G_1 \quad (21)$$

where

$$G_1 = \frac{|1 - |\Gamma_S|^2|}{(1 - |S_{22}|^2) + |\Gamma_S|^2(|S_{11}|^2 - |D|^2) - 2\mathrm{Re}\Gamma_S C_1} \quad (22)$$

The radius and location of a constant G_1 gain circle is given by:

$$r_g = \frac{(1 - 2K|S_{12}S_{21}|\, G_1 + |S_{12}S_{21}|^2\, G_1^2)^{1/2}}{1 + M_1G_1} \quad (23)$$

$$R_g = \left(\frac{G_1}{1 + M_1G_1}\right) C_1^* \quad (24)$$

where

$$M_1 = |S_{11}|^2 - |D|^2 \quad (25)$$

Figures 3 and 4 are typical examples of gain contour plots on a Smith chart. In this case, the contours are of a typical AT-41435 transistor measured at 2 GHz and 4 GHz; since K >1 and the transistor is unconditionally stable, the maximum available gain is uniquely defined at a single point.

To realize the specified gain for any arbitrary Γ_S, the output matching impedance is obtained by conjugately matching S'_{22} (Equation 11) or

$$\Gamma_L = \left[S_{22} + \frac{S_{21} S_{12}\, \Gamma_S}{1 - S_{11}\, \Gamma_S} \right]^* \tag{26}$$

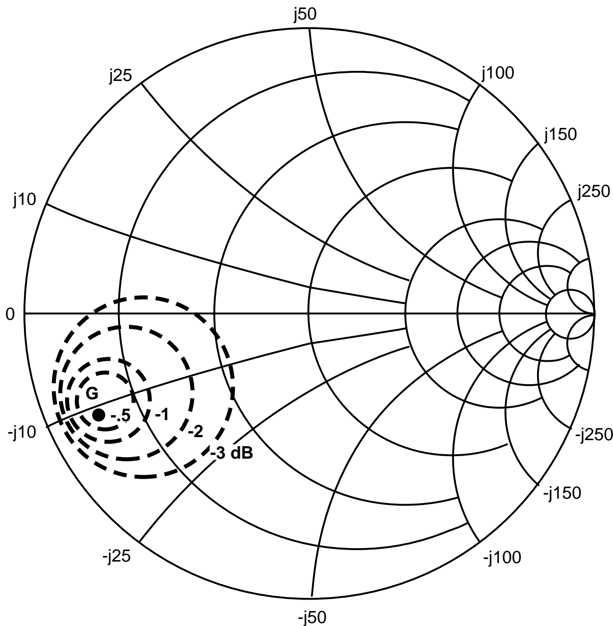


Figure 3. Constant Gain vs. Source Impedance – AT-41435
Frequency = 2 GHz, V_{CE} = 8 V, I_C = 10 mA, MAG = 16.3 dB, Γ_{ms} = 0.84, -160

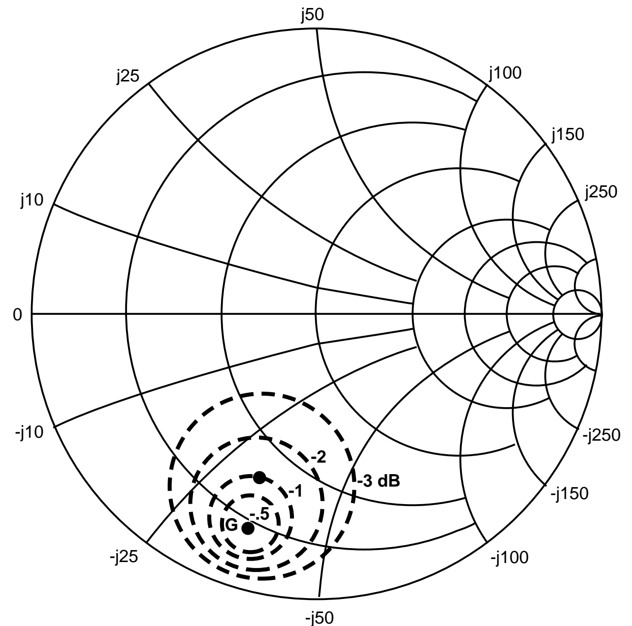


Figure 4. Constant Gain vs. Source Impedance – AT-41435
Frequency = 4 GHz, V_{CE} = 8 V, I_C = 10 mA, MAG = 10.6 dB, Γ_{ms} = 0.84, -111

V. Noise Characterization

While S-parameters completely define the stability, gain and power matching conditions of a linear two port network, they are not sufficient to describe the noise behavior of a noisy, linear, two port network such as a small signal transistor. Another set of parameters, namely noise parameters, are required in addition to S-parameters to describe the noisy linear two port.

The noise figure of a linear two port network as a function of source admittance may be represented by: [3]

$$F = F_{OPT} + \frac{R_n}{G_S} \left[(G_{OPT} - G_S)^2 + (B_{OPT} - B_S)^2 \right] \tag{27}$$

where:

$G_s + jB_s$	=	the source admittance presented to the input of the two port
$G_{opt} + jb_{opt}$	=	the source admittance at which optimum noise figure occurs
R_n	=	an empirical constant relating the sensitivity of the noise figure to source admittance, with dimensions of resistance

It may be noted that for an arbitrary noise figure measurement with a known source admittance, Equation (27) has four unknowns, F_{opt}, R_n, G_{opt}, and B_{opt}. By choosing four known values of source admittance, a set of four linear equations is formed and the solution of the four unknowns can be found.

Equation (27) may be transformed to:

$$F = F_{OPT} + \frac{R_n |Y_{OPT}|^2}{G_S} - 2R_n G_{OPT} + \frac{R_n |Y_S|^2}{G_S} - 2R_n B_{OPT} \left(\frac{B_S}{G_S}\right) \quad (28)$$

or,

$$F = F_{OPT} + \frac{R_n}{G_S} \bullet |Y_S - Y_{OPT}|^2$$

Let,

$$X_1 = F_{OPT} - 2R_n G_{OPT} \quad (29)$$

$$X_2 = R_n - |Y_{OPT}|^2 \quad (30)$$

$$X_3 = R_n \quad (31)$$

$$X_4 = R_n B_{OPT} \quad (32)$$

Then the generalized equation may be written as:

$$F_i = X_1 + \frac{1}{G_{Si}} X_2 + \frac{|Y_{Si}|^2}{G_{Si}} X_3 - 2\left(\frac{G_{Si}}{B_{Si}}\right) X_4 \quad (33)$$

Or, in matrix form:

$$[F] = [A] [X] \quad (34)$$

and the solution becomes:

$$[X] = [A]^{-1} [F] \quad (35)$$

These parameters completely characterize the noise behavior of the two port network. Direct measurement of these noise parameters by this method would be possible only if the receiver on the output of the two port were noiseless and insensitive to its input admittance. In actual practice, the receiver itself behaves as a noisy two port network and can be characterized in the same manner. What is actually being measured is the system noise figure of the two port and the receiver.

The two port noise figure, however, can be calculated using the system formula:

$$F_{1i} = F_{(Sys)i} - \frac{F_2 - 1}{G_{1i}} \tag{36}$$

Where:

F_{1i} = Two port noise figure when driven from the ith source admittance
F_2 = Second stage noise figure (or receiver noise figure)
$F_{(sys)i}$ = System noise figure when driven from the ith source
G_{1i} = Available gain of the two port when driven from the ith source.

It is important to note that F_2 is assumed to be independent of the impedance of the first stage two port, which means that an isolator must be inserted between the first stage two port and the receiver. Thus, it becomes apparent that to do a complete two port noise characterization, the system noise characterization, the receiver noise characterization, and the gain of the two port must be measured. In addition, any losses in the input matching networks must be carefully accounted for, because they add directly to the measured noise figure reading.

Figure 5 shows a generalized block diagram of a typical noise figure setup used to obtain noise parameters.

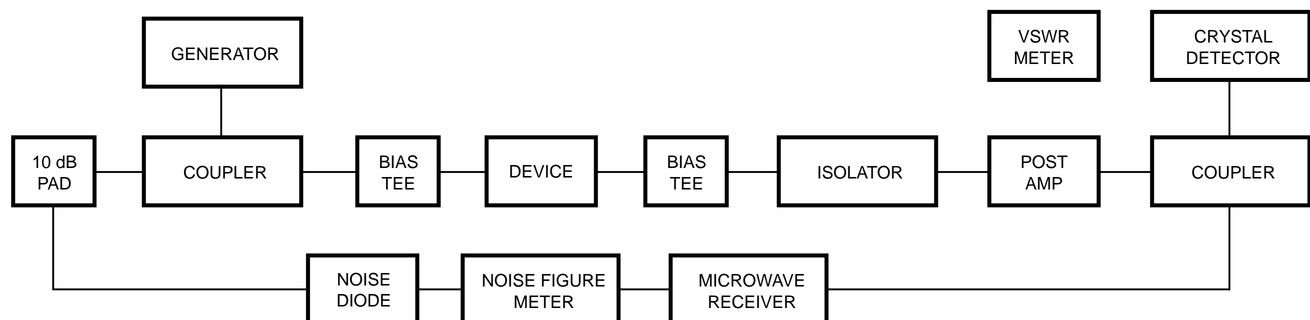


Figure 5.

VI. Noise Contours

Noise figure can be graphically presented on a Smith chart of the input plane much the same as gain. This graphical representation can be presented in the impedance plane (Z plane), admittance plane (Y plane) or reflection coefficient plane (Γ plane), all of which can be functionally related to each other. Since the noise parameters were derived in terms of admittance parameters, the noise contours will be derived in terms of normalized admittance parameters, which may be easily converted into the Z plane by a 180° angular rotation.

If we define the normalized admittances as:

$$y_S = g_S + jb_S = \frac{1}{Y_o}(G_S + jB_S) \quad (37)$$

$$y_{OPT} = g_{OPT} + jb_{OPT} = \frac{1}{Y_o}(G_{OPT} + jB_{OPT}) \quad (38)$$

where: Y_o is the real characteristic admittance of the input transmission line.

From the literature[3] it can be shown that the center of the circle of constant noise figure ($F_i \geq F_{OPT}$) is:

$$R_{Fi} = \frac{\left[(1 - g^2_{OPT} - b^2_{OPT})^2 + 4b^2_{OPT}\right]^{1/2}}{(1 + g_{OPT})^2 + b^2_{OPT} + 2\,\delta_{Fi}} \quad (39)$$

where:

$$\delta_{Fi} = \frac{F_i - F_{OPT}}{2\,R_n\,Y_o} \quad (40)$$

The angle of the vector is:

$$\theta = \tan^{-1}\left[\frac{2b_{OPT}}{1 - g^2_{OPT} - b^2_{OPT}}\right] \quad (41)$$

The radius of the circle of constant noise figure is given by:

$$r_{Fi} = \frac{2N_i}{(1 + g_{OPT})^2 + b^2_{OPT} + 2\,\delta_{Fi}} \quad (42)$$

when:

$$N_i = \frac{1}{Y_o}\left[\frac{G_{OPT}}{R_n}(F_i - F_{OPT}) + \frac{1}{4\,R_n^2}(F_i - F_{OPT})^2\right]^{1/2} \quad (43)$$

Figure 6 shows a typical plot of noise figure of the AT-41435 transistor plotted in the impedance plane.

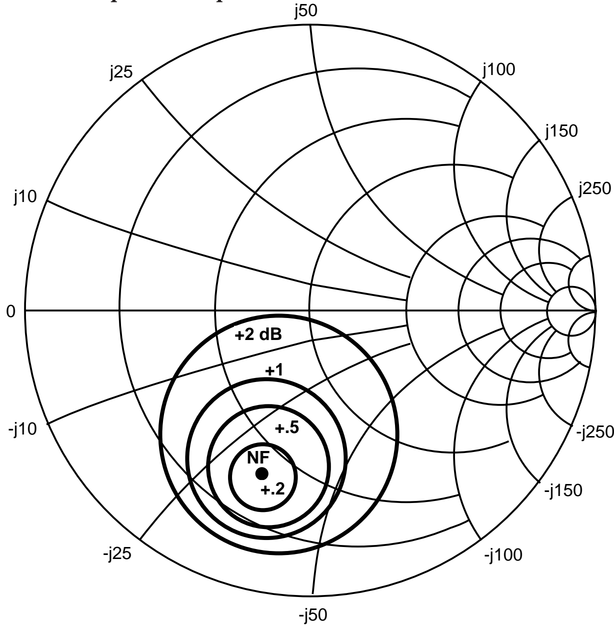


Figure 6. Constant Noise Figure vs. Source Impedance – AT-41435
Frequency = 4 GHz, V_{CE} = 8 V, I_C = 10 mA, NF_O = 3.0 dB, Γ_O = 0.64, -111

VII. Noise and Gain Contours

All practical amplifiers involve more than one internal noise generator, and as a result have an optimum noise source which is not the same as the optimum gain source. From a practical point of view, it becomes desirable to know what the tradeoffs between noise figure and gain involve. This tradeoff is best shown by plotting both the gain and noise circles on the same chart.

By taking the gain contours developed in Section IV and the noise contours developed in Section VI and superimposing them on the same Smith chart, the gain and noise figure tradeoffs become readily apparent.

Figure 7 shows the noise and gain contours of the AT-41435 transistor plotted in the input impedance plane.

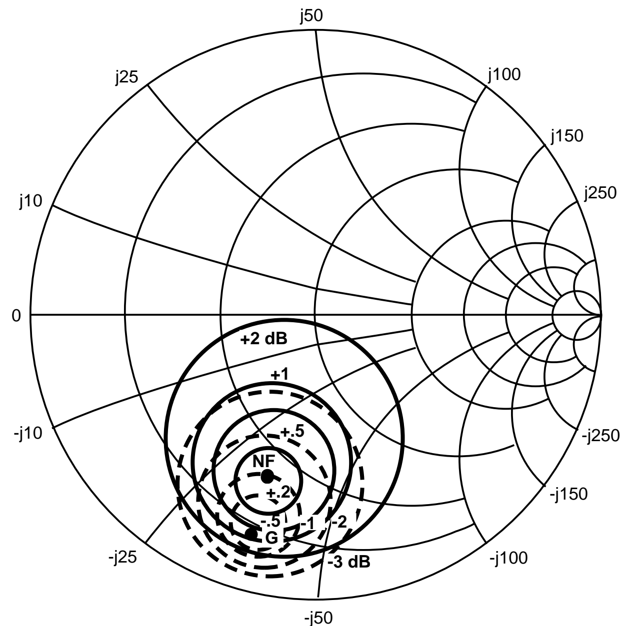


Figure 7. Constant Noise Figure and Gain vs. Source Impedance – AT-41435
Frequency = 4 GHz, V_{CE} = 8 V, I_C = 10 mA, NF_O = 3.0 dB, Γ_O = 0.64, -111, MAG = 10.6 dB, Γ_{ms} = 0.84, -111

With this chart, the circuit designer can easily pick the input matching conditions which will result in the optimum compromise for simultaneously meeting gain, VSWR and noise figure requirements.

Again, to realize the specified gain for any arbitrary point on the input plane, the output matching impedance is obtained by conjugately matching S'_{22} (Equation 11):

$$\Gamma_L = \left[S_{22} + \frac{S_{21} S_{12} \Gamma_S}{1 - S_{11} \Gamma_S} \right]^* \tag{44}$$

Summary

In the previous sections of this booklet, the basic techniques for developing a graphical display of the input plane of a noisy linear two port network have been described, and a number of specific examples were shown. This technique may be used to graphically describe any noisy linear two port network at any microwave frequency, provided that the following parameters are known at the desired frequency and, in the case of a transistor, at the desired bias conditions.

S_{11}, S_{21}, S_{12}, S_{22}, F_{OPT}, Y_{OPT}, R_n

References

1. Kurokawa, K., IEEE Trans. MTT, March 1965

2. Bodway, G.E., Two Port Power Flow Analysis Using Generalized Scattering Parameters, Microwave Journal, Vol. 10, No. 6, May 1967.

3. Fukui, H., Available Power Gain, Noise Figure and Noise Measure of Two Ports and Their Graphical Representation, IEEE Trans. on CT, Vol. CT- 13, No. 2, pp 137-142.

www.hp.com/go/rf

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Copyright © 1993 Hewlett-Packard Co.

Obsoletes 5091-8350E (7/93)

5968-1411E (9/98)

HEWLETT PACKARD

High Frequency Transistor Primer
Part III

Thermal Properties

Table of Contents

I. Thermal Resistance 1
A. Definition 1
B. Calculation of Thermal Resistance 2
II. Thermal Time Constant 6
III. Measurement of Thermal Resistance 8
IV. General Comments on Thermal Ratings 10
V. Appendix 11
A. Summary of Symbols 11
B. References 11

Preface

This is the third part of the Hewlett-Packard High Frequency Transistor Primer series. It is intended as an introduction to the thermal characteristics of GaAs FET and silicon bipolar transistors for the microwave engineer. The contents are based on the questions most often asked of members of the HP transistor group.

Using the information in this primer should enable the engineer to make the basic calculations necessary to assure that the transistors he uses will be operated at a safe temperature for long term reliability. Further discussion on the subject of transistor thermal characteristics and heat flow calculations is provided in the literature referenced in the appendix.

The other parts of the High Frequency Transistor Primer currently available are:
Part I, ***Silicon Bipolar Electrical Characteristics***;
Part II, ***Noise and S-Parameter Characterization***;
Part IIIA, ***Thermal Resistance*** and
Part IV, ***GaAs FET Characteristics.***

I. Thermal Resistance

A. Definition

A transistor, bipolar or FET, has a maximum temperature which cannot be exceeded without destroying the device or at least shortening its life. The heat is generated in a bipolar transistor directly under the emitters and very close to the upper surface of the die. In the microwave FET heat is also dissipated near the surface, under the gate and near the drain end. For all practical purposes, the heat can be considered as generated on the top surface of the chip or die.

The ability of a transistor to dissipate heat depends upon a factor called the thermal resistance, which may be designed as θ, or θ_{th} or R_{th}. It is defined as follows:

Temp. Rise $\triangleq$ Power Dissipated x Thermal Resistance

$$\Delta T = P_D \theta \qquad (1a)$$

$$\theta \triangleq \frac{\Delta T}{P_D} \qquad (1b)$$

Note that θ has the dimensions of °C/watt. The reciprocal of thermal resistance is thermal conductance. Equation 1a can be used to

calculate the temperature rise at the surface of a chip due to P_D watts being dissipated, with the bottom of the chip held at a constant temperature. Junction temperature, T_j, is given as:

$$T_j = T_A + \text{Temp. rise due to heating}$$
$$T_j = T_A + P_D\theta \quad (2a)$$

where T_A is ambient temperature.

Figure 1 shows a cross section of a chip on a mount. As can be seen, there are actually three thermal resistances involved, and

$$T_j = T_A + P_D\left(\theta_{chip} + \theta_{solder} + \theta_{mount}\right) \quad (2b)$$

Note that the thermal resistances add just like electrical resistances in series. We will now see how thermal resistance is calculated.

B. Calculation of Thermal Resistance

All materials will conduct heat to some degree, some much better than others. Silver is the best metallic heat conductor and plastics tend to be relatively poor heat conductors. BeO (beryllia) is the best ceramic heat conductor and is often used in high power transistor packages.

When thermal resistance is calculated, the physical size and placement of the chip and mount are all important. There are two general cases for thermal resistance [1].

Case I - "Columnar" Heat Flow (Figure 2)*

Figure 2 shows that if the thickness of the material is small compared to the lateral dimensions of the device and die, the heat will flow in a vertical "column." The thermal resistance is then:

$$\theta_{col} = \frac{F}{K_{TH}\,\text{Area}} = \frac{F}{K_{TH}\,4CD} \quad (3a)$$

Example:
A silicon transistor 20 x 20 mils is fabricated on a die 50 mils square and 5 mils thick. Then 2D = 2C = 20 mils, 2B = 2A = 50 mils, and F = 5 mils.

$$\frac{F}{B} = \frac{5}{25} = 0.2; \frac{F}{D} = \frac{5}{10} = 0.50 \quad (3b)$$

Heat flow is, therefore, essentially columnar. See Equation 3c.

Equation 3c:

$$20\text{ mils} = 0.051\text{ cm}$$
$$\text{Let } K_{TH} = 1.0\text{ W/cm°C}$$
$$5\text{ mils} = 0.0127\text{ cm}$$
$$\theta = \frac{0.0127}{1.0\left(0.051\right)^2} = 4.88\text{ °C/W}$$

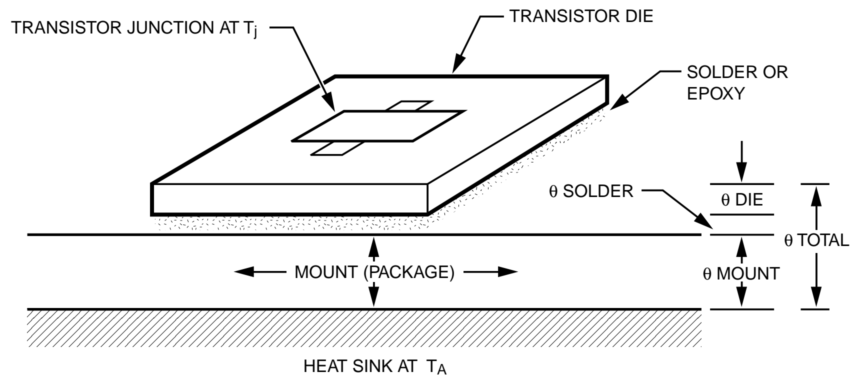


Figure 1. Transistor Thermal Resistances

Table 1. Thermal Conductivity (K_{TH}) of some Materials used in Transistors

Material	K_{TH} W/cm°C
Silicon	1.00 – 1.46
GaAs (Gallium Arsenide)	0.44
Copper	4.05
Gold	3.09
Kovar	0.2
Sapphire	0.25
Al_2O_3 (Aluminum Oxide)	0.188
BeO (Beryllium Oxide)	2.34
Silver	4.14

*The notation using a 2X multiplier for the dimensions is consistent with the figures in the reference.

Case II - "Spreading" Heat Flow (Figure 3)
If the material is thick compared to the device size, and the device dimensions are less than 20% of the die side dimension, then flow is said to be essentially spreading.

Figure 3 illustrates this case and shows how the heat "spreads out" instead of flowing in a vertical column. For this case:

$$\theta_{sp} = \frac{1}{K_{TH}\pi r}, r = \frac{C+D}{2} \qquad (4)$$

Note that r is the radius of a circle whose diameter is the average of the transistor dimensions.

Most transistor dimensions fall into a range of values which are intermediate between spreading and columnar flow, and the general equations for heat flow in 3 dimensions, X, Y, and Z, must be solved using the three-dimensional Laplace equation:

$$\frac{\partial^2 T}{\partial X^2} + \frac{M^2 T}{\partial Y^2} + \frac{M^2 T}{\partial Z^2} = 0 \qquad (5a)$$

Linstead and Surty [2] solved Eq. 5a for a number of different geometries and presented the results in a series of normalized charts (Figures 4, 5, 6). The use of these charts can be demonstrated as follows. The dimensional notation corresponds to Figure 3.

The dimensions of a representative transistor are 1.1 x 3.0 mils; the die is 10 mils square and about 5 mils thick. Therefore, in Figure 5:

$$\begin{aligned} 2A = 2B = 0.01" &= 0.0254\ \text{cm} \\ 2D = 0.003" &= 0.00762\ \text{cm} \\ 2C = 0.0011" &= 0.0028\ \text{cm} \\ F = 0.005" &= 0.0127\ \text{cm} \end{aligned}$$

$$\frac{A}{F} = 1,\ \frac{A}{B} = 1,\ \frac{C}{A} = 0.11,\ \frac{D}{C} \cong 3 \qquad (5b)$$

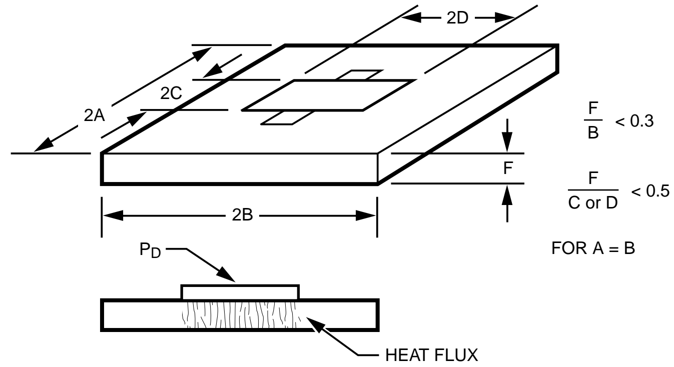


Figure 2. Columnar Heat Flow

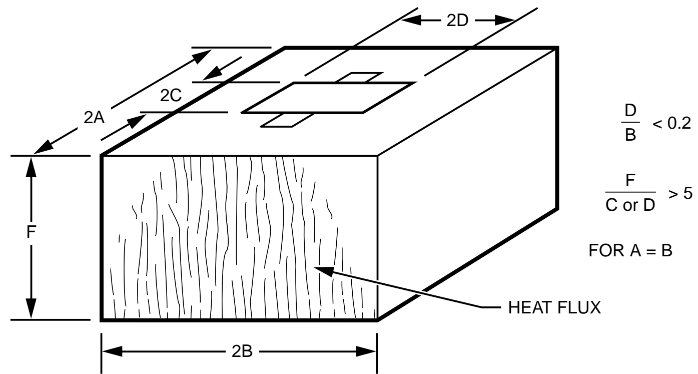


Figure 3. Spreading Heat Flow

In Figure 5, at C/A 0.11 and on the A/F = 1 curve read

$$\frac{\theta K_{TH} CD}{F} = 0.046 \qquad (5c)$$

Therefore resulting in Equation 5d, shown below.

Equation 5d:

$$\theta = \frac{0.046F}{K_{TH}CD} = \frac{0.046\left(0.0127\right)}{1.00\left(0.0014\right)\left(0.0038\right)} = 109°C/W$$

The thermal resistance for an FET cannot be calculated from the charts of Linstead and Surty since the heat source is a long thin line, not a small rectangle. Thermal resistance for a long thin line can be approximated by the analogy between fringing capacitance for an electrical conductor and thermal heat flow spreading. Since the capacitance per unit length of a transmission line is (120 πε)/Zo, formulas for transmission line characteristic impedance may be used to calculate thermal resistance. Using the formula for stripline characteristic impedance given by Cohn [3] and the equivalent ideal line as shown by Oliver [4], one can derive the following equation for FET thermal resistance:

$$\theta W_g = \frac{K(k)}{2\,K_{TH}\left(K(k')\right)}^{*} \qquad (6)$$

Where:

$$k = \operatorname{sech}\left[\frac{\pi L_g}{4F}\right] \qquad (7)$$

$$k' = \tanh\left[\frac{\pi L_g}{4F}\right] \qquad (8)$$

K = complete elliptic integral of 1st kind
L_g = gate length in cm
F = die thickness in cm ≅ 0.0125 cm
W_g = gate width in cm
K_{TH} ≅ 0.44, for GaAs

Using these numbers, θW_g has been calculated for gate lengths of 0.1 to 4 μm and is shown in Figure 7. Thermal resistance for three FETs has been calculated and is shown in Table 2.

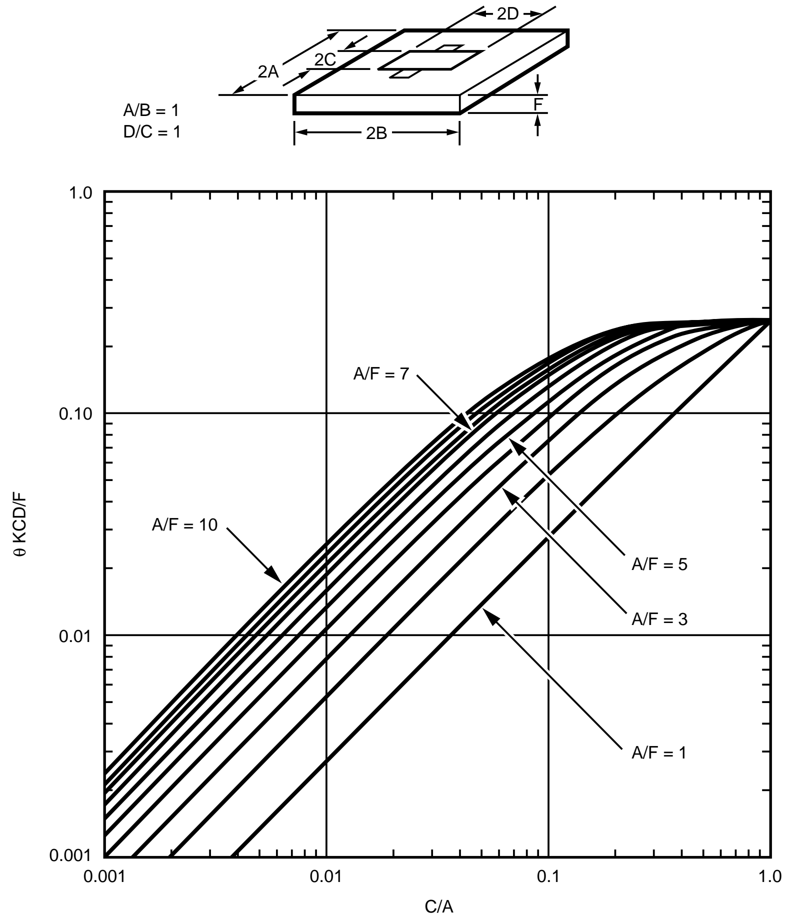


Figure 4. Thermal Resistance Curves

Thermal resistance curves for semiconductor chips from R.D. Linstead and R.J. Surty, “IEEE Transactions on Electron Devices,” Volume - ED- 19, No. 1, January 1972, pp. 41-44, Reproduced courtesy of the Institute of Electrical and Electronics Engineers. (Figures 4, 5, 6)

* Equation 6 is valid for single line gates. Devices with multiple gates (such as power FETs) could have a higher thermal resistance. This is because the gates are thermally “coupled,” i.e., there is heat - transfer between gate segments.

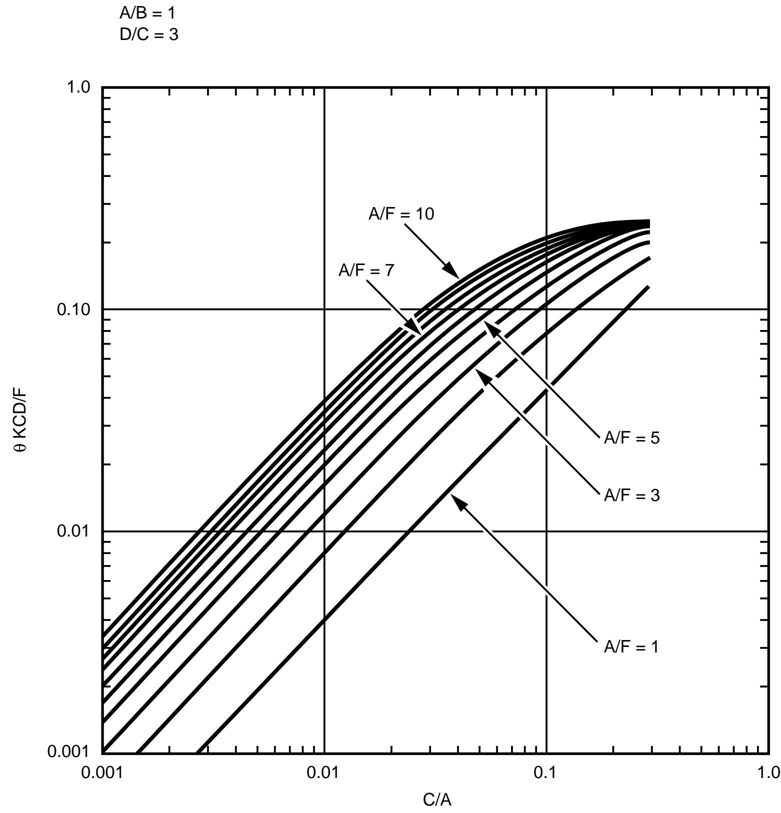


Figure 5. Thermal Resistance Curves

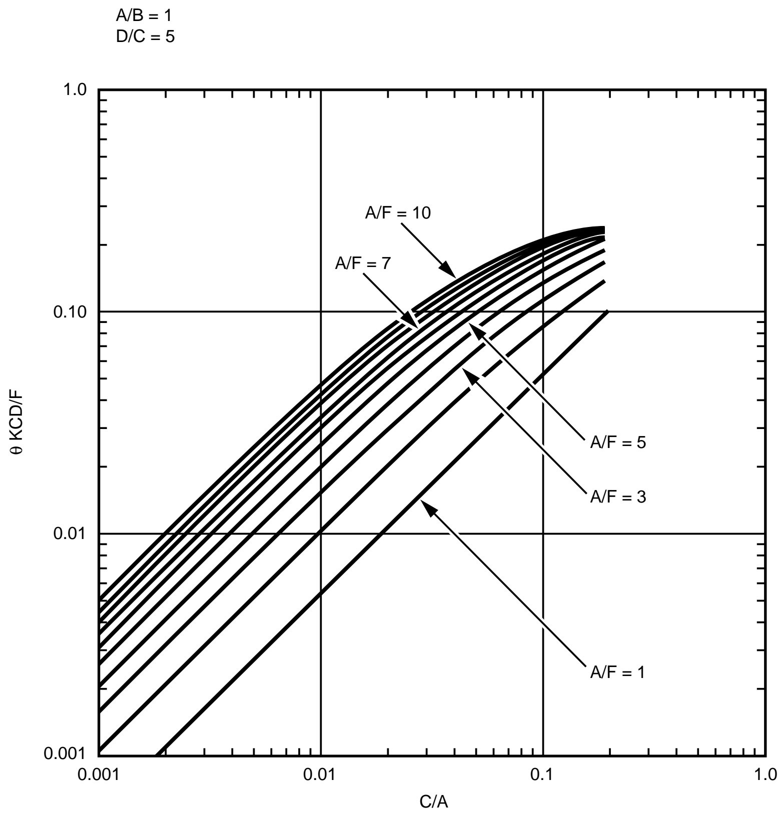


Figure 6. Thermal Resistance Curves

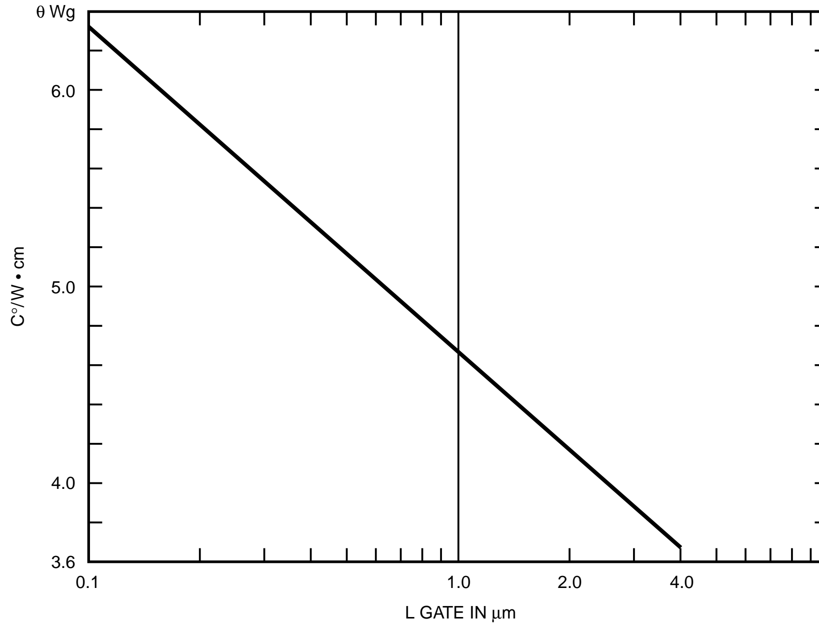


Figure 7. Thermal Resistance x Gate Width vs. Gate Length for GaAs FETs on 5 mil Thick Die

Table 2. Thermal Resistance Calculated for Two Different FETs

Device	L_g (µm)	W_g (µm)	θWg From Fig. 7 (°C cm/ W)	θ (°C/ W)
ATF-13	0.5	250	5.17	206
ATF-10	0.5	500	4.68	93.6

II. Thermal Time Constant

If a pulse of power is supplied to a semiconductor device, the temperature of the junction does not rise instantaneously. In other words, the die has a thermal time constant. Figure 8a illustrates the effect; 8b shows the electrical analog of several time constants in cascade (i.e., in series).

Semiconductor junction temperature as a function of time can be given as shown in Equation 9: *

Equation 9:

$$T_j = P_D\theta\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{t}{\tau}\right]^{1/2} + T_A \text{ for } t < \tau$$

τ = thermal time constant

τ = time

Note that the temperature is proportional to the square root of time and, thus, the RC analog is not exact. It has also been found that Eq. 9 is only accurate during the early part of the pulse, and is not correct for the entire duration, particularly near the end as the temperature approaches equilibrium, i.e., as t approaches τ.

The thermal time constant can be estimated by:

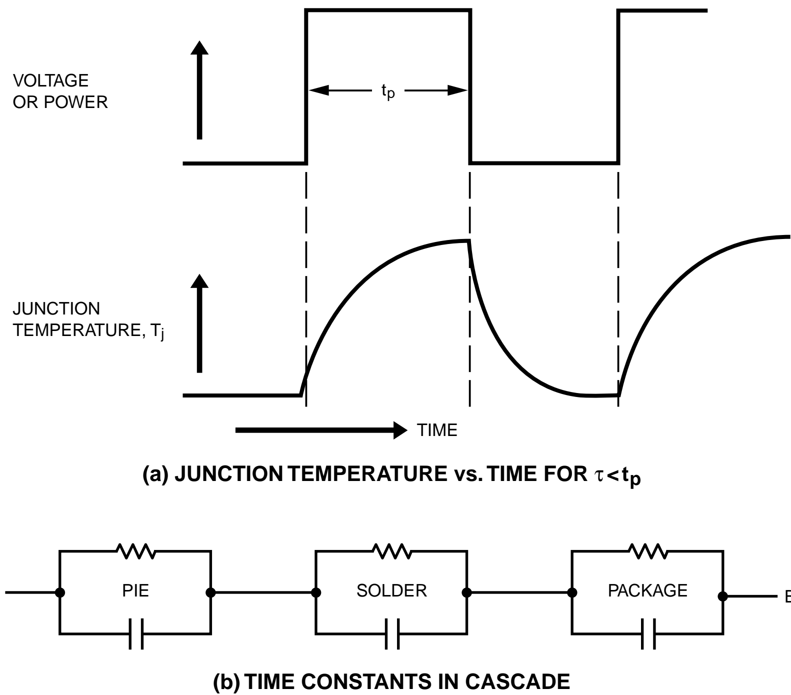
$$\tau = \left[\frac{2F}{\pi}\right]^2\left[\frac{\rho C}{K_{TH}}\right] \qquad (10a)$$

Where:

F = die thickness
ρ = density of semiconductor
K_{TH} = thermal conductivity
C = specific heat of semiconductor

The constant $\rho C / K_{TH}$ will be calculated for two semiconductors, silicon and GaAs.

* This is Eq. (9.64a) in reference [1].



(a) JUNCTION TEMPERATURE vs. TIME FOR $\tau < t_p$

(b) TIME CONSTANTS IN CASCADE

Figure 8. Thermal Time Constants

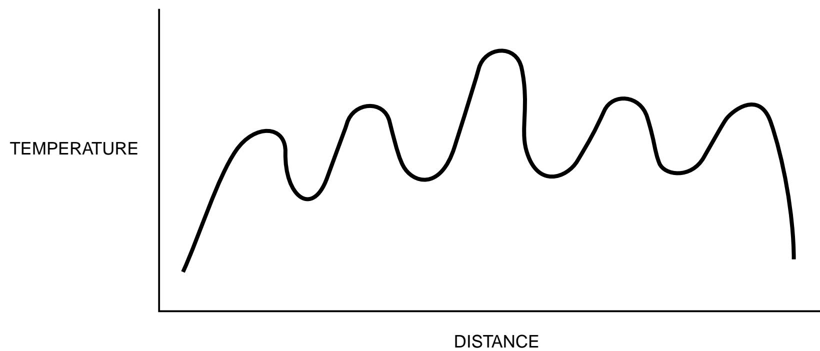


Figure 9. Temperature vs. Distance Across A Large Multi-finger Die

1. Silicon (Si)

Equation 10b:

$$\rho = 2.33\ \text{gr/cc}$$
$$C = 0.7\ \text{J/gr°C} \triangleq 0.7\ \text{W-sec/gr°C}$$
$$K_{TH} \cong 1.00\ \text{W/cm°C}$$
$$\text{Then } \frac{\rho C}{K_{TH}} = \frac{2.33 \times 0.7}{1.0} = 1.63\ \text{sec/cm}^2$$

2. Gallium Arsenide (GaAs)

Equation 10c:

$$\rho = 5.31\ \text{gr/cc}$$
$$C = 0.35\ \text{J/gr°C} \triangleq 0.35\ \text{W-sec/gr°C}$$
$$K_{TH} \cong 0.44\ \text{W/cm°C}$$
$$\text{Then } \frac{\rho C}{K_{TH}} = \frac{5.31 \times 0.35}{0.44} = 4.22\ \text{sec/cm}^2$$

The following examples of a pulsed *silicon* transistor will show the importance of the thermal time constant.

Let:

θ	= 50°C/W
T_A	= 25°C
P_D	= 5 watts, peak
F	= 5 mils = 0.0125 cm

Use the following pulse lengths:

(1)	10 µsec
(2)	100 µsec
(3)	C.W.

Calculate τ, the thermal time constant:

$$\tau = \left[\frac{2F}{\pi}\right]^2 \left[\frac{\rho C}{K_{TH}}\right] = \left[\frac{2(0.0125)}{\pi}\right]^2 1.63$$
$$= 103\ \mu s = 1.03 \times 10^{-4}\ \text{sec}$$

Then:
a.

$$T_j = 5(50)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-5}}{1.03\times10^{-4}}\right]^{1/2} + 25$$
$$= 56 + 25 = 81°\text{C for a pulse length of } 10\ \mu\text{sec} \quad (10e)$$

Or:
b.

$$T_j = 5(50)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-4}}{1.03\times10^{-4}}\right]^{1/2} + 25$$
$$= 202°\text{C for a pulse length of } 100\ \mu\text{sec} \quad (10f)$$

Or:
c.

$$T_j = 5(50) + 25$$
$$= 275°\text{C for CW}$$

Note that a Gallium Arsenide device under otherwise the same conditions would have a much higher temperature.

$$\theta = 50\left[\frac{1}{0.44}\right] = 113°\text{C/W}$$
$$\tau = 103\left[\frac{4.22}{1.63}\right] = 267\ \mu\text{sec} \quad (10g)$$

1. Therefore, with a 10 µsec pulse:

Equation 10h:

$$T_j = 5(113)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-5}}{2.67\times10^{-4}}\right]^{1/2} + 25$$
$$= 103°\text{C}$$

2. Or, with a 100 µsec pulse:
T_j = 248°C

3. Or, under CW conditions:

T_j = 113 x 5 + 25 = 590°C

The result above shows that pulses short compared to τ give a very small temperature rise, while the long pulses result in a temperature rise closer to the CW condition. Pulse lengths greater than 2τ result in essentially the CW temperature.

III. Measurement of Thermal Resistance

There are two basic approaches to the measurement of θ, the thermal resistance. A method considered by some to be the most basic uses an infrared scanner to measure the surface temperature by its infrared emission. This system has both advantages and disadvantages.

Infrared Measurement of θ
Advantages:
1. Reads peak, not average, locates "hot spot" temperature to 0.3 mil accuracy.
2. Can give temperature profiles of larger devices.

Disadvantages:
1. High cost.
2. Slow
3. Destructive (uses constant emisivity coating on die)

A temperature profile of a large device will be similar to Figure 9 where the temperature peaks occur at the emitters.

The second method of temperature measurement depends on the temperature dependence of the forward voltage across a diode. This can be emitter-base voltage of a bipolar or the gate-source voltage of an FET.

For a bipolar transistor:

$$I_E = A_e q n_i^2 \frac{D_B}{N_B}\left[\exp\frac{qV_{be}}{kT_j} - 1\right] \quad (11)$$

Where:

I_E	= emitter current
V_{be}	= emitter-base voltage
V_j	= temperature
A_e	= emitter area
n_i, D_B, N_B	= material constants

Using the previous example geometry (equation 5a), V_{be} is found to have a slope ≅ 1.6 MV/°C for I_E = 1 mA.

Therefore, by measuring V_{be} the junction temperature can be determined. The temperature thus measured is an *average* and does not indicate the peak temperature as the thermal scan method can.

Measuring temperature by the ΔV_{be} method is very simple. The device to be tested is biased to a constant low "measuring" current; e.g., 1 mA. It is then momentarily pulsed to a higher current (pulse

length >>τ). V_{be} is then measured immediately after the device returns to the lower current condition. The delay should be less than 1% τ. V_{be} is then compared to the low current “cold” value.

$$\theta = \frac{\Delta T}{\Delta P_D} = \frac{\frac{1}{mV/C} \bullet (\Delta V_{be})^*}{VI_{Hi} - VI_{meas}} \quad (12a)$$

* in mV

Equation 12b:

$$\theta = \frac{°C}{mV} \times \frac{\Delta V_{be}}{\Delta P_D} = \frac{1}{1.6} \times \frac{704 - 653}{(0.03 - 0.001)10} = 110°C/W$$

For example, our example geometry is pulsed from 1 mA and 10 volts to 30 mA and 10 volts. V_{be} changes from 0.704 volts (cold) to 0.653 volts (hot). Note that the temperature reduces V_{be} ; current increases V_{be} .

Calculate θ as shown in Equation 12b.

The instrumentation for the measurement includes a pulse generator, oscilloscope (with Tektronix type W plug-in), and power supply. Figure 10 shows simplified test setups for bipolar and FET transistors. Note that in the case of the FET, the gate bias is negative in the higher power dissipating mode and positive in the measuring mode.

Hewlett-Packard uses a θ_{jc} test set to measure ΔV_{be} semi-automatically on both types of transistors. The test set uses a sample-and-hold circuit to remember V_{be} and displays it on a digital voltmeter. Thus, for special applications, devices can be screened individually for θ_{jc} .

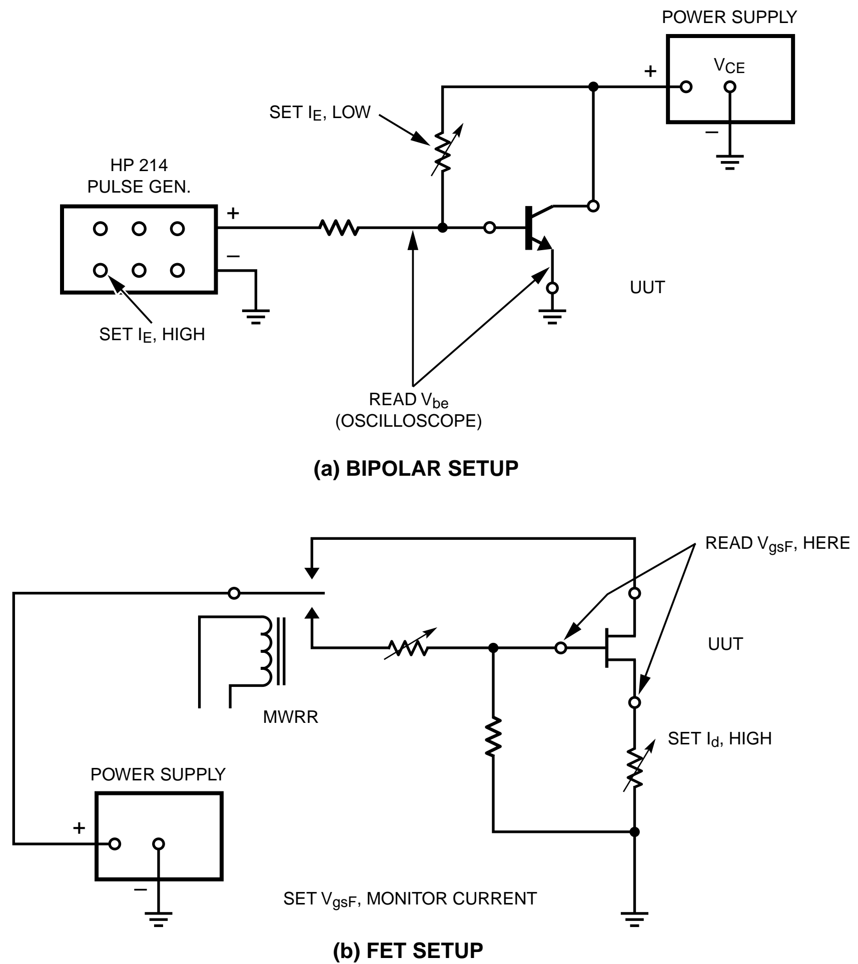


Figure 10. Simplified Test Setups for Measuring Thermal Resistance of (a) Bipolar Transistors and (b) FETs

IV. General Comments on Thermal Ratings

The thermal resistance may be stated in a number of ways, the most common of which is θ_{jc} , the thermal resistance between the junction and the external case (or package). It includes:

$$\theta_{jc} = \theta_{die} + \theta_{solder} + \theta_{case} \quad (12c)$$

The free air thermal resistance is much higher since the case is not tied to a sink, but must lose heat by radiation and convection. If heat sinking is provided through the leads only, then θ has a value between θ_{jc} and θ free air.

Derating curves are determined as follows: The maximum dissipation in the case of a bipolar transistor is determined from what is called the “safe operating area.” Within that area the VI product is such that secondary breakdown will not occur. The maximum dissipated power is then computed from this characteristic and would always be less than the maximum voltage times the maximum current. A typical value for P_{Dmax} for a small-signal microwave transistor is 100 – 200 mW.

Figure 11 shows a derating curve. P_{max} is determined from the safe operating area as explained above. The maximum junction temperature is determined from reliability studies and can vary depending upon the MTBF desired. A value of 200°C is typical for silicon bipolar transistors. The breakpoint in the curve is where the junction is at 200°C and the power is P_{max} ; i.e.,

$$T_x = 200 - P_{Dmax}\theta \quad (12d)$$

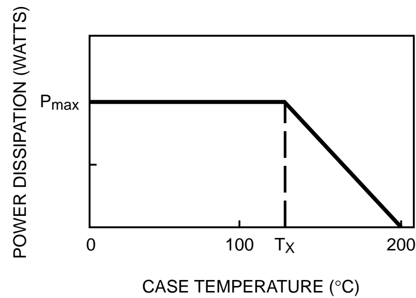


Figure 11. Power Derating Curve

When the temperature of the case is greater than T_x , the dissipation is no longer determined by the safe operating area but is a function of the thermal resistance and the maximum junction temperature.

For microwave FETs, the value for maximum channel temperature is typically between 150°C and 200°C. It will usually correspond to an MTBF on the order of 10^5 hours.

Appendix

A. Summary of Symbols

Symbol	Description	Units
ΔT	temperature rise	°C
P_D	power dissipation	watts
θ	thermal resistance	°C/watt
T_j	junction temperature	°C
T_A	ambient temperature	°C
K_{TH}	thermal conductivity	watts/cm • °C
L	gate length (of the FET)	cm
F	die (chip) thickness	cm
τ	thermal time constant	seconds
t	time	seconds
ρ	density of material	gram/m^3
c	specific heat	watt sec/gram • °C
t_p	pulse width	seconds
I_E	emitter current	amperes
V_{be}	emitter-base voltage	volts
A_e	emitter area	cm^2
n_i	intrinsic carrier density	cm^{-3}
D_B	diffusion constant for minority carriers in the base	$cm^2\ sec^{-1}$
N_B	free carrier density in the base	cm^{-3}

B. References

1. Pritchard, R.L.; *Electrical Characteristics of Transistors*, McGraw-Hill, New York, 1967; Chapter 9.4

2. Linstead, R.D. and Surty, R.J.; “Steady State Junction Temperature of Semiconductor Chips.” *IEEE Transactions on Electron Devices*, Vol. ED-19, No.1, Jan. 1972; pp. 41-44.

3. Cohn, S.B.; *IRE Transactions on Microwave Theory and Techniques*, Vol. MTT-2, No. 2, July 1954; pp. 52-57.

4. Oliver, A.A.; *IRE Transactions on Microwave Theory and Techniques*, Vol. MTT-3, March 1955; pp. 134-143.

www.hp.com/go/rf

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Copyright © 1998 Hewlett-Packard Co.

Obsoletes 300124

Printed in U.S.A. 5966-3084E (3/98)

HEWLETT® PACKARD

High-Frequency Transistor Primer

Part III-A

Thermal Resistance

A Guide to Understanding, Measuring, and Applying Power FET Thermal Resistance Coefficients

Table of Contents

I. Introduction 2

II. A Brief Look at Thermal Resistance and Its Measurement 2

A. What is thermal resistance? 2

B. Why thermal resistance is an important parameter 3

C. How is thermal resistance measured? 3

D. Interpreting the data 4

E. Problems with manufacturers' thermal resistance specifications 4

III. The Liquid Crystal Measurement Technique 5

A. Introduction 5

B. How it works 5

C. How to use it 6

D. Some tips for practical measurements 9

1. False transition points 9
2. Variation of thermal resistance with temperature 9
3. θ_{jc} vs. V_{ds} with P_d constant 10
4. Thermal cycling 10
5. Thermal equilibrium 10

E. Some results 10

F. Comparison with other methods 14

G. Summary 14

IV. The Delta V_{gs} Technique 15

A. Introduction 15

B. Principle of operation 15

C. Thermal time constants 17

1. Calculation of thermal time constants 17
2. Experimental determination of thermal time constants 19

D. Corrections to raw delta V_{gs} data 21

E. Automation of delta V_{gs} measurements 23

F. Summary 25

Appendix A. Thermal Resistance Data for HP IMFET Internally Matched FETs 26

Appendix B. Using Thermal Resistance Data: Some Practical Examples 26

1. Formula for temperature correction of θ_{jc} using Kirchoff's transformation 26
2. Example 1: Determination of maximum heatsink temperature 28
3. Example 2: Determination of maximum channel temperature 29
4. Comparison of calculated and measured θ_{jc} vs. temperature 30

Appendix C. Kirchoff 's Transformation 31

References 34

Acknowledgements 36

NOTE:
Not all Hewlett-Packard part numbers mentioned herein may be available. Contact your HP representative for current product offerings.

I. Introduction

The operating temperature of a microwave power FET is an important factor affecting both RF performance and service lifetime (MTTF). Accurate determination of device channel temperatures under working conditions is essential to the power amplifier designer. With a knowledge of ambient temperature, DC bias conditions, and RF power levels, channel temperature may be calculated using the thermal resistance (θ_c) factor.

A common error is to assume that θ_{jc} is a constant. In fact, thermal resistance varies as a function of device temperature, DC bias levels, and device geometry. Processing and assembly variations are also a factor. Channel temperature calculations which assume an invariant thermal resistance may give values far from the actual operating temperature.

Thermal resistance is one of the most important parameters given in a transistor data sheet, but it is often specified ambiguously, resulting in a value which is of little or no practical use to the device user. The majority of manufacturers' data sheets give values for θ_{jc} without specifying either the measurement techinque used or related test conditions. Thermal resistance values may vary by a factor of two or more depending on these associated parameters.

If the unwary designer uses a value of thermal resistance without knowing under what conditions it was measured, both the performance and the reliability of the final design may suffer.

This paper attempts to clarify the test techniques and definitions used by Hewlett-Packard to specify the thermal resistance of its microwave power devices. Useful information is provided to allow our customers to accurately calculate both the thermal resistance and channel temperature of our devices under the operating conditions they will experience during actual use.

II. A Brief Look At Thermal Resistance and Its Measurement

A. What is Thermal Resistance?

The thermal resistance factor may be used to compute the channel temperature of a FET under a given set of operating conditions, i.e., case (flange) temperature, DC bias, and RF power level.
Thermal resistance, illustrated in Figure II-1, is defined as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. II-1)}$$

where:

θ_{jc} = channel to case thermal resistance (°C per watt)
T_{ch} = channel temperature (highest or average) (°C)
T_c = case or flange temperature (°C)
P_d = power dissipated by the device, which is equal to the DC input power plus RF input power - RF output power (watts)
= $V_{DS} \times I_{DS} + P_{IN} - P_{OUT}$

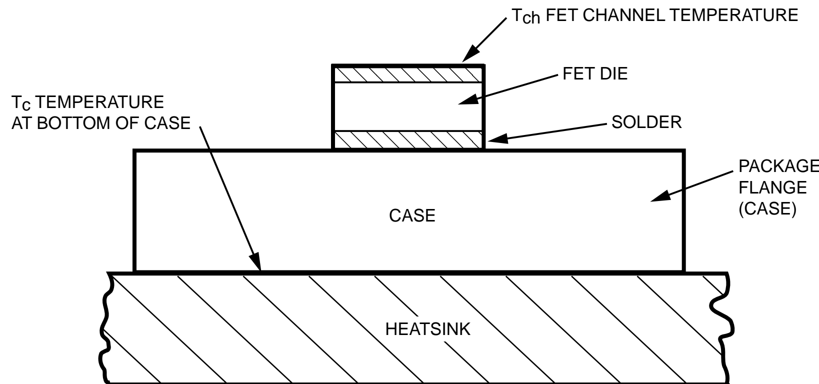


Figure II-1. Power FET Channel-To-Case Thermal Resistance

For power devices the surface of the case (flange) in contact with the heatsink is assumed to be at a constant temperature. The channel temperature, on the other hand, may vary from point to point along the active surface. This is a very important consideration as it implies that one may have more than one value of thermal resistance for the same device, measured under the same conditions, depending on the definition of channel temperature used.

At HP, we specify the so-called "hot-spot" values of thermal resistance. These values are measured using the channel temperature measured at its hottest point (a spot several µm in diameter). The advantages of using this definition will be discussed later.

B. Why is Thermal Resistance an Important Parameter?
As mentioned before, thermal resistance may be used to compute device channel temperatures when given DC, RF, and case temperature conditions. The service lifetime of the device is a strong function of channel temperature. Manufacturers typically supply plots of mean-time-to-failure vs. channel temperature for their devices.

RF performance is also affected by operating temperature. When operating FETs at elevated case temperatures, degradations in gain, efficiency, and power output must be considered.

C. How is Thermal Resistance Measured?
Several methods are used to measure thermal resistance values in both R&D laboratory and production environments. In the laboratory the number of devices evaluated is small and measurement accuracy is of prime importance. Infrared microscopy and the liquid crystal technique are commonly employed. On the production floor large numbers of sealed devices must be tested using a quick, non-destructive measurement technique. The delta V_{gs} method satisfies both these requirements.

Infrared microscopy[II-1,2,3] is one of the most widely used techniques for determining thermal resistance. A specialized microscope fitted

with infrared optics is used to detect IR emissions from the device under test (DUT). The IR radiation passes through focusing lenses onto a detector which produces an electrical output proportional to the magnitude of the IR input.

This technique is capable of ±0.5 degree Celsius accuracy and has an imaging spot size of about 15 microns in diameter. A disadvantage of this method is that the DUT must be coated with a constant emissivity coating such as lampblack. Computer driven systems are becoming available which alleviate the need for coating the sample. [II-4]

The liquid crystal technique uses a thin coating of temperature sensitive nematic crystals on the surface of the DUT to measure temperatures. A specially equipped optical microscope is used to determine channel temperatures by observing changes in the polarization of light reflected from the DUT.

Temperature accuracy is ± 0.5 degrees Celsius, and hot spots smaller than two microns can be resolved. This excellent resolution is useful in detecting small hot spots.

The delta V_{gs} method [II-5], unlike the other two precedures mentioned above, does not require coating the DUT with any sort of material. Thermal resistances are determined using the (almost linear) temperature dependent voltage drop across the gate-source diode while in forward conduction. The rapid speed, ability to test sealed devices, and non-destructive nature of this test make it ideal for production line testing. The delta V_{gs} technique is not intended for use in making absolute measurements of θ_{jc}. Rather, it is used as an indicator of die to case attach quality.

D. Interpreting the Data

It is important to realize that each of the aforementioned test techniques will yield different values of thermal resistance for the same device. An obvious precursor to interpreting data from thermal resistance testing is understanding the nature of the measurement techniques. To this end, the following sections of this application note present detailed information on both the liquid crystal and delta V_{gs} techniques.

A common misconception is that thermal resistance is a constant. This is not so! Both theory and measurements show it to be a function of device bias conditions and temperature. This application note presents both theoretical calculations and measurement data which may be used to apply the data from thermal resistance testing to determine temperatures which the device will encounter under typical operating conditions.

E. Problems with Manufacturers' Thermal Resistance Specifications

A look at power FET data sheets from several manufacturers will show that thermal resistance numbers are given without any mention of either the measurement technique used or related test conditions.

Thermal resistance measurements performed using the delta V_{gs} method may yield values several times lower than those determined using the liquid crystal technique. Device bias and temperature conditions also affect thermal resistance. Without the aforementioned information, it is difficult to compare the thermal performance of devices from different manufacturers.

At Hewlett-Packard, we specify the so-called “hot-spot” thermal resistance, measured using the liquid crystal technique. This is the most useful measure of thermal resistance as it permits the amplifier designer to determine the maximum channel temperature with a minimum of effort. The high temperature accuracy and good spatial resolution of this measurement technique coupled with the ability to perform measurements under actual device operating conditions assure realistic values of thermal resistance.

III. The Liquid Crystal Measurement Technique

A. Introduction

The liquid crystal technique finds use in laboratory applications where very fine spatial resolution and good absolute temperature accuracy are required. The spatial resolution afforded by this technique exceeds that of the more commonly used infrared method by more than an order of magnitude. Temperature may be measured to within ±0.5 degrees Celsius. The exceedingly fine spatial resolution makes possible the detection of very small (2 μm diameter) hot spots.

B. How It Works

The liquid crystal method makes use of the properties of several types of temperature sensitive bi-refringent nematic crystals. As shown in Figure III-1, the nematic-intrinsic (N-I) transition temperature, the molecules which make up the material form an orderly (nematic) array. When the transition temperature is reached or exceeded the molecules take on random (isotropic) orientations. This N-I temperature is dependent on the molecular structure of each type of nematic crystal.

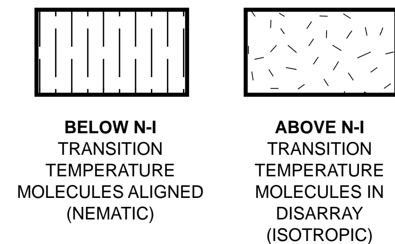


Figure III-1. The Temperature Dependent State of Liquid Crystal Molecules

This effect is utilized as follows: assume that light with a uniform linear polarization is directed towards a sample whose surface has been coated with a thin layer of nematic crystals. Let us view the reflected light from the sample through a polarizing plate which we will call the analyzer as shown at the top of Figure III-2.

If the sample is below the transition temperature, the molecules will be in an orderly (nematic) array. In this state the material is bi-refringent. Reflected light from the surface of the material will contain components polarized in two directions. Since the analyzer cannot simultaneously cancel both components, it will have little effect on the intensity of the reflected light and the sample will appear relatively bright.

Next, assume part of the sample is heated to or above the transition temperature. The crystal molecules will move into a random (isotropic) arrangement. Reflected light will have a uniform linear polarization. If

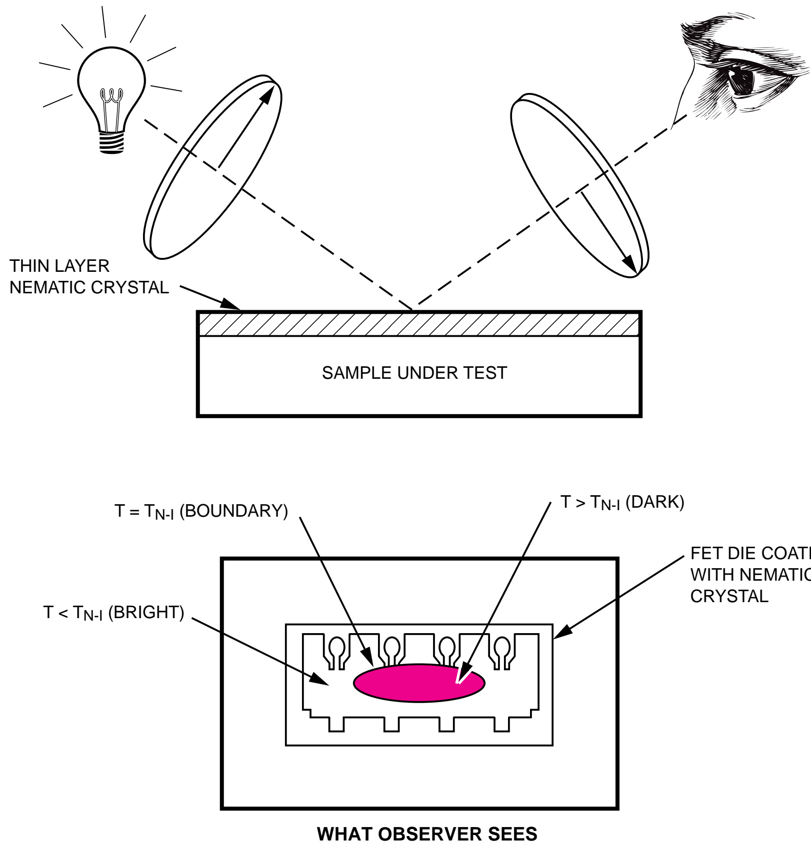


Figure III-2. Simplified Liquid Crystal Viewing

the analyzer is oriented correctly, almost all of the reflected light will be attenuated. Thus, that part of the DUT which is at or above the N-I transition temperature will appear dark, as shown at the bottom of Figure III-2.

C. How To Use It

A diagram of a typical setup used to perform liquid crystal testing is shown in Figure III-3. An optical microscope is equipped with two polarizing plates; a fixed orientation polarizer is located just after the light source and a rotatable analyzer is located in the path of the light reflected from the device under test (DUT).

A hot/cold plate is placed on top of the microscope stage to bring the DUT to the desired testing temperature. DC power supplies are used to apply bias to the device. A camera may be used to record heating patterns of the DUT. Figure III-4 shows a photograph of the liquid crystal test setup used at Hewlett-Packard.

Nematic crystals with N-I transition temperatures ranging from 50 to 240 degrees Celsius may be obtained from several manufacturers*. The material is typically supplied in powdered form.

Figure III-5 shows the steps necessary to prepare and apply a liquid crystal solution to the DUT. First, a small quantity of nematic crystal

---

*
E. Merck Laboratories
500 Executive Blvd.
Elmsford, NY 10523

Eastman Kodak Co.
Rochester, NY 14650
1-800-225-5572
(Technical Information)
1-800-225-5352 (Orders)

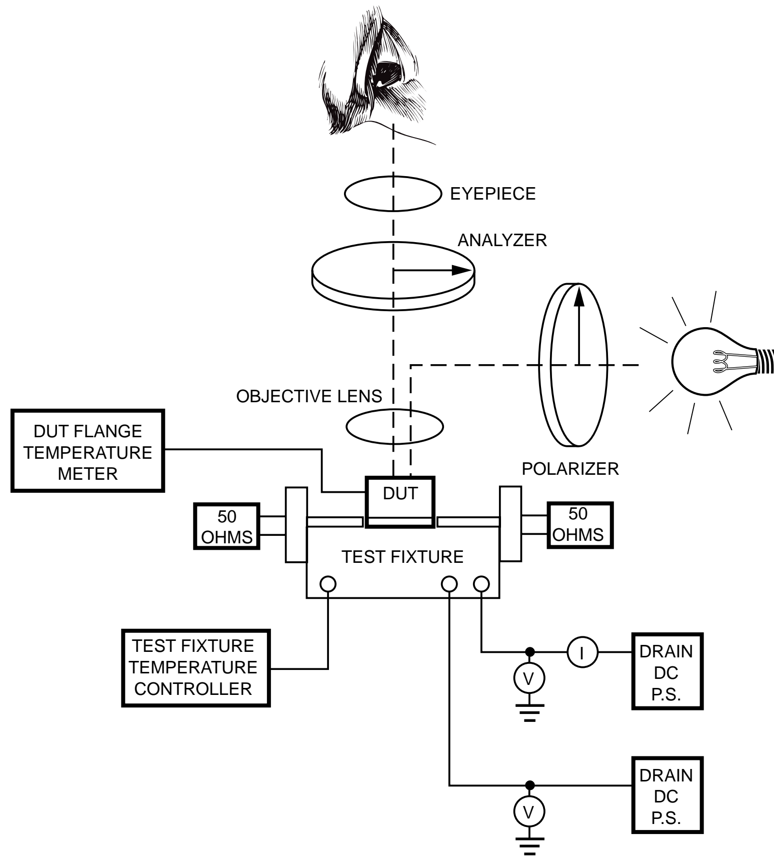


Figure III-3. Block Diagram of a Liquid Crystal Test Setup

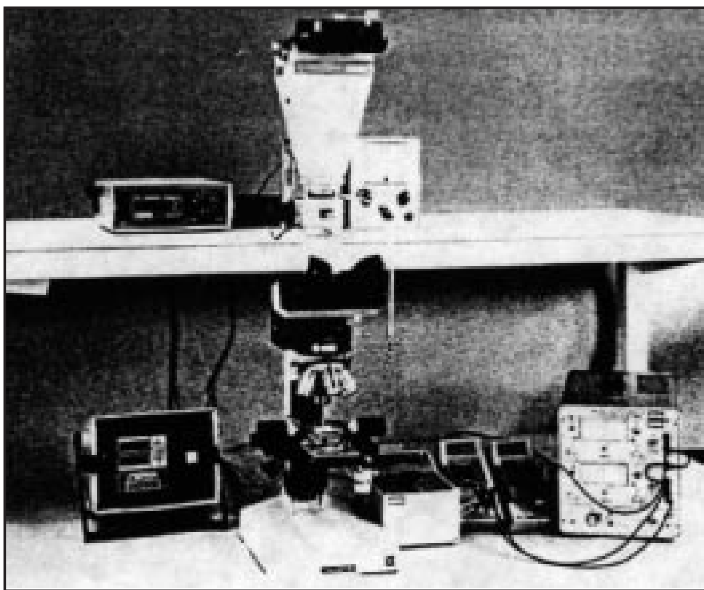


Figure III-4. Liquid Crystal Test Setup used at Hewlett-Packard

powder is added to a carrier liquid such as acetone. We typically use about 0.05 grams (a heaping pile on the tip of a jeweler's screwdriver) of nematic crystal powder mixed into 10 ml of acetone. Use caution since acetone is highly flammable. One must be careful not to add too much solid crystal to the carrier liquid as this will result in a thick coating caking the surface of the DUT when the solution dries. (If this happens, flood the DUT with solvent to clean it.) Next, the mixture is stirred until the powder fully dissolves. A few drops of the solution are placed onto the device to be tested. When the carrier liquid has completely evaporated the device is ready to be tested. The DUT, now ready for testing, is then placed into the hot/cold fixture and biased as desired.

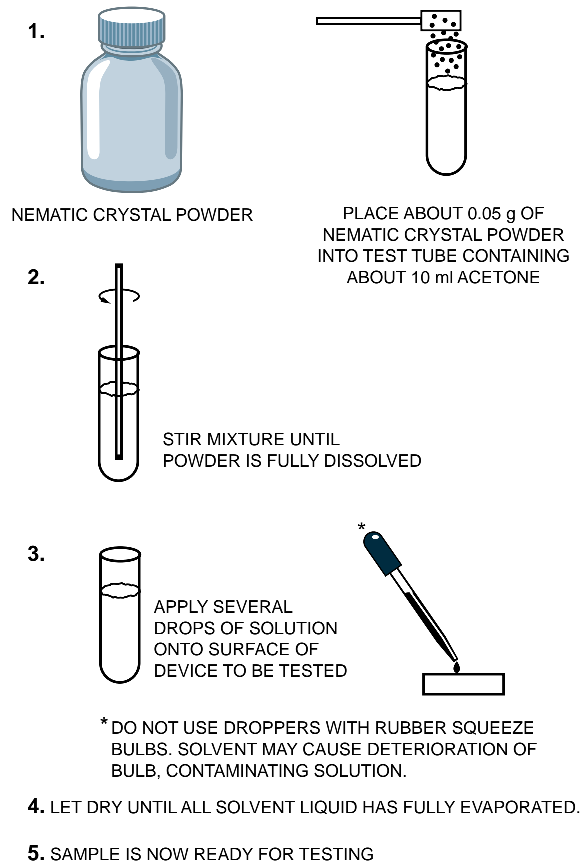


Figure III-5. Preparation and Application of Liquid Crystal Solution

The following equation is commonly used to determine the thermal resistance of the DUT:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. 111-1)}$$

where:

- θ_{jc} = channel-to-case thermal resistance (°C/watt)
- T_{ch} = channel temperature of the device under test (°C)
- T_c = device case (flange) temperature (°C)
- P_d = bias power plus RF input power – RF output power (watts)

If there is no RF power present, we may rewrite Eq. III-1 for the case of a FET under test as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{V_{ds}\, I_{ds}} \qquad \text{(Eq. III-2)}$$

where:

- T_{ch} = DUT channel temperature (°C)
- T_c = device case or flange temperature (°C)
- V_{ds} = drain to source voltage (Volts)
- I_{ds} = drain to source current (Amperes)

For a backside mounted FET, the channel temperature will be virtually the same as the temperature on the surface of the die. Thus one can substitute the N-I transition temperature for T_{ch} in Eq. III-2 and solve for θ_{jc}:

$$\theta_{jc} = \frac{T_{N\text{-}I} - T_c}{V_{ds}\, I_{ds}} \qquad \text{(Eq. III-3)}$$

where $T_{N\text{-}I}$ is the N-I transition temperature for the crystal in use.

As the above equation indicates, the DUT can be raised to the transition temperature by changing either the ambient (case) temperature or the DC input power. Alternately increasing then decreasing the DC power provides a quick indication of how heat spreads across the surface of the device.

It should be mentioned that there has been some concern expressed as to the sensitivity of the nematic crystals to variations in electric field magnitude. As sizable field values may exist between closely spaced source, gate, and drain fingers, such concern seems warranted. In fact, the types of crystal used for temperature characterization show little or no variation as a function of electric field intensity over the range of DC values commonly applied to power FETs.

This has been confirmed via the following experiment: A FET coated with nematic crystal solution was biased to pinchoff. The drain voltage was varied at flange temperatures well below, near, and above the N-I transition temperature. The only change noticed was a slight brightening of the DUT at high drain voltages when the unit was below the transition temperature.

The source of concern may be due to confusion with a class of nematic crystals which exhibit changes at relatively low intensity electric fields. These have been used to spot pinholes and defects in semiconductor device oxide and metallization layers. [III-7, 8, 9]

D. Some Tips for Practical Measurements

Experience gained over several hundred measurements yields the following practical tips:

1. Some nematic crystals exhibit a “false” transition point below the true N-I temperature. This false point is usually far below the specified N-I temperature. The user should watch out for such points which betray themselves by resulting in calculated values of thermal resistance much greater than those expected. The higher transition temperature crystals may exhibit several such points.

2. An important factor often overlooked is the variation of thermal resistance with temperature. This should be expected since the thermal resistivity of semiconducting materials (including GaAs!) varies as a function of temperature [III-10, 11, 12]. Measurements of thermal resistance may vary over thirty percent depending on channel and substrate temperatures during testing.

   In view of this, it is desirable to use a crystal with a transition temperature close to the channel temperature which the device is expected to see in normal use. This avoids the necessity of having to calculate the thermal resistance at different channel and substrate temperatures, which may be done using Kirchoff ’s transformation [III-13] as shown in Appendix B. It is especially important to be aware of this variation with temperature when

measuring thermal resistance values for use in reliability calculations or accelerated life testing.

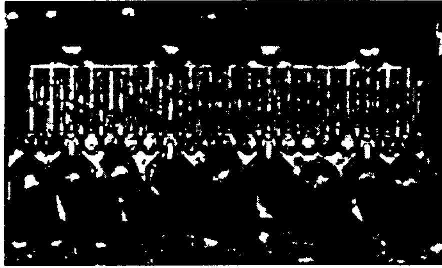
3. Thermal resistance has been observed to vary with drain-source voltage, increasing with increasing V_{ds}. Variations exceeding ten percent have been observed over a V_{ds} range spanning 2 to 11 volts [III- 14]. In view of this variation, it is desirable to measure device thermal resistances under normal operating bias conditions.

4. The DUT may be cycled above and below the transition temperature as many times as desired without degradation of crystal performance so long as the maximum temperature the sample experiences does not exceed more than about thirty degrees Celsius above the transition temperature. At elevated temperatures, the crystal sublimates and a new application of solution is required to continue testing.

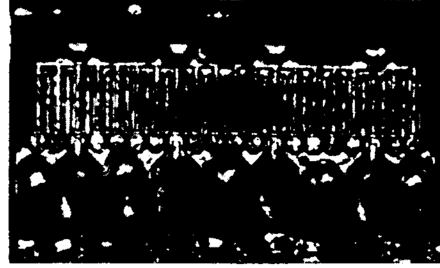
5. As the crystal is very sensitive to small changes in temperature near the N-I transition point, the user should allow sufficient time for thermal equilibrium to be established after changing either the flange temperature or DC power to the DUT. The response time of the nematic crystal is usually much faster than the thermal time constant of the DUT. Equilibrium may be observed when the boundary between light and dark areas stops moving under constant bias and flange temperature conditions. Use of a hot/cold stage with a large thermal mass (e.g., a thick copper block) will help keep DUT temperatures very stable for long periods of time.

E. Some Results

Figure III-6 shows a sequence of photographs taken of an HP AT-8141 power FET transistor chip mounted in an IMFET (98) package. (All succeeding measurements are performed using the AT-8141 unless otherwise specified.) The photos clearly show the changes in surface temperature as the device is heated. The top left photo (Figure III-6a) shows the device before heating. Photo “b” shows the appearance of the first hot spot (at or above the N-I transition temp.), on a drain finger. Succeeding photos show the expansion of the hot area as it spreads throughout the surface of the die. As expected, heating begins in the center of the die and moves outward. Note the symmetrical elliptical shape of the dark area. This is indicative of good die to flange attachment. A die which is poorly attached to its carrier may show a number of isolated hot spots, merging into one another as heating progresses.



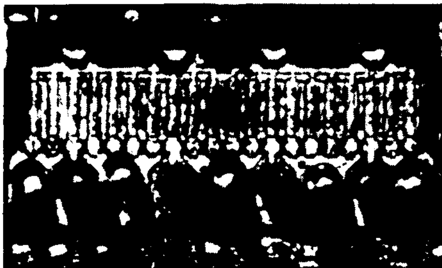
III-6a



III-6d

III-6b

III-6e



III-6c

III-6f

Figure III-6.

Measurement accuracy and repeatability are enhanced by using the power and temperature conditions commensurate with the appearance of the first hot spot (Figure. III-7) when calculating thermal resistance per Eq. III-2. Since the device will most likely fail at the hottest point ***it is desirable to define thermal resistance under the conditions at which the first hot spot appears when making calculations of device reliability.***

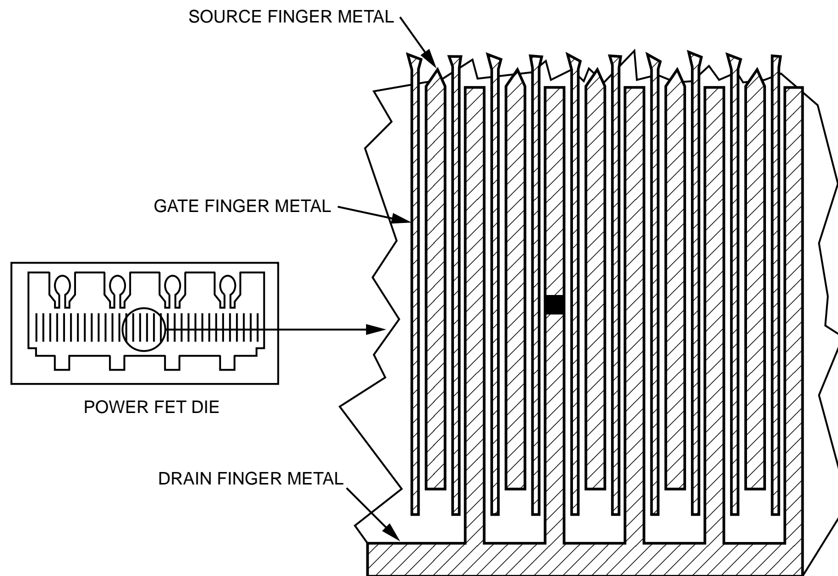


Figure III-7. Closeup of Fingers Showing Appearance of First Hot Spot

Using the liquid crystal method one may construct plots showing contours of constant temperature (isotherms) on the surface of the die under test. The isotherms are determined by using a single N-I transition temperature crystal, and varying the flange temperature in small increments. As the channel temperature increases, the dark area will increase. The boundary between the light and dark areas will be at the N-I transition temperature, and the difference between the hottest part of the die and the boundary will be given by:

$$\Delta T = T_{case1} - T_{case2} \qquad \text{(Eq. III-4)}$$

where:

T_{case1} = DUT case temperature measured when the hottest point is observed

T_{case2} = DUT case temperature

This formula assumes that the thermal resistance of the DUT is constant over temperature, a valid assumption for temperature differences on the order of several tens of degrees. Figure III-8 shows a series of isothermic contours generated from the photographs of Figure III-6.

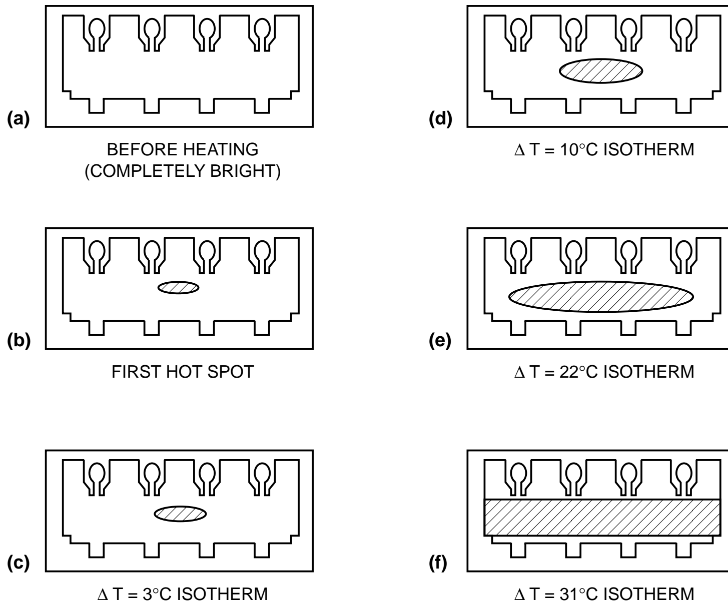


Figure III-8.

The variation of thermal resistance as a function of temperature was studied by performing hot-spot thermal resistance measurements using five different nematic crystals on the same device, each having a different N-I transition temperature. The results of these measurements are shown Figure III-9. This data was found to give excellent agreement with the values computed using Kirchoff 's transformation.

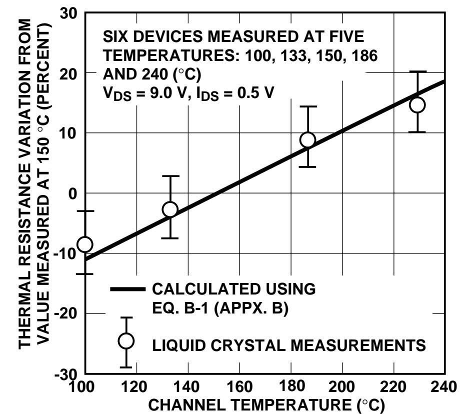


Figure III-9. Deviation of Thermal Resistance from Value at 150°C vs. Temperature

The effect of varying drain current on thermal resistance was investigated by performing hot-spot thermal resistance measurements while holding drain voltage constant. Drain current was varied by a factor of three, and case temperature was adjusted to keep the size of the hot spot constant at each value of I_{ds}. The variation of θ_{jc} due to the case temperature change was computed and subtracted from the total variation observed, yielding no net variation of thermal resistance with drain current.

An experiment was performed to determine the variation of thermal resistance as a function of drain-source voltage. V_{ds} was varied over a range spanning from 2 to 11 volts, and I_{ds} appropriately adjusted to keep the power dissipated by the DUT constant. The case temperature was set as required to keep the hot spot size constant at each set of V_{ds}, I_{ds} values. The variation of θ_{jc} due to the change in case temperature was calculated and subtracted from the thermal resistance measured, giving the variation due to changing values of V_{ds}. The results of this experiment are given in Figure III-10.

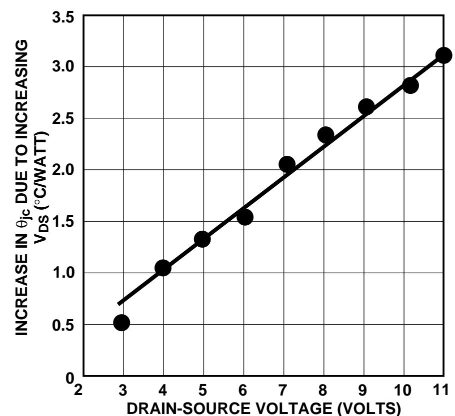


Figure III-10. Thermal Resistance vs. Drain-Source Voltage

F. Correlation With Other Methods

The excellent spatial resolution and temperature accuracy make liquid crystal measurements ideal for use as reference standards when calibrating thermal resistance measurements performed using other techniques. Liquid crystal measurements have been used at Hewlett-Packard to provide correction factors for use with delta V_{gs} measurements so that the latter may be used to give reasonable approximations of hot spot thermal resistances. Details of the correction of delta V_{gs} measurements are given in part IV.

Measurements have been performed on several devices using both the liquid crystal technique and infrared microscopy. Comparison indicates that data from the IR testing yields values of thermal resistance about ten percent lower than the values calculated using liquid crystal measurement data. This is to be expected as the IR microscope has lower spatial resolution, typically 15-30 micron spot size (spot size can be as small as 7 microns with appropriate optics), whereas the liquid crystal method can resolve hot spots on the order of several microns.

G. Summary

The liquid crystal method provides a powerful tool with which to measure the thermal resistance of microwave power devices. It offers superior spatial resolution and temperature accuracy when compared to other methods which currently find wide use. This technique permits measurements to be made which are difficult or impossible to perform using other methods. The superior spatial resolution afforded permits θ_{jc} to be defined at the onset of the first hot spot, facilitating more accurate determinations of maximum channel temperature and reliability predictions.

IV. The Delta V_{gs} Measurement Technique

A. Introduction

While not intended to give values of thermal resistance to be used in calculating operating channel temperatures, the delta V_{gs} measurement technique provides a quick, non-destructive determination of die-to-case attachment quality. This measurement, when correlated to liquid crystal measurements, may be used as a technique to guarantee the conformance of production units to thermal resistance specifications.

B. Principle of Operation

The use of the voltage drop across a forward-biased diode as an indicator of thermal performance is well documented,[IV-1, 2, 3, 4, 5, 6] and will be reviewed only briefly here for the sake of completeness.

The forward I-V characteristic of the gate-source Schottky diode may be expressed as:

$$J = AT^2 \exp\left(\frac{-qV_b}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \qquad \text{(Eq. IV-1)}$$

for $V >> \frac{3kT}{q}$

where:

J	=	forward current density
A	=	effective Richardson constant
T	=	junction temperature (K)
q	=	charge of the electron
V_b	=	built-in barrier voltage
k	=	Boltzmann constant
V	=	voltage across junction
n	=	ideality factor

Eq. IV-1 may be solved for V:

$$V = nV_b - \frac{nkt}{q}\left[21nT - 1n\left(\frac{J}{A}\right)\right] \qquad \text{(Eq. IV-2)}$$

For moderate and constant values of current density J, the voltage across the junction V decreases almost linearly with increasing temperature.

We define the K factor for a device as

$$K = \frac{\Delta T}{\Delta V} \text{ (at constant current)} \qquad \text{(Eq. IV-3)}$$

which will vary depending on the specific processing involved for each type of device. K factors are measured at Hewlett-Packard by placing the DUT in an oven and measuring the voltage across the forward conducting gate-source Schottky junction at a number of different temperatures while holding I_{gs} constant at 0.1 mA. Adequate time must be given between measurements to allow the temperature to stabilize. This procedure is repeated at several different temperatures. Figure

IV-1 shows a plot of the K factor obtained for the HP M113 power FET (with a gate periphery of 10 mm).

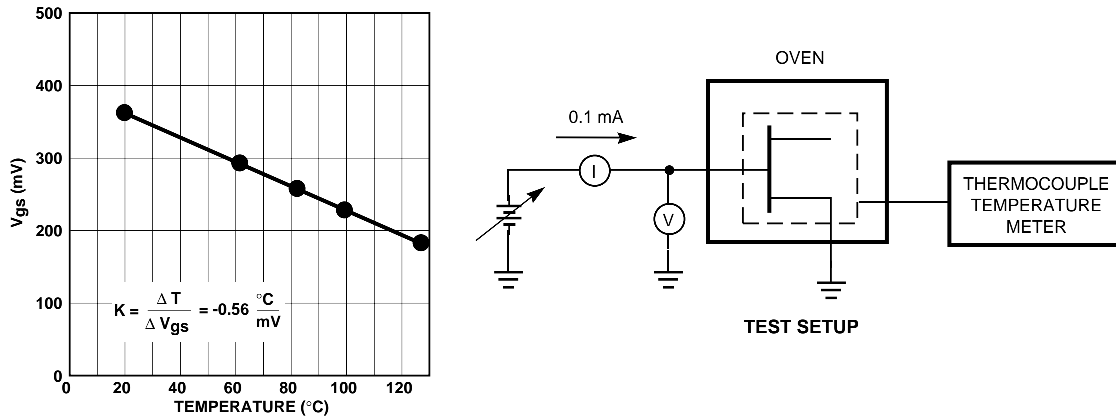
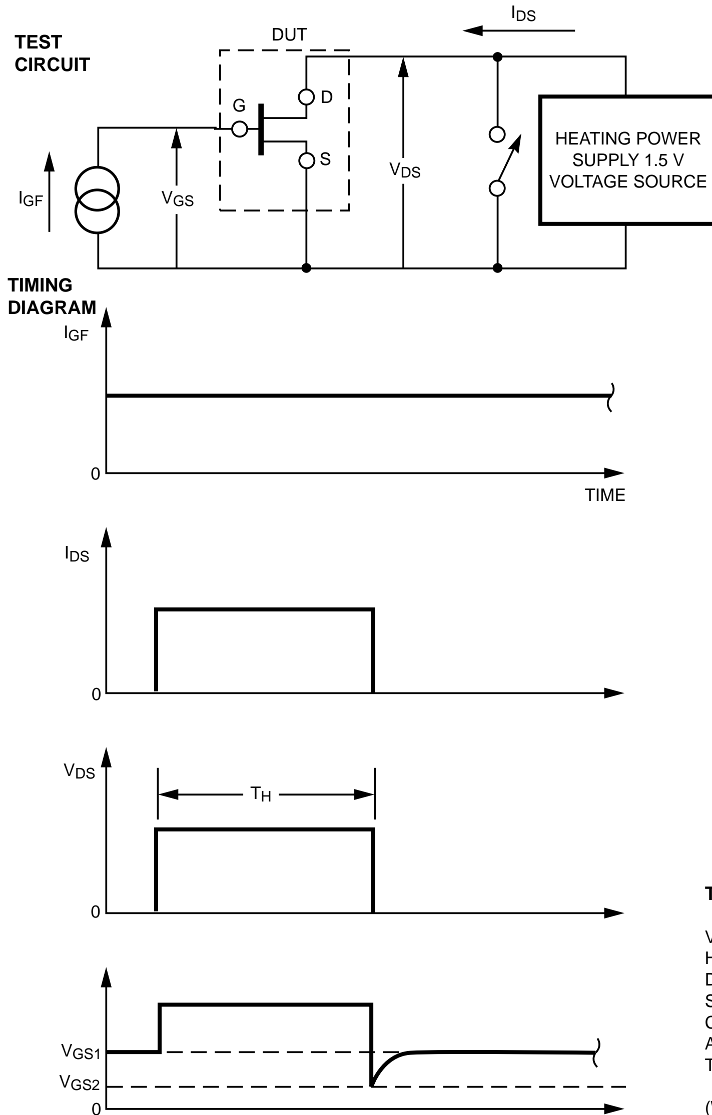


Figure IV-1. K Factor Plot for HP M113 Microwave Power FET

At HP delta V_{gs} measurements are performed using a Sage Enterprises model DAE 220. The unit provides a forward gate current through the gate-source diode and applies a voltage pulse between the drain and source to heat the device. At the end of each heating pulse, the drain and source are shorted together and a measurement of the voltage drop across the gate-source diode performed. Figure IV-2 shows a rough schematic of the setup and a timing diagram showing the relationship between the heating pulse and the measurement interval.



TEST CONDITIONS:

V_{DS} = 1.5 V, V_{GS} > 0	
HEATING PULSE WIDTH (T_H):	30 msec
DELAY TIME (T_D):	2 µsec
SENSING CURRENT (I_{GF}):	0.1 mA
CHANNEL TEMPERATURE:	60°C
AMBIENT TEMPERATURE:	25°C
TIME BETWEEN HEATING PULSES (T_P):	0.5 sec

(WHEN REPETITIVE MEASUREMENTS ARE MADE)

Figure IV-2. Simplified Schematic and Timing Diagram for Delta V_{gs} Measurements

Knowing the device K factor, the amount of power supplied by the heating pulse, and the change in gate-source voltage measured from the time before the heating pulse to the time directly following it, we may compute the thermal resistance:

$$\theta_{jc} = \frac{D_{vgs}K}{V_h I_h} \qquad \text{(Eq. IV-4)}$$

where:

- θjc = channel-to-case thermal resistance (°C/watt)
- D_{vgs} = change in voltage across gate-source diode (from time before to time after heating pulse)
- V_h = Drain-source heating pulse voltage
- I_h = Drain-source heating pulse current

C. Thermal Time Constants

At this point let's step back and see what we are really measuring. The DUT consists of a number of different materials joined together, each with different thermal characteristics. An analogous electrical equivalent of this would be a circuit consisting of a number of RC circuits in series (Figure IV-3). The time constants of the RC circuits correspond to the heating and cooling "thermal time constants" of the different constituent materials of the DUT, and will be a function of the physical properties and sizes of those materials. These time constants may be both calculated and directly measured. Examples of both follow:

1. Calculation of thermal time constants

As an example, let's compute the thermal time constant of a 4 mil thick GaAs FET die. The thermal time constant is given by:

$$t = \left(\frac{2F}{\pi}\right)^2 \left(\frac{PC}{\sigma}\right) \qquad \text{(Eq. IV-5)}$$

where:

F= die thickness (cm)
p = density of the material (g/cm^3)
σ = thermal conductivity (W/cm°C)
c = specific heat of the material (J/g°C)

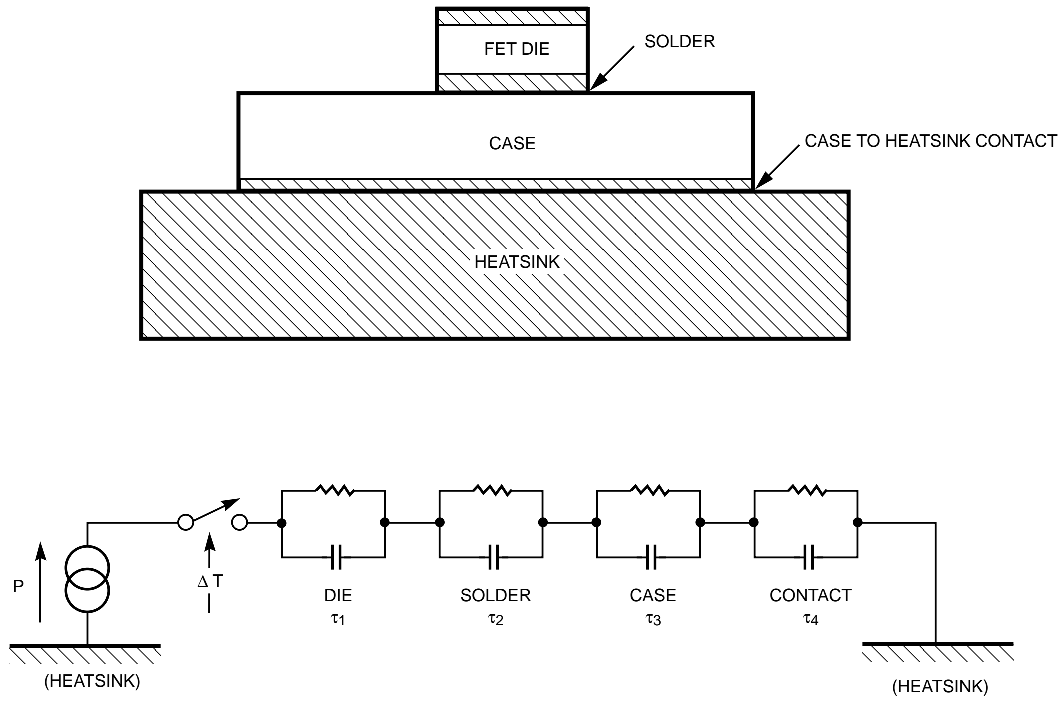
For GaAs, the appropriate values are:

p = 5.31 g/cm^3
σ = 0.44 W/cm°C
c = 0.35 J/g°C

and F = 0.01 cm for a 4 mil thick die. Substituting the above constants into (Eq. IV-5) gives:

t = 175 µs

For a packaged device, time constants for the solder between the die and flange, and contact between the flange and test fixture or chassis may be similarly computed.



ORDER OF MAGNITUDE:

DIE THERMAL TIME CONSTANT (τ_1):	200 μsec
SOLDER THERMAL TIME CONSTANT (τ_2):	VERY SHORT FOR GOOD SOLDER
CASE THERMAL TIME CONSTANT (τ_3):	10 msec
CONTACT THERMAL TIME CONSTANT (τ_4):	0.5 sec
HEATSINK THERMAL TIME CONSTANT):	LONG, MORE THAN 5 SECONDS

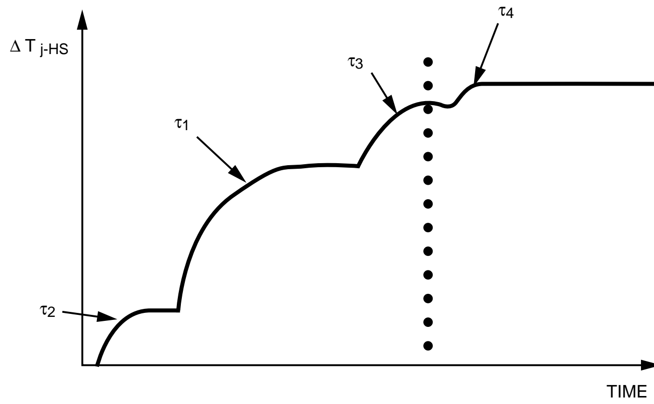


Figure IV-3. Analogous Electrical Model of Thermal Time Constants with Timing Diagram

2. Experimental Determination of Thermal Time Constants
Thermal time constants may also be evaluated experimentally. Figure IV-4 gives a plot of delta V_{gs} (linearly proportional to channel temperature) versus time for an HP 6 watt IMFET™ internally matched FET. Data was obtained by varying the heating pulse width while using a constant delay time (2 µs) between the end of the heating pulse and beginning of the V_{gs} measurement.

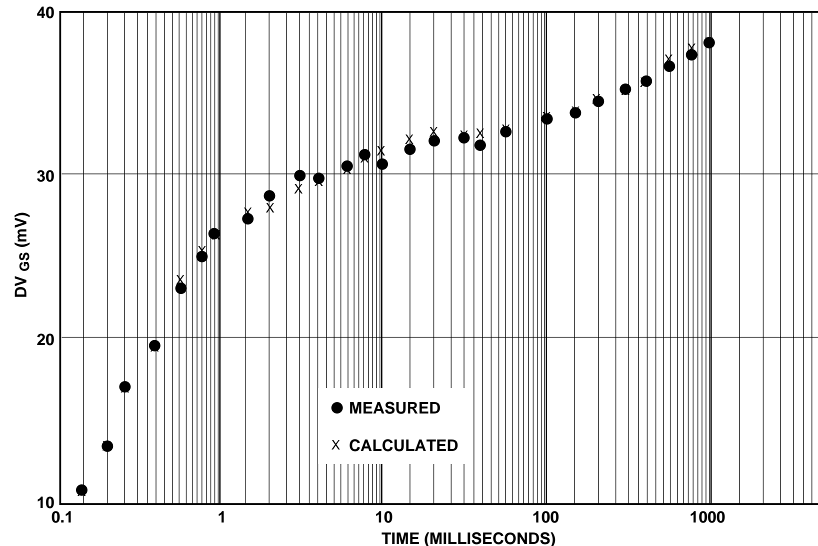


Figure IV-4. Measured and Calculated Thermal Time Constants of Internally Matched FET

We can take this experimental data and curve fit it to a form which is a sum of exponential curves. This yields the following formula giving delta V_{gs} as a function of time:

$$V_{gs} = 24.8\left[1 - \exp\left(\frac{-t}{0.262}\right)\right] + 7.3\left[1 - \exp\left(\frac{-t}{3.56}\right)\right] + 8.0\left[1 - \exp\left(\frac{-t}{658}\right)\right]$$

(Eq. IV-6)

where:

V_{gs} is in mV
t is time in msec.

Figure IV-4 shows both the measured data and delta V_{gs} as calculated using the above equation.

By comparing the time constants obtained from the experimental data to those calculated from the device material parameters we may identify the thermal time constants of the constituent members of the DUT. The first exponential in Eq. IV-6 (the smallest time constant) may be assumed to be the contribution of the FET die. The second term represents the flange, and the third the contact thermal resistance

between the flange and the heat sink (test fixture) to which the DUT is secured. The constant of the solder between the FET die and the package is probably too small to be accurately measured.

Summarizing the results for the above 6 watt IMFET device and computing thermal resistance by using Eq. IV-4 we get the following:

Component	Time Constant	Thermal Resistance
die	0.262 msec	1.85 (°C/watt)
flange	3.56	0.54
contact	658	0.60

(A good contact thermal resistance is about 0.2°C/watt. The value shown above was obtained by measuring the IMFET device in a quick-mount type fixture instead of bolting the flange down to the heatsink as would typically be done.)

Now that we have gone to all the trouble of calculating and measuring the thermal constants of our device, one may ask “What do we do with this data?” Aside from giving us some physical insight as mentioned above, knowledge of the thermal time constants will help us to perform more accurate measurements by allowing us to: (1) choose proper heating pulse widths, and (2) correct for the cooling which occurs between the end of the heating pulse and the beginning of the delta V_{gs} measurement.

The length of the heating pulse must be carefully chosen so that only the desired components of the DUT are heated. One does not want to inadvertently include the case-to-heatsink (device case-to-test fixture) contact thermal resistance in a measurement of channel-to-case thermal resistance. The dotted line in the plot at the bottom of Figure IV-3 shows the point at which the heating pulse should be terminated and delta V_{gs} measurement initiated so as not to include the contact thermal resistance in the measurement.

The DUT will begin to cool during the time between the end of the heating pulse and beginning of the delta V_{gs} measurement. A short delay is required between these two steps to allow circuit switching transients to die out. The resulting measurement error (about 10% for an IMFET device) may be corrected by measuring the thermal time constant of the DUT and extrapolating back to the time at which the heating pulse just ends.

Knowledge of the thermal time constants also allows us to know just which components within the device are heating and lets us judge the effects of changing flange, solder, and device parameters when optimizing thermal performance.

D. Corrections to the Raw Data

Having looked at the principle behind delta V_{gs} measurement and given some advice on how to perform it, we come to the point at which we have the results of the tests in our hands and must interpret the data. This is the most important part of the whole process! There are several important points regarding the delta V_{gs} method which must not be overlooked to fully understand the results of the measurement. SEVERAL CORRECTIONS TO THE VALUE OF θ_{jc} GIVEN IN EQ. IV-4 ARE REQUIRED TO OBTAIN THE TRUE VALUE OF THERMAL RESISTANCE THAT A DEVICE WILL EXPERIENCE AT THE OPERATING POINT IT WILL SEE IN NORMAL USE:

It is important for the user of delta V_{gs} measurements to be aware of the following:

1. ***The delta V_{gs} method gives a value of thermal resistance corresponding to a temperature which is averaged over an unknown fraction of the active area of the FET. Thermal resistance calculated using uncorrected delta V_{gs} measurement data is not representative of the temperature at the hottest point on the die.*** Uncorrected delta V_{gs} measurements provide a relative measurement which is useful in assessing the quality of the die attachment to the package. The delta V_{gs} technique is used primarily to determine the die attach quality of large numbers of devices in a production environment, not to determine absolute values of thermal resistance. It is possible to correlate this averaged value to the peak value of thermal resistance at the hottest part of the channel using liquid crystal measurements. The liquid crystal technique, described in part III of this application note, has spatial resolution exceeding 2 microns, and may be used to measure the thermal resistance at the hottest part of the DUT. Both liquid crystal and delta V_{gs} measurements are performed on a number of devices. A correlation factor is thus obtained relating the peak to average thermal resistance values.

2. Thermal resistance varies as a function of drain-source voltage. The Sage DAE 220 places 1.5 volts across the drain and source to heat the DUT. Typical operating drain-source voltages for power FETs may range from 8 to 10 volts. A heating pulse voltage at this level would subject the DUT to excessive electrical stress (drain current would exceed I_{dss} as the gate is forward biased). The higher value of V_{ds} might also result in high amplitude oscillations which may destroy the device.

   Liquid crystal measurements may be performed at several drain voltages to obtain correction factors for each type of device to translate the value of θ_{jc} obtained with the delta V_{gs} method to actual operating voltages. A plot of θ_{jc} vs. V_{ds} is given in Figure III-10 of section III.

3. Thermal resistance measured using the delta V_{gs} method is usually performed at a single value of flange and channel temperature. To translate this to other temperatures, correction is required. The variation of thermal resistance of semiconducting materials with

temperature is well known.[IV-7, 8, 9, 10] One may use Kirchoff's transformation [IV-11] to convert the value of thermal resistance at one channel temperature to another. Appendix C details the derivation of a form of Kirchoff's transformation useful for power FET calculations. Appendix B gives several useful "real-world" calculation examples.

When the following corrections:

1. Device cooling between heating and measurement

2. Peak (hot-spot) to averaged channel temperature

3. Channel temperature transformation

4. Flange temperature transformation

are all applied to the raw data produced by delta V_{gs} measurement, we arrive at the following correction formula which will give a value approximating the hot-spot value of thermal resistance:

$$\theta_{jc22} = \theta_{dvgs} \bullet K1 \bullet K2 \bullet K3 \bullet K4 \bullet K5 \bullet K6 \qquad \text{(Eq. IV-7)}$$

where

θ_{jc22} = thermal resistance at flange temperature T_{c2} and channel temperature T_2

θ_{dvgs} = thermal resistance measured by delta V_{gs} test at flange temperature T_{c1} and channel temperature T_1

K1 = factor which takes into account the cooling of the device in the time between the end of the heating pulse and the beginning of delta V_{gs} measurement during testing. For an IMFET device measured using a 2 μsec delay time, this number equals 1.1 (a 10% correction)

K2 = factor which relates the peak (hottest spot) channel temperature determined from liquid crystal measurements to the averaged channel temperature during delta V_{gs} testing. This factor is different for different device types, depending primarily on geometry.

K3 = factor which accounts for change in θ_{jc} due to change in V_{DS} from the 1.5 volt delta V_{gs} measurement to the value of V_{DS} which the device will see in actual operation. This factor also must be evaluated for each type of device. Figure III-10 is a plot of K3 vs. V_{DS} for the AT-8141.

$$K4 = \frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}}$$

$$K5 = \frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}$$

$$K6 = \frac{a + bT_{c2}}{a + bT_{c1}}$$

where:

T_{ch2} = desired channel temperature
T_{ch1} = channel temperature during delta V_{gs} measurement
T_{c2} = desired flange temperature
T_{c1} = flange temperature during delta V_{gs} measurement
$\alpha 11$ = Kirchoff (linearized) channel temperature as defined in Eq. C-14 in Appx. C corresponding to channel temperature T_{ch1}
22 = Kirchof f (linearized) channel temperature as defined in Eq. C-15 in Appx. C corresponding to channel temperature T_{ch2}
a = thermal resistivity coefficient for GaAs doped at n = 5E16, equal to 7.043 (see Appx. C)
b = thermal resistivity slope coefficient for GaAs doped at n = 5E16, equal to 0.00828 (see Appx. C)

(All temperatures are measured in degrees Celsius)

E. Automation of the Delta V_{gs} Measurement Setup

The outstanding advantage of the delta V_{gs} method over other techniques is that measurements made using this technique are non-destructive (do not require de-lidding the DUT or coating it with any substance) and fast. This makes it ideally suited for production line thermal resistance testing. Computer control also permits the use of untrained operators to perform testing.

At present there is no commercially available automated delta V_{gs} tester suitable for microwave power FET measurement. To meet the need at Hewlett-Packard for semi-automated production line thermal resistance measurements a Sage model DAE 220 was modified to interface with a microcomputer, printer, and plotter via the IEEE-488 instrumentation bus. A block diagram of the system is shown in Figure IV-5.

The DAE 220 does not come equipped with an IEEE-488 port, but does have a centronics-type parallel I/O port which is normally used to transfer data to an external printer. An ICS Corporation model 4871 TTL to IEEE-488 conversion unit was used to interface the DAE 220 with the other IEEE-488 compatible system components. Since the DAE 220 is not equipped to generate or receive handshake signals, and the ICS 4871 might not be fast enough to handle the data from the Sage,

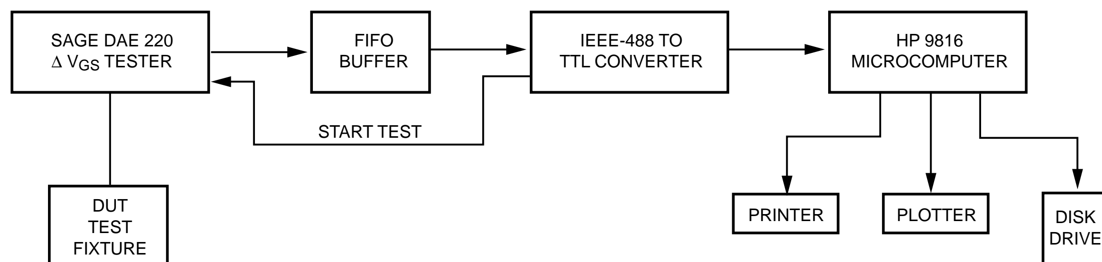


Figure IV-5. Block Diagram of Computer Controlled Delta V_{gs} Thermal Resistance Measurement Setup

a fast FIFO buffer was added between the two units. Data format conversion is handled via software. A TTL signal is sent from the computer to an open collector driver across the “TEST” switch on the Sage front panel to initiate a measurement cycle.

Test parameters such as heating voltage and pulse lengths must be manually set at the Sage front panel. Values returned from the Sage to the computer are delta V_{gs} and I_h, the heating current. For each device tested, the computer performs five identical tests then averages the data to obtain the final “raw” (uncorrected) value of thermal resistance as defined in Eq. IV-4.

Finally, the computer performs the corrections mentioned in the previous section to give a reasonable approximation of the thermal resistance for the DUT commensurate with normal operating bias and temperature levels. If a device is found to have unacceptably high thermal resistance the operator is alerted and told to reject the unit.

Figure IV-6 and Table IV-1 give examples of plotter and printer output from several typical production runs. Data may also be sent to a mass storage unit and correlated over time to monitor statistical trends.

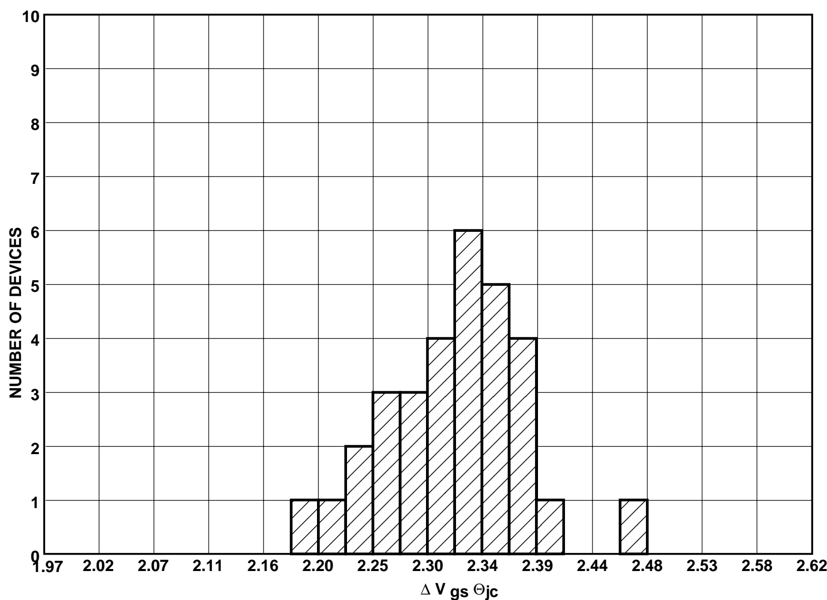


Figure IV-6. Sample of Delta V_{gs} Distribution Plot Generated Using the Setup Shown in Figure IV-5

Table IV-1. Die Attach Evaluation/Thermal Resistance Measurement

Serial Number	θ_{jc}(1.5V) (°C/Watt)	Normalized Case temp (°C/Watt)	Thermal Resistance (T_{ch} = 150°C, T_{case} = 70°C V_{DS} = 9 V)
1	2.34	2.26	5.77
2	2.43	2.36	6.00
3	2.46	2.37	6.04
4	2.36	2.28	5.80
5	2.41	2.34	5.93
6	2.47	2.38	6.07
7	2.32	2.24	5.71
8	2.40	2.32	5.91
9	2.34	2.27	5.77
10	2.46	2.37	6.03
11	2.45	2.36	6.00
12	2.57	2.48	6.32
13	2.43	2.33	5.94
14	2.49	2.40	6.12
15	2.27	2.19	5.57
16	2.40	2.31	5.89
17	2.41	2.36	5.94
18	2.40	2.31	5.89
19	2.14	2.31	5.89
20	2.30	2.21	5.62

F. Summary

An overview of the delta V_{gs} method of thermal resistance measurement has been presented including theory of operation along with methods of interpreting and correcting the raw data. Details of an automated delta V_{gs} test station suitable for production use have been given.

It should be stressed that delta V_{gs} measurements are best used as a means of determining die attach quality. The method is not intended to give absolute values of thermal resistance commensurate with the typical operating conditions of the DUT. For this purpose, liquid crystal measurements should be used. Using the correction techniques discussed above it is possible to correlate delta V_{gs} and liquid crystal measurements to some degree, but again it should be stressed that the delta V_{gs} method is not intended to give absolute values of θ_{jc}.

Appendix A.
Thermal Resistance Data for HP IMFET Internally Matched FETs

Table A-1

HP IMFET™ Internally Matched GaAs FET Family (Watts)	Typical R_{jc} at Recommended Bias Point @ t channel = 150°C [1] (°C/W)
1.5	19.9
3	11.5
6	5.3
8	6.5
2[2]	8.8
4[2]	5.1

Notes: 1. Measured using 150° N-I Liquid Crystal, at hottest spot.
2. High Frequency

Appendix B.
Using Thermal Resistance Data: Some Practical Examples

Thermal resistance is not a constant. Determining the correct value at actual device operating channel and case temperatures requires several corrections to the thermal resistance values given in device data sheets. This appendix gives several examples showing how to correct thermal resistance values to account for temperature variations. Note that the following corrections do not take into account any changes in thermal resistance due to variations in drain-source voltage. The examples given below assume operation at the values of V_{ds} listed in the thermal resistance specifications of Hewlett-Packard product data sheets. Operation at other values of V_{ds} may require additional correction as indicated in section III of this application note.

Kirchoff's transformation may be applied to determine the value of thermal resistance at one channel temperature when given the value at another. The thermal resistance of GaAs may be approximated as a linear function of temperature over the range of power FET operation. Applying the appropriate terms from Appendix C, Eq. C-13, the thermal resistance at channel temperature T_{ch2} and case (flange)

temperature T_{c2} may be determined from value given in the catalog, measured at T_{ch1} and T_{c1}, by using the following relation:

$$\theta_{jc2} = (\theta_{jc1} - \theta_{case}) \left(\frac{246.7 + T_{ch2}}{246.7 + T_{ch1}} \right) \left(\frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}} \right) \left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}} \right) + \theta_{case} \qquad \text{(Eq. B-1)}$$

where:

- θ_{jc2} = Channel to case thermal resistance at channel temperature T_{ch2} and case temperature T_{c2}
- θ_{jc1} = Channel to case thermal resistance at channel temperature T_{ch1} and case temperature T_{c1}
- θ_{case} = Thermal resistance of case, from bottom of flange to the top surface which the FET die rests upon. θ_{case} for several HP IMFET products is given in Table B-1.

$$\alpha 11 - T_{c1} + (246.7 + T_{c1}) \ln \left(\frac{246.7 + T_{ch1}}{246.7 + T_{c1}} \right) \qquad \text{(Eq. B-2)}$$

$$\alpha 22 - T_{c2} + (246.7 + T_{c2}) \ln \left(\frac{246.7 + T_{ch2}}{246.7 + T_{c2}} \right) \qquad \text{(Eq. B-3)}$$

This formula is also given in Hewlett-Packard IMFET product data sheets.

Table B-1.

Device Type (Watts)	**θ_{case} (°C/Watt)**
1.5	2.0
2	1.1
3	1.1
4	0.7
6	0.7
8	0.6

Note that θ_{jc1} and θ_{jc2} represent the total (FET plus case) thermal resistance of the device. The thermal resistance of the case is subtracted from the total thermal resistance before performing the temperature correction, then added in after correction. This is because we wish to correct only the GaAs FET thermal resistance. The case thermal resistance remains essentially constant with temperature. (Here we are assuming a perfect contact between the FET die and the case.)

If we desire to determine the ***channel-to-heatsink*** thermal resistance, the case to heatsink contact thermal resistance must be added to θ_{jc}. This contact thermal resistance is equal to approximately 0.22°C/watt for HP IMFET internally matched FETs.

Eq. B-1 may be used with a programmable calculator or PC to give a quick estimation of the thermal resistance of a device under actual operating conditions. The following examples demonstrate the most common applications involving temperature corrected thermal resistance:

For convenience, Hewlett-Packard power product data sheets include plots of channel vs. case temperature as shown in Figure B-1. These plots are constructed using the above formulation of Kirchoff's transformation. Using these plots avoids the necessity of performing the calculations shown in examples 1 and 2 below.

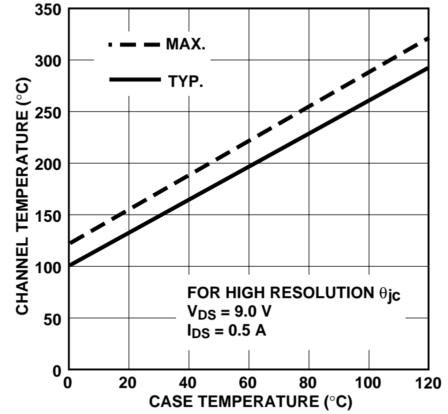


Figure B-1. Plot of Case vs. Channel Temperature

Several examples are now given illustrating how to use Eq. B-1 to find the case and channel temperatures and thermal resistance, under several real-world conditions.

Example 1: Determination of maximum heatsink temperature
Suppose we wish to operate an HP IM-6471-1.5 IMFET internally matched power FET at a channel temperature of 200°C, biased at 9 V, 0.5 A. What will the maximum permissible heatsink temperature be? Using Eq. B-1 along with the equation defining thermal resistance:

$$\theta_{jc} = \frac{T_{ch} - T_c}{V_{ds}\, I_{ds}} \qquad \text{(Eq. B-4)}$$

where:

θ_{jc} = channel to case thermal resistance at channel temperature T_{ch} and case temperature T_c.

The values of θ_{jc} and related measurement conditions listed in the Hewlett-Packard data sheet for this device are:

θ_{jc} (max.) = 23.0°C/watt

measured with:

channel temperature (T_{ch})	= 150°C
case temperature (T_c)	= 46.5°C
drain-source voltage	= 9.0 V
drain-source current	= 0.5 A

To determine the temperature of the heatsink, we must add the thermal resistance of the contact between the flange and the heatsink to the channel-to-case thermal resistance. Measurements indicate that typical case-to-heatsink thermal resistance for an IMFET power FET package is 0.22°C/watt. Thus, the last term in Eq. B-1 becomes θ_{case} + 0.22.

We may write a small program to solve Equations B-1 and B-4 iteratively, or write a program to solve Eq. B-1, then plug the resulting

values of θ_{jc} into Eq. B-4, continuing manually until a satisfactory solution is reached. This is illustrated as follows:

First, assign values to the variables in Eq. B-1:

T_{ch1} = 150 (From the product data sheet)
T_{c1} = 46.5
θ_{jc1} = 23.0

and:

θ_{case} = 2.0 (from Table 1 above)
T_{ch2} = 200 (the desired channel temp.)

For a first guess, try the value of T_{c2} = 70°C. Inserting this and the catalog values above into Eq. B-1 yields θ_{jc2} = 25.41°C per watt.

Now insert this value for θ_{jc} along with V_{ds} = 9.0 and I_{ds} =0.5 (the measurement conditions given in the data sheet) into Eq. B-4 and solve for the channel temperature:

T_{ch} = T_c (θ_{jc} • V_{ds} • I_{ds})

= 70 + (25.41) • (9.0) • (0.5)
= 184.3°C

This is too low. To get closer to the desired value of T_{ch} = 200°C let's try a flange temperature of 80°C. Solving Eq. B-1 gives θ_{jc} = 25.75°C per watt. Substituting this into Eq. B-4 gives T_{ch} =195.87°C. This is much closer. Continuing the process for several more iterations gives the final value of case temperature:

$T_{heatsink_{max}}$ = 83.6°C

Example 2: Determination of maximum channel temperature
Equations B-1 and B-4 may be used to determine the channel temperature for a given heatsink temperature. Let us compute the maximum channel temperature commensurate with a heat-sink temperature of 60°C for an IM-6471-1.5 IMFET device.

As in the previous example, we take the values of θ_{jc1}, T_{ch1}, and T_{c1} from the catalog. We substitute these along with the desired flange temperature T_{c2} into Eq. B-4 and solve for the thermal resistance θ_{jc2}.

From the IM-6471-1.5 data sheet:

θ_{jc1} = 23.0
T_{ch1} = 150
T_{c1} = 46.5

and:

θ_{case} = 2.0 (from Table 1 above)
T_{c2} = 60.0 (the desired case temp.)

As in the previous example, let us take the case-to-heatsink thermal resistance to be equal to 0.22°C/watt. Let us try T_{ch2} = 175 as a first guess at the channel temperature. Solving Eq. B-1 gives θ_{jc2} = 24.37°C/watt. Substituting this value into Eq. B-4 gives:

$$\begin{aligned} T_{ch} &= T_c + (\theta_{jc} \bullet V_{ds} \bullet I_{ds}) \\ &= 60 + (24.37) \bullet (9.0) \bullet (0.5) \\ &= 169.68°C \end{aligned}$$

This is below the 175 we guessed, so next time, let's try inserting T_{ch2} = 168 into Eq. B-1. This yields θ_{jc2} = 24.18°C/watt, which in turn yields T_{ch} = 168.8°C. This is very close to the value of channel temperature we put into Eq. B-1. Further iterations yield the final value of channel temperature:

$$T_{ch} = 168.9°C$$

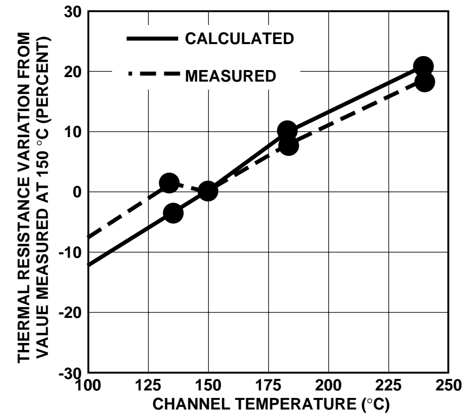


Figure B-2. Calculated and Measured Thermal Resistance vs. Channel Temperature

Comparison of Calculated and Measured Variation of θ_{jc} with Temperature

Figure B-2 gives a plot comparing the calculated change in thermal resistance versus channel temperature with measured values. The change in thermal resistance is given as a percentage, relative to the value measured at 150°C. The empirical curve shows data taken from measurements of a single AT-8141 transistor chip mounted in an IMFET (98) package using a succession of five different liquid crystal solutions, each with a different N-I transition temperature. The calculated curve was obtained by substituting the measured value of thermal resistance at 150°C for θ_{jc1} in Eq. B-1 and computing θ_{jc2} at the other temperatures shown. Comparison shows very good agreement between the measured and calculated values.

Appendix C.
Kirchoff's Transformation

The variation of semiconductor thermal conductivity with temperature is well known. [C-1, 2, 3, 4] The thermal resistance of power FETs is usually specified at a single value of flange and channel temperature, which may not be representative of conditions which the device will encounter during normal use. Given the thermal resistance at one flange and channel temperature, Kirchoff's transformation[C-5] may be used to determine the thermal resistance at other temperatures. In this appendix, a form of the transformation useful in performing power FET thermal calculations is derived.

We define the thermal resistance between two points as:

$$\theta_{12} = \frac{\Delta T_{12}}{P_d} \qquad \text{(Eq. C-1)}$$

where:

θ_{12} = Thermal resistance between points 1 and 2
ΔT_{12} = Temperature difference between points 1 and 2 (T_2-T_1)
P_d = Power dissipated by heat source (heat flux through isothermic surfaces 1 and 2)

The thermal conductivity of many materials, including semiconductors, varies as a function of temperature, i.e.,

$$\sigma = \sigma(T) \qquad \text{(Eq. C-2)}$$

To find the thermal resistance for these materials, one must solve the general non-linear heat flow equation

$$\nabla \bullet \sigma \nabla T = 0 \qquad \text{(Eq. C-3)}$$

at the two points of interest in order to find ΔT to substitute into Eq. C-1. By using Kirchoff's transformation we may define a "linearized" temperature throughout the material such that at each point x we associate a value

$$\alpha(x) = T_o + \frac{1}{\sigma_o} \int_{T_o}^{T} \alpha(T)\, dT \qquad \text{(Eq. C-4)}$$

with the true temperature T(x)

where:

$\alpha(x)$ = the linearized temperature at point x
σ_o = thermal conductivity at $T = T_o$

For power FETs $\alpha(x)$ may be thought of as the value the channel temperature would equal if the thermal conductivity of GaAs were a constant ($\sigma = \sigma_o$) over temperature.

The thermal resistivity of gallium arsenide has been measured over the temperature range spanning 300 to 1000 Kelvin for several levels of doping concentration by Amith et. al.[C-1]. Using this data we may express the thermal conductivity of GaAs as:

$$\alpha (T) = \frac{1}{a + bT} \qquad \text{(Eq. C-5)}$$

Values of the constants a and b are given in Table C-1 for several values of doping concentration.

Table C-1. a and b Constants for GaAs (Amith et. al.[C-1])

N (cm^{-3})	a (°C cm/W)	b (cm/W)
5E16	2.043	0.008280
4E17	2.106	0.009154
8E18	2.289	0.011177

Substituting Eq. C-5 into Eq. C-4 and solving for the linearized channel temperature corresponding to channel temperature T_{ch1} and case (flange) temperature T_{c1}:

$$\alpha 11 = \alpha (T_{ch1} + T_{c1}) = T_{ch1} + \frac{1}{\sigma (T_{c1})} \int_{T_{c1}}^{T_{ch1}} \sigma (T)\, dT$$

$$= T_{c1} + (a + bT_{c1}) \int_{T_{c1}}^{T_{ch1}} \frac{dT}{a + bT}$$

$$= T_{c1} + (a + bT_{c1}) \; \frac{1}{b} \Big[\ln (a + bT) \Big]_{T_{c1}}^{T_{ch1}}$$

$$\alpha 11 = T_{c1} + \left(\frac{a}{b} + T_{c1} \right) \ln \left(\frac{a/b + T_{ch1}}{a/b + T_{c1}} \right) \qquad \text{(Eq. C-6)}$$

Using the definition of thermal resistance given in Eq. C-1 to solve for the linearized channel temperature we get:

$$\alpha 11 = T_{c1} + P_d \bullet \theta(\alpha 11) \qquad \text{(Eq. C-7)}$$

where $\theta(\alpha 11)$ is the linearized thermal resistance corresponding to the linearized channel temperature $\alpha 11$. This is the value which the thermal

resistance would have if the thermal conductivity of the material did not vary with temperature. We may express $\theta(\alpha 11)$ as:

$$\theta(\alpha 11) = R_{th}(T_{ch1}) \bullet G \qquad \text{(Eq. C-8)}$$

where $R_{th}(T_{ch1})$ is equal to the thermal resistivity of the material at a temperature of T_{ch1} ($R_{th}\{T_{ch1}\} = a + bT_{ch1}$), and G is a factor dependent on device geometry.

We want to find the channel-to-case thermal resistance, defined as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. C-9)}$$

Substituting Eq. C-7 into Eq. C-9 and solving for θ_{jc}:

$$\theta_{jc11} = (\theta_{jc}\,(T_{ch1}, T_{c1}) = \frac{T_{ch1} - T_{c1}}{P_d} = \frac{\Delta T_{11} \bullet \theta(\alpha_{11})}{\alpha_{11} - T_{c1}} \qquad \text{(Eq. C-10)}$$

where:

θ_{jc} = FET channel-to-case thermal resistance for $T_{ch} = T_{ch1}$ and $T_c = T_c$

ΔT_{11} = $T_{ch1} - T_{c1}$

Similarly, for $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$ we may write

$$\theta_{jc22} = \frac{\Delta T_{22} \bullet \theta(\alpha_{22})}{\alpha 22 - T_{c2}} \qquad \text{(Eq. C- 11)}$$

A multiplicative factor relating thermal resistance at $R_{ch} = T_{ch1}$ and $T_c = T_{c1}$ to the value at $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$ is found by taking the ratio:

$$R_{21} = \frac{\theta_{jc22}}{\theta_{jc11}} = \frac{\left(\dfrac{\Delta T_{22} \bullet \theta(\alpha 22)}{\alpha 22 - T_{c2}}\right)}{\left(\dfrac{\Delta T_{11} \bullet \theta(\alpha_{11})}{\alpha 11 - T_{c1}}\right)}$$

$$R_{21} = \left(\frac{\Delta T_{22}}{\Delta T_{11}}\right)\left(\frac{\theta(\alpha 22)}{\theta(\alpha 11)}\right)\left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}\right) \qquad \text{(Eq. C-12)}$$

Substituting Eq. C-5 and Eq. C-8 into Eq. C- 12 gives:

$$R_{21} = \left(\frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}}\right)\left(\frac{a + bT_{c2}}{a + bT_{c1}}\right)\left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}\right) \qquad \text{(Eq. C-13)}$$

As the active layer is very thin in comparison with the semi-insulating portion of the die, the values of a and b in Table C-1 for n = 5E16 are commonly used. Substituting these values into Eq. C-6 gives the linearized channel temperature, α 11, corresponding to $T_{ch} = T_{ch1}$ and $T_c = T_{c1}$:

$$\alpha 11 = T_{c1} + (246.7 + T_{c1}) \ln\left(\frac{246.7 + T_{ch1}}{246.7 + T_{c1}}\right) \qquad \text{(Eq. C-14)}$$

Similarly, at $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$:

$$\alpha 22 = T_{c2} + (246.7 + T_{c2}) \ln\left(\frac{246.7 + T_{ch2}}{246.7 + T_{c2}}\right) \qquad \text{(Eq. C-15)}$$

We may substitute the above values of α from Eq. C-14 and Eq. C-15 into Eq. C-13 to determine the thermal resistance at a new channel temperature, which is much more representative of the actual temperature which the DUT will see in normal operation. Examples demonstrating the use of Kirchoff's transformation in real-world situations commonly encountered by the power amplifier designer are given in Appendix B of this application note.

References

Part II

II-1 Microwave Semiconductor Corporation, “GaAs FET Thermal Resistance Measurement by IR Scanning”, MSC Tech. Rev. TE-212, Jan. 1980

II-2 F. N. Sechi, B.S. Perlman, J.M. Cusack, “Computer Controlled Infrared Microscope for Thermal Analysis of Microwave Transistors”, MTT-S, 1977, pp. 143-146

II-3 L.G. Walshack, W.E. Poole, Thermal Resistance by IR Scanning”, Microwave Journal, Feb. 1977, pp. 143-146

II-4 H. Boulton, “Testing Hybrids Using Thermography”, Hybrid Circuit Tech., July 1984, pp. 61-65

II-5 H. Fukui, “Thermal Resistance of GaAs Field Effect Transistors”, IEDM, 1980, pp. 118-121

Part III

III-I L. G. Walshack, W. E. Poole, “Thermal Resistance by IR Scanning”, Microwave Journal, February 1977, pp. 62-65

III-2 F. N. Sechi, B. S. Perlman, J. M. Cusack, “Computer Controlled Infrared Microscope for Thermal Analysis of Microwave Transistors”, MTT Symposium Digest, 1977, pp. 143-146

III-3 Microwave Semiconductor Corporation, “GaAs FET Thermal Resistance Measurement by IR Scanning”, MSC Technical Review TE-212

III-4 B. S. Siegal, “A Proposed Method for Testing Thermal Resistance of MESFETs”, Microwave Systems News, November 1977, p. 67

III-5 B. S. Siegal, “Use Electrical Tests for Thermal Measurements”, Microwaves, June 1967 p. 48

III-6 H. Fukui, “Thermal Resistance of GaAs FETs” IEDM, 1980, p.118

III-7 D. J. Channin, “Liquid Crystal Technique for Observing Integrated Circuit Operation”, IEEE Trans. Electron Dev., October 1974, pp. 650-652

III-8 J. McDermott, “Liquid-Crystal Troubleshooting Bares Faults in ICs, Antennas”, EDN, March 20, 1979, pp. 41-45

III-9 Rome Air Development Center, “Reliability Tests and Analysis of CMOS NOR Gates with Application of Nematic Liquid Crystal Failure Analysis Techniques.”, RADC In-house report AD-A028 519, June 1976

III-10 A. Aimth, I. Kudman, E. F. Steigmeier, “Electron and Phonon Scattering in GaAs at High Temperatures”, Phys. Rev., vol. 138, 1965, pp. A1270-A1276

III-11 J. S. Blackmore, “Semiconducting and Other Major Properties of Gallium Arsenide”, J. Applied Physics, vol. 53 no. 10, October, 1982, pp. 123-181

III-12 R. J. Johnson, “Thermal Rating of RF Power Transistors”, Motorola Application Note AN-790, Motorola RF Device Data Book, Motorola Corp., 1980, pp. 8-50 — 8-57

III-13 W. B. Joyce, “Thermal Resistance of Heat Sinks with Temperature Dependent Conductivity”, Solid-State Electronics, vol. 18, 321-322, 1975

III-14 M.M. Minot, “Thermal Characterization of Microwave Power FETs Using Nematic Liquid Crystals”, IEEE MTT Symposium Digest, June 1986, pp. 495-498

Part IV

IV-1 B. S. Siegal, “A Proposed Method for Testing Thermal Resistance of MESFETs”, Microwave Systems News, November, 1977, pp. 67-70

IV-2 B. S. Siegal, “Use Electrical Tests for Thermal Measurements”, Microwaves, June 1976, pp. 48-59

IV-3 D. L. Blackburn, “An Electrical Technique for the Measurement of the Peak Junction Temperature of Power Transistors”, Trans. Electron Dev., Vol. ED-23, no. 8 Aug. 1976, pp. 831-838

HEWLETT® PACKARD

IV-4 H. Fukui, “Thermal Resistance of GaAs Field Effect Transistors”, IEDM Transactions, 1980, pp. 118-121

IV-5 B. S. Siegal, “Measuring Thermal Resistance is the Key to a Cool Semiconductor”, Electronics, July 6, 1978, pp. 121-126

IV-6 A. H. Peake, C. G. Rogers, and P. M. White, “Improved Thermal Resistance Measurement Procedure for GaAs FETs using the Pulsed Electrical Method”, Semi-Therm Proceedings, 1984, sect. A.4

IV-7 A. Amith, I. Dudman, and E. F. Steigmeier, “Electron and Phonon Scattering in GaAs at High Temperatures”, Phys. Rev., vol 138, pp. A1270-A1276, 1965

IV-8 P. D. Maycock, “Thermal Conductivity of Silicon, Germanium, III-V Compounds, and III-V Alloys”, Solid-State Electronics, vol. 10, pp. 161-168, 1967

IV-9 J. S. Blakemore, “Semiconducting and Other Major Properties of Gallium Arsenide”, J. Appl. Phys., vol. 53, pp. R123-R181, Oct. 1982

IV-10 R. J. Johnsen, “Thermal Rating of RF Power Transistors”, Motorola RF Device Data Book, pp. 8-50 to 8-57, Motorola Corp

IV-11 W. B. Joyce, “Thermal Resistance of Heat Sinks with Temperature Dependent Conductivity”, Solid-State Electronics, vol. 18, pp. 321-322, 1975

Appendix C

C-1 A. Amith, I. Kudman, and E. F. Steigmeier, “Electron and Phonon Scattering in GaAs at High Temperatures”, Phys. Rev., vol 138, pp. A1270-A1276, 1965

C-2 P. D. Maycock, “Thermal Conductivity of Silicon, Germanium, III-V Compounds, and III-V Alloys”, Solid-State Electronics, vol. 10, pp. 161-168, 1967

C-3 J. S. Blakemore, “Semiconducting and Other Major Properties of Gallium Arsenide”, J. Appl. Phys., vol. 53, pp. R123-R181, Oct. 1982

C-4 R. J. Johnson, “Thermal Rating of RF Power Transistors”, Motorola RF Device Data Book, pp. 8-50 to 8-57, Motorola Corp

C-5 W. B. Joyce, “Thermal Resistance of Heat Sinks with Temperature Dependent Conductivity”, Solid-State Electronics, vol. 18, pp. 321-322, 1975

Acknowledgements

This paper could not have been prepared without the work of the following people: Maty Pardo, Raymond Basset, Charles Beck, John Telesco, Mark Swortwood and Jim Sterrett.

www.hp.com/go/rf

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Copyright © 1998 Hewlett-Packard Co.

Obsoletes 5091-6489E

5968-1410E (11/98)

HEWLETT PACKARD

High-Frequency Transistor Primer

Part IV

GaAs FET Characteristics

Table of Contents

I. Basic Terminology ... 1
II. Transistor Structure ... 2
- A. What is a GaAs FET? ... 2
- B. Active Layer Fabrication ... 2
- C. Metallization Systems ... 2
- D. FET Elements that Affect Microwave Performance ... 2
- E. Why a GaAs FET Instead of a GaAs Bipolar or Silicon Transistor? ... 3

III. How Does The FET Work? ... 3
IV. Electrical and Performance Characteristics ... 4
- A. Performance (Operating) Characteristics ... 4
  1. Noise Figure – NF_O ... 4
  2. Associated Gain at Noise Figure – G_A ... 5
  3. Maximum Available Gain – MAG ... 5
  4. Power Output ... 5
  5. Associated Small Signal Power Gain – G_P ... 5
  6. Power Added Efficiency – η_{add} ... 5
  7. Forward Transducer Gain – $|S_{21}|$ ... 5
- B. Electrical Characteristics ... 5
  1. DC Characteristics ... 5
     - a. Transconductance – g_m ... 6
     - b. Pinchoff Voltage – V_P ... 6
     - c. Saturated Drain Source Current – I_{DSS} ... 6
     - d. Low Field Channel Resistance – R_{do} ... 6
     - e. Breakdown Characteristics – BV_{GS}, BV_{GD}, I_{GS}, I_{GD} ... 6
  2. AC Characteristics ... 6
     - a. S-Parameters ... 6
     - b. Maximum Frequency of Oscillation – f_{max} ... 6
     - c. Gate-to-Source Capacitance – C_{gs} ... 7

V. Maximum Ratings
- A. Voltage Ratings ... 7
- B. Current Ratings ... 8
- C. Dissipation Ratings ... 8
- D. Channel Temperature Ratings ... 8
- E. Storage Temperature Ratings ... 8

VI. Glossary ... 9
VII. References ... 11

Introduction

This primer (number four in a series) offers a brief explanation of the terms commonly used in Hewlett-Packard GaAs FET data sheets, advertisements and other technical communications. Some of these terms are virtually self-explanatory and are included here primarily for the sake of completeness. Others are more specialized and potentially ambiguous due to a lack of terminology standardization among manufacturers and users of high-frequency transistors – the latter receive more thorough treatment here.

I. Basic Terminology

The last section of this primer is a comprehensive glossary of the important terms associated with GaAs FETs. To make it easier for the reader with little familiarity with GaAs FETs, however, a few of the most basic terms are presented here.

GaAs: Gallium Arsenide. A semiconductor compound.

FET: Field **E**ffect **T**ransistor. A type of transistor in which the current is controlled by the application of a varying electric field.

GaAs FET: A field effect transistor made from gallium arsenide.

Source, Drain and Gate: The three basic elements of an FET. Their functions will be explained in the text.

Epi layer: A very thin (***epi***taxial) layer of semiconducting GaAs grown on an insulating GaAs wafer.

Dopant: A material added to GaAs to make it semiconducting.

Schottky Barrier: A diode formed by a rectifying metal-semiconductor junction in which majority carriers carry the current flow. Used as the gate contact in GaAs FETs.

II. Transistor Structure

A. What Is a GaAs FET?

A basic depletion mode field effect transistor (FET) is a three port device in which the gate controls the flow of current from the source to the drain by varying the electric field and thus a depleted carrier region in the semiconducting epitaxial layer, beneath the gate (See Figure 1). A GaAs FET (or GaAs MESFET for **Me**tal **S**emiconductor) is simply an FET with a diode gate structure (similar to a junction FET, but a surface device) made from gallium arsenide (GaAs) which is a compound, as opposed to silicon, which is an element.

A FET is a semiconductor analog to a triode vacuum tube. The gate acts as the control element as does the grid in the triode. The source acts as the cathode and the drain as the plate (anode). The conductivity of the epi layer under the gate, and thus the flow of current, is varied by applying a voltage to the ***gate*** which is of negative polarity with respect to the ***source***, while in a triode vacuum tube the ***grid*** is biased negative with respect to the ***cathode***. The ***drain*** terminal of the FET is biased positive with respect to the ***source***, just as the ***plate*** of a triode is biased positive with respect to the ***cathode***.

B. Active Layer Fabrication

There are several ways to fabricate the semiconducting active layer of GaAs FETs. The two main approaches are: ***Epitaxial growth*** where the active layer of doping impurities is grown on the top of the substrate crystal by the liquid-phase, vapor-phase or molecular beam process; and ***Ion implantation*** where the doping impurities are injected directly into the crystal lattice of the substrate material (which may have an undoped epitaxial layer already fabricated – or implanted – on it by the vapor-phase process).

Hewlett-Packard presently uses two approaches for GaAs FET active layer growth: Vapor phase epitaxy (VPE) and ion-implantation (I^2). The DC and RF performance of devices produced by the two approaches is virtually the same.

C. Metallization Systems

The combination of metals used to make contact to the three GaAs FET device elements (source, gate and drain) is crucial to both the reliability and performance of the device. The source and drain contacts, through which ***all*** of the drain current flows, must be of ***very low*** resistance and high stability to insure optimum device performance. Hewlett-Packard presently uses a proven alloyed gold-germanium-nickel contact (Au-Ge-Ni) for contacts to GaAs FET source and drain elements.

Several different metal systems have been used by transistor manufacturers to make the Schottky-barrier diode gate contact; the two main approaches being aluminum and gold-based systems.

Aluminum creates a good Schottky barrier on GaAs, and aluminum atoms do not diffuse easily into the GaAs – such diffusion would change the device characteristics. However, aluminum is an active element and can form intermetallic compounds, particularly at the Au-Al interface, and is relatively susceptible to damage from electrostatic discharge and high RF energy levels. Gold, on the other hand, is the element which is most stable in the presence of oxidants, and is less susceptible to electrostatic or RF damage. It does, however, diffuse quickly into GaAs and, therefore, in order for gold to be used as a gate metal, barrier metals must be introduced between the gold and the GaAs. Hewlett-Packard uses titanium (Ti) and tungsten (W) as barrier metals in its gold-based gate metal system. This metallization has proven to provide both high reliability and excellent mechanical and electrical performance.

D. FET Dimensions Affecting Microwave Performance

The important dimensions in FETs are the spacing from the source to the gate, and from the gate to the drain. For microwave operations, the most critical dimension is the “length” of the gate along the carrier (electron) path. The shorter the gate length, the higher becomes the signal

frequency which can be controlled by the depletion layer set up in the active channel beneath the gate. The spacing between the gate electrode and the source, and gate and drain introduces capacitance. If the FET is to handle larger amounts of signal current, the gate width must be increased appropriately. Viewing the FET pictorially (Figure 1) helps to understand that the "width" dimension is perpendicular to the carrier flow along the length of the channel from source to drain. RF power handling capability is proportional to this gate width. In general, the transconductance (g_m) – the influence of gate voltage on drain current – and the capacitances increase proportionally with increasing gate width while the resistances vary inversely with the width. Doubling the gate width doubles the transconductance and the feedback capacitance and halves the resistance.

E. Why a GaAs FET Instead of a GaAs Bipolar or Silicon Transistor?

The advantage of GaAs over silicon is that with GaAs the carriers (electrons, or electrons and holes) can reach about twice the limiting velocity with one third the applied bias voltage. Therefore, for a given geometry, a given current gain can be reached at more than twice the frequency as with silicon. However, because of the more difficult physical chemical properties of GaAs, the variously doped layers of the bipolar structure (emitter, base and collector), would be difficult to form in GaAs (GaAs bipolar transistors would also be undesirable because of the low mobility of P-type GaAs material).

The structure used for GaAs FET fabrication, while somewhat similar to that of the silicon junction field-effect transistor – with a reverse-biased diode acting as the gate, and operation in the depletion mode – is totally a surface structure. There are no vertically diffused elements, such as the "buried" base layer between the emitter and collector which is used in a silicon bipolar transistor, or the "buried" channel in a silicon JFET. This is the only technique which can tap the advantages offered by GaAs with present fabrication technology. The FET surface structure can be used with GaAs and the necessary FET half-micron geometry for microwave frequency operation can be fabricated routinely with the present state of the art in optical photolithography techniques.

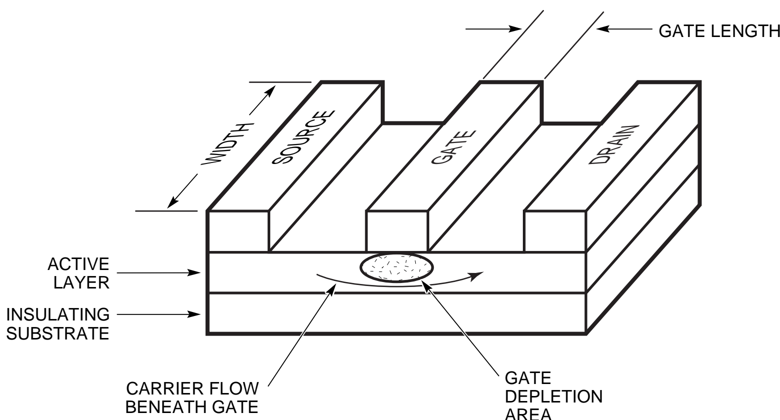


Figure 1. Basic GaAs FET Structure

There is one theoretical advantage of an FET structure as an amplifier, unrelated to the semiconductor material: the potential for low distortion. The FET is a square-law device, with its drain current proportional to the square of the ratio of the gate voltage to the pinchoff voltage.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$V_{GS(OFF)} = V_P = \text{Pinchoff Voltage} \quad (1)$$

This means that it generates little odd-order distortion, and that the small amount of even-order distortion that it does generate can easily be suppressed with a balanced-stage circuit design. An FET looks like a biased capacitor in a circuit, while a bipolar transistor looks like a forward-biased diode junction.

III. How Does the FET Work?

Gain in an FET is proportional to the channel conductivity (the "channel" being that area within the epi material under the gate). In a depletion mode FET (of which the GaAs FET is an example), as the gate is biased more negatively, the actual conducting channel cross-section is reduced, and the drain current is also reduced. A small negative voltage applied to the gate starts to "deplete" the channel of carriers, beginning immediately adjacent to the gate electrode at the top of the channel. As the gate voltage is made increasingly negative, the gate depletion layer is extended

further into the channel until it reaches the semi-insulating GaAs substrate. When the gate is made sufficiently negative, the channel is closed, or “pinched off”, and no current flows. The gate voltage at which drain current is stopped is called the ***pinchoff voltage*** (V_P).

Drain current will be highest, and the gain of the GaAs FET will be highest when the gate voltage is zero with respect to the source -- that is, with the gate connected directly to the source. This is the “saturated” drain-to-source current condition or I_{DSS}.

IV. Electrical and Performance Characteristics

Electrical characteristics may be described as uniquely defined, measurable electrical properties of the transistor which are not a function of the measuring circuit of apparatus (except insofar as standard terminations and measurement accuracy are concerned). Performance or operating characteristics are also electrical properties, but they are, in general, not unique because their values depend upon the measuring circuit (in particular, the source and load impedance, which may be arbitrary). As might be expected, these terms are often used somewhat loosely (and sometimes interchangeably), especially in cases where there are only subtle differences involved. The terms are generally used on transistor data sheets to segregate (for emphasis) under performance or operating characteristics those properties most directly applicable to the expected application.

A. Performance (Operating) Characteristics

The most fundamental characteristics specified for microwave GaAs FETs are:

1. Noise Figure
2. Gain at Noise Figure
3. Maximum Available Gain
4. Linear Power Output
5. Associated Small Signal Power Gain
6. Efficiency
7. Forward Transducer Gain

All of these characteristics are, of course, functions of frequency, bias, temperature, etc., and to completely characterize a transistor over its full frequency, bias and temperature ranges would be prohibitively costly. Consequently, characterization data is given only for restricted ranges of these variables. This data should portray sufficiently the capabilities of a particular device for its primary intended applications. As in the case of maximum ratings, some applications may require additional characterization by the user or applications assistance from the manufacturer.

1. ***Noise Figure*** – NF_O

Noise factor is a numerical value which is the common measure of the noise generated by an active two-port device – noise which sets a lower limit on amplifier sensitivity. This may be defined as:

$$F = \frac{\text{Input Signal-to-Noise Ratio}}{\text{Output Signal-to-Noise Ratio}} \qquad (2)$$

or, more generally,

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power Due To Signal Source Resistance}} \qquad (3)$$

At high frequencies, the spot noise factor, or noise factor at a small bandwidth (say 1%), is used, and is usually expressed as noise figure, NF, in decibels, e.g.

$$NF = 10 \text{ Log } F \qquad (4)$$

As already discussed, noise figure is a function of source impedance (as well as being a function of frequency, bias, etc.), and hence there is an infinity of noise figures associated with a given device corresponding to the infinity of possible impedances which may be presented to the device output. The only unique noise figure, in the sense that it does not involve arbitrary source impedances, is NF_O, the minimum noise figure obtained (at given bias and frequency) when the input is tuned to optimize this parameter. It is this noise figure which is usually given on Hewlett-Packard data sheets.

In practical amplifiers, involving more than one stage, the overall ***numeric*** noise measure, F_m, is given by:

$$F_m = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_n - 1}{G_{(n-1)}} \qquad (5)$$

n = Number of Stages,
G = Gain of nth Stage,
F_n = Noise Factor of nth Stage

This expression emphasizes the important fact that for low noise

amplifiers the first stage must be designed for the lowest noise figure and highest gain possible. Note that the noise contribution of the second stage is divided (reduced) by the gain of the first stage. Since the optimum source impedances and bias currents for optimum gain and noise figure do not often coincide, very careful circuit design is required to minimize overall noise figure.

2. *Associated Gain at Noise Figure* – G_A

This gain is simply the small-signal gain that results from optimum noise figure tuning of the circuit in which the device is installed. Best noise matching of the input of the transistor does not necessarily coincide with conjugate input S-parameter match (S_{11}*), and therefore gain at noise figure is usually lower than the maximum available gain.

3. *Maximum Available Gain* – MAG

Of the various definitions for the measure of power flow in an active two-port device, such as a transistor, two are unique enough to allow specification without recourse to specifying the complete measuring circuit in detail. One of these definitions is termed maximum available gain, MAG. It is the power gain obtained when the input and output ports are simultaneously conjugately matched to source and load impedances, respectively. Implicit in the definition is the assumption that the two-port device is unconditionally stable: i.e., no combination of input and output tuning can result in increasing the gain of the device to the point of oscillation.

The other definition of power flow is Maximum Stable Gain or MSG. This definition is used when stability is only conditional and is the maximum gain possible with stable operation.

4. *Power Output*

This characteristic is important for both amplifier and oscillator transistors. In both cases, it is extremely circuit sensitive. For amplifiers, the maximum useful power output is often limited to that power output level ($P_{1\,dB}$) at which gain has compressed 1 dB ($G_{1\,dB}$), an indicator of the upper limit of linearity range, or may be specified at a greater gain compression, such as 2 dB or 3 dB (P_{sat}), when output power is more important than linearity. For oscillators, power output is merely a quantitative measure of RF power output for a given DC input power.

5. *Associated Small Signal Power Gain* – G_P

This gain is determined by decreasing the input power to the point that the device is operating in its linear region and then measuring the gain. This gain level will be lower than MAG primarily because the output is conjugately matched for large signal conditions and some mismatch occurs when signal levels are reduced.

6. *Power Added Efficiency* – η_{add}

The most commonly used efficiency expression for GaAs FET power devices is the *power added efficiency* which is defined as:

$$\eta_{add} = \frac{P_O - P_{IN}}{P_{dc}} \bullet 100\% \qquad (6)$$

where

P_O = R_F Output Power
P_{IN} = R_F Input Power
P_{dc} = Total DC Input Power (7)

7. *Forward Transducer Power Gain* $|S_{21}|^2$

The other unique power gain is the gain realized when the transistor is inserted between a source and load with identical impedances (in practice usually 50 + j0 ohms). This particular insertion or transducer gain happens to coincide with the usual definition of the two-port forward scattering parameter, S_{21}. More precisely, it is equal to the magnitude-squared of this parameter and is therefore often identified by the symbol $|S_{21}|^2$. For wideband applications, $|S_{21}|^2$ is important since wideband terminations “not-too-different” from 50 ohms are more easily realized than are wideband transforming networks which provide the precise matching required for MAG.

B. Electrical Characteristics

Electrical characteristics may be conveniently classified into two types, DC and AC.

1. *DC Characteristics*

The importance of DC characteristics of high frequency transistors lies primarily in biasing and reliability considerations. However, certain DC characteristics are also directly related to high frequency performance. For example, high-frequency noise figure is affected by the DC current gain. The DC characteristics which are discussed here are those usually found on high-frequency transistor data sheets.

a. *Transconductance* – g_m

This parameter is the DC common-source conductance; that is the incremental change in output (drain) current with a given change in input (gate) voltage. It is usually specified at either I_{DSS} (gate voltage = 0 V) or one-half I_{DSS} although any current value or specified percentage of I_{DSS} can be used as the measurement point.

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \tag{8}$$

b. *Pinchoff Voltage* – V_P

This parameter is the gate voltage at which the drain-to-source current is reduced to some given value (usually 1 mA for small signal FETs and 5 mA for power FETs). See point A on the curves in Figure 2.

c. *Saturated Drain-to-Source Current* – I_{DSS}

This current occurs when the gate-to-source voltage is held to zero and the drain-to-source voltage set to a specified (usually 3 volts) value. See point B on Figure 2 curves.

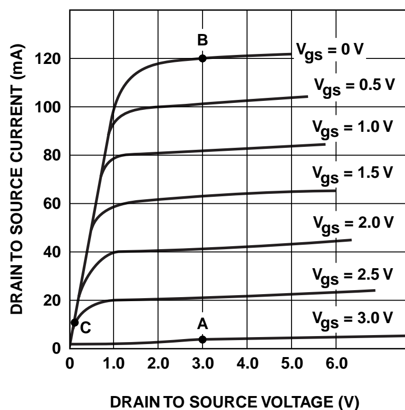


Figure 2. Typical GaAs FET DC Characteristic

d. *Low-Field Channel Resistance* – R_{do}

This is the slope of the drain I-V characteristic near the origin of the curve and is an indicator of the active channel resistivity and the drain and source contact quality. See the region around point C on Figure 2 curves.

e. *Breakdown Characteristics*

The breakdown characteristics of the gate contact can be measured in both directions (gate-to-drain and gate-to-source). In general, since the device is close to physically symmetrical, only one of the two is needed to verify device quality. Most often the gate-to-drain characteristics are used. There are two ways of characterizing the breakdown characteristics: Specifying the gate-to-drain current and measuring the voltage at that point (BV_{gd}), or specifying the voltage and measuring the reverse current (I_{gd}). In either case they are go-no-go type tests, failing when either the reverse current exceeds the specified value or the breakdown voltage is lower than the specified value, and are non-destructive as long as the current levels are kept low (in the µA range).

2. *AC Characteristics*

Of the numerous AC characteristics which are defined for transistors, only relatively few are commonly used in characterizing high-frequency transistors. Some of the more pertinent parameters are briefly covered here.

a. *S-Parameters*

The standard definitions of S-parameters are covered in a variety of sources including volumes one and two of this Primer series. That information will not be repeated here. What will be discussed is the measurement technique and fixturing utilized in Hewlett-Packard's transistor S-parameter measurements.

Packaged device S-parameters are measured in 50 ohm test fixtures* using Hewlett-Packard's TFP microstripline or TF coaxial test fixtures. The test fixture introduces errors which can be corrected by either a reference plane extension or a THRU/DELAY calibration[1]. The most accurate data for frequencies above 6 GHz uses the THRU/DELAY calibration, which is also referred to as de-embedded S-parameter data. This is the data in the Hewlett-Packard RF Semiconductor Designers Catalog.

Chip devices are measured in the 50 ohm microstripline test fixture shown in Figure 3. The S-parameter data should be de-embedded for frequencies above 6 GHz. At present, bonding wire inductances are *not* subtracted out of the chip S-parameter values. A sketch of the standard chip test carrier is shown in Figure 3.

b. f_{max}

The maximum frequency of oscillation, f_{max}, is the frequency at which a curve of unilateral power gain (U) vs. frequency intercepts zero dB gain. The gain of both bipolar and FET transistors drops at a rate of approximately 6 dB per octave in the microwave region. If gain is measured at convenient frequencies between 2 and 12 GHz

* TFP test fixtures and de-embedding software are available from *Intercontinental Microwave*, 2370B Walsh Ave., Santa Clara, CA 95051.

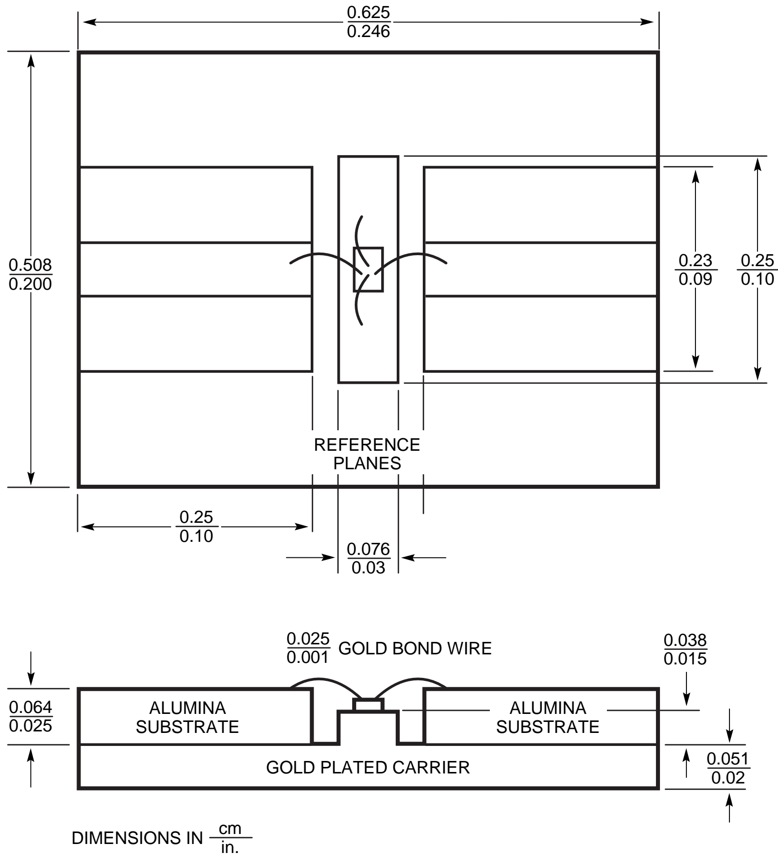


Figure 3. Test Carrier Used to Characterize Unpackaged GaAs FET Chips

the points will approximately fit a straight line curve when gain in dB is plotted on a linear vertical scale against frequency plotted on a log scale horizontally. The frequency at which the unilateral power gain extrapolates to 0 dB gain is f_{max}.

c. *Gate-to-Source Capacitance* – C_{gs}

This capacitance measurement is usually made at 1 MHz, and varies with the value of DC voltage applied to the gate. A zero-volt measurement is used most often to give an idea of the gate metallization area or, more precisely, the gate length. For a given device gate width, the capacitance is directly proportional to gate length. A negatively-biased gate will result in a lower value of capacitance, because carriers have been depleted in the region under the gate. This value is more useful in estimating the gate capacitance for RF performance or device modeling.

V. Maximum Ratings

(Also refer to ***Hewlett-Packard High-Frequency Transistor Primer, Part I***, Section II for additional information.)

In addition to the normal maximum ratings defined for GaAs devices, which limit externally-applied stress to values below those which, if exceeded, may result in irreversible damage to the device, some manufacturers are including ratings called “recommended maximums for continuous operation.” This latter set of ratings may be interpreted as the values above which the life expectancy of the device may be shortened. Of course, in situations where the device lifetime is less important than achieving the maximum possible performance, these ratings may be intentionally exceeded through any combination of temperature, voltage or current conditions.

The following parameters normally appear on Hewlett-Packard GaAs FET data sheets, and provide adequate information for most applications.

A. Voltage Ratings

GaAs FET voltage ratings are usually derived from, and usually coincide with, the minimum device breakdown voltages. However, since this is not ***always*** true, it has become common practice to include both maximum voltage ratings and minimum breakdown voltages on data sheets.

It can be argued that such practice erodes the meaning of maximum ratings. Since, strictly speaking, maximum ratings should not be exceeded under any circumstances, strict adherence to the voltage ratings would preclude the measurement of the breakdown voltages of any but marginal devices. In fact, drain-to-source breakdown voltage measurements may be destructive tests except when conducted using a sophisticated pulsed measurement technique. Gate-to-source and gate-to-drain breakdown voltages can be measured without damage to the device, since there is no avalanche characteristic in these breakdown phenomena.

B. Current Ratings

The maximum current ratings for GaAs FETs are derived from a number of considerations, including the current-carrying capacity of the bonding wires and the performance degradation which can be produced by excessive current causing physical changes in the active region. Maximum ratings are normally only specified for *drain* current.

C. Dissipation Ratings

Besides the individual voltage and current ratings, there is also a limit to the product of voltage and current which can be safely handled by a GaAs FET. That is, there is a power dissipation rating which must be adhered-to for any device. Since the power dissipation capability of a GaAs FET is a function of the temperature of the external environment, the power dissipation rating is specified at a specific temperature or over a stated temperature range. For the DC case, this is usually the only significant functional dependence.

In the AC case, device dissipation varies significantly with time, so that power dissipation capability becomes a generally complex function of the signal waveform. Due to the complexity of the general AC case, transistors are seldom characterized completely enough to include complete AC power dissipation rating information. Most transistors are rated only in terms of maximum continuous dissipation – the maximum DC and maximum average dissipation. This rating is typically specified in terms of a maximum continuous dissipation at or below a stated reference temperature (usually 25°C), with a linear derating factor to be applied at higher temperatures.

Two external temperature reference points are commonly used. The one which is the more valid depends on the application. They are:

1. ***Air ambient***, T_A, also known as free air temperature, since no forced-air or other “artificial” cooling is applied to the transistor. This is the air temperature in proximity to the transistor case as mounted in its normal manner.
2. ***Case ambient***, T_C, which is the temperature of the point on the transistor package at which a heatsink is the most effective in reducing temperature.

D. Channel Temperature Rating

Another temperature reference point implicit in the previously-mentioned ratings, is the actual temperature at the transistor channel. The maximum internal reference temperature $T_{ch\ (max)}$ corresponds to the maximum channel temperature, since at $T_{ch\ (max)}$, the power dissipation of the transistor must be derated to zero. Strictly speaking, channel temperature is not properly classified as a ***maximum*** rating, since it is not an external stress under the direct control of the user – as opposed to power dissipation and external operating temperature which ***are*** user-controlled.

Thus, a more appropriate term for this rating would be ***maximum operating temperature.*** However, since it is a limiting factor in the transistor power dissipation capability, and since its use simplifies time-varying thermal analysis, this rating still appears on many transistor data sheets.

One key factor that should be kept in mind when specifying operating bias and calculating channel temperature is that the thermal resistance of GaAs is not constant with temperature. The thermal resistance from channel to case is a function of temperature and varies directly as the thermal resistance of bulk GaAs. This temperature variation can be approximated as:

$$\theta_{jc} = \theta_{jc}\left(60°C\right) \left\{1 = 0.00355\left(T_{CH} - 60°C\right)\right\} \quad (9)$$

where T_{CH} equals channel temperature and θ_{jc} (60°C) is the channel-to-case thermal resistance at a T_{CH} of 60°C. For a more complete discussion of thermal resistance, refer to Hewlett-Packard’s ***High Frequency Transistor Primer Series, Part III (Thermal Properties) and Part IIIA (Thermal Resistance)***.

E. Storage Temperature Rating

This rating defines the range of temperature over which the transistor may be stored in a non-operating condition, without damage. Because of possible electrical-temperature interactions, the storage temperature range and operating temperature range do not necessarily coincide. In practice, however, they usually ***do*** coincide and, in the absence of stated restrictions on operating temperature range, storage temperature range may be taken to be the operating temperature range as well.

VI. Glossary of GaAs FET Terms

Active layer
The doped layer of gallium arsenide (GaAs) through which the electrons flow in a GaAs FET and upon which the source, gate and drain electrodes are placed. The region between the source and drain electrodes is known as the channel.

Avalanche breakdown
The application of excessive voltage to a semiconductor material creates an excess of high-energy (or hot) electrons. These electrons can excite additional carriers into a high-energy state, which makes the semiconductor more conductive and can, with the same voltage applied, result in a high current flow with resulting destructive breakdown of the material. Drain-to-source breakdown in a GaAs FET is an avalanche effect.

Bipolar
Refers to a transistor in which both majority and minority carriers (electrons and holes) carry current, and which is formed with PN junctions.

Breakdown voltage
The reverse bias voltage at which a rectifying junction begins to conduct a large reverse current (higher than normal reverse leakage). Reverse breakdown can be caused by avalanche breakdown (see entry) or by other electrical or thermal effects. Gate-to-source and gate-to-drain breakdown in a GaAs FET are not avalanche effects, and may take place without damage to the device so long as the reverse current is limited to a safe value.

BV_{GD}
Breakdown voltage, gate-to-drain – The reverse breakdown characteristic of the gate-drain Schottky-barrier diode in a GaAs FET. BV_{GD} is usually specified at some specific value of leakage current.

BV_{GS}
Breakdown voltage, gate-to-source – The reverse breakdown characteristic of the gate-source Schottky-barrier diode. BV_{GS} is usually specified at some value of leakage current.

Depletion layer
The portion of the epitaxial layer that lies directly beneath the gate of an FET and becomes depleted of carriers (electrons) when a negative bias is applied to the gate.

Dopant
A substance added to GaAs (or silicon or other transistor base material) to make it semi-conductive.

Drain
The terminal of an FET to which electrons flow. (See also: source, gate)

C_{GS}
Capacitance, gate-to-source – The capacitance that exists between the gate and source electrodes in a GaAs FET, and which is dependent on the Schottky diode characteristics and applied bias voltage.

Conjugate match
A transistor input or output port is conjugately matched when connected to an impedance which has the same resistance as the transistor port and a reactance of the same magnitude but opposite sign. This means that the reactances cancel, and that maximum power transmission takes place and that there is no mismatch loss.

Epitaxial (epi) layer
A doped layer of GaAs grown on top of the substrate crystal as a continuation of the crystal lattice structure. Gallium, arsenic and other dopants are carried to the substrate surface in a variety of ways, including liquid-phase, vapor-phase and molecular beam approaches.

f_{max}
Maximum Frequency of Oscillation – The frequency at which the unilateral power gain (U) of a transistor approaches unity.

FET
Field Effect Transistor – A unipolar device in which the number of carriers available to carry current in the conducting region is controlled by the application of an electric field to the surface (in the form of a capacitor or reverse-biased diode junction) of the semiconductor. As a unipolar device, the current in an FET is carried only by the free majority carriers (in an N-channel FET, ***electrons***) in the conducting channel and there is little or no current carried by the minority carriers (in an N-channel FET, ***holes***). Compare this to the bipolar transistor in which both positive and negative free carriers carry approximately equal current.

GaAs
Gallium Arsenide – A type III-V (from the periodic table) compound of gallium and arsenic which has a resistivity sufficiently high to fabricate field-effect

transistors. Compared to silicon, the free carriers can reach about twice the limiting velocity with one-third the applied voltage.

GaAs FET
A field effect transistor made of gallium arsenide.

Gate
The terminal of an FET that controls the flow of current from the drain to the source. (See also: drain, source)

Gate length
The distance along which the electrons must travel when moving from source to drain. That is, length is the ***shorter*** of the two gate dimensions (gate width is the longer dimension). The frequency response of a GaAs FET, with all other things equal, is inversely proportional to its gate length.

Gate width
The size of the GaAs FET channel that carries current. That is, width is the longer of the two gate dimensions (gate length is the shorter dimension). The power handling capacity of a GaAs FET, with all other things equal, is directly proportional to its gate width.

$G_{1\ db}$
1 dB gain compression point -- The level of gain from a device which is 1 dB less than the gain measured under small signal conditions when the device is tuned at $G_{1\ dB}$. This is usually considered to be the upper limit of linear amplification. See also $P_{1\ dB}$.

g_m
DC transconductance, which is the ratio of the change in the drain current to changes in gate voltage:

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \qquad (10)$$

G_{NF}
Small signal gain, resulting from tuning for optimum noise figure. Also designated: G_A.

G_P
Small signal gain, resulting from tuning for optimum output power.

G_T
Transducer power gain – The insertion power gain of a transistor, with no assumptions made concerning S_{12}, S_{11}, S_{22} or the source or load impedances. The maximum value of G_T for an unconditionally stable transistor is MAG. $|S_{21}|^2 = G_T$ when the source and load impedances equal 50 Ω.

G_{Tu}
Unilateral transducer power gain – Transducer power gain with S_{12} assumed equal to zero.

I_{DSS}
Saturated drain-to-source current – The current that results from a given voltage applied to the GaAs FET with the gate voltage held at zero.

I_{GD}
Gate-to-drain leakage current at a stated reverse gate-to-drain voltage.

I_{GS}
Gate-to-source leakage current at a stated reverse gate-to-source voltage.

Implanted layer
An active layer formed by the implantation of dopants directly into the substrate crystal, or an insulating layer produced by vapor-phase epitaxy.

MAG
Maximum available gain, at a frequency where the transistor is unconditionally stable and the input and output ports are simultaneously conjugately matched. Also designated: $G_{A\ (max)}$, G_{max}.

MESFET
Metal Semiconductor Field Effect Transistor – A GaAs FET can more formally be described as a GaAs MESFET.

NF_O
A measure of the noise generated by a transistor when tuned for minimum noise figure at a given frequency. Also designated NFmin and NFopt.

NF_{50}
Noise figure of a transistor at a given frequency, when inserted in an untuned 50 ohm circuit. This figure is most often used for the calculation of noise resistance.

$P_{1\ dB}$
Power output at the 1 dB gain compression point – Essentially the maximum output power available from the transistor while providing linear amplification. Also designated: P_{OUT}, $P_{O\ -1\ dB}$, and in numerous other ways. See also $G_{1\ db}$.

P_{sat}
Saturated power output – Usually specified at some level of small signal gain compression, such as 2 dB or (most usually) 3 dB.

P_{max}
Maximum continuous power dissipation at or below a stated reference temperature (usually 25°C), or linearly derated at a higher ambient temperature.

R_{do}
Low field drain-to-source resistance – The slope of the drain I-V characteristic near the origin of the curve, and an indicator of the active channel resistivity and the drain and source contact quality.

R_N
Equivalent noise resistance, used in the GaAs FET model to predict noise figure performance.

S_{11}
S-parameter input reflection coefficient – Expresses the magnitude and phase of the input match with respect to a pure resistance of 50 ohms.

S_{12}
S-parameter reverse transfer coefficient – Expresses the reverse isolation magnitude and phase, measured with the input terminated in 50 ohms.

S_{21}
S-parameter forward transfer coefficient – Expresses the forward gain amplitude and phase, measured with the input terminated in 50 ohms.

S_{22}
S-parameter output reflection coefficient – Expresses the magnitude and phase of the output match with respect to a pure resistance of 50 ohms.

Schottky diode
A rectifying junction formed by depositing a layer of metal onto the surface of a semiconductor. This creates an electrostatic barrier which gives the metal-semiconductor interface rectifying properties, with the metal acting as the anode and the N-type semiconductor as the cathode. Since the Schottky diode is a surface device, and since its metal layer can be fabricated at the same time as ohmic (drain and source) contacts, it is used to provide the gate structure of GaAs FETs. Also designated: Schottky-barrier diode, metal-semiconductor diode, hot-carrier diode.

Source
The terminal of an FET from which electrons flow (see also: drain, gate).

T_{ch}
Channel Temperature – The measured or estimated temperature of the GaAs FET channel under operating conditions.

T_{stg}
Storage Temperature – For an unbiased transistor.

V_P
Pinchoff Voltage – The gate-to-source voltage at which the drain current is reduced to some small, specified level. Also known as $V_{GS(OFF)}$.

Pinchoff Voltage
See: V_P

Transconductance
See: g_m

U
Unilateral Power Gain – The power gain of a transistor amplifier when lossless feedback has been used to neutralize the reverse transfer coefficient (S_{12}) to zero; the input reflection coefficient (S_{11}) has been matched to zero with lossless circuit elements; and the output reflection coefficient has been matched to zero with lossless circuit elements. The unilateral power gain is the highest power gain which can be achieved from the transistor, and the frequency where this gain is unity (or zero dB) is f_{max}.

Γ_o
Optimum Source Reflection Coefficient – The input source reflection which results in the lowest device noise figure. This value does not coincide with the S_{11} conjugate match. Also sometimes designated Γ_{opt}.

η_{add}
Power Added Efficiency – The ratio of RF power output minus RF input power to the DC input power:

$$\eta_{add} = \frac{P_O - P_{IN}}{P_{dc}} \bullet 100 \qquad (11)$$

VII. References

1. ***Measurement and Modelling of GaAs FET Chips,*** Hewlett-Packard Application Note ATP-1054, 0ctober, 1983.

www.hp.com/go/rf
For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Copyright © 1997 Hewlett-Packard Co.

Obsoletes 5963-2025E

Printed in U.S.A. 5966-0779E (9/97)