PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

NJ8812

CONTROL CIRCUIT FOR FREQUENCY SYNTHESIS

The NJ8812 is an N-channel MOS integrated circuit that provides all the decoding and controlling circuitry for frequency synthesisers. It is intended to be used in conjunction with a 2-modulus prescaler such as the SP8793 to produce a universal binary coded synthesiser for mobile radio applications.

FEATURES

- High Frequency Range
- Low Pin Count
- Direct Interface to ROM or PROMS
- Preset Channel Spacings 20, 25, 30 kHz and Sub Multiples.
- High Comparison Frequency.
- Low Level Sinewave Crystal Oscillator Input up to 10 MHz.
- Systems Clock Available — Constant Data Select Frequency of 1.2kHz. (Reference Oscillator = 4.8 MHz)
- Microprocessor Compatible.

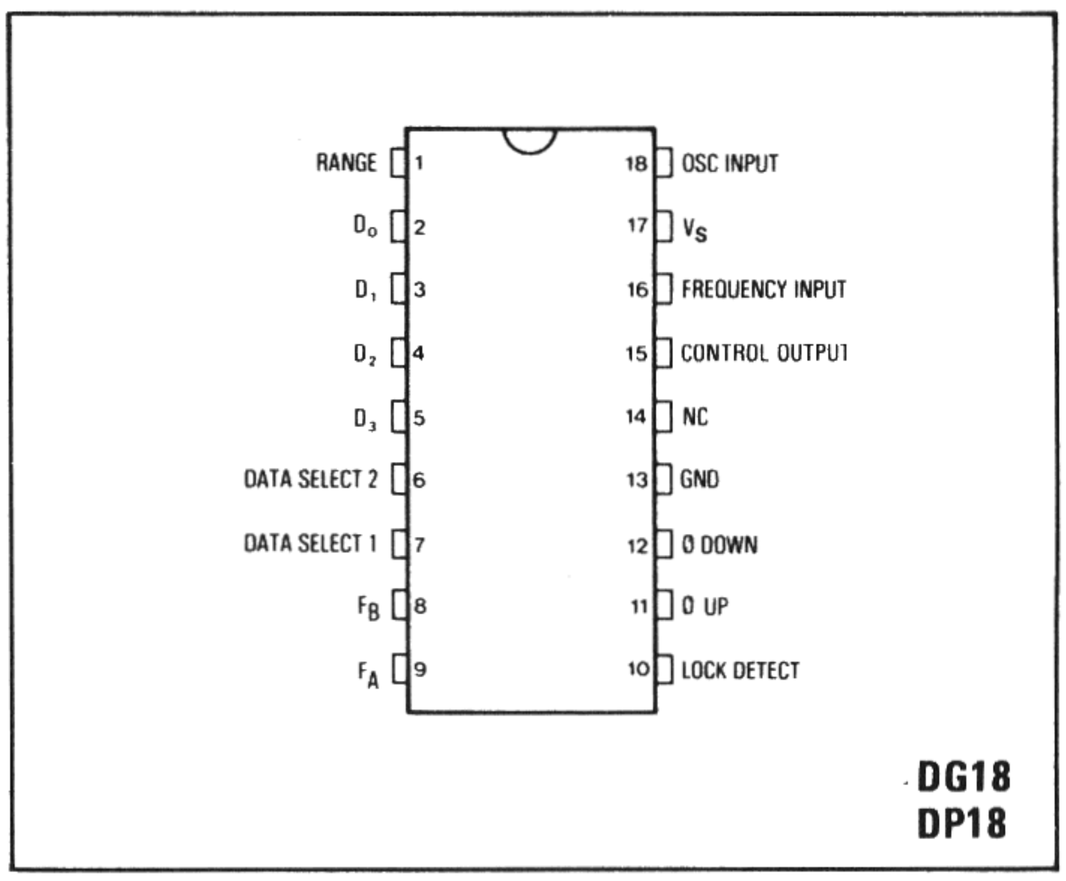

Fig.1 Pin connections

GENERAL DESCRIPTION

The NJ8812 can be described by 3 system blocks: the reference divider, the programmable divider and the phase/frequency comparator, as shown in Fig.2. All control inputs and outputs are TTL compatible.

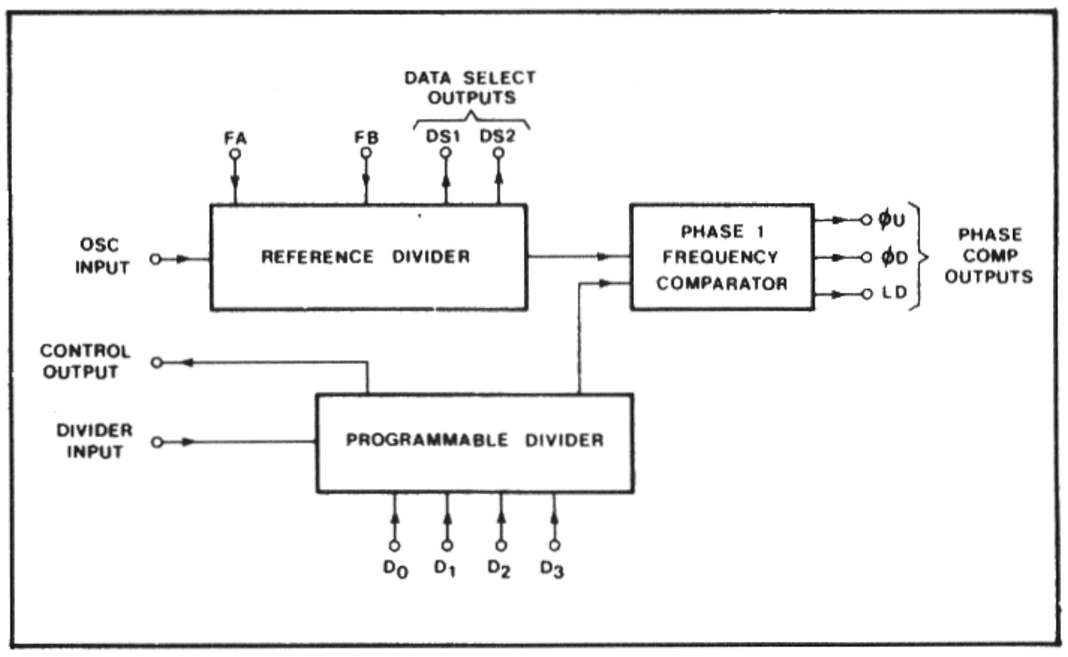

Fig.2 NJ8812 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_S: 5.0V ±0.25V
Temperature range: −30°C to +70°C

Characteristic	Value			Units	Conditions
	Min	Typ.	Max		
Oscillator input	50		200	mV RMS	4.8MHz reference oscillator AC coupled sinewave FA, FB O/C.
Max. oscillator input frequency	10			MHz	200mV RMS sinewave.
Supply current		8.0	12	mA	All data inputs O/C.
Max. counter input frequency	5.0			MHz	Input TTL compatible.
DS1/DS2 Output					
High Level	2.4			V	Outputs TTL compatible.
Low Level			0.4	V	
Phase comparator output current sink	1			mA	$Ø_U$ $Ø_D$ 0.5V max.

The Reference Divider

The reference divider is driven externally from a 4.8MHz crystal oscillator and can be externally preset to one of sixteen division ratios. These division ratios enable all commonly used reference frequencies to be applied to the phase/frequency comparator. Selection is accomplished using the two pins FA and FB. These pins may be connected to ground (logic '0') or left open circuit (logic '1'), connected to Data Select 1 output or to Data Select 2 output. On-chip decoding enables the latter two states to be recognised as independent states. All sixteen selections may be latched on-chip by grounding the Data Select 2 output. Table 1 gives reference frequencies that can be preset using a 4.8MHz crystal oscillator.

The data select outputs (crystal oscillator frequency ÷4096) are independent of the preset reference frequency.

Programmable Divider

The programmable division section of the NJ8812 consists of a 6-bit programmable divider and an 8-bit programmable divider. The 6-bit divider controls the modulus of the external prescaler and the 8-bit counter determines the total count period. The SP8793/NJ8812 combination is capable of dividing by all integer values between 1600 and 11839. When the Range pin on the NJ8812 is grounded the programme range is shifted to between 6720 and 16959.

The programming data is multiplexed as 3 words of 4 bits and 1 of 2 bits completing a 14-bit binary number. This input data may be stored on chip by grounding the Data Select 2 output after data transfer has occurred (See Fig.4). All on-chip multiplexing may then be inhibited, if desired, by grounding Data Select 1 output.

Phase/Frequency Comparator

The outputs of the fixed and variable dividers on the NJ8812 are internally connected to a phase/frequency comparator. The comparator provides three open drain outputs. The logic diagram is shown in Fig.3.

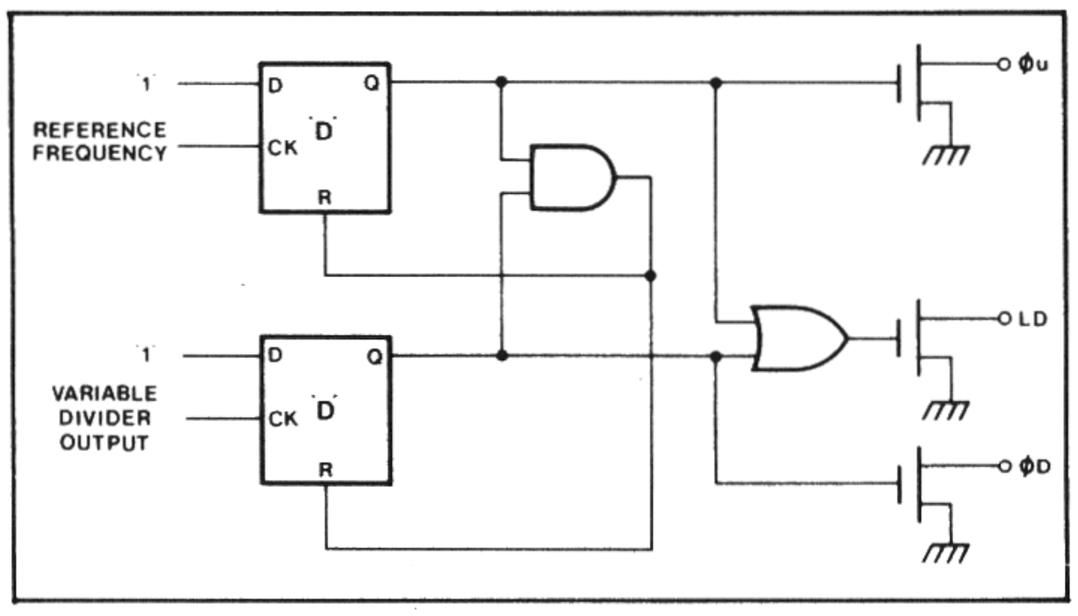

Fig.3 Logic diagram

Data Selection

To programme the synthesiser the following information is required:

1. The reference comparison frequency — typically equal to the channel spacing.
2. The frequency of the VCO.

The frequency programme information is presented to the device in multiplexed form. The reading of this data by the device is controlled by the two data select outputs from the device. This sequence is shown in Fig.4.

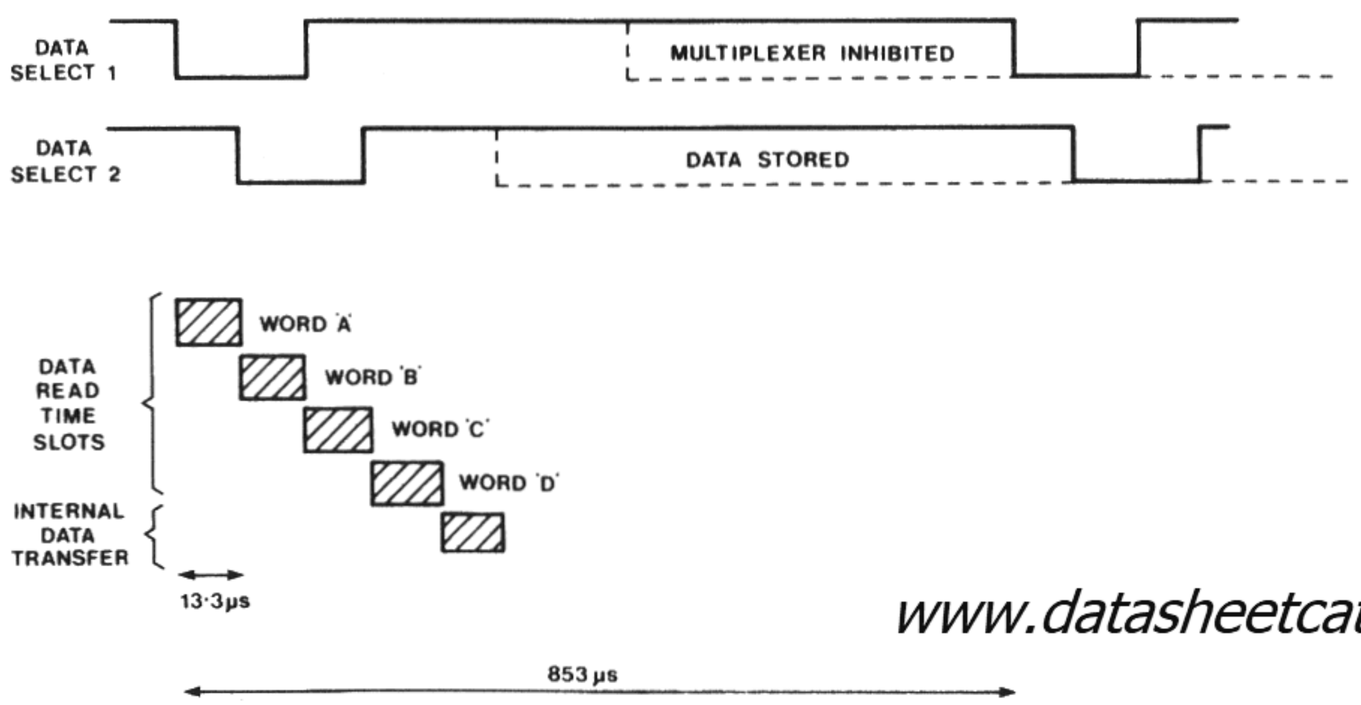

Fig.4 Data Read timing diagram

FB \ FA	GND	O/C	DS1	DS2
Gnd	20	10	5	2.5
O/C	25	12.5	6.25	3.125
DS1	30	15	7.5	3.75
DS2	37.5	18.75	9.375	4.6875

Table 1 Reference frequency selection (all frequencies in kHz) (4.800MHz crystal)

Channel Spacing	20kHz	25kHz	30kHz
Low Range (MHz)	32.0—(200)	40.0—(200)	48.0—(200)
High Range (MHz)	134.4—(200)	168.0—(200)	

Channel Spacing	10kHz	12.5kHz	15kHz
Low Range (MHz)	16.0—118.4	20.0—148.0	24.0—177.6
High Range (MHz)	67.2—169.6	84.0—(200)	100.8—(200)

Channel Spacing	5kHz	6.25kHz	7.5kHz
Low Range (MHz)	8.0—59.2	10.0—74.0	12.0—88.8
High Range (MHz)	33.6—84.8	42.0—106.0	50.4—127.2

Channel Spacing	2.5kHz	3.125kHz	3.75kHz
Low Range (MHz)	4.0—29.6	5.0—37.0	6.0—44.4
High Range (MHz)	16.8—42.4	21.0—53.0	25.2—63.6

Table 2 Frequency programme range

To calculate the Programme number for a given VCO frequency and channel spacing the following equation is used:

$$\text{Programme Number } N = \frac{1000 \times f}{C} - R$$

where f = VCO frequency in MHz
C = channel spacing in kHz
R = range number (R = 1600 range = 1)
(R = 6720 range = 0)

The programme number is converted to a 14 bit binary number and is segregated as 3 words of 4 bits and 1 word of 2 bits.

The least significant word is first entered during the Data Read 1 time slot via the inputs D_3, D_2, D_1 and D_0 and the most significant last (Data Read 4 time slot).

The second least significant word contains only two bits entered via the inputs D_1 and D_0. Data presented to the inputs D_2 and D_3 during the second time slot is ignored by the NJ8812.

For example, with a VCO frequency of 121.2MHz and channel spacing of 50.0kHz

f = 121.2
C = 50.0
R = 1600
N = 824

Conversion to a 14-bit binary number is performed as follows:

	Result
1. Divide by 640	1.2875
2. Write down number before decimal place (WORD 'D')	1
3. Subtract this number	0.2875
4. Multiply by 16	4.60
5. Write down number before decimal place (WORD 'C')	4
6. Subtract this number	0.60
7. Multiply by 40	24.0
8. Write down nearest whole number (WORD 'A + B')	24

The three decimal numbers obtained may now be directly converted to binary, and these are presented to the data inputs as shown in Table 3.

DS1	DS2	D_3	D_2	D_1	D_0	
0	1	1	0	0	0	WORD 'A'
0	0	X	X	0	1	WORD 'B'
1	0	0	1	0	0	WORD 'C'
1	1	0	0	0	1	WORD 'D'

Table 3

The data may be latched internally by grounding the DS2 output. This is useful when interfacing to a microprocessor. The NJ8812 is also compatible with most types of PROM and ROM for data coding applications.

APPLICATION NOTES

The NJ8812 is designed for use in phase locked loop frequency synthesisers. In these synthesisers, the voltage controlled oscillator (VCO) operates at the output frequency and the output frequency is divided down to a reference frequency. Another signal at this reference frequency is derived from the crystal controlled reference oscillator, and the divided VCO signal is compared at this frequency with the reference signal in a phase and frequency comparator. The output signal derived from this comparison consists of short pulses whose mark-space ratio is such that when the pulses are integrated, a DC level is obtained, which, when applied to the VCO, locks the loop by maintaining the VCO on-frequency.

Simple division to the reference frequency in a fully programmable divider is limited to frequencies of about 50MHz and below, because of the difficulty of producing fully programmable dividers. However, a two-modulus divider which divides by N and N+1 may be easily made. A system as shown in Fig.5 then provides for the programmable division to be done at lower frequencies.

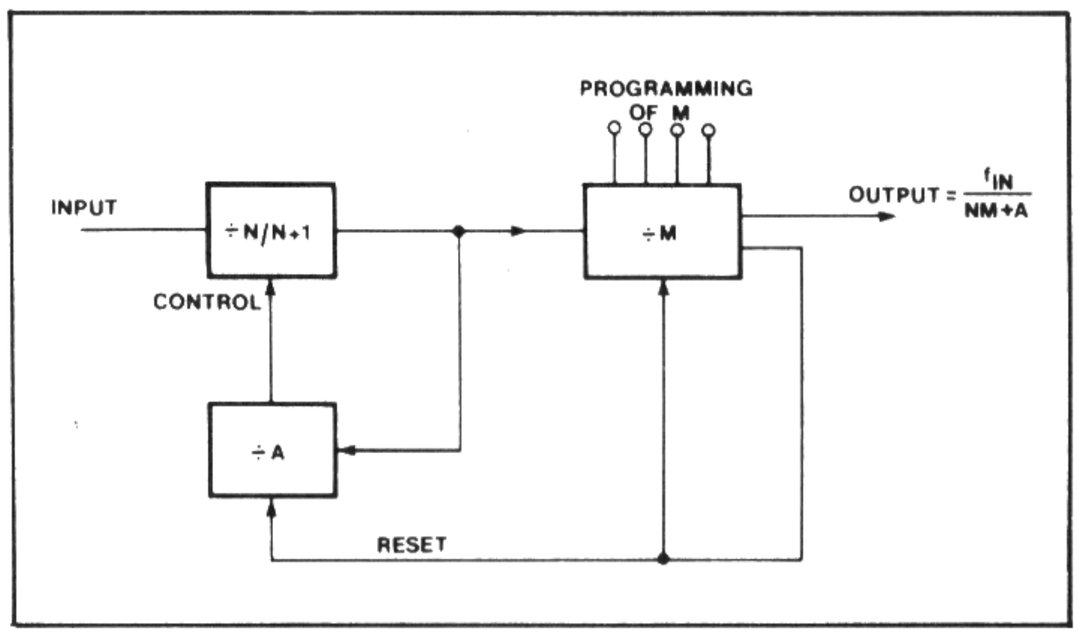

Fig.5 2-modulus counter

The system works as follows:

The two-modulus counter divides by N+1 until counter A is full. The two-modulus stage then divides by N until the M counter is full. The resultant division ratio is NM+A.

In the NJ8812, the value of M is set to between 40 and 295, while A is programmed between 0 and 39. The full scope of the NJ8812 in a synthesiser is achieved using a ÷40/41, such as the SP8793, and under these conditions, the division ratio is from 1600 to 11839. By using the Range input, the M counter programme is changed such that the division ratio becomes 6720 to 16959.

The reference frequency is derived from a 4.8MHz crystal by a programmed divider. This divider is programmed by the FA and FB inputs: these may be tied to V_{CC} (logic '1'), Ground (logic '0') or to DS1 and DS2, depending upon the reference frequency required. In general the reference frequency is made equal to the channel spacing, as the higher the reference frequency, the easier it is to filter the control line to the VCO to prevent spurious sidebands at reference frequency appearing on the output.

Phase Detector

In the NJ8812, this circuit function is implemented by the use of two D type flip-flops. These drive 'open drain' output FETs, and if these are taken to V_S via resistors, waveforms as shown in Fig.6 may be expected.

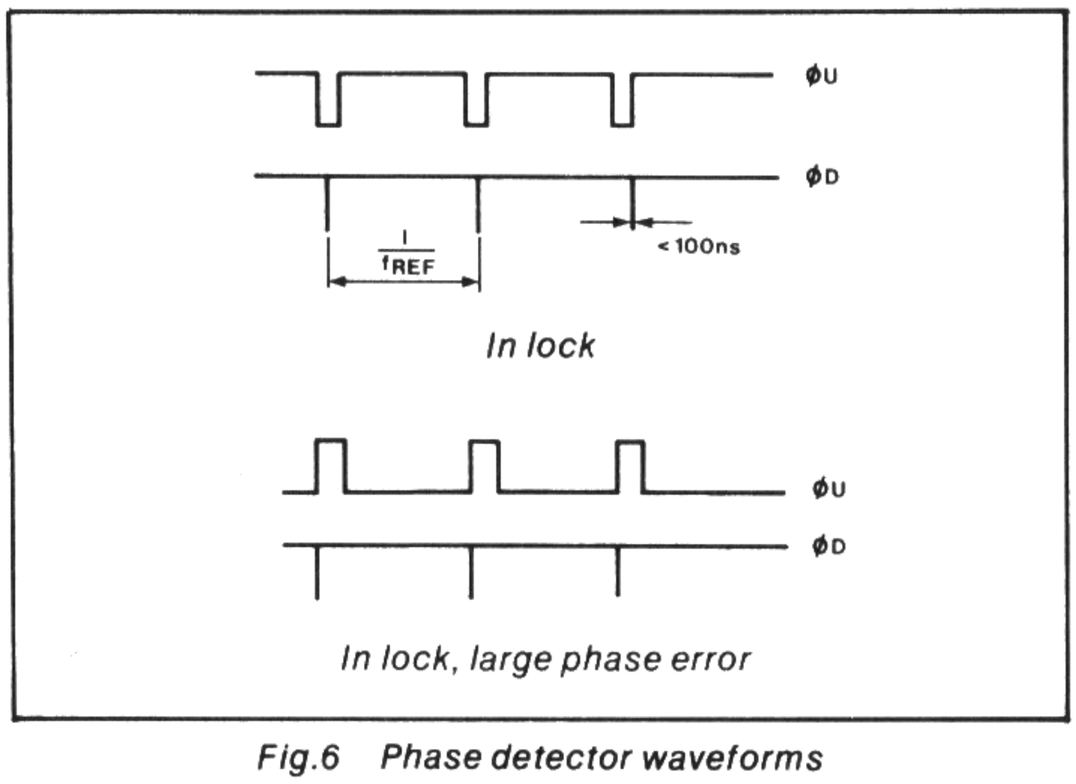

Fig.6 Phase detector waveforms

When out of lock, $Ø_D$ and $Ø_U$ have no definite phase relationship. These outputs may be combined in a suitable circuit, as shown in Fig.7.

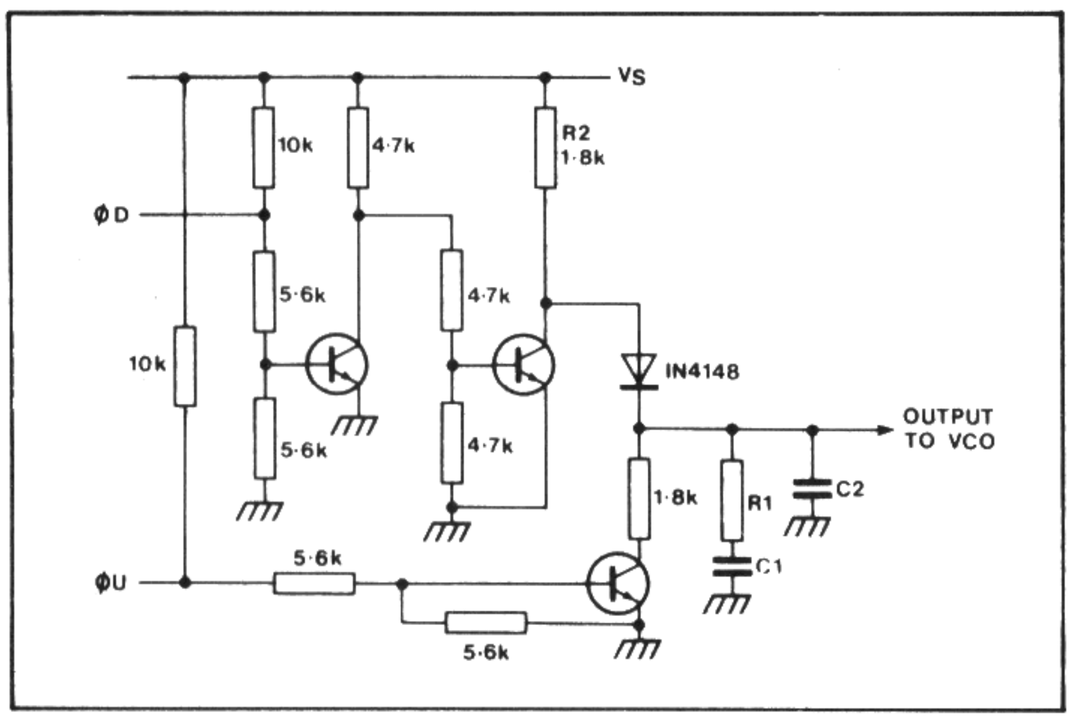

Fig.7 Circuit for combining $Ø_D$ and $Ø_U$

Loop Filter Design

A simple approach will provide a workable, but not necessarily optimum system. For more detailed methods, reference to one of the many textbooks is recommended. The following method provides a simple design.

1. Choose the loop natural frequency ω_n. This frequency affects the settling time of the loop, and this settling time is, to a first order approximation, $10/\omega_n$, where ω_n is in radians per second.
2. Choose a value of damping factor to give adequate loop stability without excessive overshoot. A satisfactory value is 1.0, giving an overshoot of approximately 10%.
3. **Determine:**
   KV = VCO Gain in rads/Volt-sec
   $= 2\pi \times$ Hz/V
   where Hz/V is the deviation in Hz for 1 volt change on the control line.
   N = VCO frequency/Reference Frequency.
4. Choose R_2. For convenience, $4.7k\Omega > R_2 > 470\Omega$
   $C_1 = \dfrac{KV}{2\pi N \omega_n^2 R_2}$
5. $R_1 = D/\omega_n C_1$ where D is the damping factor.
6. $C_2 = \dfrac{1}{15\,\omega_n R_1}$

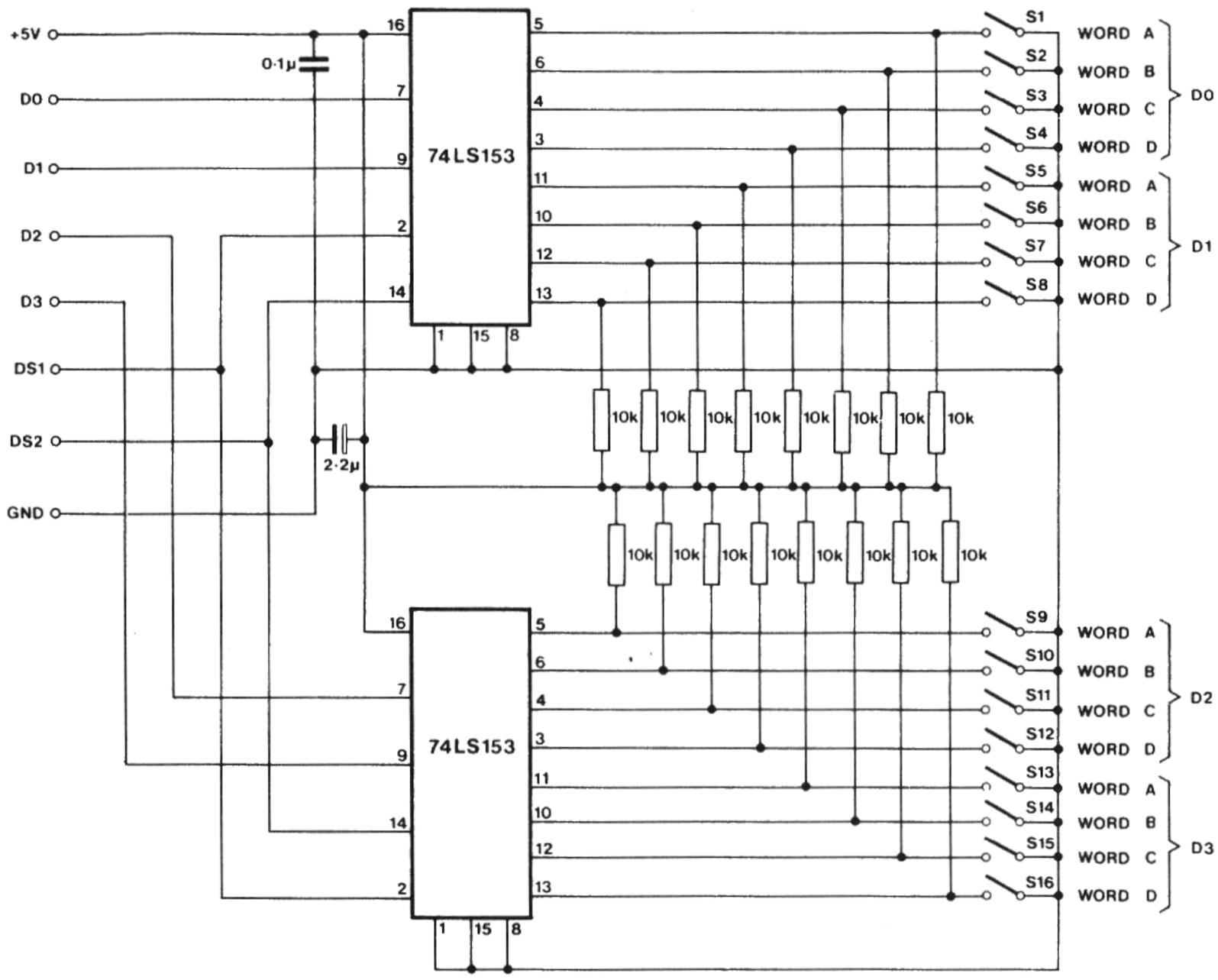

Fig.8 Programming board

Reference Oscillator Requirements

Because the frequency synthesiser effectively multiplies the reference oscillator to the working frequency, any variations or inaccuracies in the reference oscillator appear at the output. For this reason, the accuracy of the reference oscillator must be no worse than that of the signal which it is required to synthesise, while the signal-to-noise ratio must be as high as possible. Incidental FM must be minimised.

VCO Requirements

The VCO should cover the frequency range desired with a suitable control line voltage swing. In addition, its power level and Q should be such as to maintain phase noise sidebands as low as is required. It is frequently found that the high impedance control line is very susceptible to picking up stray signals; screening and careful decoupling of the VCO and its supplies is often necessary. Buffering between the VCO and the prescaler is required to prevent VCO modulation from this source, and dual gate MOSFETS are very useful in this position.

A Typical Synthesiser

Fig.9 shows a typical frequency synthesiser using the NJ8812 and SP8793. Programming is from the binary programming board of Fig.8, or from a suitably programmed PROM or ROM. It should be noted that the binary programming board produces four 4-bit words, and therefore, two of the bits are redundant (see Programming the NJ8812).

The synthesiser of Fig.9 uses a 40673 or similar dual gate MOSFET as a buffer prior to the SP8793 divider. The three 2N5770 transistors provide a charge pump circuit, and the fourth a crystal oscillator. This synthesiser draws some 25mA maximum, excluding the VCO and the programming system, and further development could well reduce the current appreciably. If modulation is required, this may be applied to the control line, provided that the peak deviation is not such as to drive the loop out of lock.

The connection of an LED from pin 10 of the NJ8812 to 5V via a 2.2kΩ resistor will provide an indication of lock, the lamp being alight when the loop is unlocked.

FA, FB and the range pin are connected according to the requirements of frequency spacing and operating frequency.

Performance, in terms of spurious sidebands and noise, depends upon construction and design of the VCO and PC board, and good RF practice should be followed with regard to these components. In particular, attention should be paid to the VCO screening. Further applications information is available in AN1017.

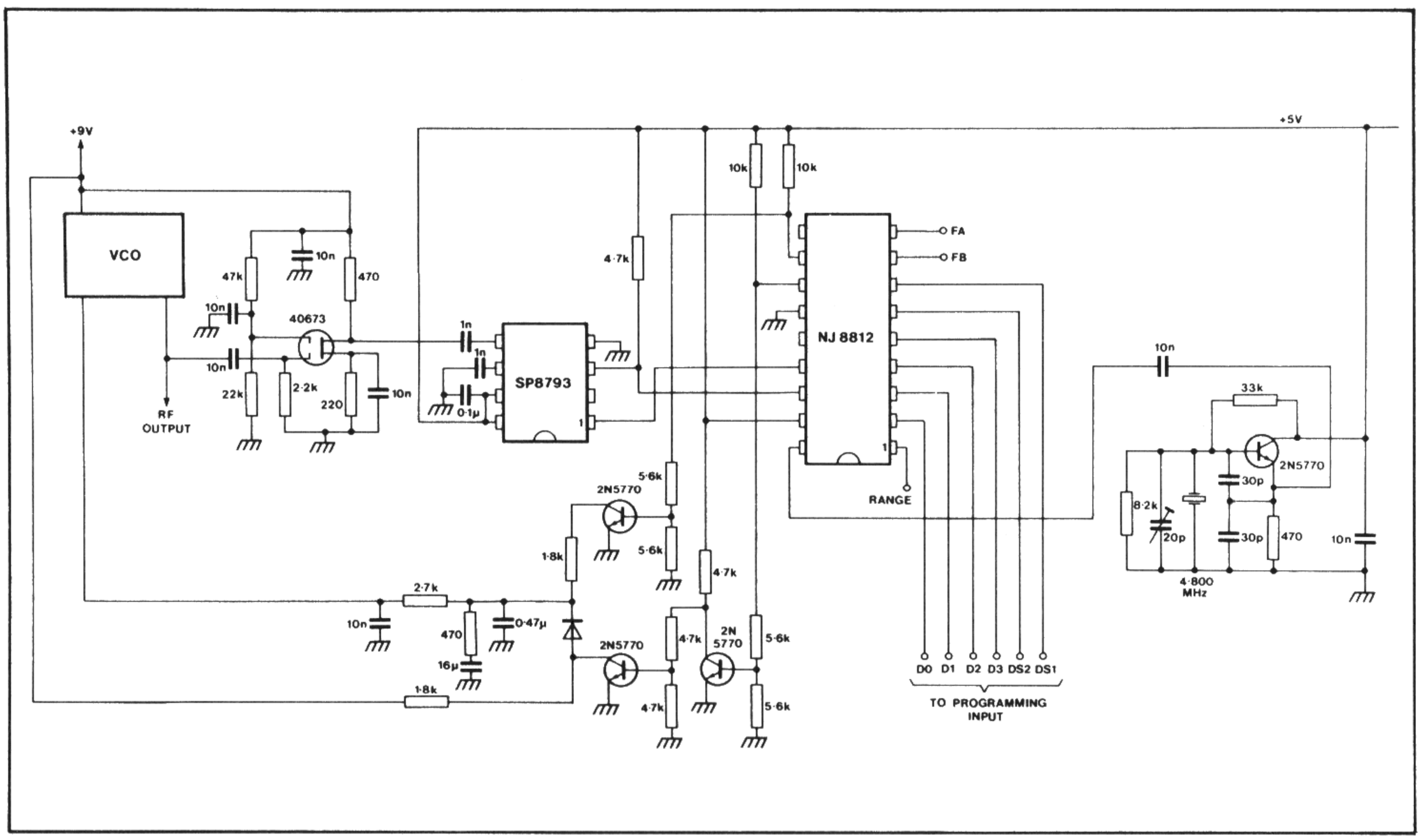

Fig.9 Frequency synthesiser using NJ8812 and SP8793