Digital Sweep Generator

The digital sweep generator is based on the Dig_TX board. The DSP and its memory, as well as the audio- and RF-ADCs remain unassembled. Signal synthesis is completely performed within the FPGA. A miniMAX-40 module with a little hand-made logic on a prototype board controls the sweep generator. The FPGA master clock frequency is 80 MHz.

A seventh order reconstruction filter is implemented at the RF-DAC output. With a 40 MHz Nyquist frequency, the bandwidth design target for the sweep generator was 100 kHz ~ 30 MHz. The lower frequency is limited by a transformer between the DAC and the LP filter, while the upper frequency is limited by the filter roll-off.

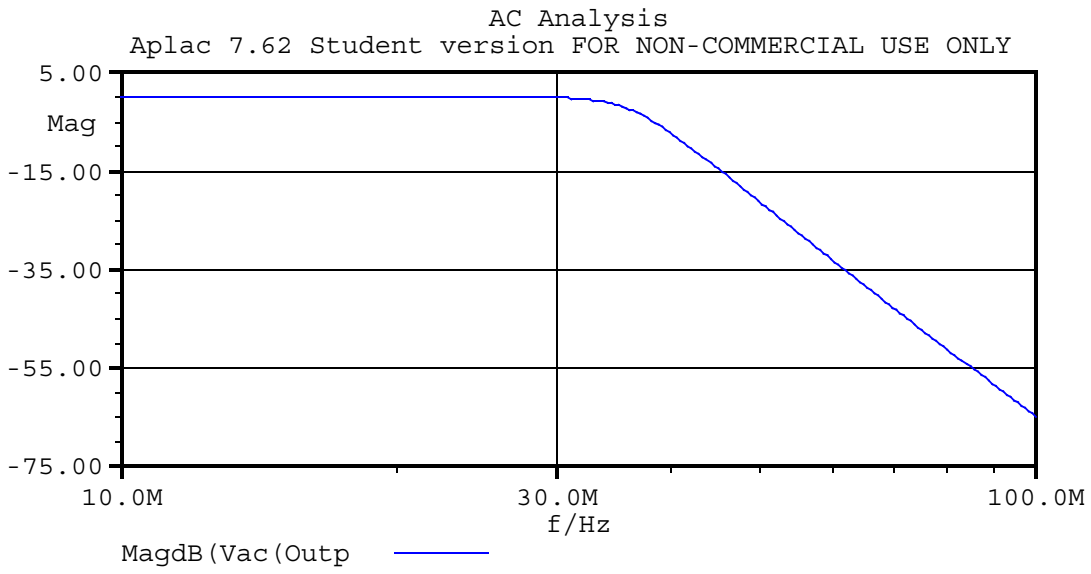
The maximum usable frequency is that frequency below the Nyquist frequency ($f_n = f_{clk}/2$; f_{clk}=master clock frequency), at which the alias frequency $f_a = f_{clk}-f_o$ (f_a=alias frequency, f_o=desired output frequency) is still sufficiently attenuated. The term „sufficiently“ is application dependent and means that the alias signal and its intermodulation products must not disturb the desired signal. Generally it is a good idea to attenuate the alias signal to below the required signal-to-noise ratio of the DDS signal generator. For the digital sweep generator, which shall be used for measurement applications, a minimum SNR of 60 dB seems adequate. While that is not extremely good if compared to commercially available sweep generators, it is sufficient for amateur measurements. In most cases, the SNR is actually better than 70 dB.

In order to keep the passband ripple flat, so that a wide frequency range can be covered without introducing artifical ripple due to the anti-aliasing filter response, a seventh order Butterworth lowpass filter was initially considered and implemented. Its attenuation at 30 MHz was below 1 dB, but the attenuation at the alias of 50 MHz was less than 30 dB. The filter has been designed for 50 input and output impedance. The following table shows the calculated and the really selected capacitances and inductivities. Also the number of windings on an Epcos (Siemens) double hole core type B62152 A8-X17 (A_L=9nH/W^2) for the inductivities are listed. Fractions are estimated values.

Seventh order Butterworth filter (-1dB at 30 MHz; -30dB at 58 MHz)

component	ideal value	real values	turns
L1	300 nH	297 nH	5 3/4
L2	482 nH	410 nH	6 3/4
L3	300 nH	297 nH	5 3/4
C50	43 pF	44 pF	-
C51	174 pF	165 pF	-
C52	174 pF	165 pF	-
C53	43 pF	44 pF	-

Simulation results with real values:



It turned out, that the attenuation of the alias frequency was not satisfactory. Either a higher order Butterworth filter or a change of the filter topology to a much steeper Chebychev filter of the same seventh order was required. A higher order Butterworth filter will be considered for a future redesign, but for the existing board, it was more convenient to implement a Chebychev filter.

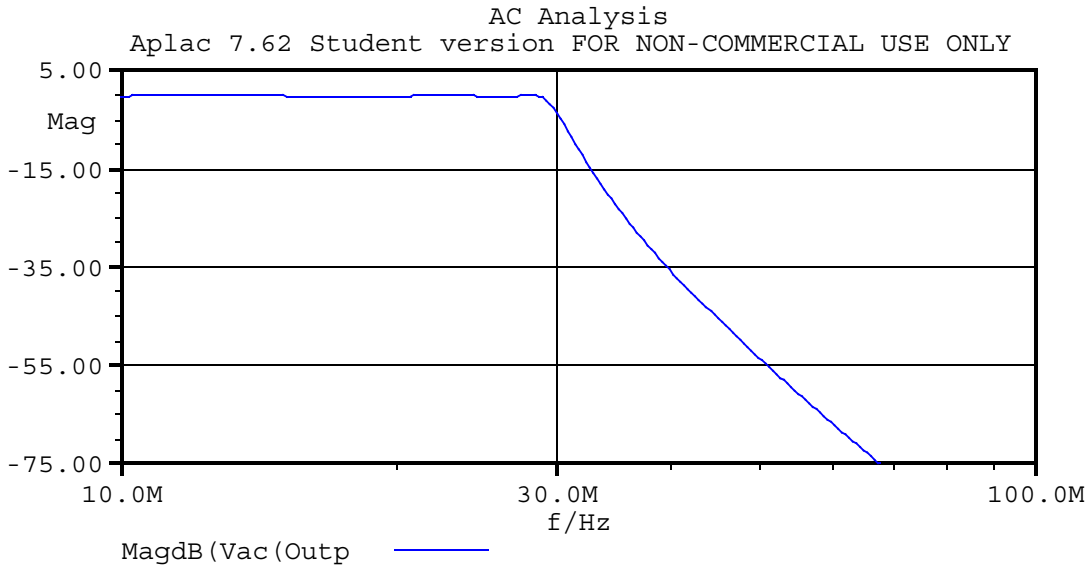
The goal was to find a compromise between the passband ripple and a steep filter transition. The following table shows the calculated and the really chosen values for a 7th order Chebychev filter with 0.5 dB passband ripple up to 30 MHz and almost 60 dB attenuation at 50 MHz.

Seventh order Chebychev filter (-0.5 dB at 30 MHz; -60 dB at 50 MHz)

component	ideal value	real values	turns
L1	334 nH	350 nH	7
L2	357 nH	375 nH	7 1/4
L3	334 nH	350 nH	7
C50	184 pF	183 pF (150//33)	-
C51	280 pF	288 pF (220//68)	-
C52	280 pF	288 pF (220//68)	-
C53	184 pF	183 pF (150//33)	-

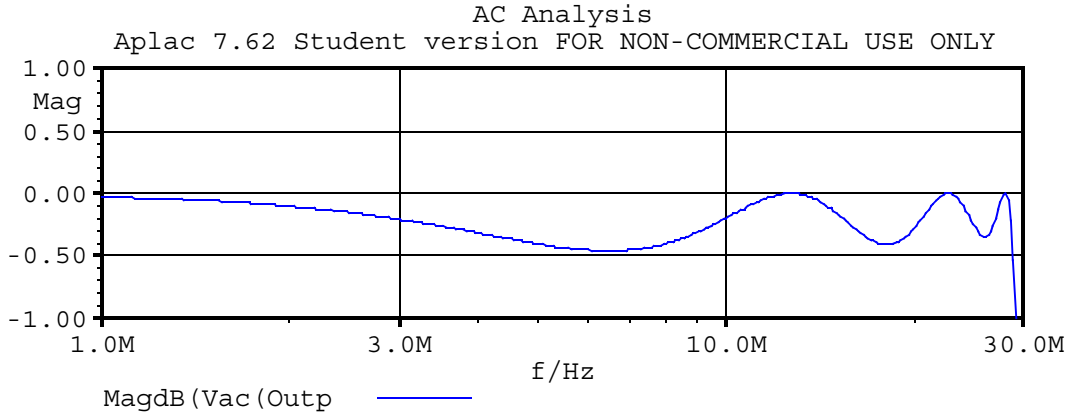
(real value means calculated, not measured!)

Simulation results with real values:



Due to the unprecise realisation with the real values, the attenuation of 0.5 dB is already reached at about 29 MHz.

The following diagram shows the passband ripple of the Chebychev filter.



miniMAX-40 LCA Pinout

Pin	Description	XC 3020	XC 3030	XC 3042	Signal	connector
1	DOUT-I/O				DOUT	J1-59
2	CCLK				CCLK	J1-61
3	VCC				VCC	J1-1
4	GND				GND	63,64
5	A0--I/O				NIOWR	J2-32
6	A1-CS2-I/O				CSLCA	-
7	I/O				-	-
8	A2-I/O				NIORD	J2-31
9	A3-I/O				**Taster U/D (In)**	J1-44
10	I/O				**Taster L/R (In)**	J1-43
11	I/O				**Drehgeber B (In)**	J1-41
12	A15-I/O				A15	J2-18
13	A4-I/O				IO24	J1-40
14	A14-I/O				A14	J2-17
15	A5-I/O				IO23	J1-39
16	GND				GND	63,64
17	A13-I/O				A13	J2-16
18	A6-I/O				**SER_SPARE**	J1-38
19	A12-I/O				A12	J2-15
20	A7-I/O				**SERADR (Out)**	J1-37
21	I/O				BS0	J2-52
22	I/O				**SERDATA (Out)**	J1-36
23	A11-I/O				A11	J2-14
24	A8-I/O				**SERCLK (Out)**	J1-35
25	A10-I/O				A10	J2-13
26	A9-I/O				**-5V clock (Out)**	J1-33
27	VCC				VCC	J1-1
28	GND				GND	63,64
29					VCC	J1-1
30	TCLKIN-I/O				CLKOUT	J2-47
31	I/O				IO16	J1-32
32	I/O				IO13	J1-29
33	I/O				IO14	J1-30
34	I/O				**LCD_E (Out)**	J1-27
35	I/O				IO12	J1-28
36	I/O				**LCD_RS (Out)**	J1-25
37	I/O				**LCD_R/W (Out)**	J1-26
38	I/O				**LCD_DB6 (I/O)**	J1-23
39	I/O				**LCD_DB7 (I/O)**	J1-24
40	I/O				**LCD_DB4 (I/O)**	J1-21
41	VCC				VCC	J1-1
42	I/O				**LCD_DB5 (I/O)**	J1-22
43	I/O				**LCD_DB2 (I/O)**	J1-19
44	I/O				**LCD_DB3 (I/O)**	J1-20
45	I/O				**LCD_DB0** (I/O)	J1-17

46	I/O				NMRD	J2-29
47	I/O				NMWR	J2-30
48	I/O				SELECT	J1-58
49	I/O				**LCD_DB1 (I/O)**	J1-18
50	I/O				TOUT1	J2-48
51	I/O				STDP	-
52	M1-				GND	63,64
53	GND				GND	63,64
54	M0-RT				VCC	J1-1
55	VCC				VCC	J1-1
56	M2-I/O				VCC	J1-1
57	HDC-I/O				IO15	J1-31
58	I/O				**LCD Backlight PWM (Out)**	J1-34
59	-I/O				SSN	-
60	I/O				A16PS0	-
61	I/O				A17PS1	-
62	I/O				A18PS2	-
63	I/O				A19PS3	-
64	I/O				**Drehgeber A (In)**	J1-42
65	-I/O				NINIT	-
66	GND				GND	63,64
67	I/O				HLDAK	J2-46
68	I/O				HLDRQ	J2-45
69	I/O				INTP3	J2-58
70	I/O				INTP2	J2-57
71	I/O				INTP1	J2-56
72	I/O				DMARQ0	J2-36
73	I/O				NDMAAK0	J2-37
74	I/O				DMARQ1	J2-38
75	I/O				NDMAAK1	J2-39
76	XTAL2-I/O				**D6 (Wobbel-PA)**	J1-45
77	GND				GND	63,64
78					NRESET	J1-57
79	VCC				VCC	J1-1
80	DONE-				DONEPG	J1-62
81	D7-I/O				AD7	J2-10
82	BCLKIN-XTAL1-I/O				BCLKIN	J1-56
83	D6-I/O				AD6	J2-9
84	I/O				**D12 (Wobbel-PA)**	J1-46
85	I/O				**D24 (Wobbel-PA)**	J1-47
86	I/O				ASTB	J2-28
87	D5-I/O				AD5	J2-8
88	-I/O				A8	J2-11
89	D4-I/O				AD4	J2-7
90	I/O				BUFRW	J2-34
91	VCC				VCC	J1-1
92	D3-I/O				AD3	J2-6
93	-I/O				A9	J2-12

94	D2-I/O				AD2	J2-5
95	I/O				**D48 (Wobbel-PA)**	J1-48
96	I/O				BS1	J2-53
97	I/O				BS2	J2-54
98	D1-I/O				AD1	J2-4
99	-/RDY-I/O				NBUSY	-
100	D0-DIN-I/O				AD0	J2-3

Folgende Register sind im XC3030 FPGA auf dem MiniMax-40 Board definiert und an der jeweils angegebenen I/O-Adresse vom V40HL aus ansprechbar:

0x7000 LCD Data Register

7	6	5	4	3	2	1	0
LCD_DB7	LCD_DB6	LCD_DB5	LCD_DB4	LCD_DB3	LCD_DB2	LCD_DB1	LCD_DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data to be written to or read from LCD. The direction is switched by LCD Data Direction Register.

0x7001 LCD Control Register

7	6	5	4	3	2	1	0
-	-	-	-	-	E	R/W	RS
-	-	-	-	-	W	W	W

LCD control signals.

0x7002 LCD Backlight

7	6	5	4	3	2	1	0
-	-	-	-	B3	B2	B1	B0
-	-	-	-	W	W	W	W

Brightness of LCD backlight. B[3..0] = 0000: Backlight off; B[3..0] = 1111: Backlight max

0x7003 Keyboard Input

7	6	5	4	3	2	1	0
-	-	-	-	Taste U/D	Taste L/R	Drehgbr B	Drehgbr A
-	-	-	-	R	R	R	R

Inputs the logical levels of the keys on the front panel. An interrupt is generated when these values change.

0x7004 LCD Data Direction Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DIR
-	-	-	-	-	-	-	W

DIR=0: LCD port is input; DIR=1: LCD port is output;

0x7005 Serial Output Buffer

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
W	W	W	W	W	W	W	W

Data to be sent via serial port

0x7006 Serial Control/Status Register

7	6	5	4	3	2	1	0
TXBE	-	-	-	-	-	SPARE	SERADR
R	-	-	-	-	-	R/W	R/W

Data may be written to the serial output buffer, when TXBE is high. SERADR outputs the serial address. The receiver latches the data when SERADR changes its level. SPARE is currently unused.

0x7007 Port4

7	6	5	4	3	2	1	0
-	-	-	-	D48	D24	D12	D6
-	-	-	-	W	W	W	W

Port4 controls the attenuation of the resistor ladder inside the PA. This ladder consists of four resistor stages with 6, 12, 24 and 48dB attenuation. The attenuation is inserted by a relay, when the respective bit in the Port4 output register is set.

WOBBELTX

1	TCK
2	CONF_DONE
3	nCEO
4	TDO
5	VCCINT
6	
7	
8	
9	
10	GNDINT
11	CLKUSR
12	
13	
14	
15	
16	VCCINT
17	**WAITB**
18	**BSTBB**
19	**RDB**
20	**WRB**
21	
22	GNDINT
23	RDYnBSY
24	
25	
26	INIT_DONE
27	VCCINT
28	
29	
30	

31	
32	GNDINT
33	**DSPCLK**
34	
35	
36	
37	VCCINT
38	
39	
40	
41	
42	GNDINT
43	
44	
45	
46	**SERCLK**
47	**VCCINT**
48	**SERDATA**
49	**SERADR**
50	**SER_SPARE**
51	**GPIO11**
52	GNDINT
53	**GPIO10**
54	**Trigger out**
55	**Marker out**
56	**GPIO7**
57	VCCINT
58	TMS
59	TRST
60	nSTATUS

61	**GPIO6**
62	**GPIO5**
63	**GPIO4**
64	**GPIO3**
65	**GPIO2**
66	**GPIO1**
67	**GPIO0**
68	**DAC_D0**
69	GNDINT
70	**DAC_D1**
71	**DAC_D2**
72	**DAC_D3**
73	**DAC_D4**
74	**DAC_D5**
75	**DAC_D6**
76	**DAC_D7**
77	VCCINT
78	**DAC_D8**
79	**DAC_D9**
80	**DAC_D10**
81	**DAC_D11**
82	**DAC_D12**
83	**DAC_D13**
84	**DAC_CLK**
85	GNDINT
86	
87	**P2**
88	**P3**
89	VCCINT
90	IN, **RESETB**

91	CLK, **CLK_SPX**
92	IN
93	GNDINT
94	
95	
96	VCCINT
97	
98	
99	
100	
101	
102	
103	
104	GNDINT
105	
106	**ADC_CLK**
107	
108	**ADC_D11**
109	**ADC_D10**
110	**ADC_D9**
111	**ADC_D8**
112	VCCINT
113	**ADC_D7**
114	**ADC_D6**
115	**ADC_D5**
116	**ADC_D4**
117	**ADC_D3**
118	**ADC_D2**
119	**ADC_D1**
120	**ADC_D0**

WOBBELTX

121	nCONFIG
122	VCCINT
123	MSEL1
124	MSEL0
125	GNDINT
126	
127	
128	
129	
130	VCCINT
131	
132	
133	
134	
135	GNDINT
136	
137	**AUDCLK**
138	**FSY**
139	
140	VCCINT
141	
142	**SCK**
143	**AIDATA**
144	
145	GNDINT
146	**D0**
147	**D1**
148	**D2**
149	**D3**
150	VCCINT

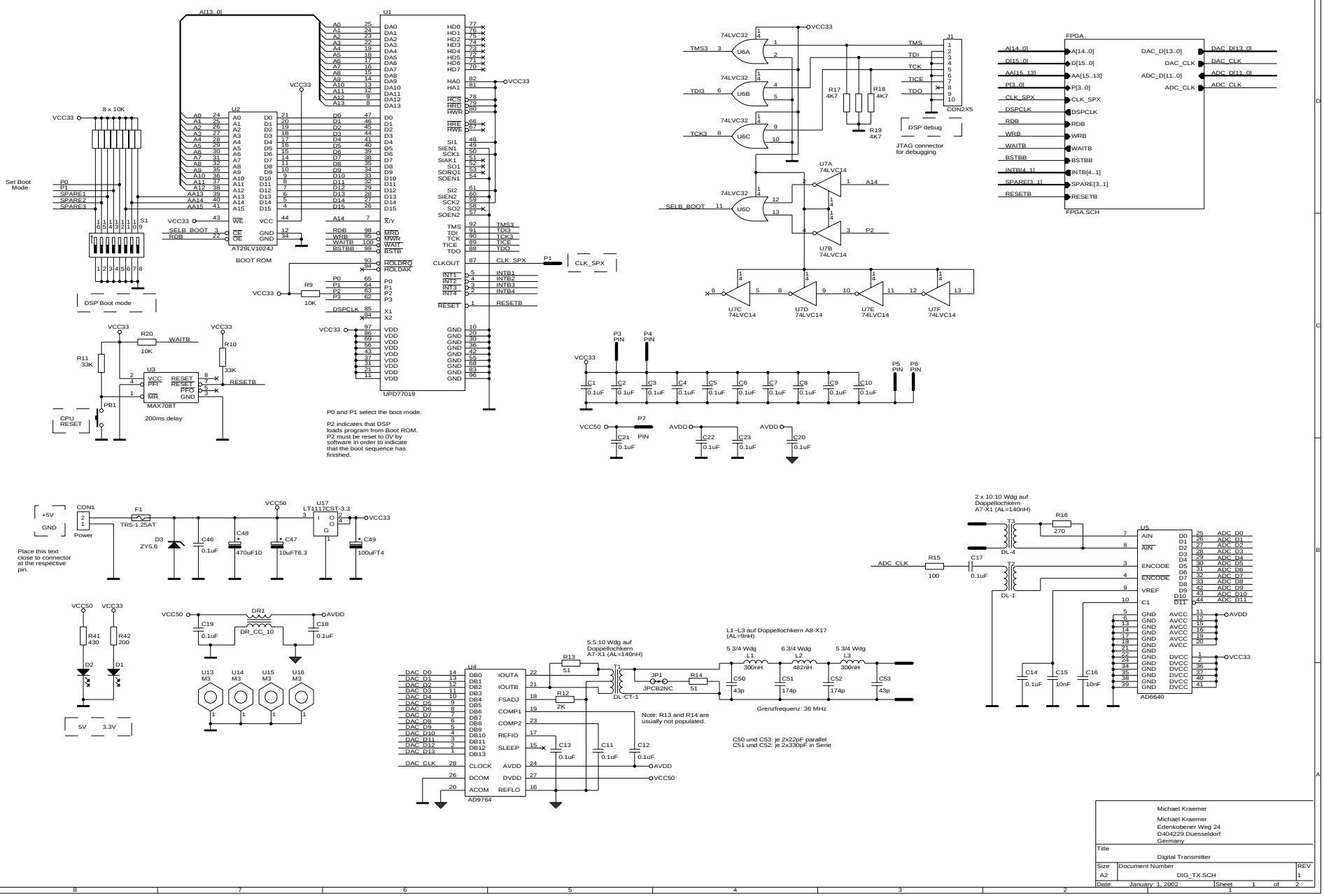
151	**D4**
152	**D5**
153	**D6**
154	**D7**
155	GNDINT
156	**D8**
157	**D9**
158	**D10**
159	**D11**
160	VCCINT
161	**D12**
162	**D13**
163	**D14**
164	**D15**
165	GNDINT
166	
167	
168	
169	
170	VCCINT
171	
172	
173	
174	
175	
176	GNDINT
177	TDI
178	nCE
179	DCLK
180	DATA0

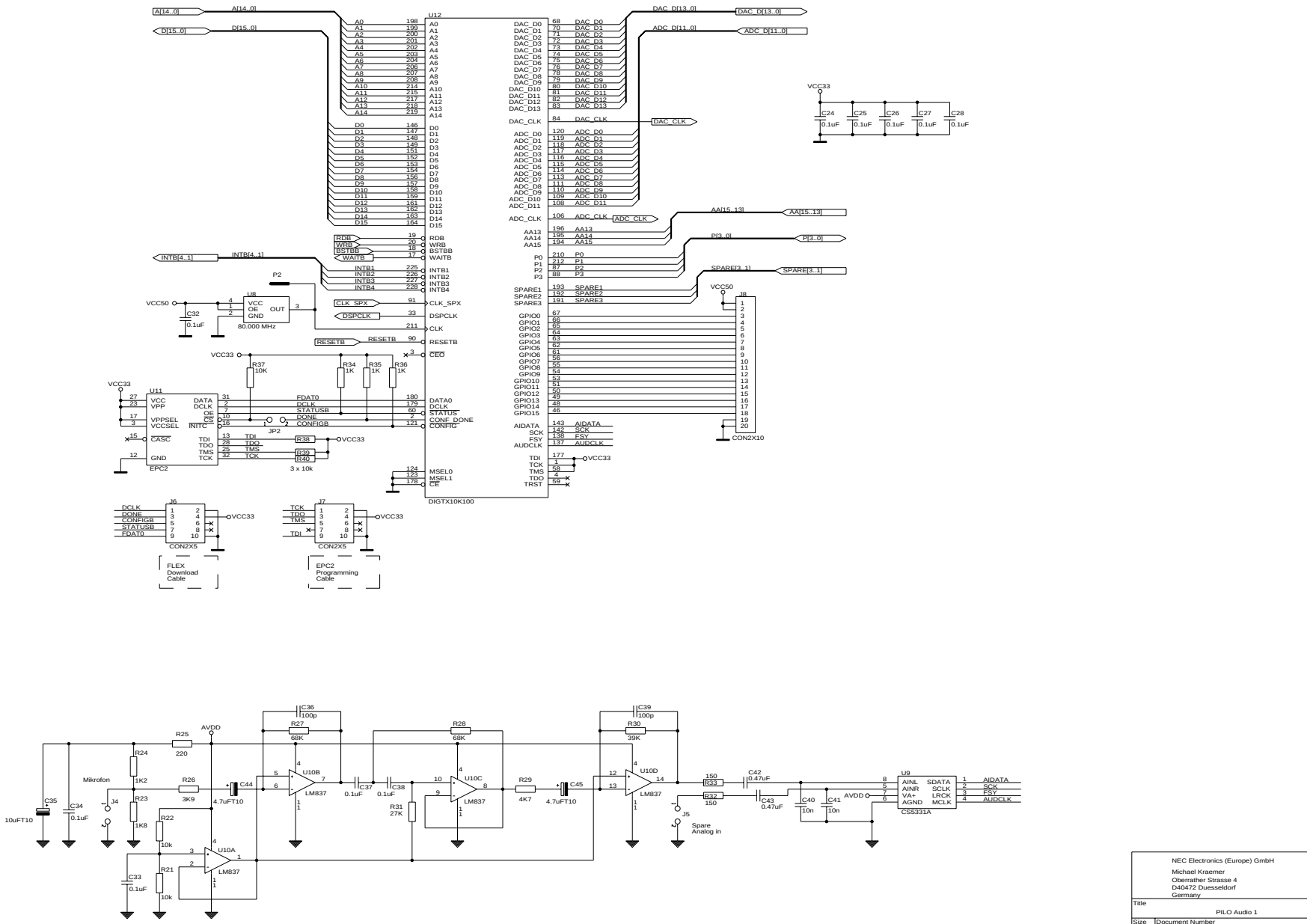
181	DATA1
182	DATA2
183	DATA3
184	
185	DATA4
186	DATA5
187	
188	DATA6
189	VCCINT
190	DATA7
191	**SPARE3**
192	**SPARE2**
193	**SPARE1**
194	**AA15**
195	**AA14**
196	**AA13**
197	GNDINT
198	**A0**
199	**A1**
200	**A2**
201	**A3**
202	**A4**
203	**A5**
204	**A6**
205	VCCINT
206	**A7**
207	**A8**
208	**A9**
209	DEV_CLRn
210	IN, **P0**

211	CLK, **CLK**
212	IN, **P1**
213	DEV_OE
214	**A10**
215	**A11**
216	GNDINT
217	**A12**
218	**A13**
219	**A14**
220	
221	
222	
223	
224	VCCINT
225	**INTB1**
226	**INTB2**
227	**INTB3**
228	**INTB4**
229	
230	
231	
232	GNDINT
233	
234	
235	
236	nRS
237	
238	nWS
239	CS
240	nCS

Schematics

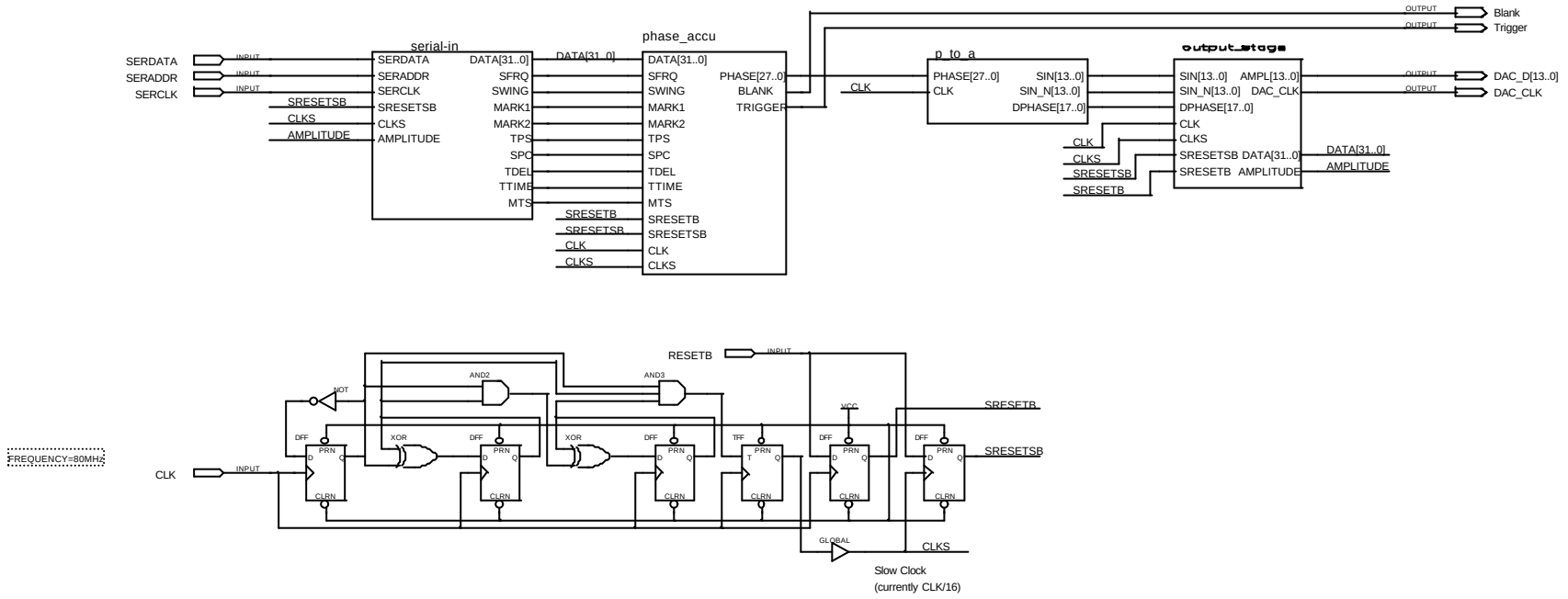
WOBBELTX


U1
UPD77019
U2
AT29LV1024J
BOOT ROM
8 x 10K
Set Boot Mode
DSP Boot mode
P0 and P1 select the boot mode.
P2 indicates that DSP loads program from Boot ROM. P2 must be reset to 0V by software in order to indicate that the boot sequence has finished.
U3
MAX708T
200ms delay
CPU RESET
U7A 74LVC14
U7B 74LVC14
U7C 74LVC14
U7D 74LVC14
U7E 74LVC14
U7F 74LVC14
J1
CON2X5
DSP debug
JTAG connector for debugging
FPGA
FPGA.SCH
CON1
Power
Place this text close to connector at the respective pin.
U17
LT1117CST-3.3
U4
AD9764
5:5:10 Wdg auf Doppellochkern A7-X1 (AL=140nH)
L1–L3 auf Doppellochkern A8-X17 (AL=9nH)
Grenzfrequenz: 36 MHz
Note: R13 and R14 are usually not populated.
C50 und C53: je 2x22pF parallel
C51 und C52: je 2x330pF in Serie
2 x 10:10 Wdg auf Doppellochkern A7-X1 (AL=140nH)
U5
AD6640
Michael Kraemer
Michael Kraemer
Edenkobener Weg 24
D404229 Duesseldorf
Germany
Title
Digital Transmitter
Size A2
Document Number DIG_TX.SCH
REV 1
Date: January 1, 2002
Sheet 1 of 2

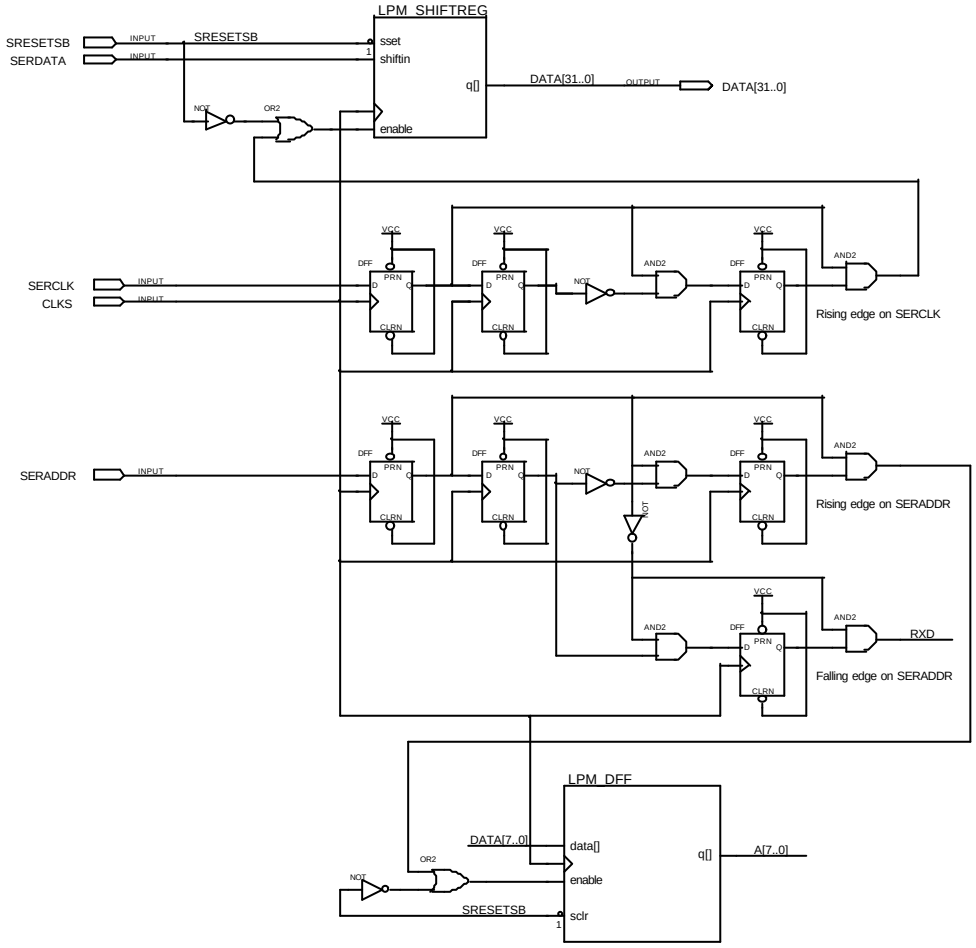

U12
DIGTX10K100
U8
80.000 MHz
U11
EPC2
JP2
3 x 10k
CON2X5
FLEX
Download
Cable
EPC2
Programming
Cable
CON2X10
U9
CS5331A
LM837
Mikrofon
Spare
Analog in
NEC Electronics (Europe) GmbH
Michael Kraemer
Oberrather Strasse 4
D40472 Duesseldorf
Germany
Title
PILO Audio 1
Size
A2
Document Number
PILOAUD1.SCH
REV
1
Date: January 1, 2002
Sheet 2 of 2

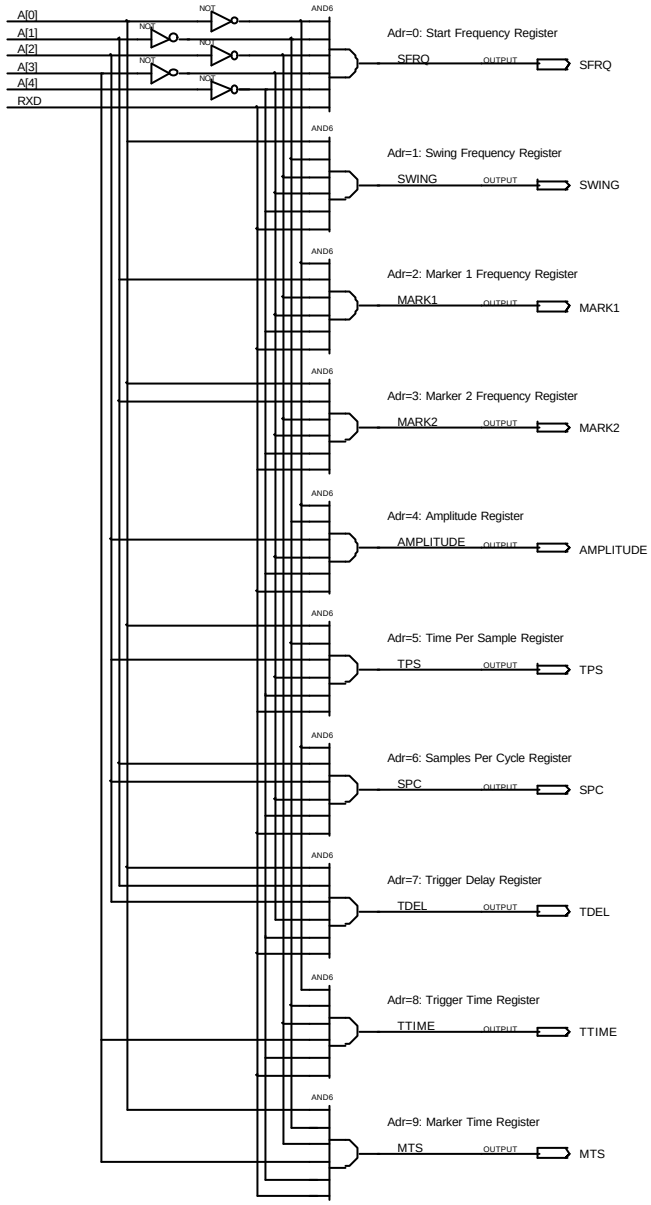
Schematics

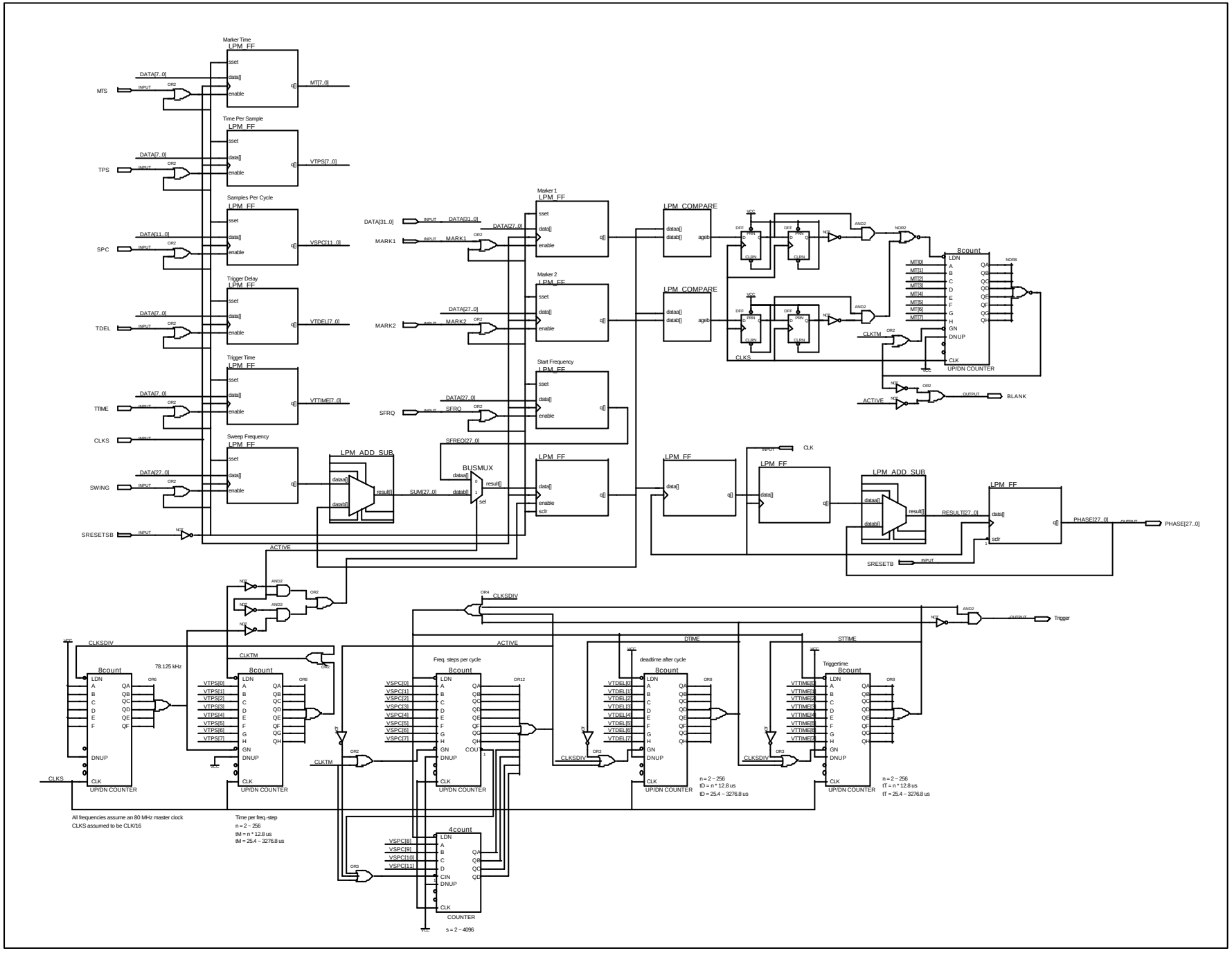
Wobbel-FPGA

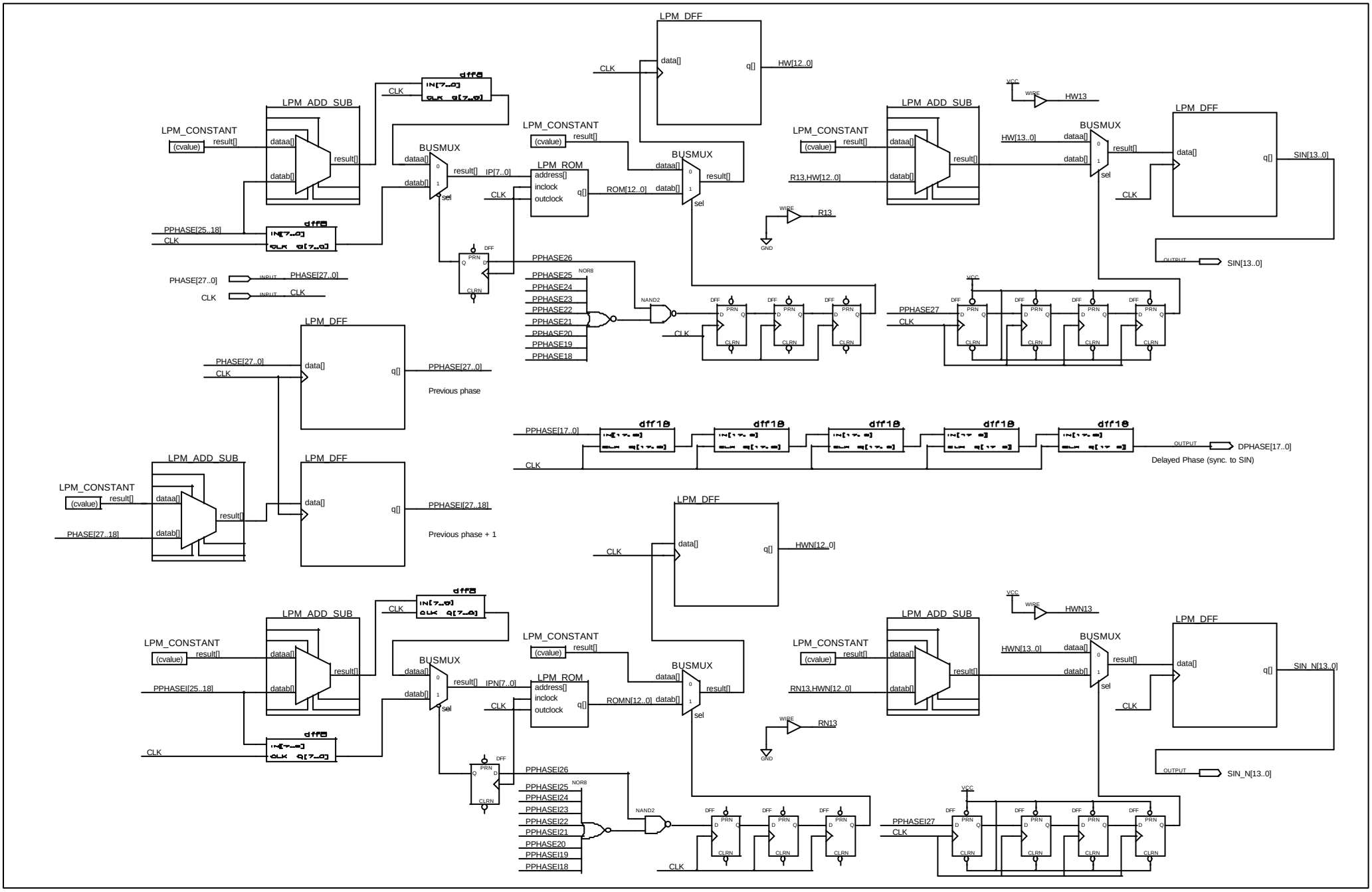

SERDATA
SERADDR
SERCLK
INPUT
SRESETSB
CLKS
AMPLITUDE
serial-in
SERDATA
SERADDR
SERCLK
SRESETSB
CLKS
AMPLITUDE
DATA[31..0]
SFRQ
SWING
MARK1
MARK2
TPS
SPC
TDEL
TTIME
MTS
DATA[31..0]
phase_accu
DATA[31..0]
SFRQ
SWING
MARK1
MARK2
TPS
SPC
TDEL
TTIME
MTS
SRESETB
SRESETSB
CLK
CLKS
PHASE[27..0]
BLANK
TRIGGER
SRESETB
SRESETSB
CLK
CLKS
CLK
p_to_a
PHASE[27..0]
CLK
SIN[13..0]
SIN_N[13..0]
DPHASE[17..0]
output_stage
SIN[13..0]
SIN_N[13..0]
DPHASE[17..0]
CLK
CLKS
SRESETSB
SRESETB
AMPL[13..0]
DAC_CLK
DATA[31..0]
AMPLITUDE
OUTPUT
Blank
Trigger
DAC_D[13..0]
DAC_CLK

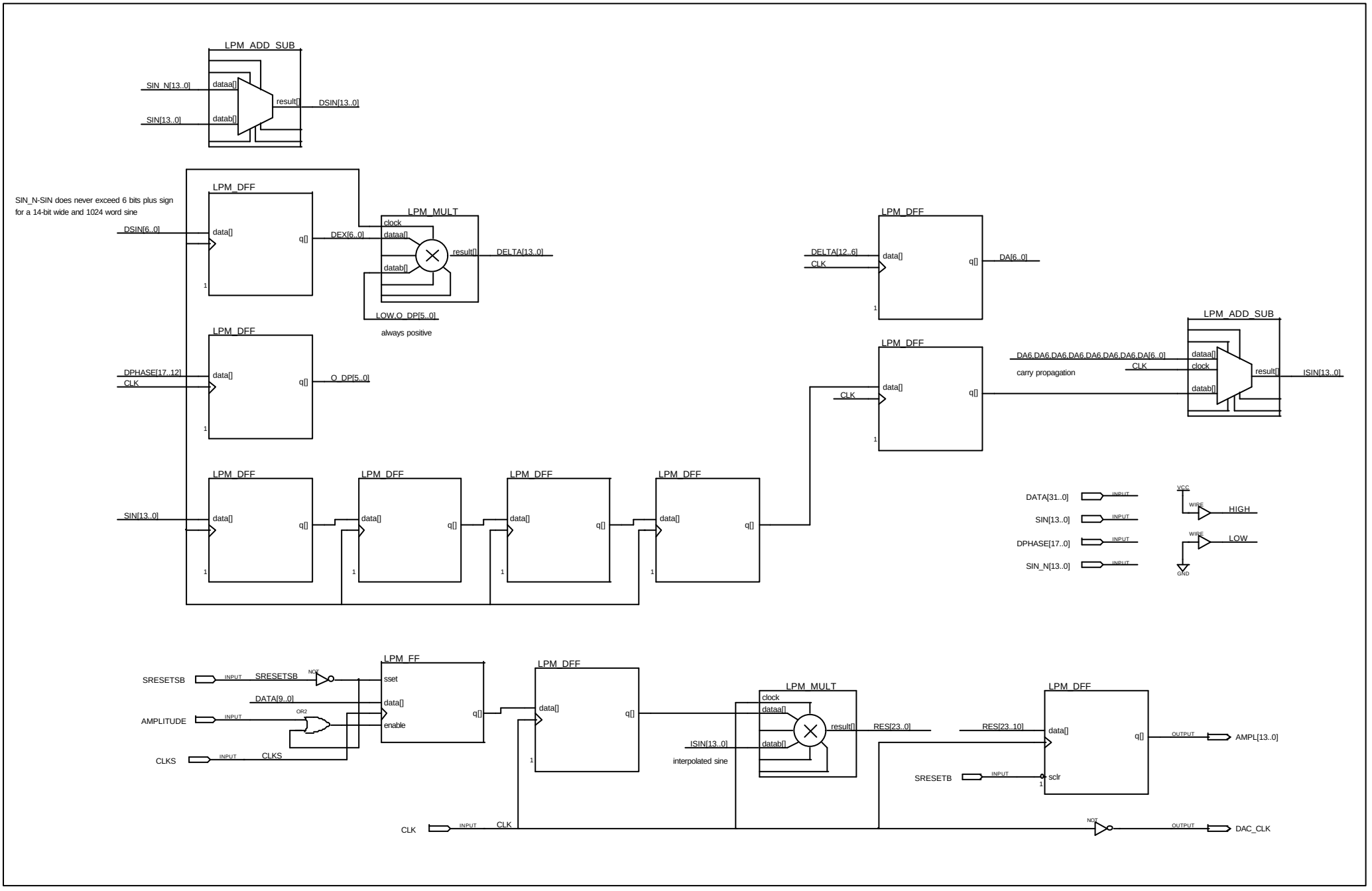
FREQUENCY=80MHz
CLK
INPUT
RESETB
AND2
AND3
NOT
XOR
DFF
TFF
PRN
CLRN
VCC
SRESETB
SRESETSB
GLOBAL
CLKS
Slow Clock
(currently CLK/16)


LPM_SHIFTREG
SRESETSB
SERDATA
INPUT
sset
shiftin
q[]
DATA[31..0]
OUTPUT
enable
NOT
OR2
SERCLK
CLKS
DFF
PRN
CLRN
AND2
VCC
Rising edge on SERCLK
SERADDR
Rising edge on SERADDR
RXD
Falling edge on SERADDR
LPM_DFF
DATA[7..0]
data[]
A[7..0]
sclr


A[0]
A[1]
A[2]
A[3]
A[4]
RXD
AND6
Adr=0: Start Frequency Register
SFRQ
Adr=1: Swing Frequency Register
SWING
Adr=2: Marker 1 Frequency Register
MARK1
Adr=3: Marker 2 Frequency Register
MARK2
Adr=4: Amplitude Register
AMPLITUDE
Adr=5: Time Per Sample Register
TPS
Adr=6: Samples Per Cycle Register
SPC
Adr=7: Trigger Delay Register
TDEL
Adr=8: Trigger Time Register
TTIME
Adr=9: Marker Time Register
MTS

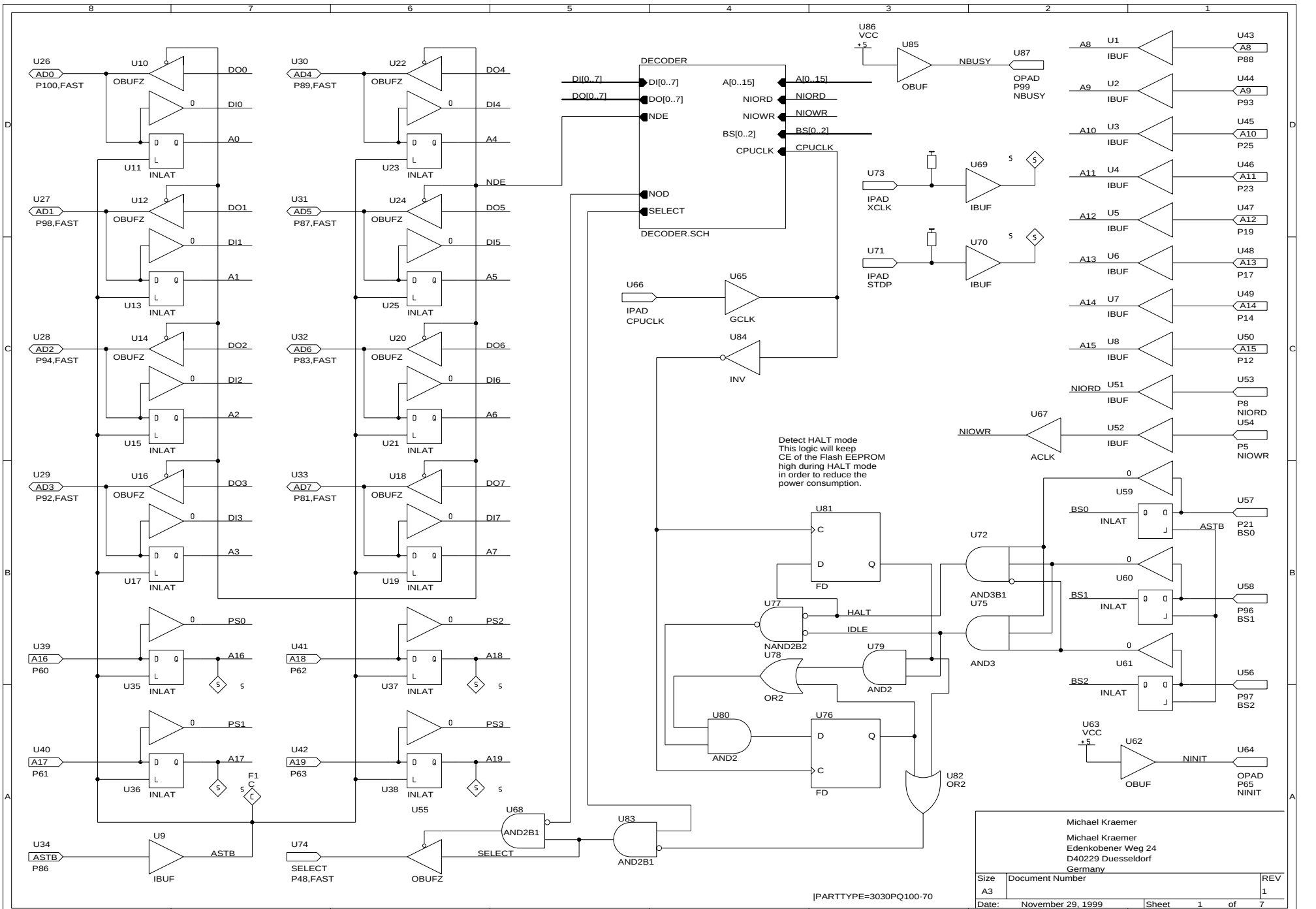

Marker Time
LPM_FF
MTS
DATA[7..0]
MT[7..0]
Time Per Sample
TPS
VTPS[7..0]
Samples Per Cycle
SPC
DATA[11..0]
VSPC[11..0]
Trigger Delay
TDEL
VTDEL[7..0]
Trigger Time
TTIME
VTTIME[7..0]
Sweep Frequency
SWING
CLKS
SRESETSB
Marker 1
Marker 2
Start Frequency
SFRQ
DATA[31..0]
MARK1
MARK2
LPM_COMPARE
8count
MT[0]
MT[1]
MT[2]
MT[3]
MT[4]
MT[5]
MT[6]
MT[7]
CLKTM
CLKS
ACTIVE
BLANK
LPM_ADD_SUB
BUSMUX
SUM[27..0]
SFREQ[27..0]
RESULT[27..0]
PHASE[27..0]
SRESETB
CLK
CLKSDIV
78.125 kHz
Freq. steps per cycle
deadtime after cycle
Triggertime
DTIME
STTIME
Trigger
UP/DN COUNTER
4count
COUNTER
All frequencies assume an 80 MHz master clock
CLKS assumed to be CLK/16
Time per freq.-step
n = 2 – 256
tM = n * 12.8 us
tM = 25.4 – 3276.8 us
n = 2 – 256
tD = n * 12.8 us
tD = 25.4 – 3276.8 us
n = 2 – 256
tT = n * 12.8 us
tT = 25.4 – 3276.8 us
s = 2 – 4096

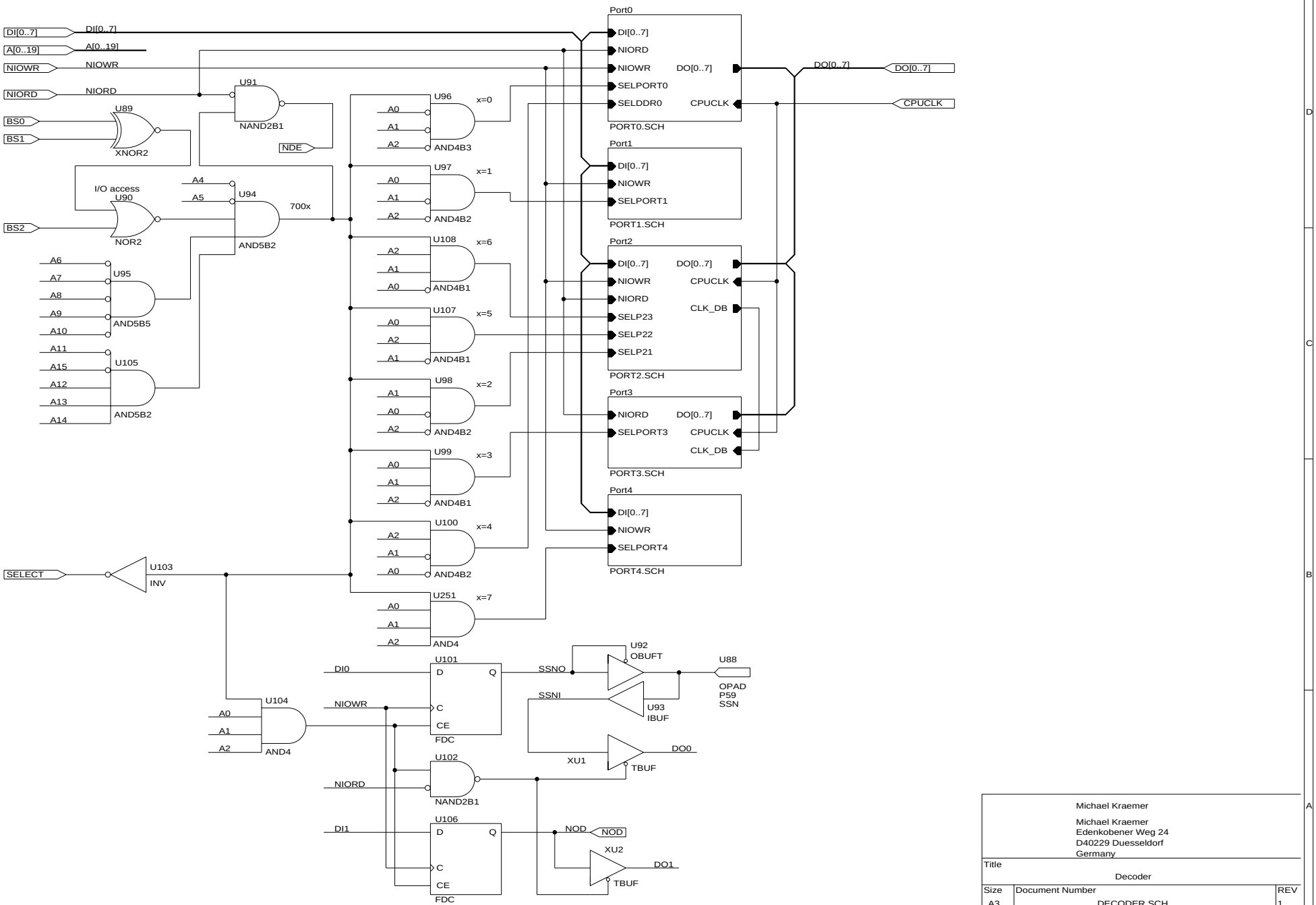

LPM_DFF
data[]
q[]
CLK
HW[12..0]
LPM_ADD_SUB
LPM_CONSTANT
(cvalue)
result[]
dataa[]
datab[]
BUSMUX
sel
LPM_ROM
address[]
inclock
outclock
ROM[12..0]
IP[7..0]
R13,HW[12..0]
WIRE
R13
VCC
HW13
GND
SIN[13..0]
OUTPUT
PPHASE[25..18]
PHASE[27..0]
INPUT
PHASE[27..0]
CLK
PPHASE26
PPHASE25
PPHASE24
PPHASE23
PPHASE22
PPHASE21
PPHASE20
PPHASE19
PPHASE18
NOR8
NAND2
DFF
PRN
CLRN
PPHASE27
PPHASE[27..0]
Previous phase
PPHASE[17..0]
dff18
DPHASE[17..0]
Delayed Phase (sync. to SIN)
PHASE[27..18]
PPHASEI[27..18]
Previous phase + 1
HWN[12..0]
RN13,HWN[12..0]
RN13
HWN13
SIN_N[13..0]
PPHASEI[25..18]
IPN[7..0]
ROMN[12..0]
PPHASEI26
PPHASEI25
PPHASEI24
PPHASEI23
PPHASEI22
PPHASEI21
PPHASE20
PPHASEI19
PPHASEI18
PPHASEI27


LPM_ADD_SUB
SIN_N[13..0]
dataa[]
result[]
DSIN[13..0]
SIN[13..0]
datab[]
SIN_N-SIN does never exceed 6 bits plus sign
for a 14-bit wide and 1024 word sine
LPM_DFF
DSIN[6..0]
data[]
q[]
DEX[6..0]
LPM_MULT
clock
dataa[]
result[]
DELTA[13..0]
datab[]
LOW,O_DP[5..0]
always positive
LPM_DFF
DELTA[12..6]
CLK
data[]
q[]
DA[6..0]
LPM_ADD_SUB
LPM_DFF
DA6,DA6,DA6,DA6,DA6,DA6,DA6,DA[6..0]
carry propagation
CLK
dataa[]
clock
result[]
ISIN[13..0]
data[]
q[]
CLK
datab[]
LPM_DFF
DPHASE[17..12]
CLK
data[]
q[]
O_DP[5..0]
LPM_DFF
LPM_DFF
LPM_DFF
LPM_DFF
SIN[13..0]
data[]
q[]
DATA[31..0]
INPUT
SIN[13..0]
INPUT
DPHASE[17..0]
INPUT
SIN_N[13..0]
INPUT
VCC
WIRE
HIGH
WIRE
LOW
GND
LPM_FF
SRESETSB
INPUT
SRESETSB
NOT
sset
DATA[9..0]
data[]
AMPLITUDE
INPUT
OR2
enable
q[]
CLKS
INPUT
CLKS
LPM_DFF
data[]
q[]
LPM_MULT
clock
dataa[]
result[]
RES[23..0]
ISIN[13..0]
databb[]
interpolated sine
LPM_DFF
RES[23..10]
data[]
q[]
OUTPUT
AMPL[13..0]
SRESETB
INPUT
sclr
CLK
INPUT
CLK
NOT
OUTPUT
DAC_CLK

Schematics

MiniMAX-FPGA


U26
AD0
P100,FAST
U10
OBUFZ
DO0
DI0
A0
U11
INLAT
U27
AD1
P98,FAST
U12
OBUFZ
DO1
DI1
A1
U13
INLAT
U28
AD2
P94,FAST
U14
OBUFZ
DO2
DI2
A2
U15
INLAT
U29
AD3
P92,FAST
U16
OBUFZ
DO3
DI3
A3
U17
INLAT
U30
AD4
P89,FAST
U22
OBUFZ
DO4
DI4
A4
U23
INLAT
NDE
U31
AD5
P87,FAST
U24
OBUFZ
DO5
DI5
A5
U25
INLAT
U32
AD6
P83,FAST
U20
OBUFZ
DO6
DI6
A6
U21
INLAT
U33
AD7
P81,FAST
U18
OBUFZ
DO7
DI7
A7
U19
INLAT
U39
A16
P60
PS0
A16
U35
INLAT
U41
A18
P62
PS2
A18
U37
INLAT
U40
A17
P61
PS1
A17
U36
INLAT
F1
U42
A19
P63
PS3
A19
U38
INLAT
U55
U34
ASTB
P86
U9
IBUF
ASTB
U74
SELECT
P48,FAST
OBUFZ
SELECT
U68
AND2B1
U83
AND2B1
DECODER
DI[0..7]
DO[0..7]
NDE
NOD
SELECT
DECODER.SCH
A[0..15]
NIORD
NIOWR
BS[0..2]
CPUCLK
U86
VCC
+5
U85
OBUF
NBUSY
U87
OPAD
P99
NBUSY
U73
IPAD
XCLK
U69
IBUF
U71
IPAD
STDP
U70
IBUF
U66
IPAD
CPUCLK
U65
GCLK
U84
INV
Detect HALT mode
This logic will keep
CE of the Flash EEPROM
high during HALT mode
in order to reduce the
power consumption.
U81
C
D
Q
FD
U77
NAND2B2
U78
OR2
HALT
IDLE
U72
AND3B1
U75
U79
AND2
AND3
U80
AND2
U76
D
Q
C
FD
U82
OR2
U67
NIOWR
ACLK
U59
U60
U61
BS0
BS1
BS2
INLAT
ASTB
U57
P21
BS0
U58
P96
BS1
U56
P97
BS2
U63
VCC
+5
U62
OBUF
NINIT
U64
OPAD
P65
NINIT
A8
U1
IBUF
U43
A8
P88
A9
U2
IBUF
U44
A9
P93
A10
U3
IBUF
U45
A10
P25
A11
U4
IBUF
U46
A11
P23
A12
U5
IBUF
U47
A12
P19
A13
U6
IBUF
U48
A13
P17
A14
U7
IBUF
U49
A14
P14
A15
U8
IBUF
U50
A15
P12
NIORD
U51
IBUF
U53
P8
NIORD
U52
IBUF
U54
P5
NIOWR
|PARTTYPE=3030PQ100-70
Michael Kraemer
Michael Kraemer
Edenkobener Weg 24
D40229 Duesseldorf
Germany
Size
A3
Document Number
REV
1
Date:
November 29, 1999
Sheet
1
of
7



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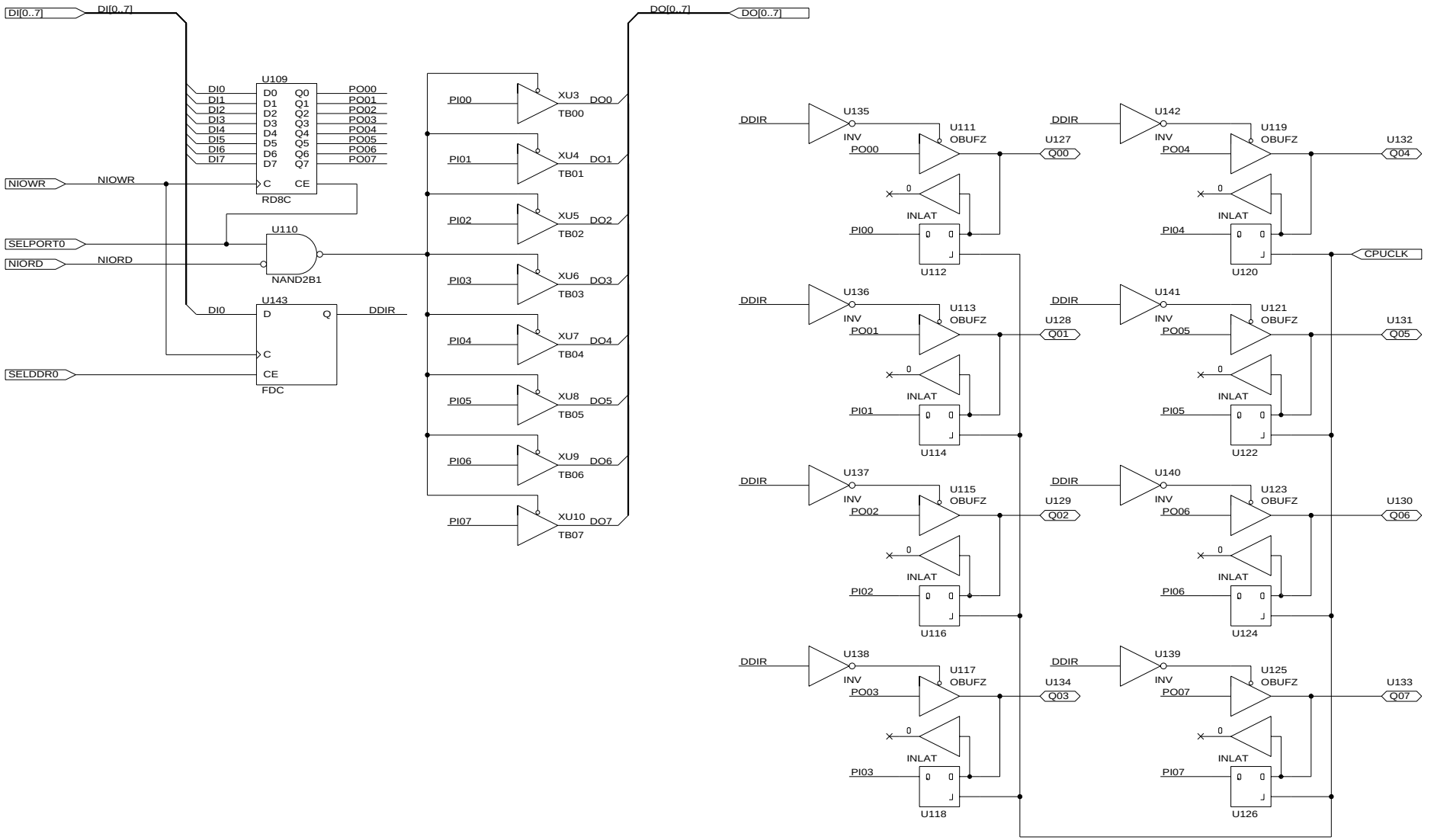
Germany

Title	Decoder	
Size: A3	Document Number: DECODER.SCH	REV: 1
Date: December 31, 2001	Sheet 2 of 7	



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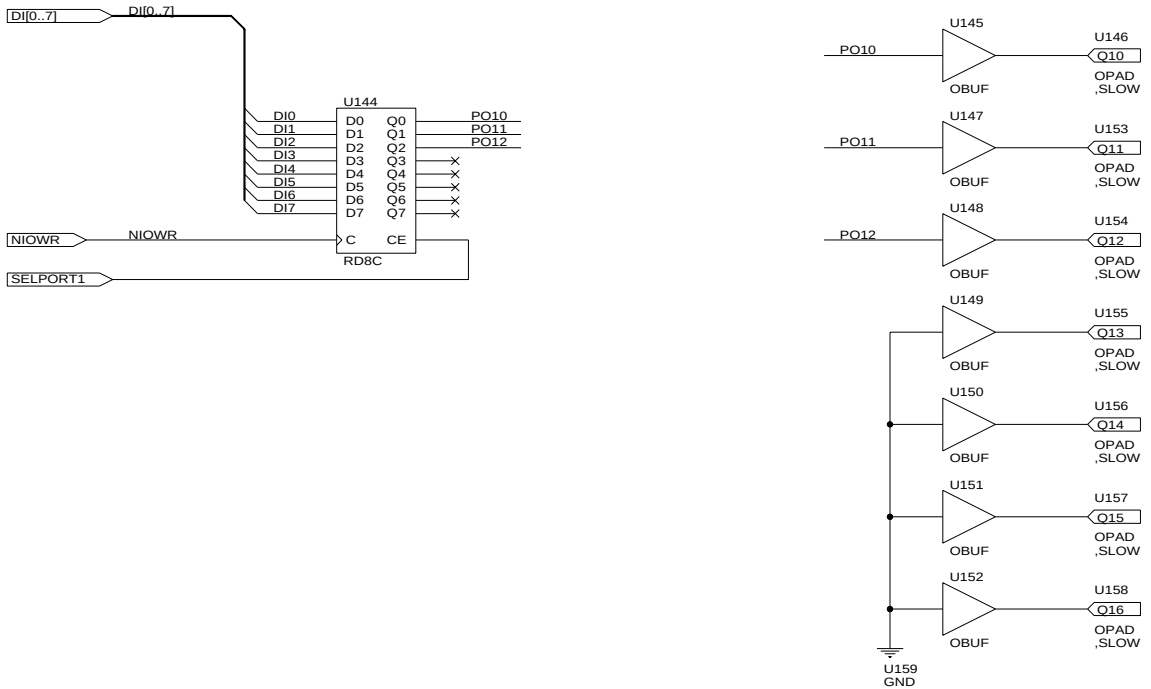
Title	Port 0
Size: A3	Document Number: PORT0.SCH
REV: 1	
Date: December 19, 1999	Sheet 3 of 7



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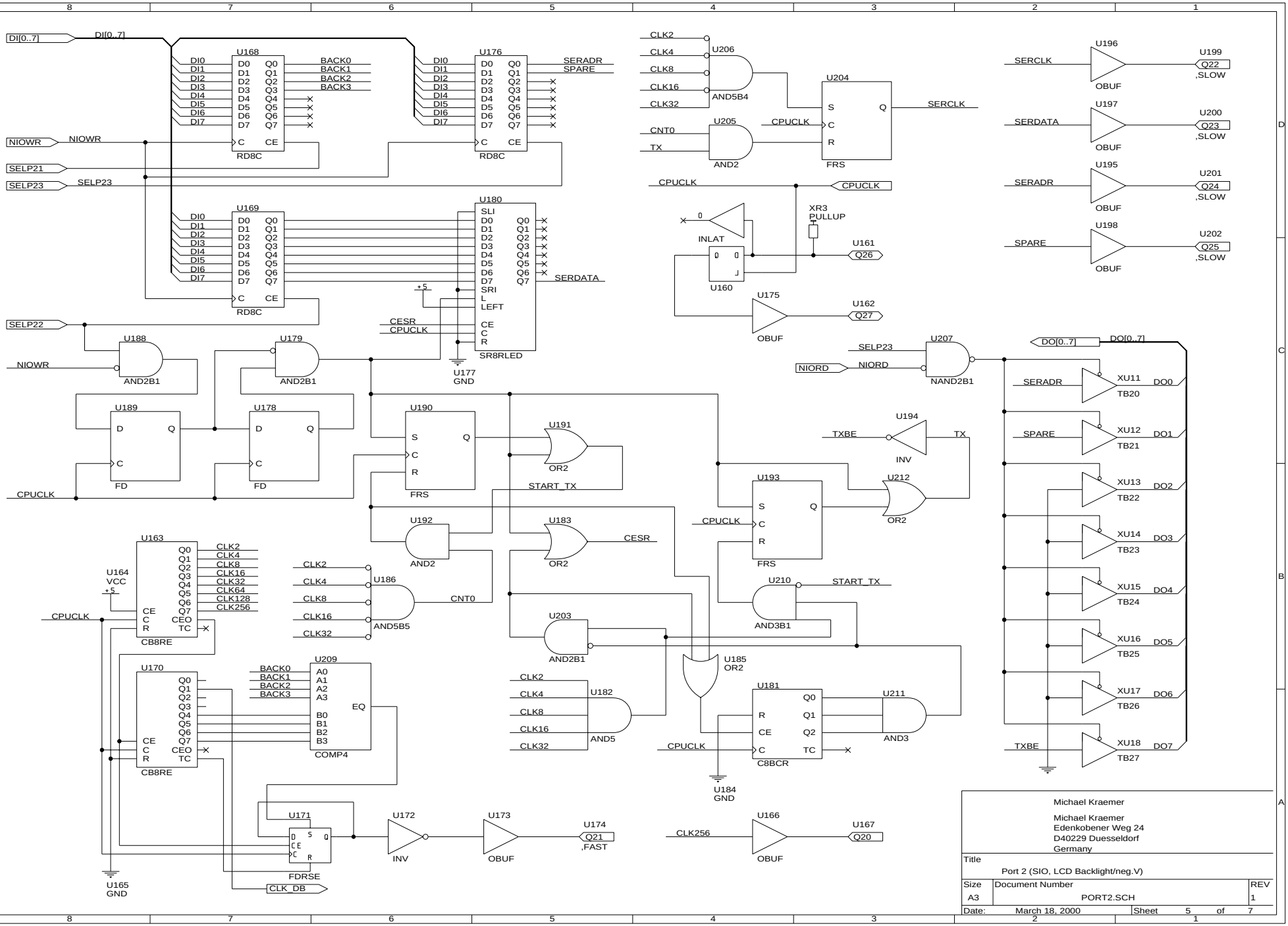
Title	Port 1 (Output Port)	
Size: A3	Document Number: PORT1.SCH	REV: 1
Date: December 19, 1999	Sheet 4 of 7	



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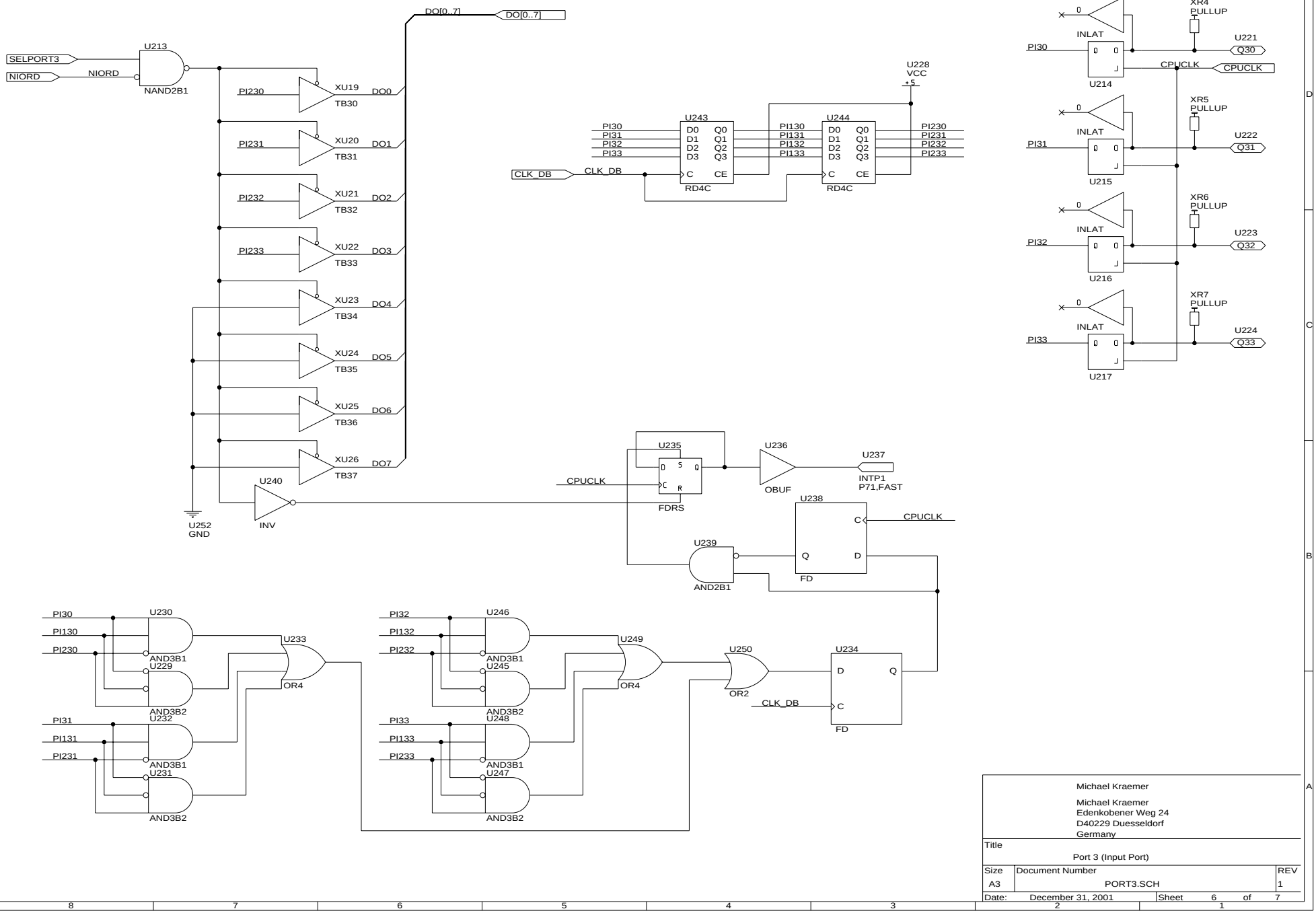
Germany

Title	Port 2 (SIO, LCD Backlight/neg.V)	
Size: A3	Document Number: PORT2.SCH	REV: 1
Date: March 18, 2000	Sheet 5 of 7	



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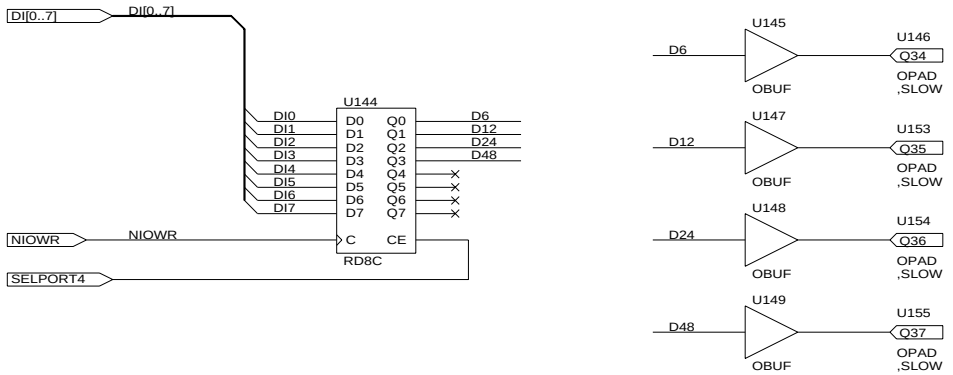
Title	Port 3 (Input Port)
Size: A3	Document Number: PORT3.SCH
REV: 1	
Date: December 31, 2001	Sheet 6 of 7



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Title

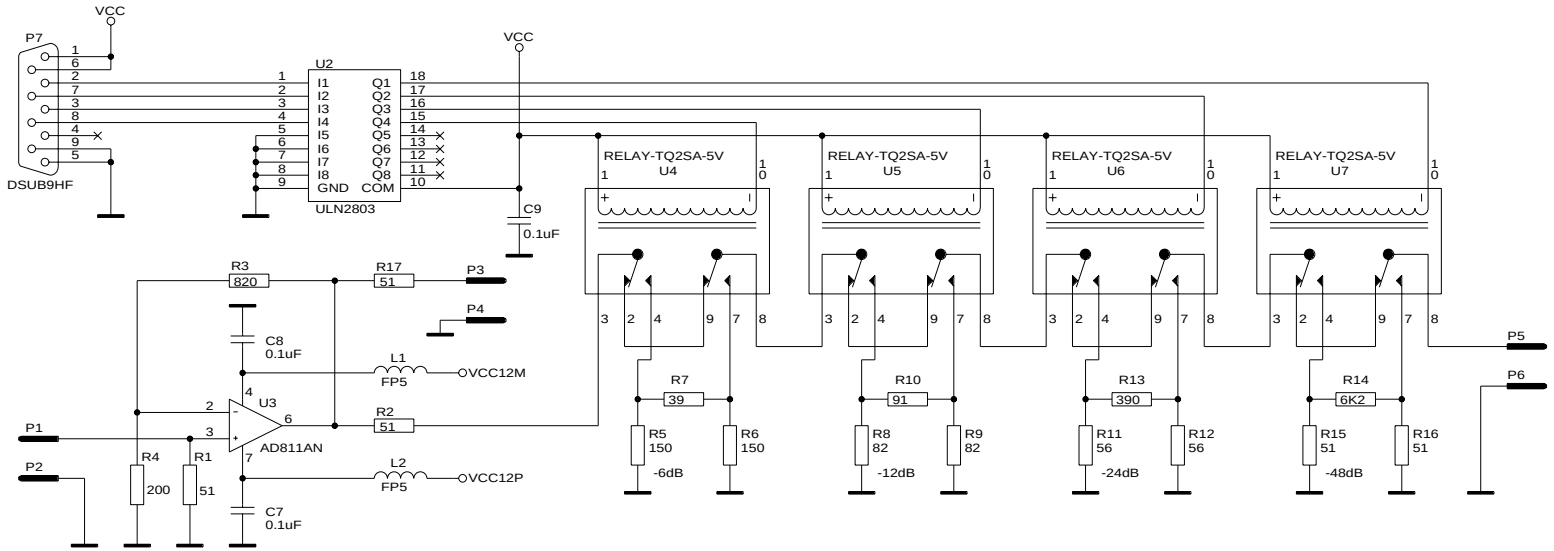
Port 4 (Output Port)

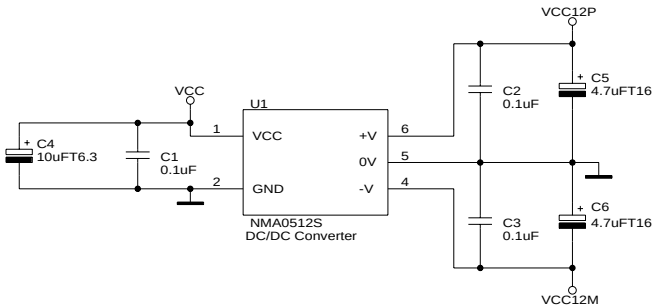
Size	Document Number	REV
A3	PORT4.SCH	1

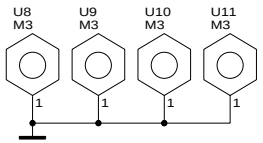
Date: December 31, 2001 Sheet 7 of 7

Schematics

WOBBEL-PA







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Title	Endstufe fuer Wobbelsender	
Size: A3	Document Number: WOBBELPA.SCH	REV: 1
Date: May 14, 2000	Sheet 1 of 1	