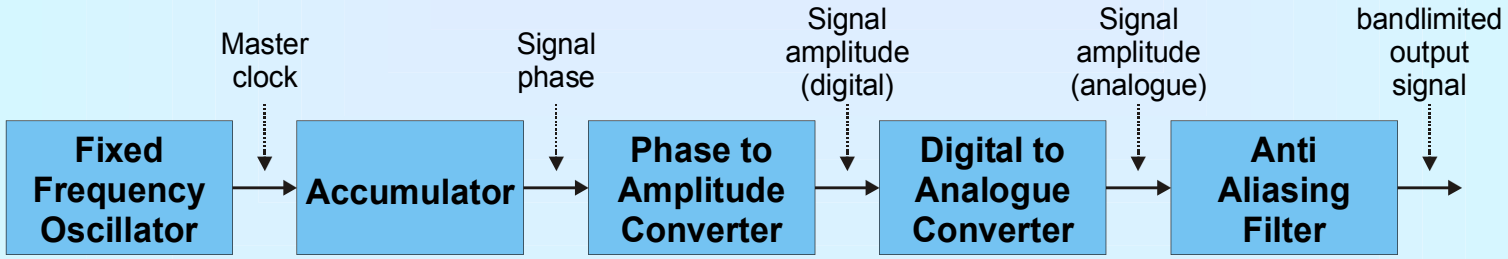
Direct Digital Synthesis

for amateur radio applications and beyond...

Table of contents

Numerically Controlled Oscillator

- Principles
  - Fixed frequency oscillator clocks an accumulator
  - The output of the accumulator represents the current signal phase
  - The signal phase is converted to the signal amplitude
    - Usually implemented as a ROM lookup-table
  - The amplitude is converted to analog by a suitable D/A converter
  - An analog filter selects the required alias frequency range
    - This is usually, but not necessarily, a low-pass filter



Numerically Controlled Oscillator

- Applicable laws: Shannon's sampling theorem
  - maximum signal bandwidth is half the clock frequency
    - This law is often misunderstood as „maximum signal frequency“, but actually the anti-aliasing filter can select any frequency band (or „image“) whose width is less than half the clock frequency:

$$F_{Signal} = \left[0 \ldots \frac{1 * F_{Clk}}{2}\right] \text{ or } \left[\frac{1 * F_{Clk}}{2} \ldots \frac{2 * F_{Clk}}{2}\right] \text{ or } \left[\frac{2 * F_{Clk}}{2} \ldots \frac{3 * F_{Clk}}{2}\right] \text{ or } \ldots$$

    - Often only the first image is used and then the signal frequency is limited to the range between 0 and clk/2. Due to limited filter parameters, the practical bandwidth is limited to something like:

$$F_{Signal} = \left[0 \ldots 0.4 * F_{Clk}\right]$$

Numerically Controlled Oscillator

- Signal to Noise ratio (SNR) over DAC resolution
  - The SNR depends on the DAC resolution according to the following equation (where „ρ“ is the number of bits):

$$\frac{SNR}{bit} = 20 \cdot \log(2) \cdot \rho = 6.02 \cdot \rho \quad [dB]$$

This equation applies for signals that use the full dynamic range and for which all values appear with the same probability. The SNR for a sine wave is about 1.76 dB higher.

Numerically Controlled Oscillator

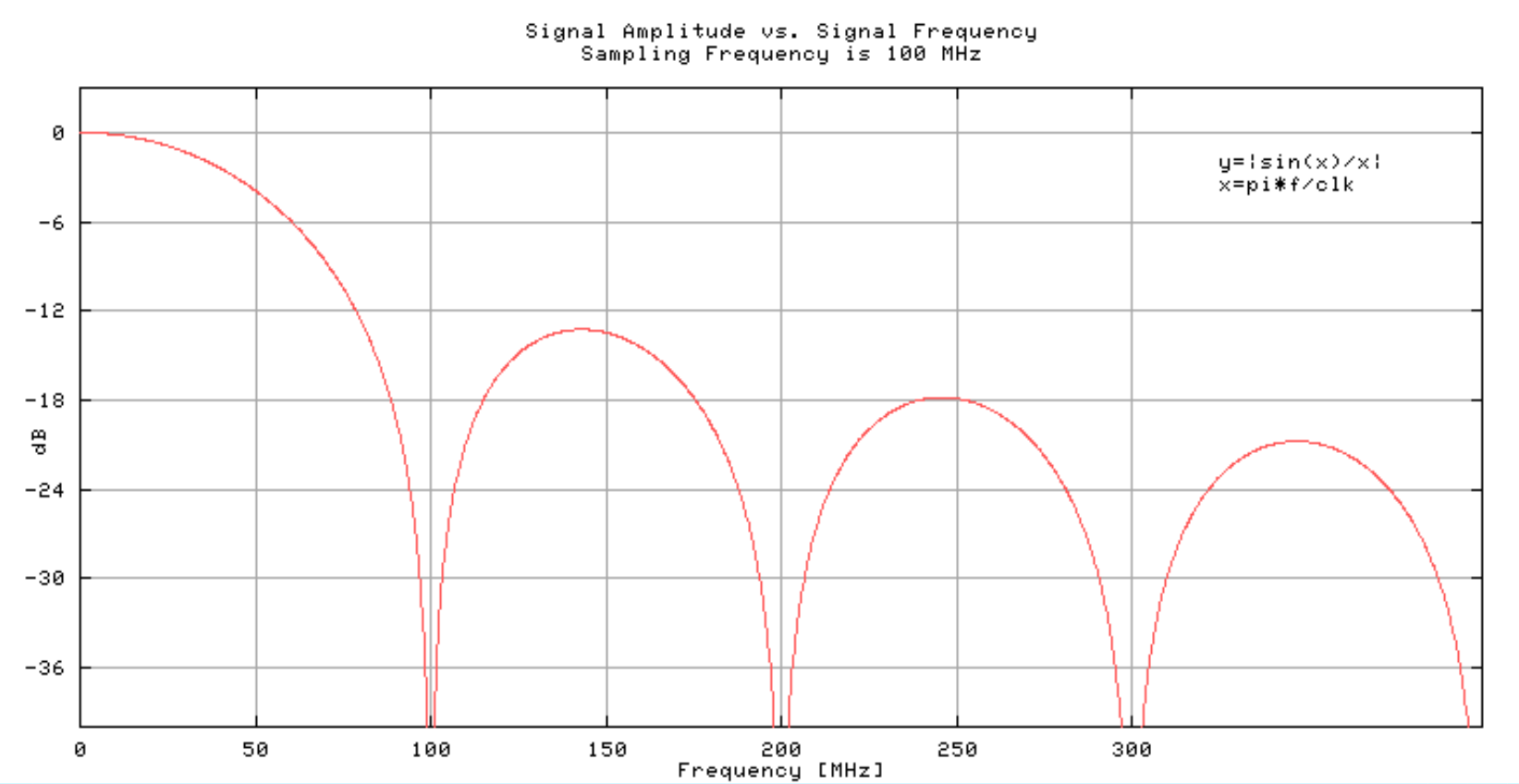
- Signal to Noise ratio (SNR) over sampling rate
  - The noise power is evenly distributed over half the bandwidth. The noise is therefore further reduced, when the bandwidth is limited to Δf by an additional filter:

$$\frac{SNR}{bit} = 6.02 \cdot \rho + 10 \cdot \log\left(\frac{f_{Clk}/2}{\Delta f}\right) \quad [dB]$$

This equation also shows that oversampling improves the signal to noise ratio by about 3 dB per factor of two.

Numerically Controlled Oscillator

- Output amplitude changes with |sin(x)/x|
  - The generated signal amplitude follows a |sin(x)/x| fuction as depicted below. Note that the master clock frequency in this example is 100 MHz.



Fixed Frequency Oscillator

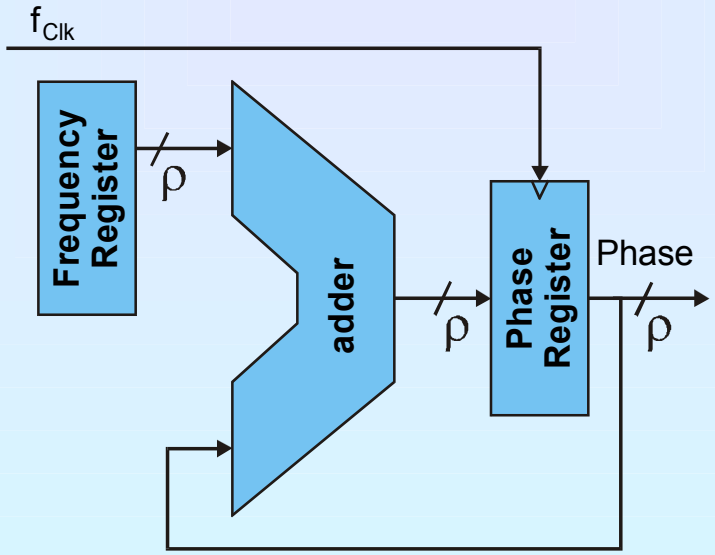
- Requirements:
  - Superior frequency precision and low drift
  - Low jitter
- Typically achievable frequency with today's FPGAs:
  - 25 ~ 150 MHz system frequency
  - 10 ~ 60 MHz signal output frequency in case of low-pass anti-aliasing filter

Accumulator

- Requirements and constraints:
  - Add an increment to the current phase in one clock cycle
  - Bitsize ρ of accumulator determines the frequency resolution r

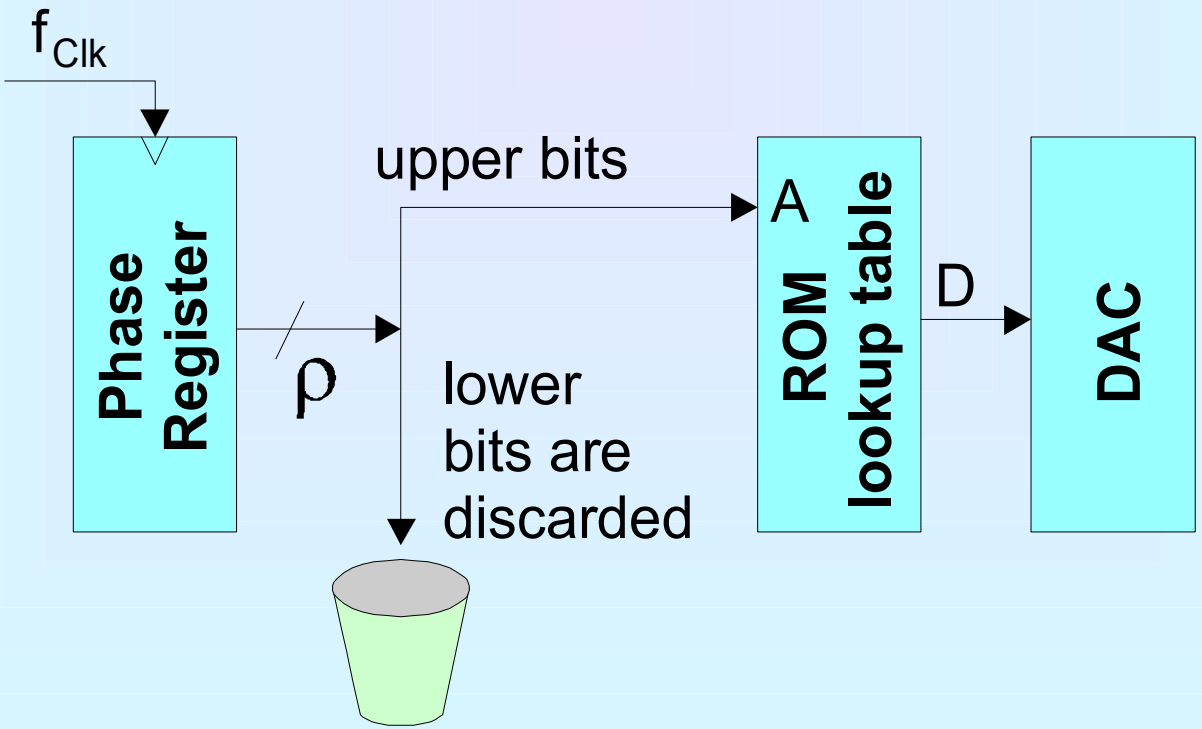
$$r = \frac{f_{Clk}}{2^{\rho}} \quad [Hz]$$

typical implementation (ρ is typically between 24 and 32 bits):



Phase-to-Amplitude Converter

- ROM lookup table
  - The sines for a limited number of arguments are stored in ROM
  - The address lines are connected to the upper output signals from the phase accumulator. Its lower outputs are discarded
  - The ROM data output feeds the DAC



Phase-to-Amplitude Converter

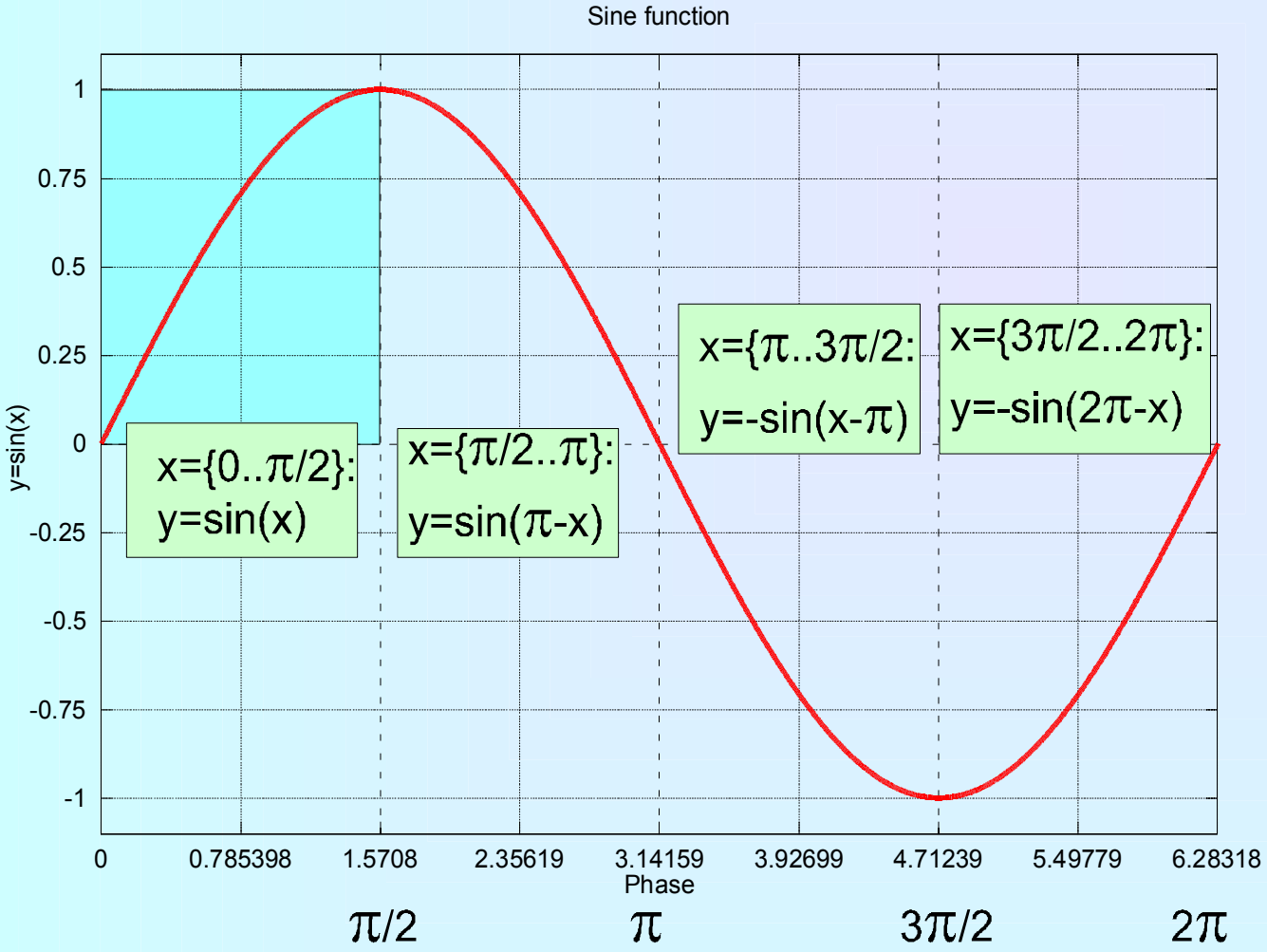
- ROM lookup table
  - Which ROM size is required for a given ADC resolution, so that the previously calculated SNR is not impaired?
    - The slope of the sine function, which is the dependency of the output signal from the input, is highest in the vicinity of $x = n * \pi$
    - When x is small, then this relation applies: $\sin(x) \approx x$
    - The range of x is $\{0..2\pi\}$ and the range of y is {-1..+1}. From this we conclude, that we need about π-times as many argument x-values than function y-values.
    - In the binary world, this translates to two more bits for the addresses than for the data.
    - → For an DAC resolution of 14 bits, we need 2^{16} = 64K entries in ROM, so that any input value can generate any 14-bit output value without missing codes

Phase-to-Amplitude Converter

- ROM lookup table (contd.)
  - To preserve amplitude and phase accuracy, the ROM must typically have a size of a 64~128 kWords and an access time that satisfies the master clock
  - The access time is achievable in an FPGA, but it can typically hold only 256 ~ 2048 entries. What can be done?
    - Using the symmetry of the sine function, the size can be reduced to ¼
    - Implementing linear interpolation between ROM values, the size of the lookup table can be easily further reduced to 1/32 or more without noticable loss of precision (i.e. increase of noise.)

Phase-to-Amplitude Converter

- ROM lookup table (contd.)
  - Using symmetry

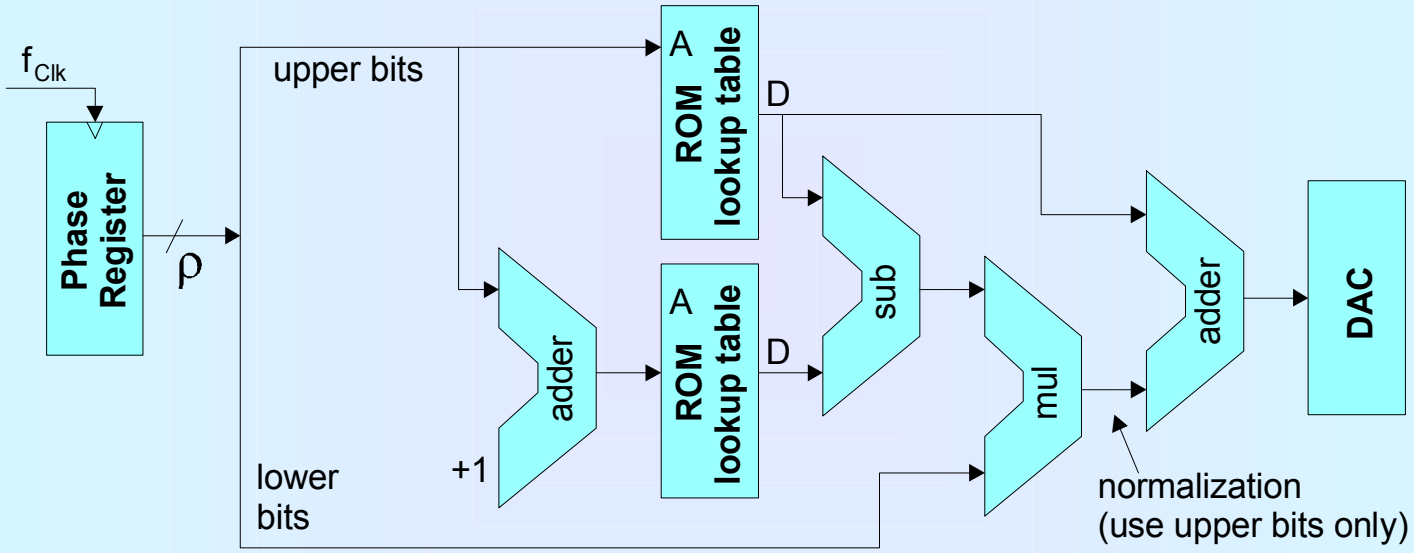


Only the shaded part of the sine is stored in ROM. All other arguments are mapped into that range.

The table size is reduced to a quarter (ROM address is two bits smaller) and the results are reduced to half the original range (one bit less data).

Phase-to-Amplitude Converter

- ROM lookup table (contd.)
  - Using interpolation



  - Amplitude of current and next phase are calculated. Their difference is multiplied with a weighing factor taken from the lower (previously discarded) phase, the result is normalized and added to the current amplitude.

Phase-to-Amplitude Converter

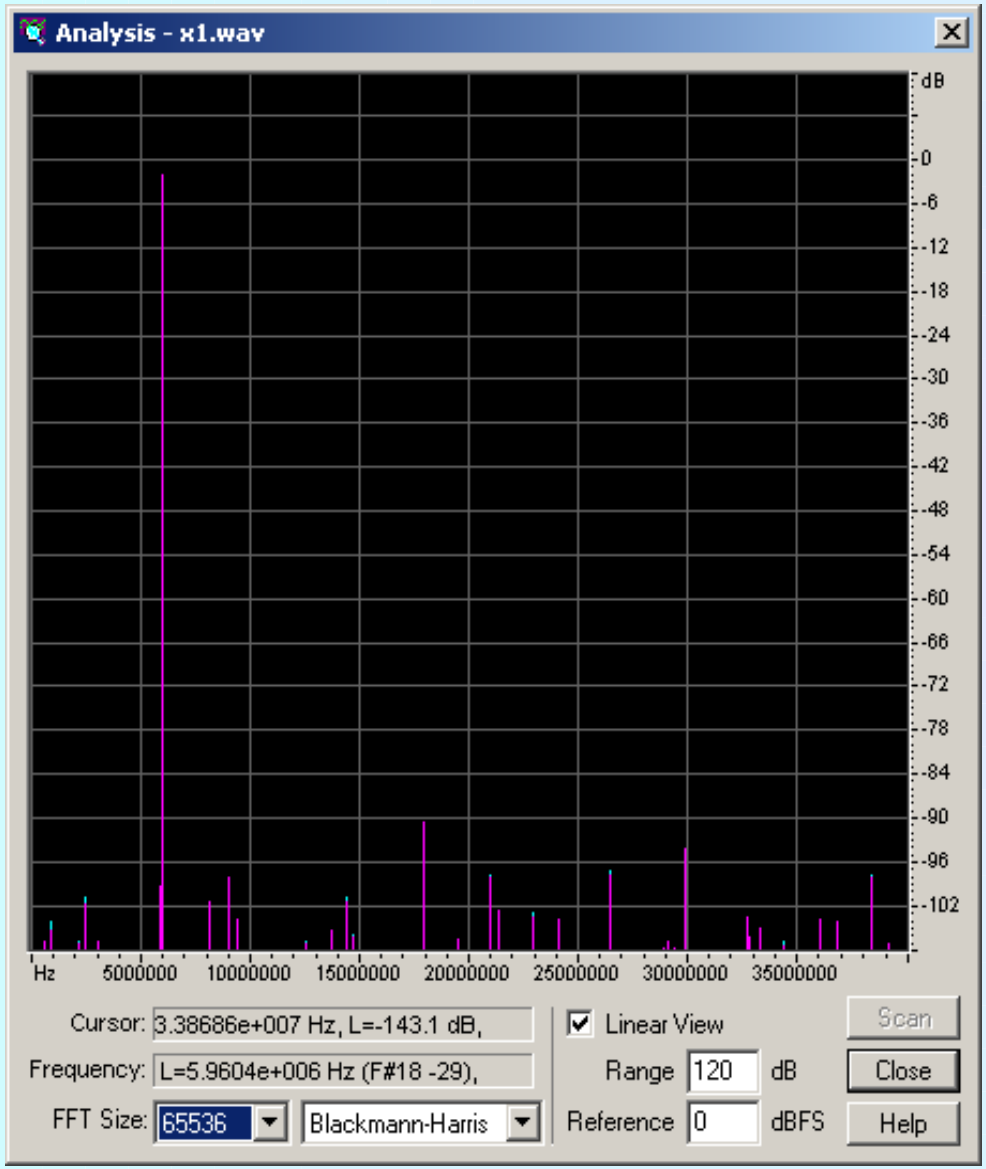
- Cordic Algorithm
  - **CO**ordinate **R**otation **DI**gital **C**omputer
  - Algorithm to calculate complex rotating pointer iteratively
  - Fairly simple to implement in hardware or software, but slower than lookup table
  - Precision grows with number of iterations
  - Cordic is often used in audio applications

Digital-to-Analogue Converter

- DAC must have the following features:
  - Clock rate more than twice the signal bandwidth
  - Resolution as required by the application
  - Low noise and low total harmonic distortion
- Selected data of currently available devices

Anti Aliasing Filter

- The anti aliasing filter is usually a passive LC or RC filter
- It limits the signal bandwidth in such a way, that the desired frequencies can pass with almost no attenuation, while the closesed alias is attenuated to below the SNR


Analysis - x1.wav
dB
0
-6
-12
-18
-24
-30
-36
-42
-48
-54
-60
-66
-72
-78
-84
-90
-96
-102
Hz
5000000
10000000
15000000
20000000
25000000
30000000
35000000
Cursor: 3.38686e+007 Hz, L=-143.1 dB,
Frequency: L=5.9604e+006 Hz (F#18 -29),
FFT Size: 65536
Blackmann-Harris
Linear View
Range 120 dB
Reference 0 dBFS
Scan
Close
Help