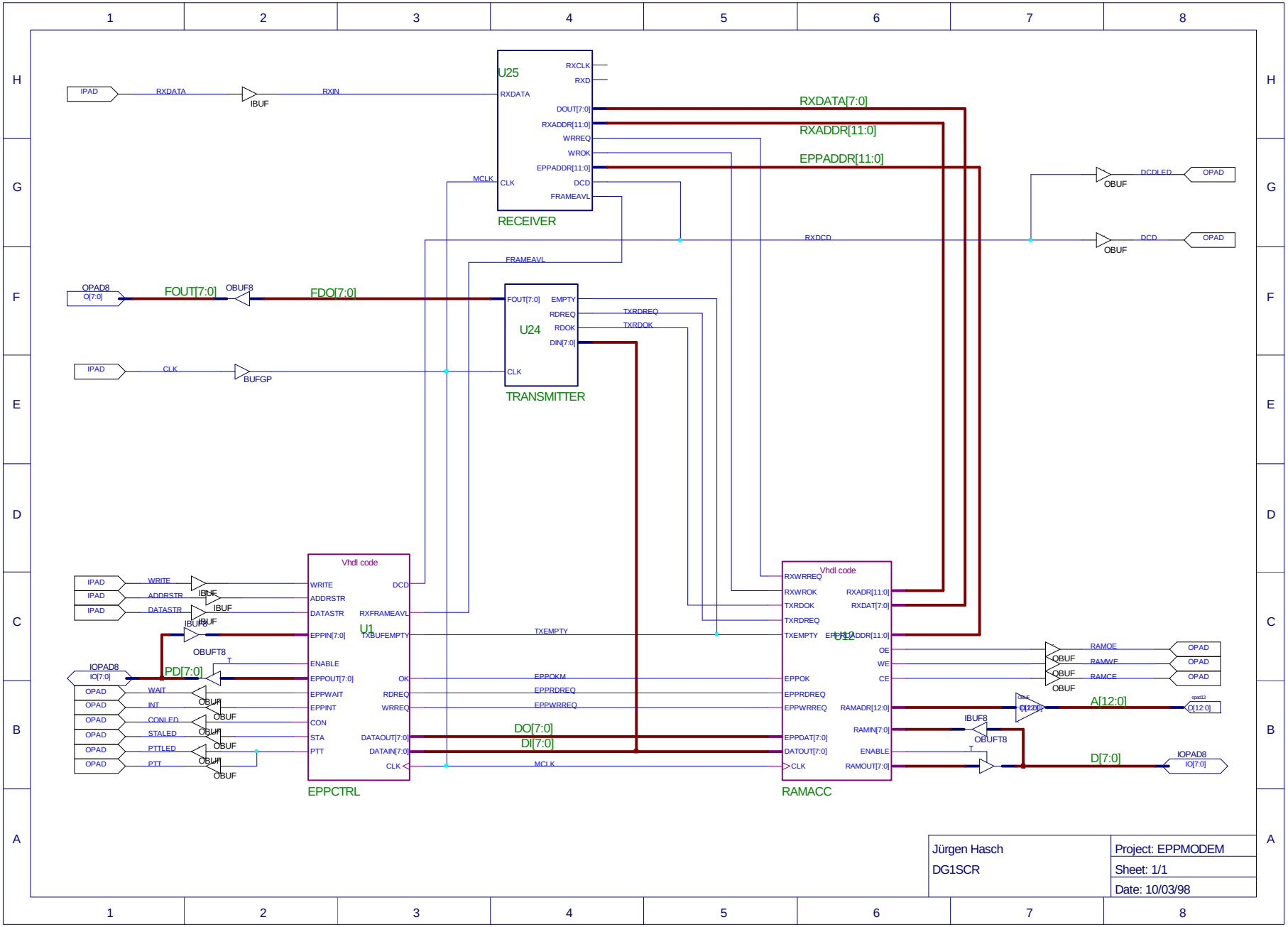
U25
RECEIVER
RXCLK
RXD
RXDATA
DOUT[7:0]
RXADDR[11:0]
WRREQ
WROK
EPPADDR[11:0]
DCD
FRAMEAVL
CLK
MCLK
IPAD
RXDATA
IBUF
RXIN
RXDATA[7:0]
RXADDR[11:0]
EPPADDR[11:0]
OBUF
DCDLED
OPAD
RXDCD
DCD
OPAD8
O[7:0]
FOUT[7:0]
OBUF8
FDO[7:0]
FRAMEAVL
U24
TRANSMITTER
FOUT[7:0]
EMPTY
RDREQ
RDOK
DIN[7:0]
TXRDREQ
TXRDOK
IPAD
CLK
BUFGP
Vhdl code
U1
EPPCTRL
WRITE
ADDRSTR
DATASTR
EPPIN[7:0]
ENABLE
EPPOUT[7:0]
EPPWAIT
EPPINT
CON
STA
PTT
DCD
RXFRAMEAVL
TXBUFEMPTY
OK
RDREQ
WRREQ
DATAOUT[7:0]
DATAIN[7:0]
CLK
IBUF
OBUFT8
IOPAD8
IO[7:0]
PD[7:0]
OPAD
WAIT
INT
CONLED
STALED
PTTLED
PTT
OBUF
TXEMPTY
EPPOKM
EPPRDREQ
EPPWRREQ
DO[7:0]
DI[7:0]
MCLK
Vhdl code
U12
RAMACC
RXWRREQ
RXWROK
TXRDOK
TXRDREQ
TXEMPTY
EPPOK
EPPRDREQ
EPPWRREQ
EPPDAT[7:0]
DATOUT[7:0]
CLK
RXADR[11:0]
RXDAT[7:0]
EPPADDR[11:0]
OE
WE
CE
RAMADR[12:0]
RAMIN[7:0]
ENABLE
RAMOUT[7:0]
RAMOE
RAMWE
RAMCE
A[12:0]
D[7:0]
IBUF8
OBUFT8
Jürgen Hasch
DG1SCR
Project: EPPMODEM
Sheet: 1/1
Date: 10/03/98