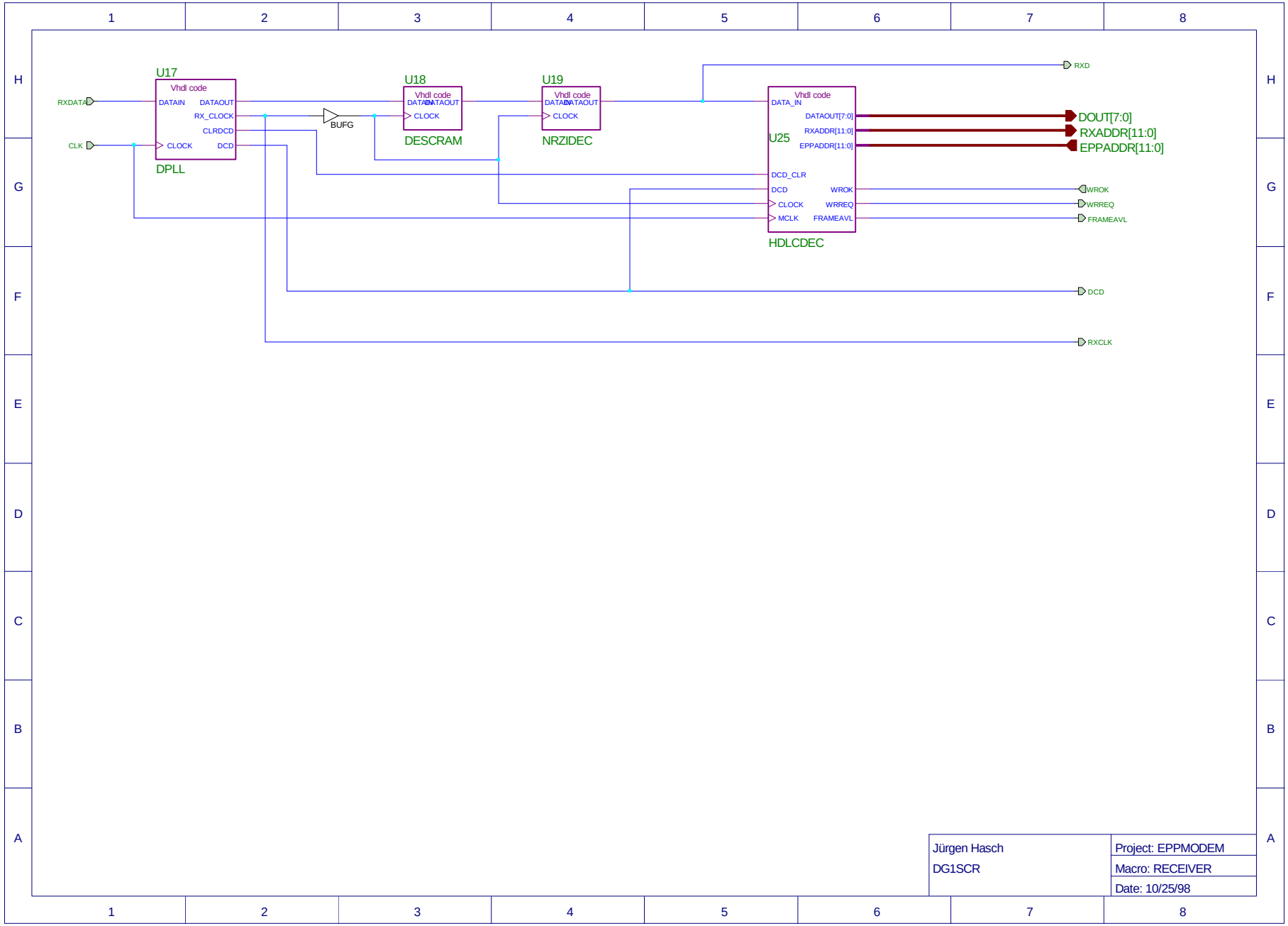
U17
Vhdl code
RXDATA
DATAIN
DATAOUT
RX_CLOCK
CLRDCD
CLK
CLOCK
DCD
DPLL
BUFG
U18
Vhdl code
DATAIN
DATAOUT
CLOCK
DESCRAM
U19
Vhdl code
DATAIN
DATAOUT
CLOCK
NRZIDEC
RXD
Vhdl code
DATA_IN
DATAOUT[7:0]
RXADDR[11:0]
EPPADDR[11:0]
U25
DCD_CLR
DCD
CLOCK
MCLK
WROK
WRREQ
FRAMEAVL
HDLCDEC
DOUT[7:0]
RXADDR[11:0]
EPPADDR[11:0]
WROK
WRREQ
FRAMEAVL
DCD
RXCLK
Jürgen Hasch
DG1SCR
Project: EPPMODEM
Macro: RECEIVER
Date: 10/25/98