

[illegible]

The schematic diagram shows two 74LS-series decoders, IC21 (74LS541) and IC22 (74LS574), connected to a system of 14 input lines (INB-1 to INB-14) and 8 output lines (OUTB-1 to OUTB-8).

IC21 (74LS541) Decoder:

- Inputs:** INB-1 to INB-14 are connected to pins D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, and D23 respectively.
- Outputs:** OUTB-1 to OUTB-8 are connected to pins Q1, Q2, Q3, Q4, Q5, Q6, Q7, and Q8 respectively.
- Control:** The clock input (CLK) is connected to pin 10, which is also connected to the clock input of IC22. The output enable (OC) is connected to pin 11, which is connected to the output enable of IC22.
- Power:** The power supply (VCC) is connected to pin 16, and ground (GND) is connected to pin 15.

IC22 (74LS574) Decoder:

- Inputs:** INB-1 to INB-14 are connected to pins D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, and D23 respectively.
- Outputs:** OUTB-1 to OUTB-8 are connected to pins Q1, Q2, Q3, Q4, Q5, Q6, Q7, and Q8 respectively.
- Control:** The clock input (CLK) is connected to pin 10, which is also connected to the clock input of IC21. The output enable (OC) is connected to pin 11, which is connected to the output enable of IC21.
- Power:** The power supply (VCC) is connected to pin 16, and ground (GND) is connected to pin 15.

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- Figure 1: Pin connections for the CN1 connector. The diagram shows a vertical list of pins from D0 to A15, followed by PRG_RD, YEN_RD, YEN_WR, WR, /HOLD, /HOLDA, CLK, ECLK, /BST, and CN1-39 to CN1-40. Each pin is connected to a specific signal or ground. Pins D0-D7 are connected to CN1-1 to CN1-8. Pins A0-A15 are connected to CN1-11 to CN1-26. Pins PRG_RD, YEN_RD, YEN_WR, and WR are connected to CN1-29, CN1-30, CN1-31, and CN1-32 respectively. Pins /HOLD and /HOLDA are connected to CN1-34 and CN1-35 respectively. Pins CLK and ECLK are connected to CN1-36 and CN1-37 respectively. Pin /BST is connected to CN1-38. Pins CN1-39 and CN1-40 are connected to ground.