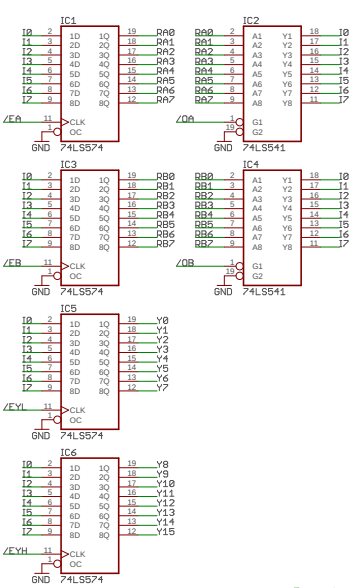
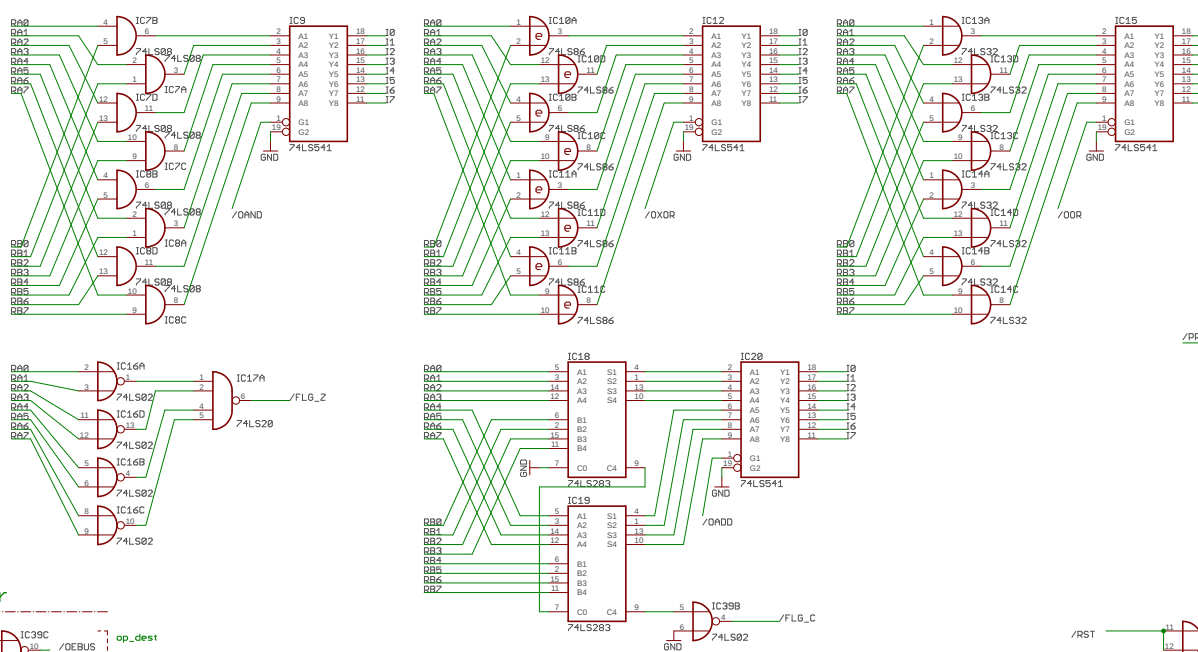


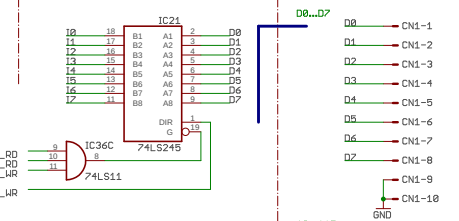
Reg. A, B, YL, YH



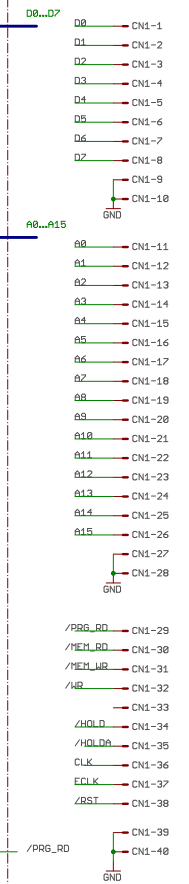
Arithmetic & Logic



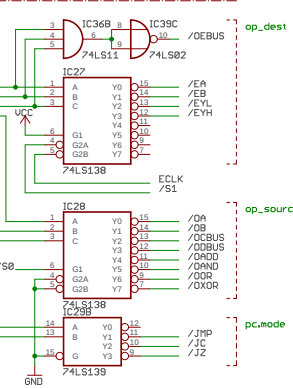
Buses



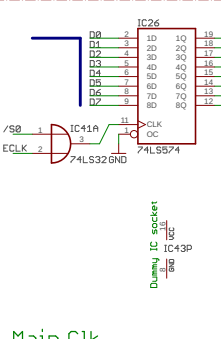
CPU connect



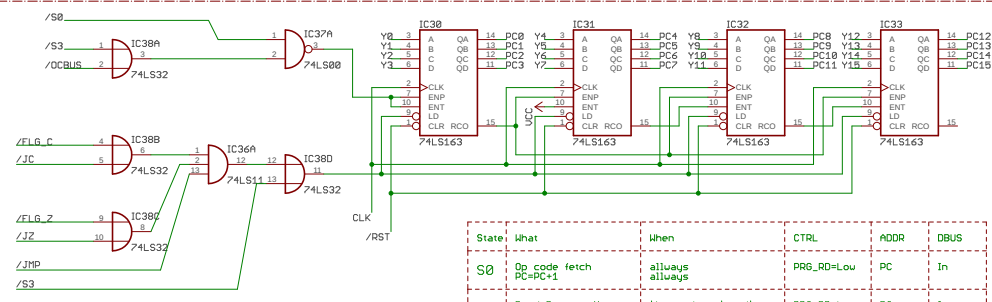
Op.decoder



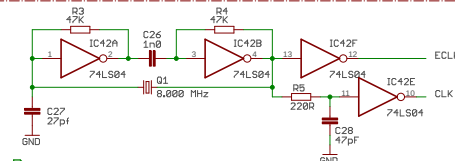
Op.reg



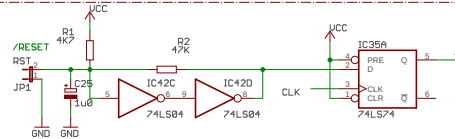
PC



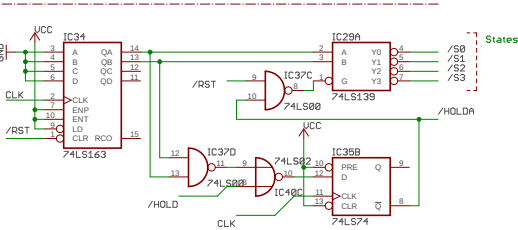
Main.Clk



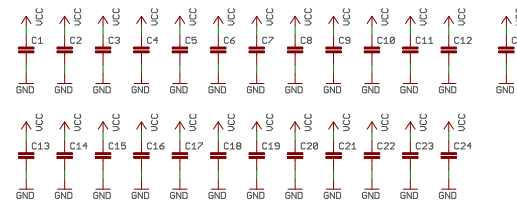
Reset



States S0..S4



State	What	When	CTRL	ADDR	DBUS
S0	Op code fetch PC=PC+1	always always	PRG_RD=Low	PC	In
S1	Read Program Memory	if opcode = immediate if opcode = origin_mem	PRG_RD=Low MEM_RD=Low	PC reg_Y	In In
S2	Write data memory	if opcode = dest_mem	MEN_WR=Low	reg_Y	Out
S3	PC = reg_Y PC=PC+1 nothing	if opcode = Jump if opcode = immediate if opcode = others	none	reg_Y	tri-state



U02