Locking VCXOs to 10MHz
for the Microwave and mmWave local oscillators.

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Most microwave and millimeter wave converters use a quartz controlled oscillator in the 70 to 130MHz frequency range at the base of their local oscillator generation. The need for frequency stability is often guaranteed by temperature compensated and/or temperature controlled oscillators, however the (relative) accuracy can only be obtained by calibrating against a reference standard, or even better, by maintaining it locked to an external reference. 10MHz GPS disciplined sources are becoming quite popular and a few good designs were already published. The following article presents a universal locking circuit for any VCXO source up to 130MHz, with the particularity of being done with the latest programmable logic technology that enables it to be tailored to specific requirements without changing the PCB board.

Introduction

Locking a VCXO that operates in the 70 to 130MHz range, to a 10MHz reference, doesn't have any *a priory* difficulty, and the use of today's integrated circuits would make this job quite easy. The obvious scheme would employ a PLL circuit with programmable dividers a suitable phase comparator and loop filter. This could be achieved using different technologies. - It could be done using discrete logic either with CMOS or TTL circuits, or done using integrated PLL's with direct BCD or binary programming, or using a modern pll chip and a small microcontroller, or, at last, employing programmable digital circuitry, a gate-array configured with all the dividers and phase comparators we would need to accomplish the job.

Technologies

In the next paragraphs the technologies and their advantages and disadvantages to our application are analyzed.

Using **Discrete logic** we could tailor the circuit to our needs however if we have to accommodate several LO configurations the circuit may become too complex and maybe too big. Variations on this scheme were used in Europe to lock to DCF77 /1/, and circuits were at least the size of a 10x16cm eurocard.

Using an **old style PLL chip with direct interface** would be a reasonable compromise as it could be done essentially on a single chip, or in two chip if we need a prescaler to lower the VCXO frequency. Some of these PLL chips are however not too good when it comes to phase comparator performance as we discuss later on. Using this approach we may have a reasonable performance on the lower microwave bands but certainly unacceptable phase noise on the mmW bands /2/.

Using **a modern PLL chip plus a micro-controller** would result in a quite good solution, we could have all the flexibility we want driven by the software and still have a very compact design (all components would be available in SMD). We would still be limited by the specific internal architecture of the IC and phase comparators performance. Although these are much better than the first generation of PLL chips but some types still exhibit a certain amount of phase backlash. This solution would be simple to implement using a PLL chip from the LMX series (national) or MB series (fujitsu) along with a PIC processor and some dip switches. Despite the programmability of both reference and main dividers we still would have a fixed hardware configuration.

At last we could use a **gate-array** (a CPLD to be more precise) configured to have all the dividers and phase comparators we would need. This solution is topologically the same as the first one presented only this time it is not implemented with discrete logic and interconnecting wires but rather uses generic logic inside a gate array configured in the same way as if it was done discretely. The digital circuitry implemented contains all dividers and phase comparators required, and the phase comparator must then be done in such a way that it does not present any of the drawbacks we may find in the previous solutions.

The “always active” phase comparator output and Phase backlash.

One of the known problems of the first generation of PLL chips was the resulting backlash of the “leading edge” type phase comparator’s output, although it did not represent any serious problem to the typical application (usually NBFM radios at VHF and UHF frequencies) in which the few Hz wandering would be negligible. However to control an LO that will be multiplied by factors of 100 to 200 (for use at the microwave frequencies) or by a factor above 300 (for use at the millimeter wave frequencies), the story is completely different. This is the reason why most of the PLO’s don’t employ any of the popular PLL chips and those who did only serve to confirm the present considerations for the best /3/ and the worst /2/ as the disastrous arrangement of an MB1501 on the PCOM local oscillators /2/ or the CTI PLO’s that employ uncommon Qualcom PLL chips /3/ that work quite well.
However when it comes to the ultimate precision the diode mixer and the XOR phase comparators are still the winners. For this application, I decided to include a phase comparator that operates at 45degree (a simple XOR gate) plus a sequential phase comparator that operates at 90 degree keeping an output signal average proportional to the phase difference. Nevertheless on a gate-array we may try many other types of phase comparators and control circuits if we are not satisfied.

A little bit about PLD's, CPLD's and FPGA's.

It may be useful to briefly introduce these technologies as this article is mainly targeted to RF and MW readers that are sometimes not aware of great jobs these digital chips can do for the RF and MW designs. However it is out of the scope of the present article to go into detail about these devices.

Some common acronyms:
(PLD – Programmable Logic Device, it usually retains the configuration permanently on fuses, EEPROM or FLASH cells. These can replace a few TTL SSI/MSI)
(CPLD – Complex Programmable Logic Device, it usually retains the configuration permanently on EPROM(obsolete), EEPROM or FLASH cells. These can replace many TTL MSI or a few LSI)
(FPGA – Field programmable Gate Array, usually bigger than a CPLD but configuration resides in RAM cells therefore requiring a configuration download each time it boots up from power off. These can implement a complete system on a single chip).
(JTAG – Joint Test Action Group)

The fist PLD's, that appeared in the eighties presented us with the possibility of replacing a few TTL with a one-time-programmable chip (ex. the PAL and GAL devices) allowing the developer to reduce the board size and enabling logic changes without the need to modify the PCB. The fast evolution of digital circuitry shortly provided bigger devices with erase/program capability. In the nineties, devices with several thousand gates that could replace large boards of TTL MSI become available both in program once and in many erasable flavors. Today (2002) devices with over one million gates are being routinely used by the telecommunications industry. Application that span from building your own microprocessor to a complete system on a chip are the within the actual capabilities of these devices. While very large amounts of logic can be configured in those expensive devices (100 to 300€), smaller devices start to exist at low prices (20€ for a 5000 gates device). The most well know manufacturers of these devices are ACTEL www.actel.com , ALTERA www.altera.com , ATMEL www.atmel.com , LATTICE www.latice.com , XILINX www.xilinx.com but there are others competing on the market.

The CPLD's are quite attractive to be used on the digital circuitry for RF and MW applications namely on digital frequency control, as they retain the configuration after power off and have a size capable of hosting several counters and phase comparators etc. Most manufacturers provide CPLD's within the 5000 gates with EEPROM or FLASH programmed via a JTAG interface. (JTAG interface allows you to configure the chip in circuit via a simple connection to the PC parallel port using an appropriate adaptor and software).

The present design.

The circuit is built around an ALTERA device EPM3064ATC44-4 which is a device that can be configured to a maximum usage of 64 macro-cells, that are, in practice, capable of implementing 64 flip-flops in total. With this we want to implement the

programmable dividers, the several N and R configurations and to build a phase comparator with the desired performance. The chip configuration was written in VHDL compiled with MAX+Plus II and programmed via JTAG.
As this device (EPM3064ATC44-4 the -4 denotes 4 ns delay) can operate directly at 130MHz of clock we can use it without the need of any prescaler. It will only require that input signals are shaped to the appropriate logical levels, this task is easily accomplished by a 74F04.
Three phase-comparator outputs were made available, a classical XOR one phase proportional positive slope and one phase proportional negative slope.
In this design the comparison frequency is always above 50KHz allowing a simple RC loop filter however the R and C component values must be changed according to the VCXO tuning characteristics for best performance and stability.

The VCXO frequency selection is done with 3 bits allowing up to 8 different oscillators to be used for the same chip configuration, of course we can program the chip to whatever 8 values we desire. The actual values during the tests and most relevant for European stations are those with 144MHz intermediate frequency as listed below:

-- conf=000 xtal=96.0000 MHz for 1296MHz >> 144 MHz
-- conf=001 xtal=90.0000 MHz for 2304GHz >> 144 MHz
-- conf=010 xtal=90.666(6) MHz for 2320GHz >> 144 MHz
-- conf=011 xtal=117.0000 MHz for 5760GHz >> 144 MHZ
-- conf=100 xtal=106.5000 MHz for 10GHz >> 144 MHz
-- conf=101 xtal=125.2500 MHz for 24GHz >> 144 MHz
-- conf=110 xtal=122.2500 MHz for 47GHz >> 144 MHz
-- conf=111 xtal=100.0000 MHz for secondary 100MHz standard.

(note that configuration 010 implements the exact .6666(6) infinite quotient)

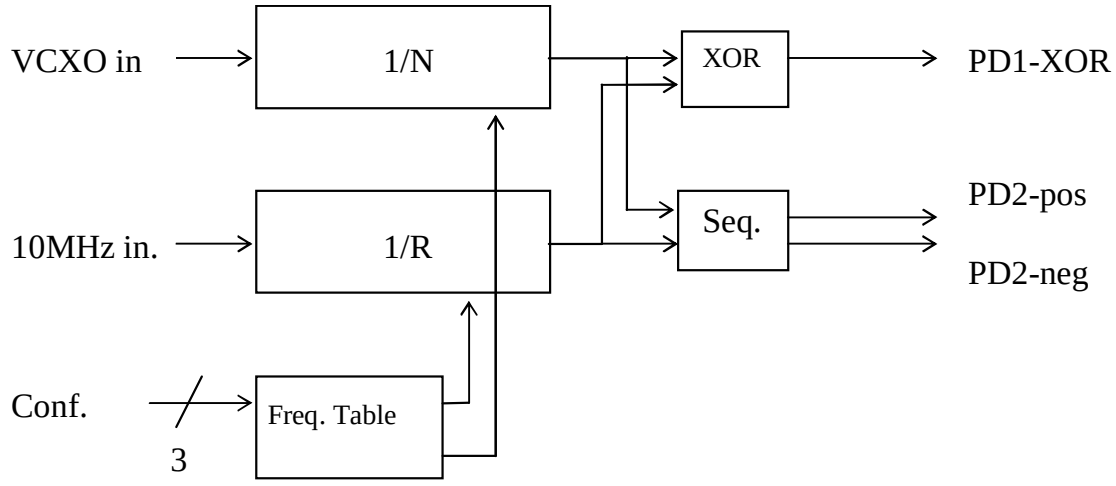

Fig 1 – Block diagram of the logic implemented inside the EPM3064.

Future plans and 1pps from a GPS receiver.

There are a few other interesting standards we may want to lock our VCXOs to. For example VLF transmissions or TV Hsync. Any of those will run on the same principles as the described before, therefore requiring small changes on the VHDL source code that could be made straight away.

Using the GPS 1 pps output is probably the most attractive option for portable operations, however, this will require a totally different phase lock hardware that thanks to the fact of using programmable logic it is possible to implement without a single change on the PCB (as long as if fits inside the CPLD we are using, the 3064). Preliminary tests are being done with a phase-lag counting PLL with 14bit DAC output implemented on PWM and results are quite promising. It may well become the simplest form of portable frequency accuracy. Not to mention that it could serve also to make a 10MHz GPS controlled standard with an incomparable simplicity. This development will be presented as soon as fully tested, hopefully in the next issue.

Thanks for the support received during this project, beta-testers Geert,PA3CSG and PE1KXH.

Hardcopies of the PCB's at 4:1 scale, diagrams and ready to program *.pof and *.jam files can be found at my web page: http://gref.cfn.ist.utl.pt/cupido Thanks to all that helped with ideas info and components. If you have any specific configuration needs that are not covered by the actual listed configuration table please le me know by email cupido@mail.ua.pt .

/1/ - Synchronization to DCF77, E.Seibt DC4RRH, VHF/UHF-1994 Muenchen.
/2/ - PCOM oscillators info and modifications http://lance.rfdude.com/11ghz
/3/ - CTI sources at http://www.cti-inc.com
/4/ - Qualcom at www.qualcomm.com