Excerpt from “HF Radio Systems and Circuits”, Sabin et al., ch. 4, Receiver Design, pp.145-148.

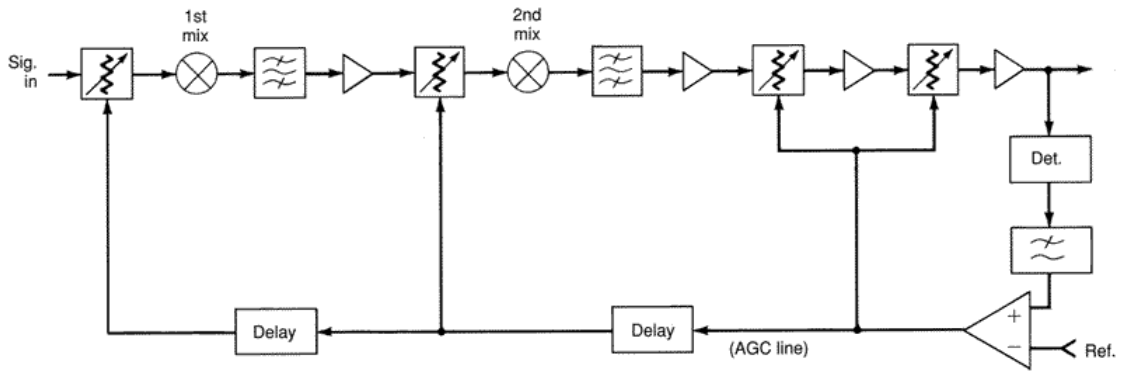

Figure 4.13 A double-conversion receiver has distributed AGC attenuators to prevent stage overload while also causing the output signal-to-noise ratio to rise with signal increases.

AGC design

The means for providing AGC for the overall receiver are important aspects of the block diagram design for an HF SSB receiver. The receiver is operationally required to have nearly constant audio output as the signal input ranges from the 1-μV region to perhaps 1 V or more and to do so without having loop oscillation or distorting the received signal. A receiver primarily designed to be used by an operator for signal search or monitoring will typically allow an audio output rise of 6 dB or so over the input signal range. A receiver for data signals, on the other hand, can have a very flat output requirement so that the following data detection circuits have a constant-amplitude input.

Some insight into AGC loop design can be obtained by studying the receiver signal path shown in Figure 4.13, which includes voltage-controlled attenuators in the RF, first-IF, and second-IF sections. A detector at the output develops a dc output voltage proportional to the IF or AF output level. Intermediate frequency detection is normally used because it gives less time delay (more charging cycles per second) and has output even when the product detector audio output frequency is zero. After low-pass filtering, the voltage is compared with a reference such that gain control action commences when the signal input has reached some threshold level, such as that causing a 6-dB signal-to-noise ratio. As the input signal rises, attenuators at the end of the IF path are used first, preventing overload of the output stages as they reach their signal amplitude limit. Since attenuators at the input of the receiver are not yet being used, the gain into the first and second mixers does not change and the input noise figure is not materially increased. This results in a very nearly linear increase in output signal-to-noise ratio versus input signal increase. If all of the attenuation were placed at the receiver's input, the output signal-to-noise ratio would rise to the threshold value and stay there (or rise only slightly) as the signal level is increased. The delay blocks represent voltage delay circuits that enable the forward-placed IF and RF attenuators at signal levels which are ideally just in advance of succeeding stage overload or IM level specification limits. As the input attenuator begins to operate with rising signal strength, the output signal-to-noise ratio becomes constant with a value ranging from 30 to 50 dB in typical designs. The ultimate signal-to-noise ratio is usually limited by the synthesizer phase noise when the IF delays are properly placed.

The amount of dc gain needed in the AGC loop is dependent upon the output rise characteristics previously described. If the audio output as represented by the detected dc voltage is 1 V at threshold, and a 6-dB output rise is acceptable for input signals at some maximum level, the dc voltage will rise to 2 V and the differential output will be 1 V. An AGC amplifier gain of only 10 would suffice to cause a 10-V AGC line increase to operate the RF and IF attenuators. On the other extreme, if virtually no output rise is desired, the AGC amplifier is replaced by an operational amplifier integrator whose huge low-frequency gain makes the output as constant as the nonlinearities of the final IF stage and detector will allow. When an integrator is used, it forms part of the low-pass filter which is required to remove envelope audio from the gain control voltage. This can result in unacceptable signal attack time delays unless nonlinear circuits are used.

The dynamics of the AGC loop constitute the most difficult part of the gain control design. An AGC loop is a feedback system having gain that is dependent upon the carrier strength in the forward path. Stability analysis is further complicated by the fact that in a sideband receiver, the AGC detector time constant holds the peak value for a period of time. Thus, when the signal level decreases, the AGC system becomes open loop and the receiver gain increases at a rate determined by the detector time constant. When the signal level is constant or increasing, the AGC loop can be described and analyzed as a linear servomechanism if the signal level and the attenuation are expressed in logarithmic units. Porter [7] gives a complete analysis of the closed-loop condition, including the case where one stage of delayed gain control is added to the simple one-loop system. The general result is that the attenuators should have logarithmic slope, with attenuation increasing by 1 dB per unit of control voltage throughout the control range. High attenuation slope, such as is found near the cutoff point of dual-gate field-effect transistor amplifiers, will decrease the loop phase margin, leading to overshoot or outright oscillation at a specific signal level.

Practical design of a multi-delayed AGC system is done experimentally by setting up a stepped value signal source and observing the audio output and AGC voltage with an oscilloscope. The signal source steps can be obtained from a bus-controlled signal generator or an external attenuator driven by a low-frequency square-wave oscillator to produce steps in the 3- to 10-dB range at about a 1-Hz rate. The mean value of the signal should be moved from near zero to the maximum rated input signal level. Output overshoot, ringing, or oscillation problems are readily observed by this method.

The impulse-loading characteristic of the AGC system must be considered in the receiver block design so that overshoot in gain control is not excessive when a strong signal or noise impulse is received. A dual time constant approach has been used to solve the impulse-loading problem. The loop filter is designed to have some transmission at frequencies in the 100- to 300-Hz range, such that some gain control can be rapidly applied without causing a large amount of charge in the integrator or low-pass filter. The receiver gain will then rapidly recover after the noise burst or signal impulse has ceased so that a weak signal can be immediately recognized. This technique is a compromise, with envelope distortion caused by envelope frequency appearing on the control voltage to the attenuators.

Another problem associated with the narrow-bandwidth IF filters of the receiver is the absolute time delay incurred by the signal as it passes through the IF. When a rapidly rising signal is at the input, the AGC detector has no output until the signal propagates through the filters. The input stages then may be in overload during the delay time interval. When the signal does reach the detector, the system may overcompensate by reducing the gain more than necessary because of the energy stored in the IF filter. This effect can be practically reduced by using lead compensation on the voltage driving the attenuators ahead of the IF selectivity. The dual time constant filter mentioned above also helps reduce the effects of filter time delay.

A state variable type of AGC loop called hang AGC is very often used to obtain rapid recovery of receiver gain after signal cessation, while also having very low envelope distortion due to audio on the gain control line. The loop filter is designed to charge rapidly to follow the rising signal input and then to remain at that level after the signal drops. In effect, the receiver gain "hangs" for a preset amount of time. For voice systems the attack time should be in the 2-ms region, with a hang time of about 0.3 sec, followed by a gradual recovery time of up to 1 sec. Adaptive circuits can be designed that give shorter hang and recovery time as the signal on-time decreases, thus minimizing impulse loading of the AGC system.

Since a microprocessor is often used elsewhere in an otherwise analog receiver, it is an attractive possibility to consider a digitally closed gain control loop. The output of the AGC detector or even the detected audio can be sampled and processed for average, rms, or peak amplitude determination. After adaptive processing, the gain control is applied with D/A converters to the various attenuators in the receiver. Alternatively, step-value attenuators can be used as opposed to continuous-function attenuators. The latter generate IMD when the control current or voltage is low, which occurs near the minimum attenuation end of the range. Computed AGC can achieve infinite hang time when needed. An example of this would be to return the receiver to a set gain point after a companion transmitter completes its transmission, thereby readying the receiver for an expected signal strength.

Excerpt from "HF Radio Systems and Circuits", Sabin et al., ch. 8, Digital Signal Processing, pp.341-342.

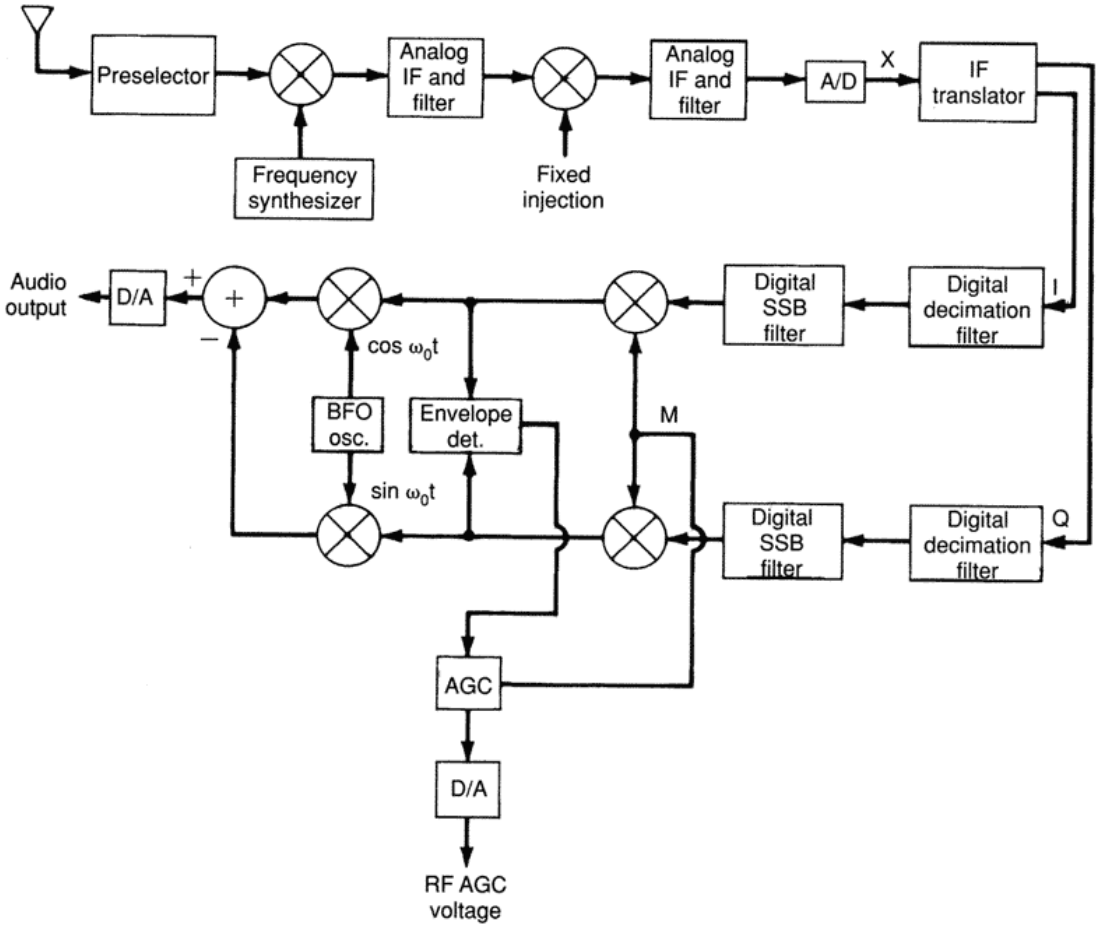

Figure 8.10 Block diagram of a digital SSB receiver.

8.6 Digital AGC Methods

Automatic gain control provides the same overall function in a digital receiver as in a purely analog receiver. However, there can be significant differences in the design approach used, because of receiver hardware differences. For instance, more gain is generally required before the digital IF filter in the digital receiver in order to drive the A/D converter at a satisfactory level. This means that appreciable AGC must be applied before the digital IF filter. In addition, because of the envelope delay associated with a high-performance digital filter, special techniques must be used to provide an AGC with adequate speed, while still controlling overshoot. A digital receiver block diagram illustrating a typical AGC processor interconnection was shown in Figure 8.10.

The AGC processor operates on the digital IF signal components to provide a desired gain control value to a D/A converter, which in turn controls the attenuators in the IF translator, and consequently the signal level at the A/D converter. It also provides a digital gain multiplier to control the signal level at the audio output D/A converter.

The desired receiver gain distribution, or analog versus digital receiver gain, is selected on the basis of a system level analysis. The maximum analog translator gain must be great enough so that the quantizing noise of the A/D converter does not degrade the receiver noise figure or sensitivity below the desired limit. As the signal level increases above the sensitivity level, the analog gain should not be decreased by AGC action until an adequate signal-to-noise ratio is obtained. As the signal level increases still further, the analog AGC should hold the signal level at the A/D converter essentially constant. In addition, adequate headroom at the A/D converter and D/A converter must be provided to avoid saturation during normally high peak-to-average voltage ratio periods of the desired signal.

Strong signals that fall outside the narrowband digital filter bandwidth, but inside the analog IF translator bandwidths, can overload or saturate the A/D converter. This results in the generation of in-band IMD products and can result in significant degradation of the desired signal. If large signal levels are detected at the A/D converter, the receiver gain may have to be re-distributed by reducing the pre-conversion analog gain and increasing the digital gain to maintain the desired signal output level. This will, however, reduce the desired signal-to-quantization noise ratio.