

Development and Use of
Embedded Capacitance

EDC

Materials in Printed Circuit Boards



Conference Goal

This Conference will provide a forum in which program results can be disseminated to a targeted group of industry representatives. Specifically, members of the project team and the NCMS program manager will offer Conference participants information and facilitated discussions on the following: project goals and objectives, test vehicle design, material test results, reliability test results, electrical test results (decoupling and EMI), and modeling of the electrical performance of embedded distributed capacitance (EDC).

A conference conducted by:

The National Center for
Manufacturing Sciences and

Embedded Decoupling
Capacitance Consortium

August 21, 2000

**NIST Campus
Gaithersburg, Maryland**

The Need

The need for power-ground decoupling capacitance is nearly universal in electronic circuits. Today, the solution to that need is found in discrete chip capacitors. These devices provide a wide range of capacitance values and many excellent properties, such as stability over temperature and frequency and reliability. However, use of discrete chip capacitors also poses some fundamental problems – problems such as the amount of surface area they consume on the circuit board. In addition, few designers or maintenance engineers understand, with any rigor, how many decoupling capacitors are truly required, how much capacitance they should have, and where to locate them on the circuit.

In response to these inherent problems, and supported by the findings of recent industry roadmaps, OEMs are now viewing embedded passives technology as a promising alternative to discrete passives in electronics manufacturing. Embedding the capacitance in the circuit board frees up space that can be used for other functions. The technology may also improve performance for high frequency decoupling and reliability by reducing the number of solder joints and discrete capacitors, and the associated failure modes. In addition, total system cost may also be lowered as a result of parts reduction and circuit integration. However, development efforts by one company – or even a small group of companies – would not have high probability of success. The case for a group effort was justified: the investigation of multiple materials, with multiple fabricators, produces multiple chances for success, with the efforts of each participant being highly leveraged.

The Project

Recognizing the value of a collective solution, NCMS, together with more than a dozen partners, organized a collaborative effort aimed at advancing the use of embedded capacitance technology for power supply decoupling. The goal of the project was to encourage the development and use of embedded capacitive materials in printed circuit boards. The project team focused on the embedding of a single large (distributed) capacitance within the circuit board. The team anticipates that this capacitance will be utilized for power supply decoupling. Commercially available materials and developmental materials were evaluated for compatibility with the circuit board manufacturing process, for materials properties, for reliability, and for their ability to perform the decoupling function. The project has thus taken some of the first steps towards the realization of embedded passives in organic substrates.

Featured Speakers

Todd Hubing is a Professor of Electrical Engineering at the University of Missouri-Rolla and one of the principal faculty in the UMR Electromagnetic Compatibility Laboratory. He holds a B.S.E.E. degree from the Massachusetts Institute of Technology, an M.S.E.E. degree from Purdue University, and a Ph.D. in Electrical Engineering from North Carolina State University. Prior to joining the faculty at the University of Missouri-Rolla in 1989, Todd was an EMC engineer at IBM in Research Triangle Park, North Carolina. Since joining the university, the focus of his research has been measuring and modeling sources of electromagnetic interference. He also teaches EMC, Antenna and High-Speed Digital Design courses at UMR.

Joseph P. Dougherty is an Associate Professor of Electrical Engineering and Materials at Pennsylvania State University, State College, PA. He received a B.E.E. from Villanova University and received an M.S.E.E. and Ph.D. in EE from Penn State University. From 1973-79 he was a research scientist at Philips Laboratories in Briarcliff Manor, New York including 1 ½ years at Philips' Central Research Labs in the Netherlands. He then joined Gulton Industries as Director of Engineering for the Piezoelectric Division and later for Electronic Products in the Electro-Voice Division. He formed Advanced Materials Technologies, a consulting firm specializing in electronic ceramics. He holds 6 patents and has co-authored more than 50 papers and parts of 5 books. Dougherty is a Fellow of the American Ceramic Society and the Chair of the AcerS Electronics Division. Dougherty is Co-Chair of the National Electronics Manufacturing Initiative (NEMI) Technical Working Group on Passive Components. He is a member of IMAPS and IEEE, the UFFC Society, the UFFC Committee on Ferroelectrics and the CHMT Society. Dougherty is a co-author of the IEEE Standard on Ferroelectric Definitions.

Jan Obrzut received a Ph.D. degree in Technical Sciences from the Cracow Polytechnic, Poland. He worked as a Postdoctoral Fellow at the Polymer Science Department, University of Massachusetts for three years on theoretical and experimental aspects of electrooptic polymers and dielectric waveguides. He then spent ten years with IBM doing research and development in the area of chip-scale packaging for microwave and high-speed electronics. He joined the NIST Polymers Division in 1997, where he pursues research in metrology of dielectric films and composites for electronic applications. He authored numerous publications on electromagnetic and electrooptic properties of polymers.

The Embedded Decoupling Capacitance Consortium Members

StorageTek

Delphi Automotive Systems

Raytheon Systems Company

3M

DuPont /Technologies

Conference Date:

August 21, 2000

Conference Fee:

\$300.00 before August 7, 2000

\$350.00 after August 7, 2000

Project report available to conference participants for \$75.00 – an 80% savings.

EDC Phase II Project

NCMS is inviting participants for an EDC second phase “live product” collaborative project.

Candidate participants would include:

- OEMs with design and test resources as well as a candidate product.
- PWB fabricators willing to fabricate boards using the technology
- Government manufacturing or maintenance organizations or facilities responsible for electronic components manufacturing, maintenance or repair.

Suggested scope of Phase II includes:

- Build additional “live products” to further demonstrate the technologies
- Determine capability ratios of the board fabrication processes
- Determine embedded capacitance materials defect density levels
- Complete transfer and promote use of the technologies within the industry
- Further develop design rules and modeling tools to enable wide-spread use
- Develop cost models to analyze tradeoffs between the various technologies
- Develop strategies and methods for bare board and system level test

Polyclad

Litton Interconnect Technologies

HADCO

Merix

University of Missouri-Rolla

Conference Location:

NIST Campus, Gaithersburg, Maryland

NIST Administration Bldg. 101, Lecture Room B

Lunch will be provided in the NIST cafeteria. Business casual attire is appropriate. Hotel reservations to be made by individual. Contact the Holiday Inn Gaithersburg located at 2 Montgomery Village Avenue, Gaithersburg, Maryland at 301-948-8900 and request the “NCMS/National Center for Manufacturing Sciences” negotiated room rate of \$90.00 per night. The room block expires **August 7, 2000**.

Registration Form

Embedded Decoupling Capacitance Conference

Fax back to Shirley Phillips at 734-995-1150 no later than Monday, August 7, 2000. If the Conference is canceled for any reason, the liability of NCMS is limited to refund of the registration fee.

Name _____

Title _____

Company _____

Address _____

Telephone _____

Fax _____

E-mail _____

Method of payment:

CHECK (made payable to NCMS)

VISA MC AMEX

Account Number _____

Expiration date _____

Signature _____

For further technical information contact Lee Patch at 734-995-4972 or email at leep@ncms.org. For additional logistical information, contact Shirley Phillips at 734-995-7986 or email at shirleyp@ncms.org.

Penn State University

National Institute of Standards and Technology

National Center for Manufacturing Sciences

Tobyhanna Army Depot

Conference Agenda

- 8:30 Registration & Coffee
8:45 **Welcome & Introductions**
Dr. Eric Amis, Chief of the NIST Polymers Division
9:15 **Decoupling Theory and Applications**
Todd Hubing
10:00 **EDC Project Overview**
Rick Charbonneau
10:30 Break
10:45 **Materials Properties**
Joseph Dougherty
11:30 **Board Fabrication**
John Davignon
12:00 Lunch
12:45 **Reliability Results**
Weiping Li
1:30 **PWB Impedance Measurements**
Todd Hubing
2:00 **Power Bus Noise Measurements**
Todd Hubing
2:30 Break
2:45 **NIST Dielectric Test Results**
Jan Obrzut
3:15 **Radiated Emissions**
Todd Hubing
3:45 **Discussions**
Rick Charbonneau
4:15 **Summary/Conclusions**
Rick Charbonneau
5:00 Adjourn



National Center for Manufacturing Sciences
3025 Boardwalk
Ann Arbor, MI 48108-3266

734-995-0300
<http://www.ncms.org>

Why attend

- Learn when, where, how to use these new EDC materials
- Learn from PWB fabricators technical know-how and lessons learned
- Learn recommended design guidelines
- Receive Conference proceedings
- Receive project final report at 80% savings



Who should attend

Individuals responsible for:

- Electronic Products Designs
- PWB Design
- PWB Fabrication

High-Speed Digital Designers should **NOT** miss this Conference.

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