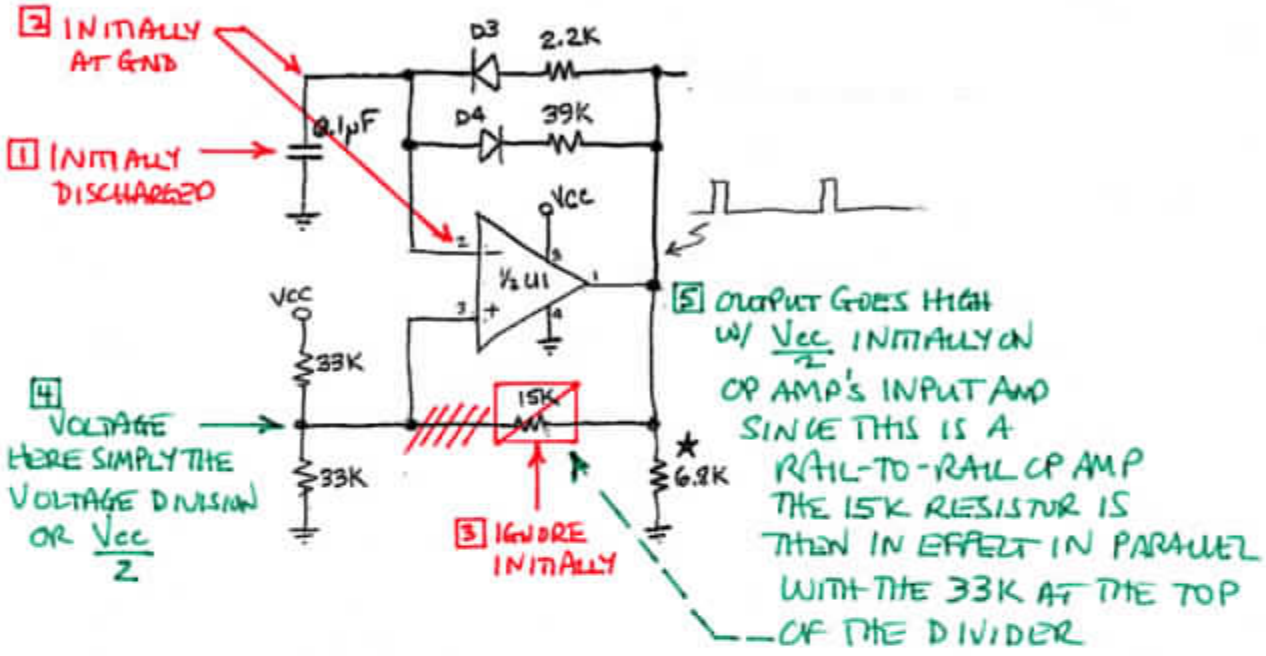
SOME NOTES FOR W2AEW'S VIDEO #231: CIRCUIT FUN: STAIRSTEP GENERATOR USING 555 AND OP AMPS

(KLOS)

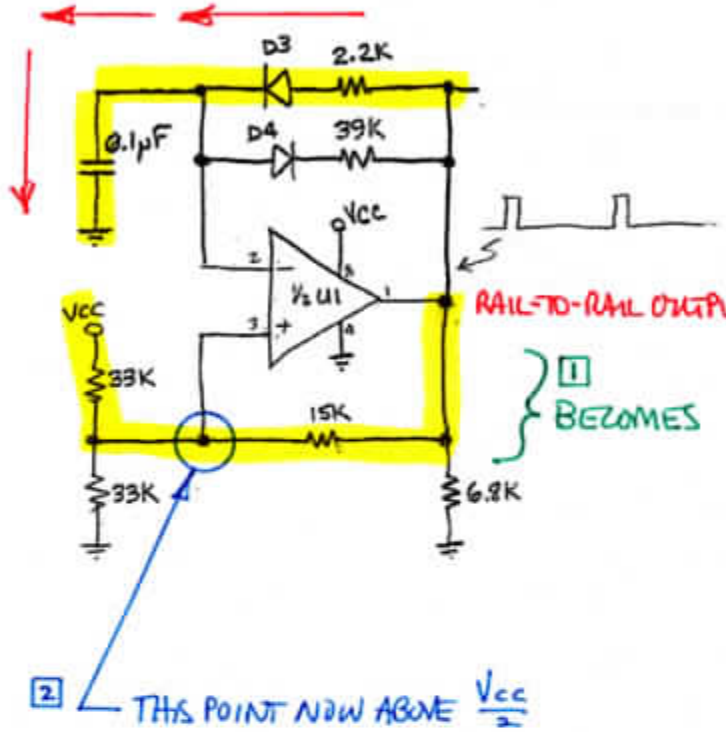
(A)

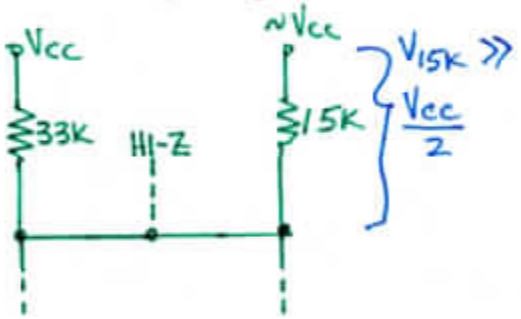


★ NOTE: THIS 6.8K RESISTOR IS NOT NEEDED IF THE OP AMP USED IS A GOOD RAIL-TO-RAIL DEVICE. SOME OP AMPS MAY NEED A PULL-DOWN RESISTOR AT THE OUTPUT TO FUNCTION CORRECTLY.

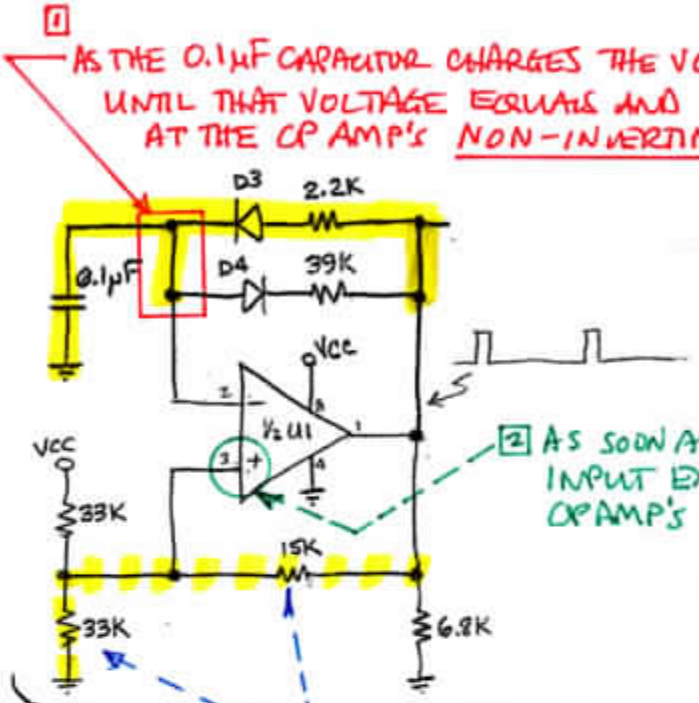
(B)

[2] WITH OUTPUT INITIALLY HIGH CURRENT FLOWS VIA D_3 AND BEGINS TO CHARGE THE 0.1μF CAPACITOR



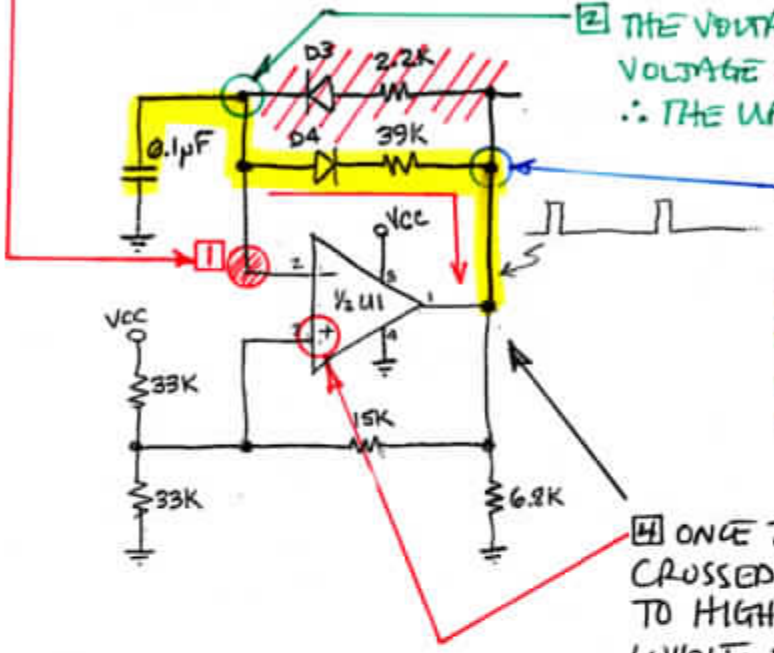


(c)


1
AS THE 0.1μF CAPACITOR CHARGES THE VOLTAGE AT THIS POINT RISES UNTIL THAT VOLTAGE EQUALS AND THEN EXCEEDS THE VOLTAGE AT THE OP AMP'S NON-INVERTING (+) INPUT
D3
2.2K
0.1μF
D4
39K
Vcc
½ U1
2
AS SOON AS THE VOLTAGE AT THE INVERTING INPUT EXCEEDS THE VOLTAGE HERE THE OP AMP'S OUTPUT GOES LOW
Vcc
33K
15K
33K
6.8K
3
ONCE THE OUTPUT GOES LOW THE 15K RESISTOR WILL BE IN PARALLEL W/ THE LOWER 33K RESISTOR AND THE VOLTAGE AT THE NON-INVERTING INPUT THEN DROPS BELOW Vcc/2
Vcc
33K
33K
15K
VOLTAGE DROPS SINCE
15K||33K
<< 33K
AS A VOLTAGE DIVIDER

(D)

ONCE THE VOLTAGE AT THE INVERTING INPUT (-) BECOMES MUCH HIGHER THAN THAT AT THE NON-INVERTING INPUT (+) [SINCE 15K IS IN EFFECT || TO THE LOWER 33K RESISTOR]

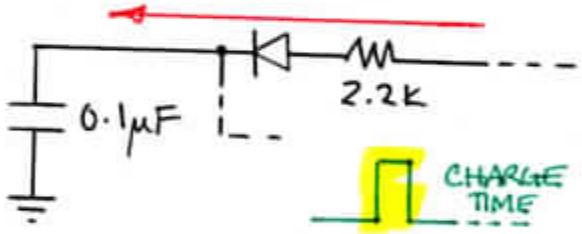


[2] THE VOLTAGE HERE IS NOW ABOVE THE VOLTAGE AT THE OP AMP'S OUTPUT PIN ∴ THE UPPER DIODE IS TURNED OFF

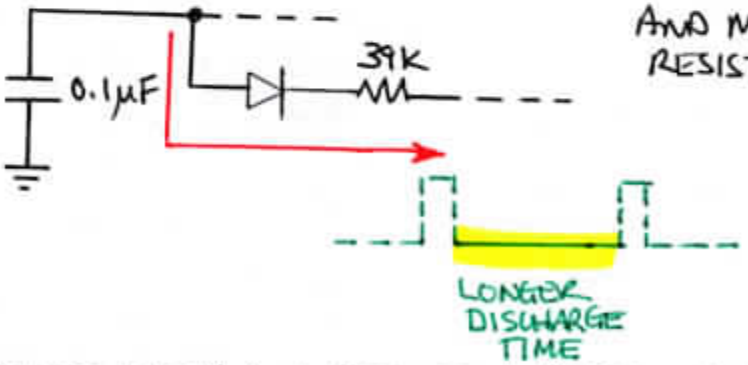
[3] THE DIODE D4 IS NOW BIASED ON AND PROVIDES A DISCHARGE PATH FOR THE 0.1μF CAPACITOR. THIS CONTINUES UNTIL THE VOLTAGE AT THE INVERTING (-) INPUT DROPS BELOW THE "LOWER" THRESHOLD VOLTAGE AT THE NON-INVERTING INPUT.

[4] ONCE THAT VOLTAGE THRESHOLD IS CROSSED THE OP AMP'S OUTPUT RETURNS TO HIGH (POSITIVE RAIL) AND THE WHOLE PROCESS BEGINS AGAIN.

- THE TWO "STEERING DIODES" ARE USED TO CONTROL HOW QUICKLY THE 0.1μF CAPACITOR IS CHARGED AND THEN DISCHARGED



HERE THE CAPACITOR CHARGES MORE QUICKLY SINCE WE'RE GOING THRU A RELATIVELY SMALL 2.2K RESISTOR



AND MORE SLOWLY THRU THE 39K RESISTOR

[39K >> 2.2K]

- PULSE WIDTH AND REPETITION RATE CAN BE CHANGED BY ADJUSTING THE VALUES OF THE 2.2K AND 39K RESISTORS.
- TO CHANGE AND MAINTAIN THE RATIO SIMPLY CHANGE THE CAPACITOR.

(E)

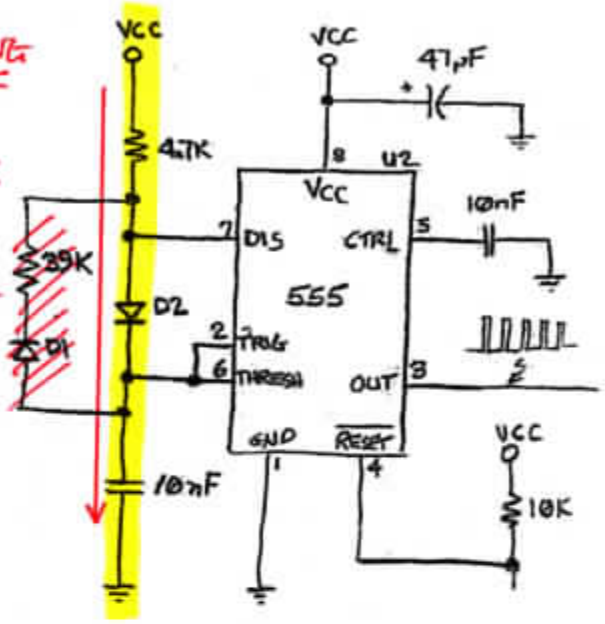
▲ THE "STEPS" OF THE CIRCUIT ARE CREATED USING A 555 TIMER (COULD HAVE USED THE SAME OP AMP RELAXATION OSCILLATOR)

▲ LOW DUTY-CYCLE PULSE TRAIN

1 INITIAL CHARGING PATH FOR THE 10nF CAPACITOR

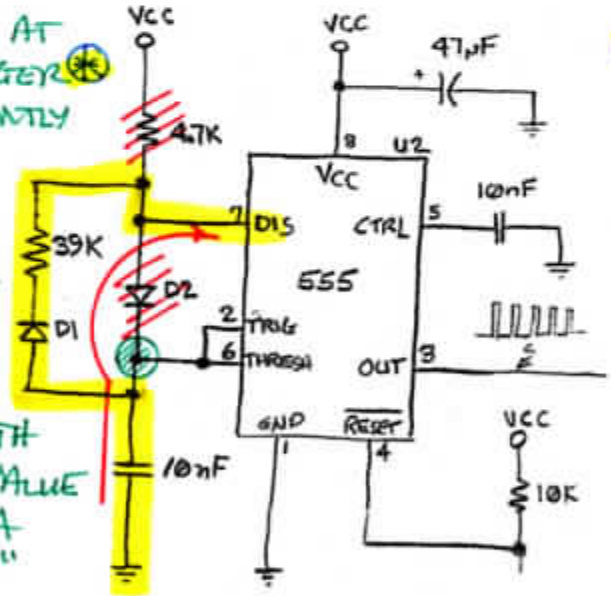
▲ THE CHARGE PATH IS THRU THE SMALLER 4.7K RESISTOR

∴ A SHORTER CHARGE TIME (PULSE) AND IS ESSENTIALLY THE "ON TIME" OF THE OUTPUT.



2 ONCE THE VOLTAGE AT THE THRESHOLD – TRIGGER PINS RISES SUFFICIENTLY THE TIMER RESETS AND THE VOLTAGE ON THE 10nF CAP BLEEDS OFF VIA THE TIMER'S DISCHARGE PIN.

▲ THE DISCHARGE PATH THRU THE HIGHER VALUE RESISTOR CREATES A LONGER "OFF TIME"

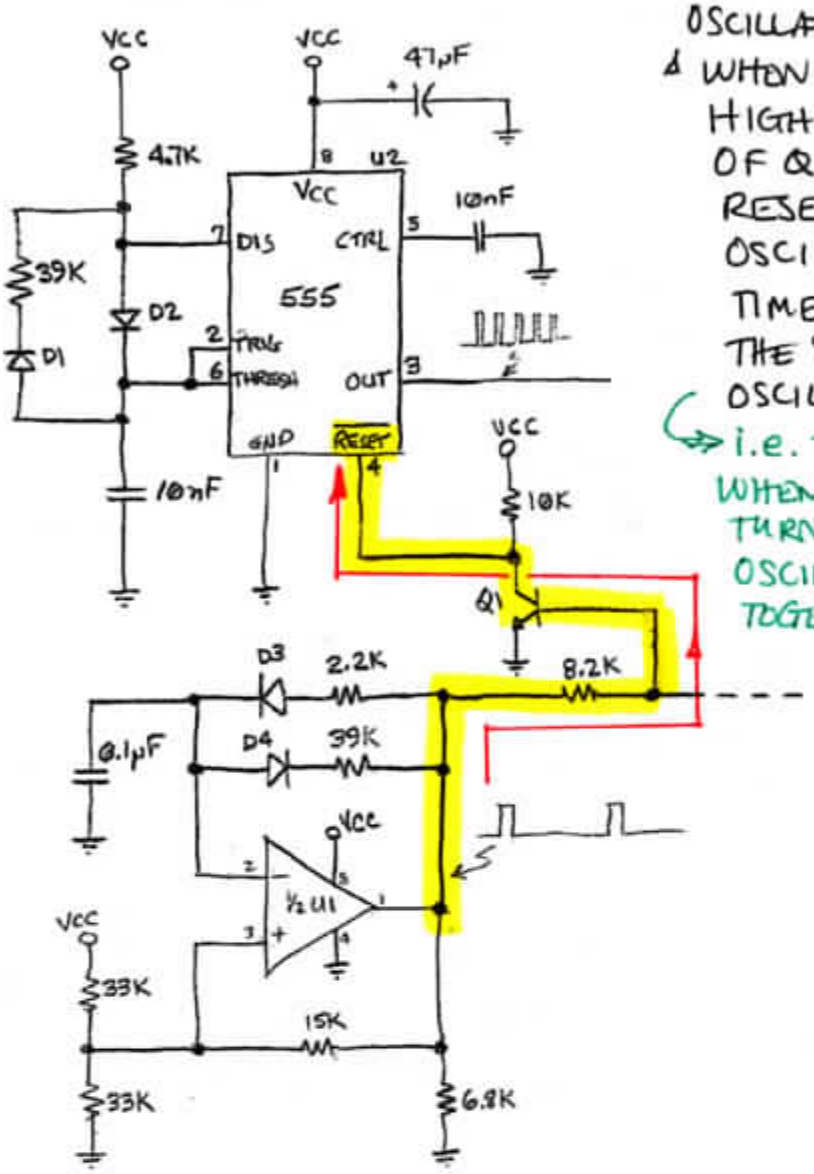


✱ THE "THRESHOLD" IS 2/3 OF Vcc AT WHICH POINT THE DISCHARGE IS TURNED ON – WHEN THE VOLTAGE FALLS TO 1/3 OF Vcc THE DISCHARGE FUNCTION DISENGAGES AND THE CHARGING CYCLE BEGINS AGAIN.

▲ ADJUSTING THESE VALUES CHANGES THE PULSE WIDTH AND REPETITION RATE.

✱ THE VALUE OF USING A 555 IS THAT IT CAN BE STARTED AT A PARTICULAR TIME AND THUS BE SYNCHRONIZED WITH THE OTHER RELAXATION OSCILLATOR

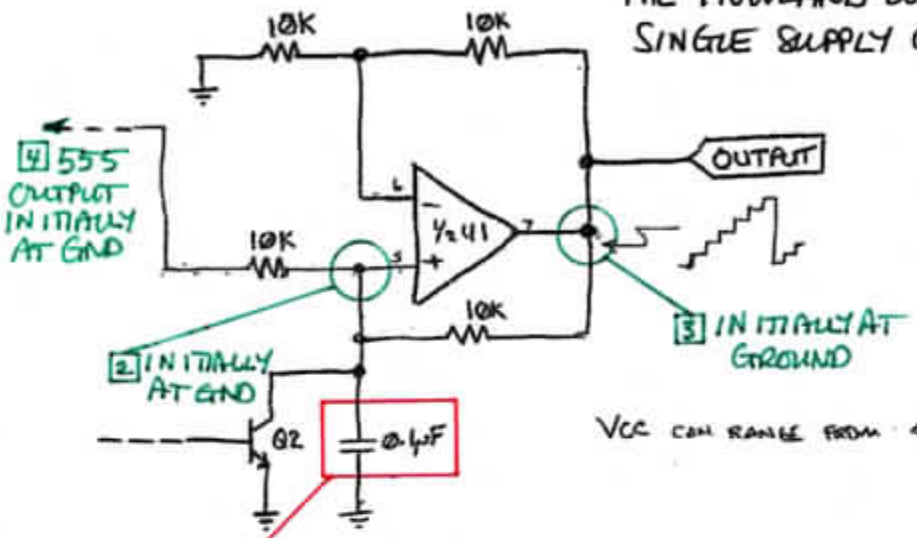
(F)



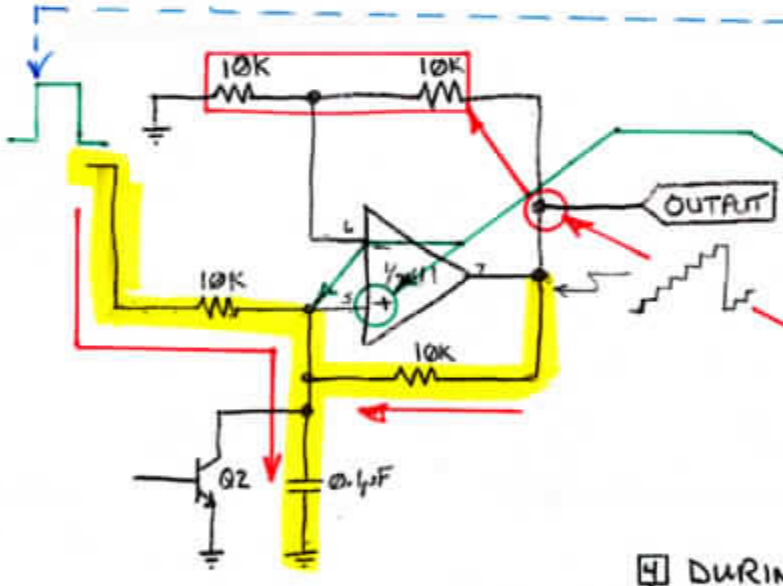
- TRANSISTOR Q1 IS BEING DRIVEN BY THE OP AMP RELAXATION OSCILLATOR'S OUTPUT
- WHEN THE OP AMP'S OUTPUT GOES HIGH IT PULLS DOWN THE COLLECTOR OF Q1 THUS GROUNDING THE 555 RESET PIN AND BEGINNING ITS OSCILLATOR ACTION; THE 555 TIMER STARTS ESSENTIALLY WITH THE SAME PERIOD AS THE OP AMP OSCILLATOR ACTION.
  - ↳ i.e. THE FIRST "STEP" BEGINS WHEN THE OP AMP OSCILLATOR TURNS ON; THAT'S HOW THE TWO OSCILLATORS ARE SYNCHRONIZED TOGETHER.

(?) SO HOW DO THE TWO OSCILLATORS COMBINE TO CREATE THE STAIRSTEP SIGNAL?

(G) A THIS PART OF THE CIRCUIT IS CONFIGURED AS A PULSE INTEGRATOR OR ACCUMULATOR [SEE THE "DEBOO INTEGRATOR" WHICH IS BASED ON THE HOWLAND CURRENT SOURCE — GOOD FOR A SINGLE SUPPLY CIRCUIT SINCE IT'S NON-INVERTING]



VCC CAN RANGE FROM <5V TO >12V



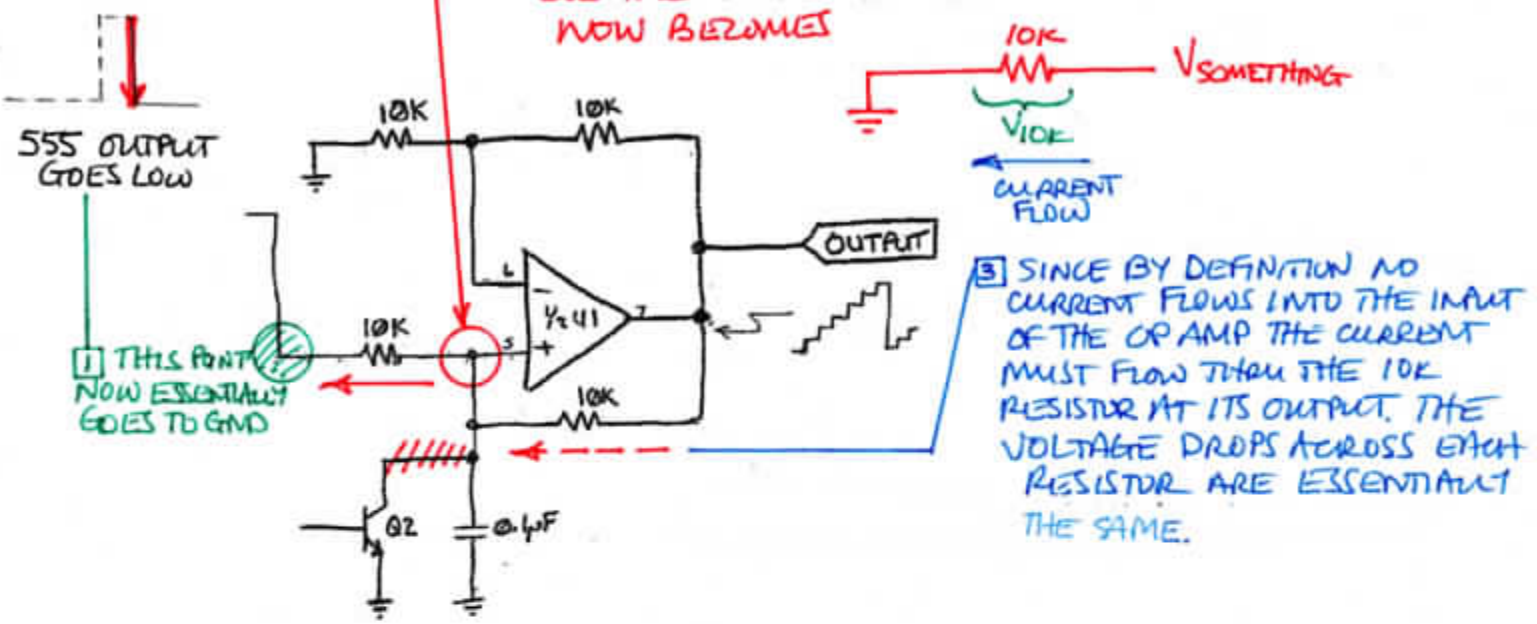
1 AS SOON AS THE 555 OUTPUT GOES HIGH THE 0.1μF CAPACITOR BEGINS TO CHARGE VIA THIS PATH.

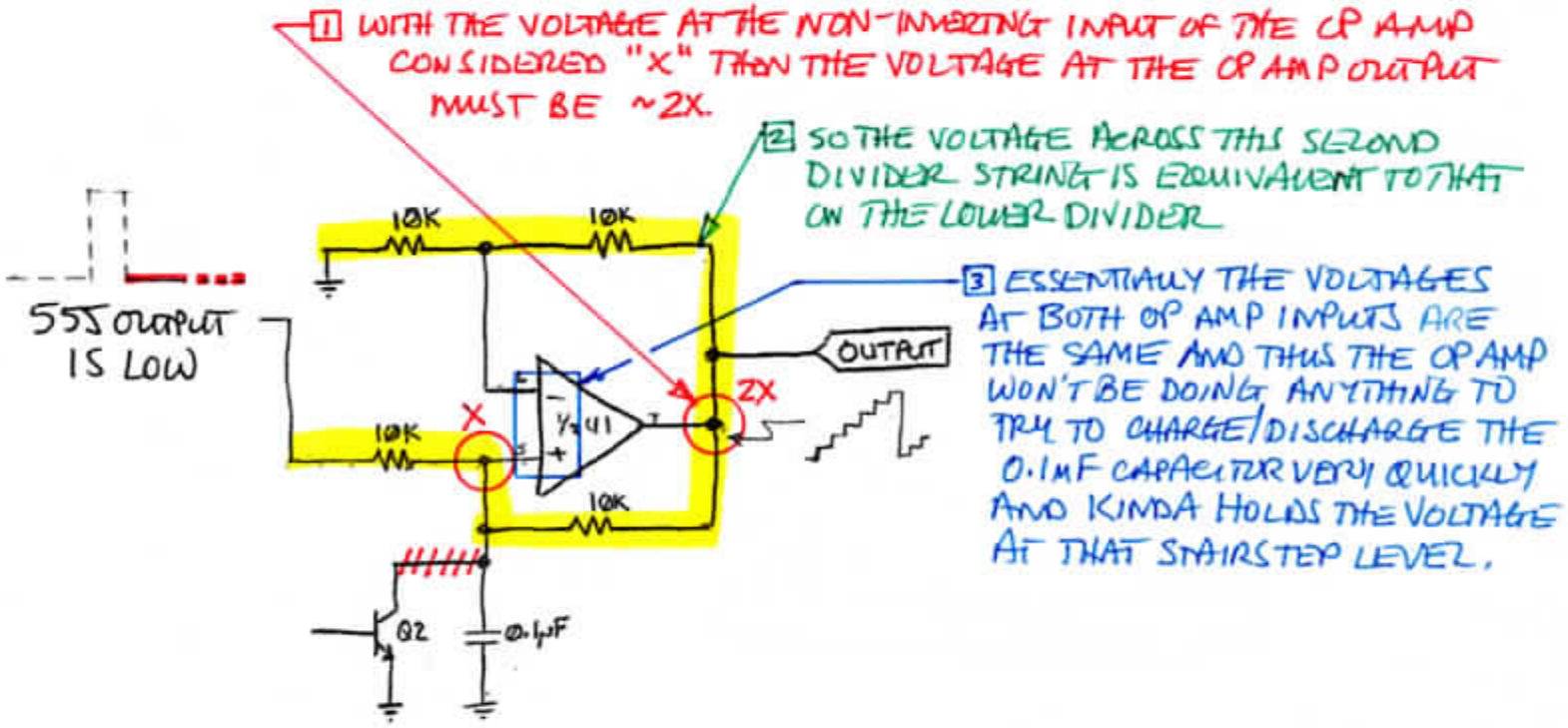
2 AS THIS POINT GETS HIGHER IN VOLTAGE THE OP AMP OUTPUT GOES HIGH AND THAT VOLTAGE ALSO ADDS TO THE CHARGING ACTION OF THE CAPACITOR.

3 NOTE THAT THE VOLTAGE HERE DOES NOT "SLAM" TO THE RAIL BECAUSE OF THE NEGATIVE FEEDBACK ACTION OF THE TWO UPPER 10K RESISTORS.

4 DURING THE SHORT PULSE OUTPUT OF THE 555 TIMER WE CHARGE UP THE LEADING EDGE OF THE STAIRSTEP.

(H)

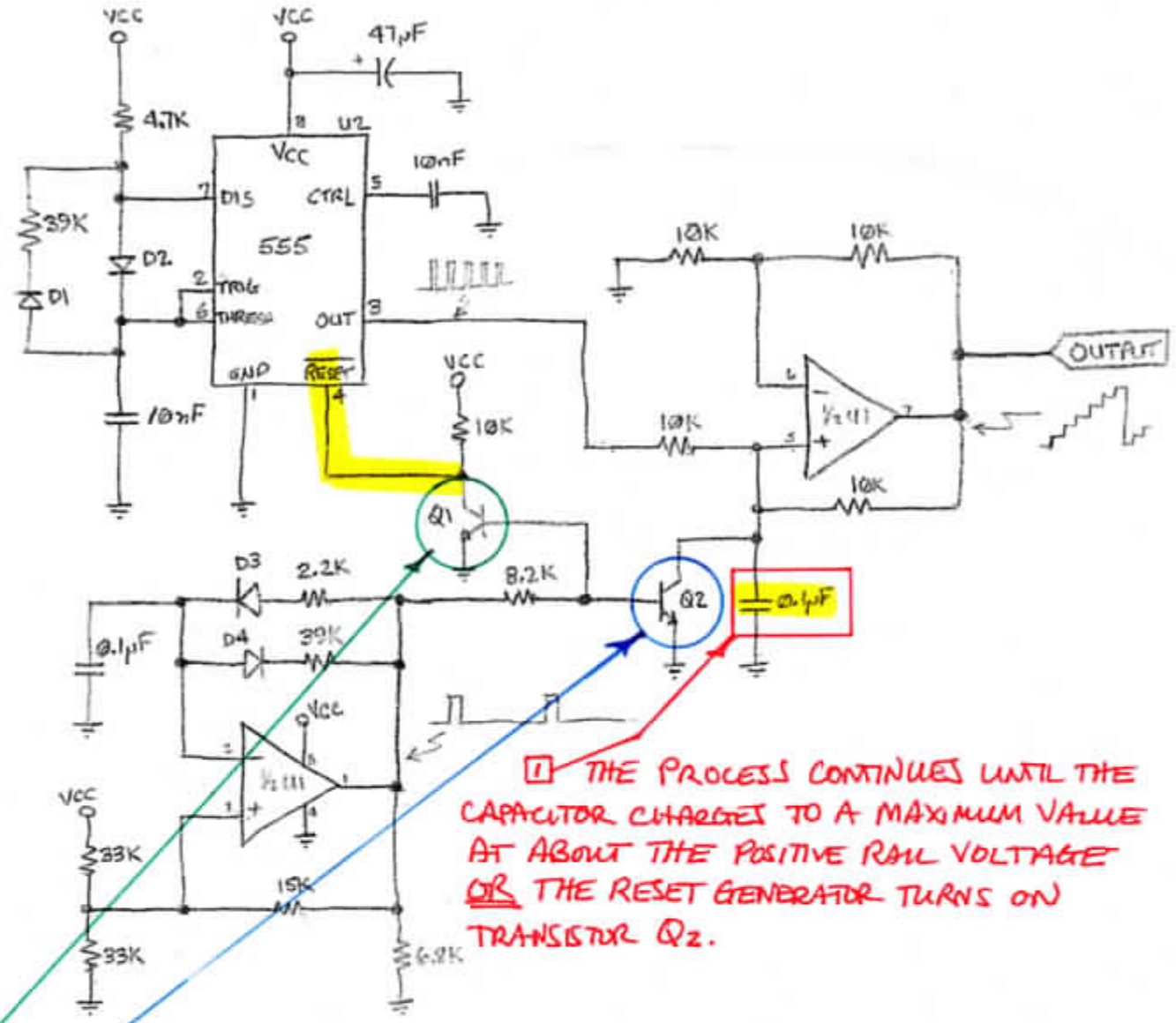




5 SO WHEN THE 555 TIMER OUTPUT IS LOW THE OP-AMP OUTPUT REMAINS STATIC. THERE WILL BE SOME MINOR DROP OFF DUE TO LEAKAGE BUT NOT A SIGNIFICANT AMOUNT.

6 WHEN THE 555 OUTPUT GOES HIGH AGAIN THE CAPACITOR BEGINS TO CHARGE AGAIN THEREBY ADDING TO THE VOLTAGE ALREADY PRESENT AND CREATES THE NEXT STAIRSTEP; WHEN THE 555 OUTPUT GOES LOW AGAIN THE CIRCUIT AGAIN HOLDS THIS HIGHER VOLTAGE.

(I)



[1] THE PROCESS CONTINUES UNTIL THE CAPACITOR CHARGES TO A MAXIMUM VALUE AT ABOUT THE POSITIVE RAIL VOLTAGE OR THE RESET GENERATOR TURNS ON TRANSISTOR Q2.

[2] ONCE Q2 IS TURNED ON IT EFFECTIVELY SHORTS THE 0.1μF CAPACITOR TO GROUND AND REMOVING THE CHARGING VOLTAGE.

[3] AT THE SAME TIME Q2 IS TURNED ON SO IS Q1 WHICH BRINGS THE RESET PIN OF THE 555 TO GND AND INITIATING A TIMER RESET.

▲ THE WHOLE PROCESS THEN BEGINS AGAIN.

- SO THIS CURCUIT PROVIDES STAIRSTEPS FROM NARROW PULSES, RESET BY ANOTHER PULSE → CREATES AN ANALOG STAIRSTEP GENERATOR WITH NO MEMORY OR DIGITAL A/D CONVERTER.