HI1172
6-Bit, 20 MSPS, Video A/D Converter (CMOS)

Features

- Resolution .......................... 6-Bit
- Maximum Sampling Frequency ........ 20 MSPS
- Low Power Consumption at 20 MSPS (Typ)
  (Reference Current Excluded) .............. 40mW
- Built-In Sample and Hold Circuit
- Three-State TTL Compatible Output
- Power Supply ........................ 5V Single
- Low Input Capacitance ....................... 4pF
- Reference Impedance ....................... 250Ω (Typ)

Applications

- Video Digitizing
- Wireless Communications

Description

HI1172 is a 6-bit, CMOS A/D converter for video use. The adoption of a 2-step parallel conversion achieves speeds of 20 MSPS minimum, 35 MSPS typical.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI1172JCP</td>
<td>-20 to 75</td>
<td>16 Ld PDIP</td>
<td>E16.3A-S</td>
</tr>
<tr>
<td>HI1172JCB</td>
<td>-20 to 75</td>
<td>16 Ld SOIC</td>
<td>M16.2-S</td>
</tr>
</tbody>
</table>

Pinout

HI1172 (PDIP, SOIC)
TOP VIEW

D0  D1  D2  D3  D4  D5  CLK  DVSS  AVDD  DVDD  AVSS  VRT  VRB  VDD  DVDD

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Block Diagram

Typical Application Circuit
### Pin Descriptions

<table>
<thead>
<tr>
<th>NUMBER</th>
<th>SYMBOL</th>
<th>EQUIVALENT CIRCUIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 to 6</td>
<td>D0 to D5</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>D0 (LSB) to D5 (MSB) Output.</td>
</tr>
<tr>
<td>7</td>
<td>CLK</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Clock Input.</td>
</tr>
<tr>
<td>8</td>
<td>DV_SS</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Digital GND.</td>
</tr>
<tr>
<td>9, 15</td>
<td>DV_DD</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Digital +5V.</td>
</tr>
<tr>
<td>10, 14</td>
<td>AV_DD</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Analog +5V.</td>
</tr>
<tr>
<td>11</td>
<td>V_RT</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Reference Voltage (Top).</td>
</tr>
<tr>
<td>13</td>
<td>V_RB</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Reference Voltage (Bottom).</td>
</tr>
<tr>
<td>12</td>
<td>V_IN</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Analog Input.</td>
</tr>
<tr>
<td>16</td>
<td>AV_SS</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
<td>Analog GND.</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings**  \( T_A = 25^\circ C \)
- Supply Voltage (\( V_{DD} \)) .......................... 7V
- Reference Voltage (\( V_{RT}, V_{RB} \)) .................. \( V_{DD} \) to \( V_{SS} \)
- Analog Input Voltage (\( V_{IN} \)) .................. \( 0.9 \)V to 5V
- Digital Input Voltage (\( V_{IH}, V_{IL} \)) ......... \( V_{DD} \) to \( V_{SS} \)
- Digital Output Voltage (\( V_{OH}, V_{OL} \)) .......... \( V_{DD} \) to \( V_{SS} \)

**Operating Conditions**
- Supply Voltage Range, \( AV_{DD}, AV_{SS} \) ........................ 4.75V to 5.25V
- Reference Voltage, \( DV_{DD}, DV_{SS} \)
  - \( V_{RT} \) .......................... 0.9V to 5V
  - \( V_{RB} \) .......................... 0V to 4.1V
  - \( V_{RT} - V_{RB} \) .................. 0.9V to \( AV_{DD} \)
- Analog Input Voltage (\( V_{IN} \)) .................. \( V_{RB} \) to \( V_{RT} \)
- Clock Pulse Width
  - \( t_{PW1} \) .......................... 25ns (Min)
  - \( t_{PW0} \) .......................... 25ns (Min)
- Temperature Range .......................... -20°C to 75°C

**CAUTION:** Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**
1. \( \theta_{JA} \) is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  \( V_{DD} = +5V, V_{RB} = 1V, V_{RT} = 2V, T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Speed, ( f_C )</td>
<td>( f_C )</td>
<td>( V_{IN} = 1V ) to 2V</td>
<td>0.5</td>
<td>-</td>
<td>20</td>
<td>MSPS</td>
</tr>
<tr>
<td>Integral Non-Linearity</td>
<td>( E_L )</td>
<td>( f_C = 20 ) MSPS, ( V_{IN} = 1V ) to 2V</td>
<td>-</td>
<td>( \pm 0.3 )</td>
<td>( \pm 0.5 )</td>
<td>LSB</td>
</tr>
<tr>
<td>Differential Non-Linearity</td>
<td>( E_D )</td>
<td>( f_C = 20 ) MSPS, ( V_{IN} = 1V ) to 2V</td>
<td>-</td>
<td>( \pm 0.3 )</td>
<td>( \pm 0.5 )</td>
<td>LSB</td>
</tr>
<tr>
<td>Supply Current</td>
<td>( I_{DD} )</td>
<td>( f_C = 20 ) MSPS, NTSC Ramp Wave Input</td>
<td>-</td>
<td>7</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td>Reference Pin Current</td>
<td>( I_{REF} )</td>
<td>( V_{IN} = 1.5V + 0.07V_{RMS} )</td>
<td>( 3 )</td>
<td>( 4 )</td>
<td>5.7</td>
<td>mA</td>
</tr>
<tr>
<td>Analog Input (-1dB)</td>
<td>( BW )</td>
<td>( V_{IN} = 1V ) to 2V</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Analog Input Capacitance</td>
<td>( C_{IN} )</td>
<td>( V_{IN} = 1.5V + 0.07V_{RMS} )</td>
<td>15</td>
<td>35</td>
<td>55</td>
<td>pF</td>
</tr>
<tr>
<td>Reference Resistance (( V_{RT} ) to ( V_{RB} ))</td>
<td>( R_{REF} )</td>
<td>( V_{IN} = 1V ) to 2V</td>
<td>175</td>
<td>-</td>
<td>325</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>( E_{OT} )</td>
<td>( V_{IN} = 1.5V + 0.07V_{RMS} )</td>
<td>0</td>
<td>-20</td>
<td>-40</td>
<td>mV</td>
</tr>
<tr>
<td>Digital Input Voltage</td>
<td>( V_{IH} )</td>
<td>( V_{DD} = ) Max</td>
<td>4.0</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>( V_{DD} = ) Min</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Digital Input Current</td>
<td>( I_{IH} )</td>
<td>( V_{DD} = ) Max</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>( V_{DD} = ) Min</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Digital Output Current</td>
<td>( I_{OH} )</td>
<td>( V_{DD} = ) Min</td>
<td>-1.1</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OL} )</td>
<td>( V_{OL} = 0.4V )</td>
<td>3.7</td>
<td>-</td>
<td>-</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output Data Delay</td>
<td>( T_{DL} )</td>
<td>With TTL 1 Gate and 10pF Load</td>
<td>-</td>
<td>18</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Differential Gain Error</td>
<td>( DG )</td>
<td>NTSC 40 IRE Mod</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>Differential Phase Error</td>
<td>( DP )</td>
<td>Ramp, ( f_C = 14.3 ) MSPS</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>deg</td>
</tr>
<tr>
<td>Aperture Jitter</td>
<td>( t_{AJ} )</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Sampling Delay</td>
<td>( t_{SD} )</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Information**
- Thermal Resistance (Typical, Note 1) .......................... \( \theta_{JA} (\circ C/W) \)
  - SOIC Package .......................... 120
  - PDIP Package .......................... 94
- Maximum Junction Temperature (Plastic Package) .......................... 150°C
- Maximum Storage Temperature Range .......................... -65°C to 150°C
- Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only) .......................... 300°C
**Test Circuits**

![Circuit Diagram]

**FIGURE 1. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY, OFFSET VOLTAGE**

- **S1**: ON IF $A < B$
- **S2**: ON IF $B > A$

**FIGURE 2. MAXIMUM OPERATIONAL SPEED, DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR**

**FIGURE 3. DIGITAL OUTPUT CURRENT TEST CIRCUIT**
Timing Diagrams

**FIGURE 4. TIMING CHART 1**

- **CLOCK**
- **ANALOG INPUT**
- **DATA OUTPUT**

- **t_PW1**
- **t_PW0**
- **t_D = 18ns**

**FIGURE 5. TIMING CHART 2**

- **ANALOG INPUT**
- **EXTERNAL CLOCK**
- **UPPER COMPARATOR BLOCK**
- **UPPER DATA**
- **LOWER REFERENCE VOLTAGE**
- **LOWER COMPARATOR BLOCK A**
- **LOWER DATA A**
- **LOWER COMPARATOR BLOCK B**
- **LOWER DATA B**
- **DIGITAL OUTPUT**

- **V_i(1)**
- **V_i(2)**
- **V_i(3)**
- **V_i(4)**

- **S (1)**
- **C (1)**
- **S (2)**
- **C (2)**
- **S (3)**
- **C (3)**
- **S (4)**
- **C (4)**
- **MD (0)**
- **MD (1)**
- **MD (2)**
- **MD (3)**
- **RV (0)**
- **RV (1)**
- **RV (2)**
- **RV (3)**
- **LD (-1)**
- **LD (1)**
- **H (0)**
- **C (0)**
- **S (2)**
- **H (2)**
- **C (2)**
- **S (4)**
- **H (4)**
- **LD (-2)**
- **LD (0)**
- **LD (2)**
- **OUT (-2)**
- **OUT (-1)**
- **OUT (0)**
- **OUT (1)**
### Digital Output

Compatibility between analog input voltage and the digital output code is indicated in the chart below.

<table>
<thead>
<tr>
<th>INPUT SIGNAL VOLTAGE</th>
<th>DIGITAL OUTPUT CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>STEP</td>
</tr>
<tr>
<td>$V_{RT}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{RB}$</td>
<td>31</td>
</tr>
<tr>
<td>$V_{RB}$</td>
<td>32</td>
</tr>
<tr>
<td>$V_{RB}$</td>
<td>63</td>
</tr>
</tbody>
</table>

### Operation

(See Block Diagram and Waveform)

The HI1172 is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between $V_{RT}-V_{RB}/8$ is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols, i.e., input sampling (auto zero) mode, input hold mode and comparison mode.

The operation of respective parts is as indicated in the chart. Input voltage $V_i$ (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

The upper comparators block finalizes comparison data $MD$ (1) with the rising edge of the first clock. Simultaneously, the reference supply generates the lower reference voltage $RV$ (1) that corresponded to the upper results. The lower comparator block finalizes comparison data $LD$ (1) with the rising edge of the second clock. $MD$ (1) and $LD$ (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

### Notes On Operation

- $V_{DD}$, $V_{SS}$ - To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog $V_{DD}$ pins, use a ceramic capacitor of about 0.1 μF set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input - Compared with a flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to drive with an amplifier featuring sufficient bandwidth and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.
- Clock Input - The clock line wiring should be as short as possible. Also, to avoid any interference with other signals, separate it from the other circuits.
- Reference Input - Voltage between $V_{RT}$ to $V_{RB}$ is compatible with the dynamic range of the analog input. By bypassing $V_{RT}$ and $V_{RB}$ pins to GND with a capacitor of about 0.1 μF, stable characteristics are obtained.
- Timing - Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.
- About Latch Up - It is necessary that $AV_{DD}$ and $DV_{DD}$ pins to be the common source of power supply. This is to avoid latch up due to the voltage difference between $AV_{DD}$ and $DV_{DD}$ pins when power is ON.

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