Telephone Repair
252-1578 ext. 300
serial # 3700087

1900A
Multifunction Counter

Instruction Manual

P/N 384875
January 1976
Rev. 1 2/77

FLUKE ®

WARRANTY

Notwithstanding any provision of any agreement the following warranty is exclusive:

The JOHN FLUKE MFG. CO., INC., warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries (rechargeable type batteries are warranted for 90-days), or any product or parts which have been subject to misuse, neglect, accident, or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within 1 year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. JOHN FLUKE MFG. CO., INC., SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify the JOHN FLUKE MFG. CO., INC., or nearest Service facility, giving full details of the difficulty, and include the model number, type number, and serial number. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of JOHN FLUKE MFG. CO., INC., instruments should be made via United Parcel Service or "Best Way"* prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The JOHN FLUKE MFG. CO., INC, will be happy to answer all applications or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX C9090, EVERETT, WASHINGTON 98206, ATTN: Sales Dept. For European Customers: Fluke (Holland) B.V., P.O. Box 5053, 5004 EB, Tilburg, The Netherlands.

*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

Rev. 6/81

Table of Contents

(continued on page ii)

TABLE OF CONTENTS, *continued*

List of Illustrations

(continued on page iv)

LIST OF ILLUSTRATIONS, *continued*

List of Tables

Section 1

Introduction & Specifications

1-1. INTRODUCTION

1-2. The Fluke Model 1900A is a 5 Hz to 80 MHz multiple-function counter capable of making frequency, period, period averaging and totalize measurements. In the frequency mode, resolution is manually selectable at 0.1 Hz, 1.0 Hz, 10 Hz and 100 Hz. In the period averaging mode, the number of periods averaged is manually-selectable at 10^0, 10^1, 10^2 and 10^3 periods. Automatic selection of resolution and number of periods averaged (autoranging) is also provided to automatically select the optimum range for a particular input signal. However, the 100 Hz resolution and 10^3 periods must be manually selected.

1-3. The measurement display is six digits, light-emitting-diode-type (LED) with leading-zero suppression and automatic decimal point positioning. Annunciators are provided to indicate measurement units (kHz, MHz, milliseconds and microseconds) and also overflow when the capacity of the display is exceeded. All displayed information is also available, in parallel BCD format, at a rear-panel connector when the unit is equipped with an optional Data Output Unit (DOU).

1-4. The Model 1900A is equipped with a selectable 1 MHz low-pass filter for use in electrically noisy environments, and a selectable 10:1 attenuator for use with high-level inputs. A self-check mode of operation is provided to verify overall performance of the unit. Power requirements are 100, 115 or 230 volts at 50 to 400 Hz for the line-powered version. An optional battery-powered version, Model 1900A–01, provides for use away from ac power lines and is equipped with rechargeable nickel-cadmium batteries. The battery-powered version also operates from the ac lines, but only at the power line frequency and voltage specified on the bottom of the instrument.

1-5. SPECIFICATIONS

1-6. The pertinent specifications for the Model 1900A are listed in the following Table 1-1.

Table 1-1. MODEL 1900A SPECIFICATIONS

OPERATING RANGES

Frequency:
5 Hz to 80 MHz

Period:
5 Hz to 1 MHz single and multiple period averages

Totalize:
1 count to 999999 counts

INPUT CHARACTERISTICS

Sensitivity:
25 mV, typically 15 mV rms sine wave, 5 Hz to 80 MHz
Frequency and totalize: 200 mV P-P pulse amplitude with minimum pulse width of 20 nsec. Duty cycle > 10%.
Period: 200 mV P-P pulse amplitude with minimum pulse width of 200 nsec. Duty cycle > 10%.

Impedance:
1 MΩ shunted by less than 30 pf for signal levels < 500 mV decreasing to approx. 220K shunted by less than 40 pf for levels greater than 500 mV.

Filter:
1 MHz (3dB point) lowpass

Attenuator:
Decreases sensitivity by 10

Overload:
250V rms 5 Hz to 1 kHz decreasing to 20V at 80 MHz

RESOLUTION

Frequency:
Four manually selected gate times of:
10ms (100 Hz resolution)
100ms (10 Hz resolution)
1s (1 Hz resolution)
10s (0.1 Hz resolution)

Autorange position will automatically seek to fill all 6 digits but will not select a gate time greater than 1 second (1 Hz resolution)

Period:
Manual selection of single period through 10^3 periods averaged ratios:
10^0 single period (100 ns resolution)
10^1 periods averaged (10 ns resolution)
10^2 periods averaged (1 ns resolution)
10^3 periods averaged (100 ps resolution)

Autorange position will automatically seek to fill all 6 digits. Autoranging will not select a period average of greater than 10^2 averages.

Totalizing:

Accumulates up to 999999 counts, then activates overflow indicator.

TIME BASE CHARACTERISTICS

Frequency: 10 MHz

Stability:
Aging Rate: $< \pm 5 \times 10^{-7}$ month
Short Term: $< \pm 5 \times 10^{-8}$ over 1 second
Temperature: $< \pm 5 \times 10^{-6}$ 0°C to 50°C
$< \pm 2 \times 10^{-6}$ (typical) 20°C to 30°C

Line Variation:
$< \pm 1 \times 10^{-7}$ for ±10% variation in line voltage

GENERAL

Display:
6 digit LED, leading zero suppression
Time between successive measurements is 200 ms plus measurement time

Annunciation:
MHz, kHz, msec, µs overflow

Automatic Features:
AUTORANGE:
In both frequency and period modes, autoranging includes a unique 20% hysteresis in its switching thresholds, to eliminate redundant up range/down range commands. This allows measurements to be made on signals containing large amounts of FM and PM.
Hysteresis memory can be reset by depressing the reset button.
AUTORESET:
A new measurement sequence is started every time a front panel button is activated.

Operating Temp: 0°C to +50°C (0°C to +40°C for -01 Battery option if operated from line.

Storage Temp: –40°C to +60°C

Power Requirements:
115/230 VAC ±10% - 100 VAC available - 50, 60, 400 Hz - 6.5 watts line model - 8.5 watts battery model

Fuses:
1/4A AC-line version-½ A slo-blo battery version

DIMENSIONS

Width:	8.55 inches	217.2 mm
Height:	2.52 inches	64.0 mm
Depth:	10.65 inches	270.5 mm
Weight:	2.75 lbs	1.2 Kg

DATA OUTPUT OPTION

8-4-2-1 BCD output from each digit, plus encoded decimal point and units annunciation information. All outputs CMOS/Low Power TTL compatible, high true. Print command is provided.

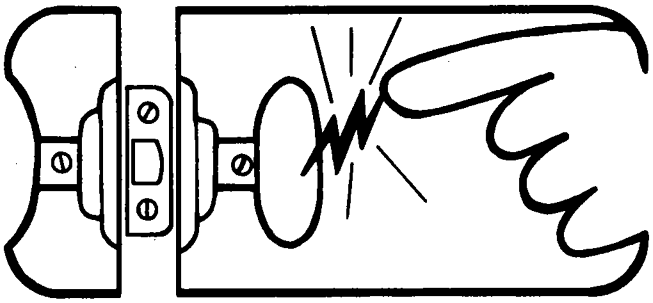
BATTERY

NICAD rechargeable - discharge time 5 hours - charge time 14 hours @ ≤ 30°C ambient with unit inoperative.

static awareness

A Message From

John Fluke Mfg. Co., Inc.



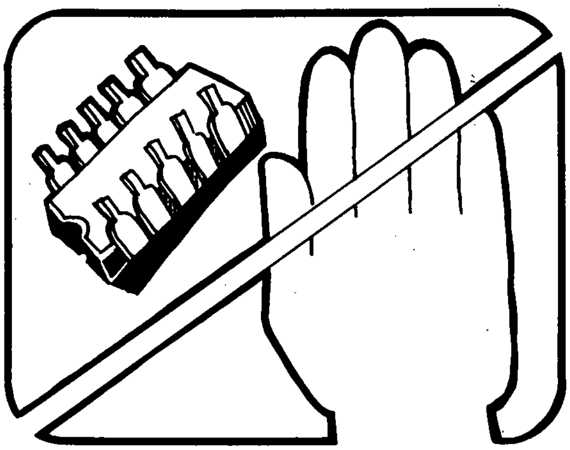
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

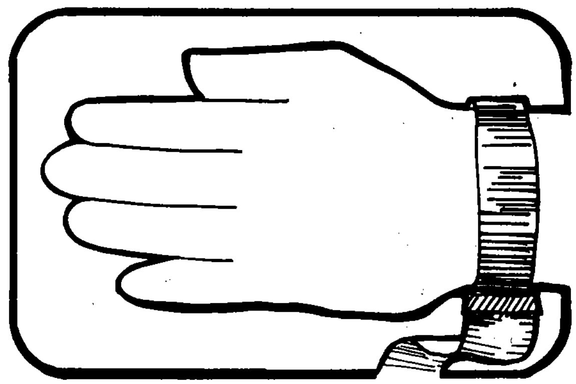
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol

" ⊗ "

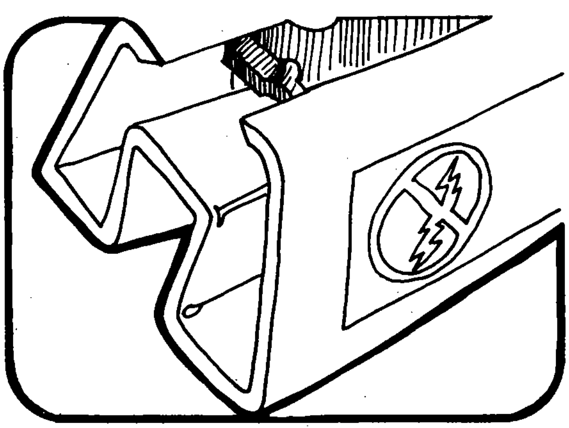
The following practices should be followed to minimize damage to S.S. devices.



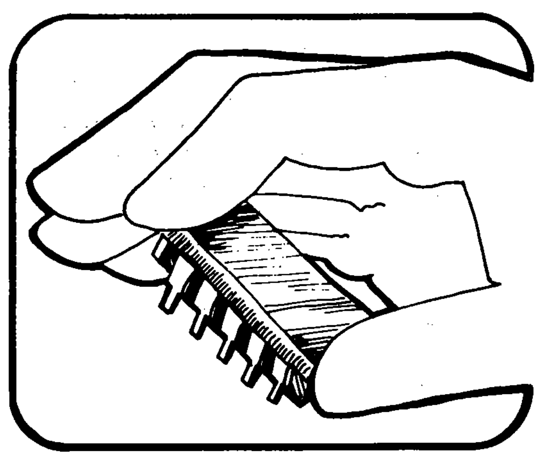
1. MINIMIZE HANDLING



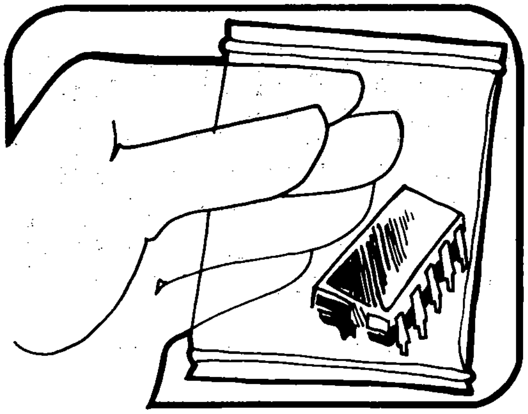
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES



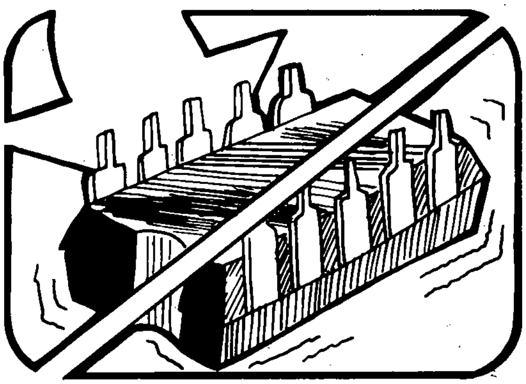
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



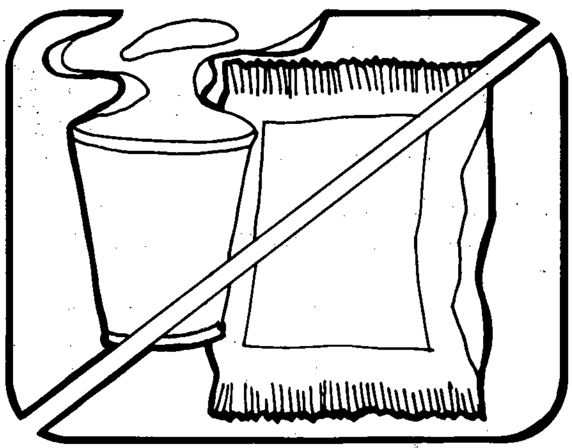
4. HANDLE S.S. DEVICES BY THE BODY



5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT

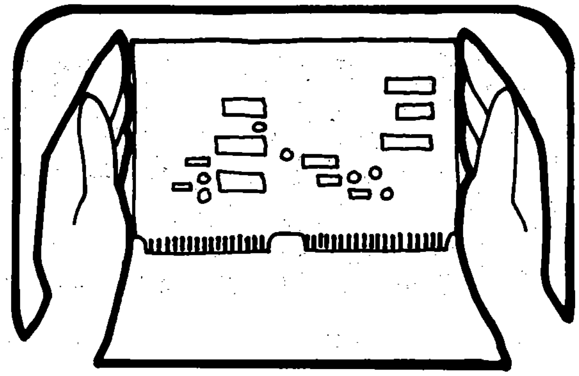


6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE

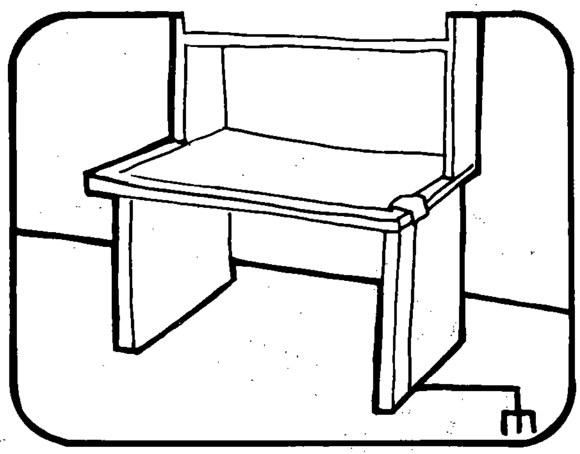


7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

® Dow Chemical



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR USUALLY PROVIDES COMPLETE PROTECTION TO INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Description
453522	6" X 8" Bag
453530	8" X 12" Bag
453548	16" X 24" Bag
454025	12" X 15" Bag
Pink Poly Sheet	Wrist Strap
30"x60"x60 Mil	P/N TL6-60
P/N RC-AS-1200	$7.00
$20.00	

J0089B-07U7810/SE EN Litho in U.S.A.

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. This section contains operating information for the Model 1900A. The contents of this section should be read before operating the counter. Should any difficulties arise during operation of this instrument, please contact your nearest John Fluke Sales Representative, or the John Fluke Mfg. Co., Inc., P.O. Box 43210, Mountlake Terrace, WA 98043; telephone (206) 774-2211. A list of Sales Representatives is located at the rear of this manual.

2-3. SHIPPING INFORMATION

2-4. The Model 1900A is packaged and shipped in a protective container. Upon receipt of the equipment, a thorough inspection should be made to reveal any possible shipping damage. Special instructions for inspection and claims are included in the shipping carton.

2-5. If reshipment of the equipment is necessary, the original container should be used. If the original container is not available, a new container can be obtained from the John Fluke Mfg. Co. Please reference the equipment model number when requesting a new shipping container.

2-6. INPUT POWER

2-7. The Models 1900A and 1900A–01 are supplied with one of three ac input power configurations. These consist of 100Vac, 115Vac and 230Vac; at 50 to 400 Hz. Before connecting to the ac line power, insure that the instrument is in the proper configuration for your power lines. A decal on the underside of the instrument indicates the ac line voltage and frequency required.

CAUTION

The battery-powered version must be operated at the line frequency stamped on the bottom–panel decal.

2-8. RACK INSTALLATION

2-9. The Model 1900A may be mounted in a standard 19-inch rack when supplied with the appropriate rack mounting kit. Rack mounting kits are available to allow left, right or center mounting. Instructions for installing units in the rack mount are supplied with the rack mounting kit. The center rack mounting kit is Model No. M00-200-612. The offset rack mounting kit is Model No. M00-200-611.

2-10. OPERATING FEATURES

2-11. The location and function of all controls, connectors, and indicators are shown in Figure 2-1. Operating features and instructions for accessories are discussed in Section 6.

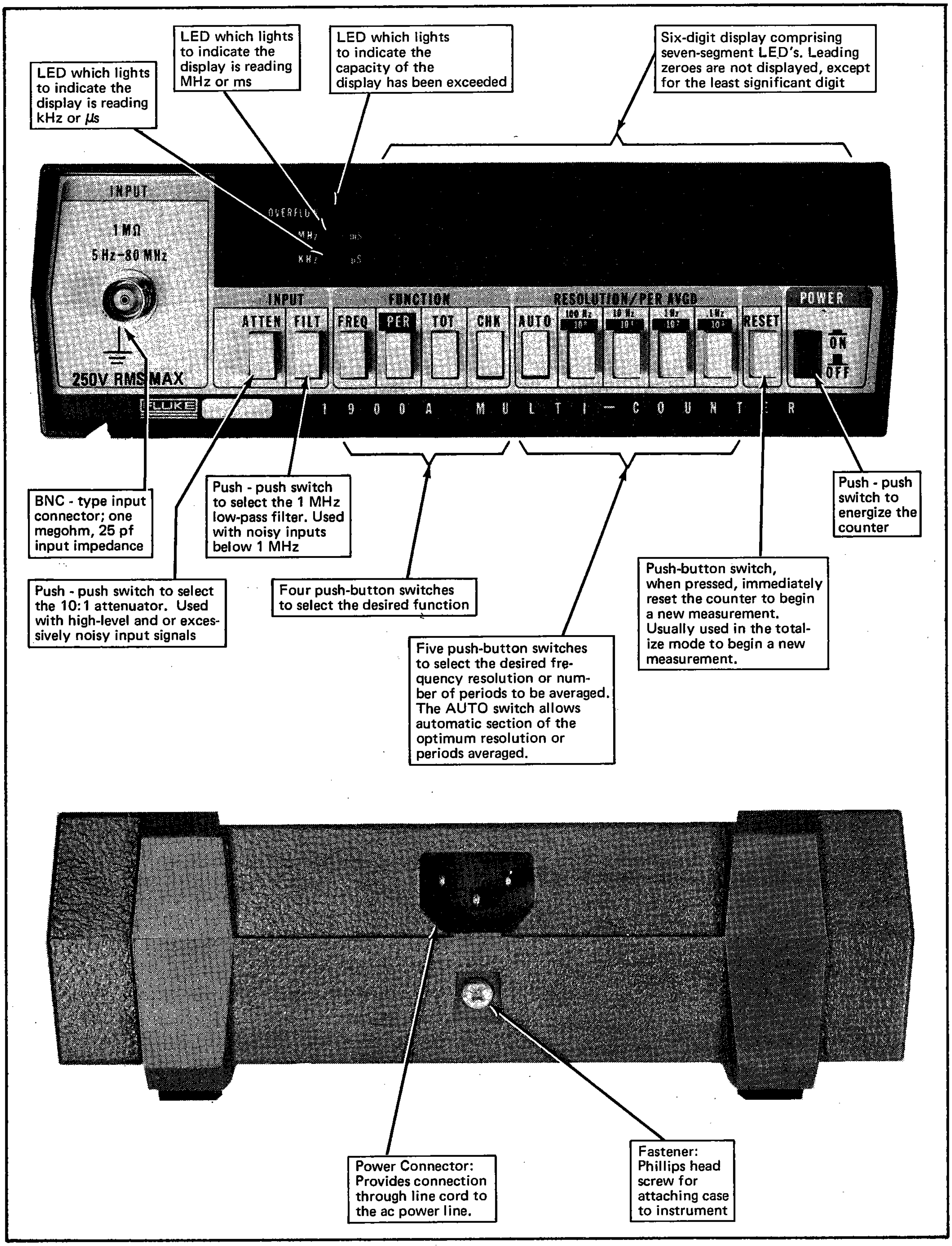


Figure 2-1. CONTROLS, CONNECTORS AND INDICATORS

2-12. OPERATING NOTES

2-13. Input Connection

2-14. Signals to be measured by the Model 1900A are applied to the front-panel BNC connector. Connection of all input signals should be by means of coaxial-type cable fitted with a mating BNC connector. Input impedance is one megohm shunted by < 30 pf. Input sensitivity is 25 millivolts rms. The input impedance derates to approximately 220K shunted by less than 40 pf for input levels greater than 500 mV.

WARNING

The outside contact of the BNC connector is tied directly to earth ground through the power plug. DO NOT connect the active lead of input signals to the outside contact. Irrepairable damage to the 1900A may result. To measure power line frequencies, use an isolation transformer.

2-15. Overload Protection

2-16. The Model 1900A will accept inputs as high as 250 volts rms at frequencies below 1 kHz without damage. Overload capability decreases linearly from 250 volts rms at 1 kHz to 20 volts rms at 80 MHz input, as illustrated in Figure 2-2.

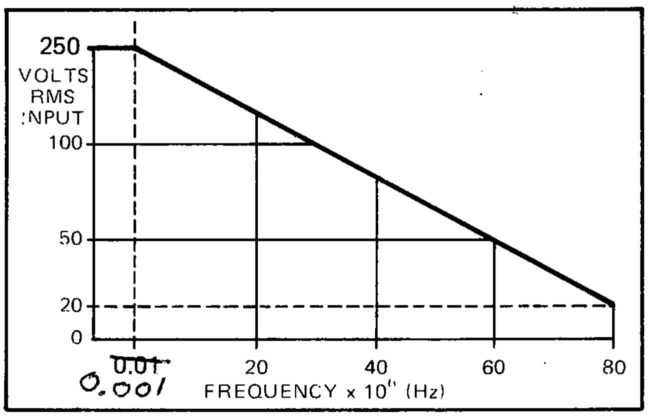


Figure 2-2. INPUT OVERLOAD PROTECTION LEVELS

2-17. FREQUENCY MEASUREMENTS

2-18. Perform frequency measurements as follows:

a. Press the POWER switch to the ON position.

b. Press the FREQ switch to select the frequency mode of operation.

c. Select the desired resolution, or the autorange mode by pressing the AUTO switch. If the input signal is completely unknown, the autorange mode will select the optimum range.

NOTE

In the autorange mode, automatic selection is made between the lower three resolutions. The 0.1 Hz resolution can only be manually selected (by means of the .1 Hz RESOLUTION switch).

d. Connect the input signal to the front-panel BNC connector. In the case of input waveform jitter or noise, spiked waveforms, or ripple on TTL waveforms, the reading obtained may be incorrect or unsteady due to false triggering of the schmitt trigger in the input section. If the signal level is greater than 150mV, depressing the ATTEN switch will decrease the triggering sensitivity of the input section by a factor of ten and reduce errors.

e. If the input signal is below 1 MHz, high-frequency noise can be eliminated by pressing the FILT switch.

f. Read the frequency on the display, and observe the unit of measurement indication (kHz or MHz) to the left of the display.

2-19. PERIOD MEASUREMENTS

2-20. Perform period measurements as follows:

a. Press the POWER switch to the ON position.

b. Press the PER switch to select the period mode of operation

c. Select the desired number of periods to be averaged, or the autorange mode by pressing the AUTO switch. If the input signal is completely unknown, the autorange mode will select the optimum number of periods to average.

NOTE

In the autorange mode, automatic selection is made between 10^0, 10^1 and 10^2 periods to be averaged. The 10^3 (1000) periods averaged can only be manually selected (by means of the 10^3 PER AVGD switch).

d. Connect the input signal to the front-panel BNC connector. In the case of input waveform jitter or noise, spiked waveforms, or ripple on TTL waveforms, the reading obtained may be incorrect or unsteady due to false triggering of the schmitt trigger in the input section. If the signal level is greater than 150mV, depressing the ATTEN switch will decrease the triggering sensitivity of the input section by a factor of ten and reduce errors.

e. If the input signal is below 1 MHz, high-frequency noise can be eliminated by pressing the FILT switch.

f. Read the period time on the display, and observe the unit of measurement indication (ms or μs) to the left of the display.

2-21. TOTALIZE MEASUREMENTS

2-22. Perform totalize measurements as follows:

a. Press the POWER switch to the ON position.

b. Press the TOT switch to select the totalize mode of operation, and the RESET switch to initialize the counter.

c. Connect the input signal to the front-panel BNC connector. In the case of input waveform jitter or noise, spiked waveforms, or ripple on TTL waveforms, the reading obtained may be incorrect or unsteady due to false triggering of the schmitt trigger in the input section. If the signal level is greater than 150mV, depressing the ATTEN switch will decrease the triggering sensitivity of the input section by a factor of ten and reduce errors.

d. If the input signal is below 1 MHz, high-frequency noise can be eliminated by pressing the FILT switch.

e. Read the accumulated total on the display.

2-23. SELF-CHECK MODE

2-24. The self-check mode provides a means of verifying proper overall operation of counter, excluding input section, time base accuracy, and time base dividers used in the period mode.

a. Press the POWER switch to the ON position.

b. Press the CHK switch to select the self-check mode.

c. Press the 100 Hz RESOLUTION switch; the display should read 1.0000 MHz, with the leading zero blanked (X1.0000).

d. Press the 10 Hz RESOLUTION switch; the display should read 1000.00 kHz.

e. Press the 1 Hz RESOLUTION switch; the display should read ~~00.0000~~ 000,000 kHz, and light the OVFL annunciator.

f. Press the AUTO switch; the display should read 1000.00 kHz, as in step d.

Section 3
Theory of Operation

THEORY OF OPERATION

3-1. INTRODUCTION

3-2. This section of the manual is divided into two parts. Overall Functional Description gives an overview of the circuit functions and how they are used in each mode. Circuit Description details the operation of each circuitry section. Simplified block diagrams are referred to by figure number. Complete schematic diagrams are located in section 8. Table 3-1 is a list of definitions for the mnemonics used in the schematic diagrams and text.

Table 3-1. MNEMONIC DEFINITIONS

BCD	Binary Coded Decimal
BL	Blank or Blanking
CLK	Clock
DP	Decimal Point
DS	Decimal Signal
FF	Flip-Flop
ICR	Iteration Counter Reset
KL	Annunciator Signal (MHz - mSec)
LSD	Least Significant Digit
ML	Annunciator Signal MHz - mSec)
MSD	Most Significant Digit
MSDM	MSD Memory
MUP	Memory Update
OV, OVFL	Overflow
RMAX	Reset to Maximum Count
RNG	Range
TOT	Total or Totalize

3-3. OVERALL FUNCTIONAL DESCRIPTION

3-4. Introduction

3-5. Seven basic sections compose the circuitry of the 1900A multicounter: an input section, main gate, decade counters/display memory/ display multiplexer, display, time base, range control logic, and program control logic. The input section conditions the signal with regard to amplitude and waveshape. The main gate controls the application of the signal to be counted to the decade counters. A signal is counted by the decade counters, stored in the display memory, and multiplexed to the display on a common data bus.

3-6. The time base section provides two frequencies which compose the time base against which other signals are compared. Range control divides the time base (or the input signal in the period mode) to control the main gate. Decimal information is derived from range control. Program control consists of a sequencer and autorange logic. Understanding the sequencer logic, which controls the timing of events, is very important to understanding the functioning of the instrument. An outline of the sequence of events is given in the explanation of the frequency mode.

3-7. Frequency Mode

3-8. In the frequency mode the signal from the input section is applied to the first decade counter. Refer to figure 3-1. The duration of the count is derived from the time base. The sequence of events, as ordered by the pro-

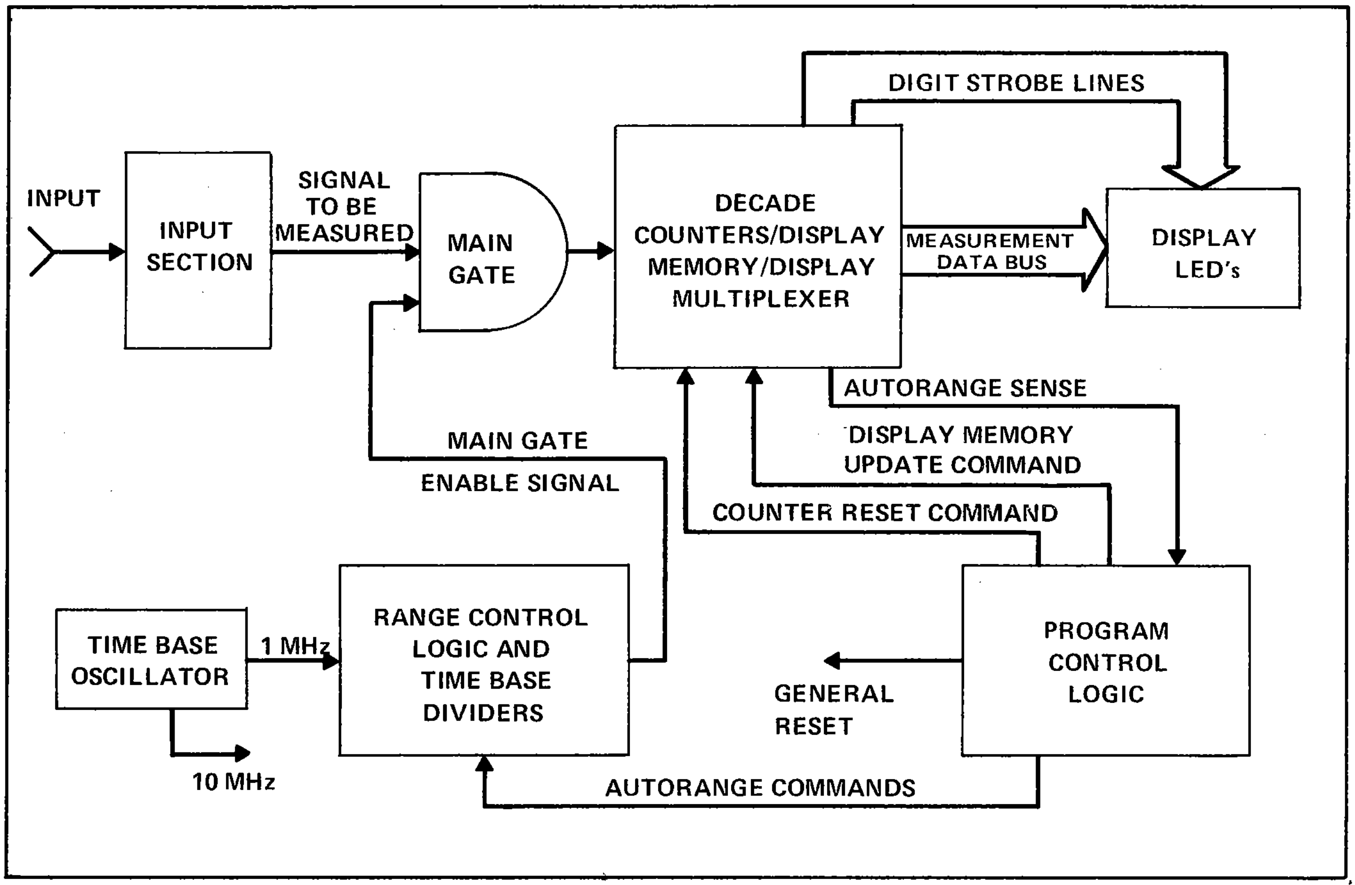


Figure 3-1. MODEL 1900A, SIMPLIFIED BLOCK DIAGRAM – FREQUENCY MODE

gram control section, begins with step 9. Refer to figure 3-2. Range logic is reset to the shortest gate time. A new measurement always begins with the shortest gate time. Any time a front panel switch is depressed, a new measurement is initiated by resetting the program control to step 9. The next event is general reset (GR), step 1. All the decade counters are set to 0 and the autorange logic is reset. Step 2 is skipped as only odd numbered steps are used to order events. At step 3 the time base dividers in the time base and the range control sections are enabled. The count is initiated by enabling the main gate to apply data to the first decade counter. The signal from the input section is applied to the clock input and toggles the counter. The output from the first counter is used to toggle the subsequent counters. At the end of the measurement period, the main gate is disabled and the count is held.

3-9. During step 5 the autorange logic decides whether or not the range is adequate for optimum resolution. If the most significant digit (MSD) is one or more, optimum resolution has been achieved. If the MSD is less than one, range control increases the gate time by a factor of ten. Manual selection of a range appears to the autorange logic as though the MSD is greater than one. Steps 7 and 9 are skipped and another count is taken in the new range. However, if in the previous measurement the MSD was equal to one, the second significant digit (2SD) must fall below 8 before a range change will be initiated This range hysteresis prevents an unstable display if a measurement happens to vary a few cycles above or below MSD = 1. When a count is obtained with optimum resolution, the sequence may go on to step 7.

3-10. A memory update signal, MUP, occurs at step 7. The count obtained in step 5 is memorized for presentation to the display section. The display runs continuously. BCD digit information is strobed by the multiplexer from the memory on a data bus to the display. Six strobes are used, one for each digit. Each strobe enables one digit byte to be applied to the data bus and simultaneously enables the appropriate LED to light. MUP also enables the range logic conditions to be memorized by the decimal point logic. The decimal point logic decodes the range information and applies a pulse to the decimal bus during the correct strobe.

3-11. Range logic is reset to the shortest gate time during step 9. The measurement cycle is now complete and the instrument is ready to take a new measurement. Every new measurement starts with the shortest gate time.

3-12. Period Mode

3-13. The signal from the input section is applied to range control to derive the gate time in the period mode.

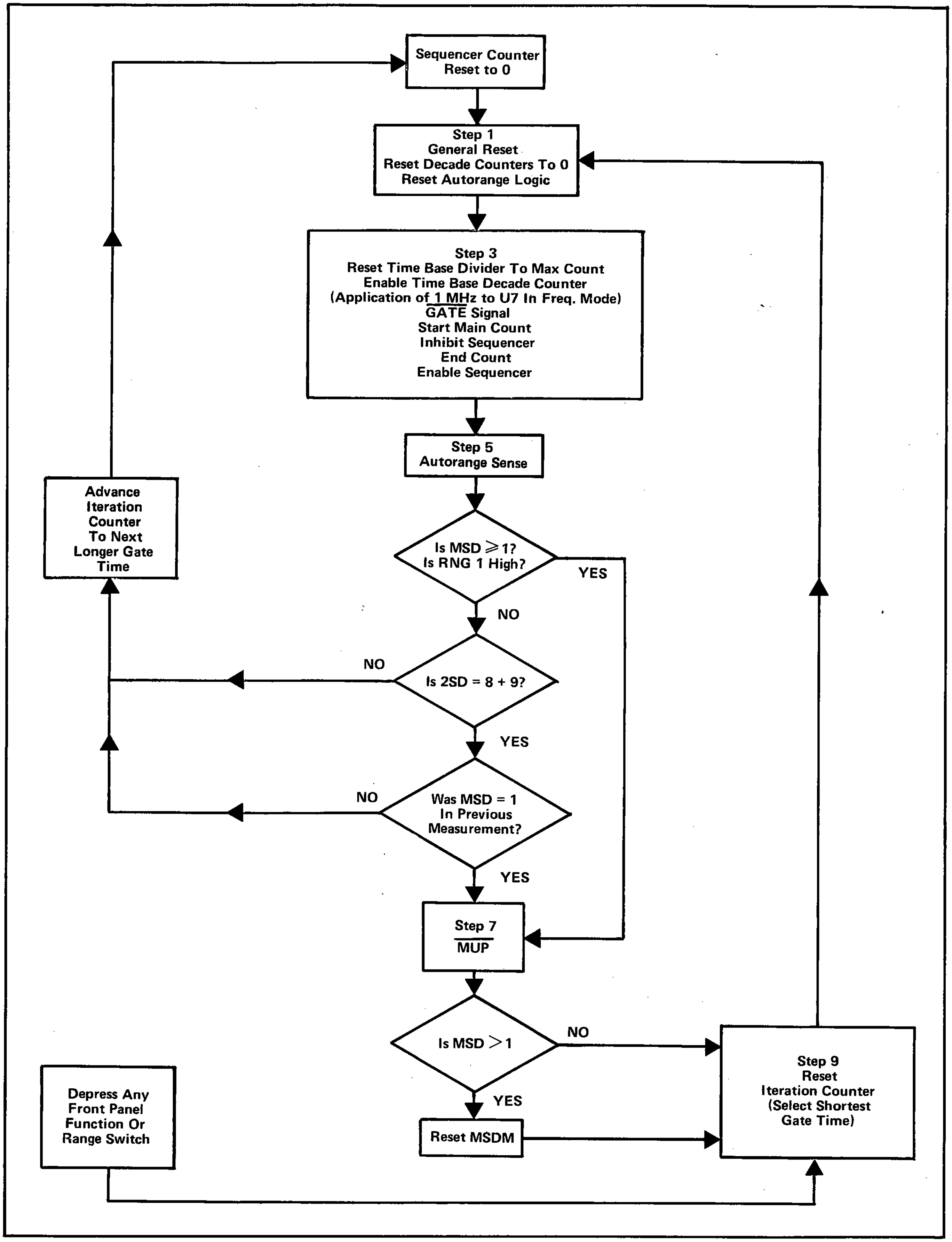


Figure 3-2. 1900A SEQUENCE FLOW CHART

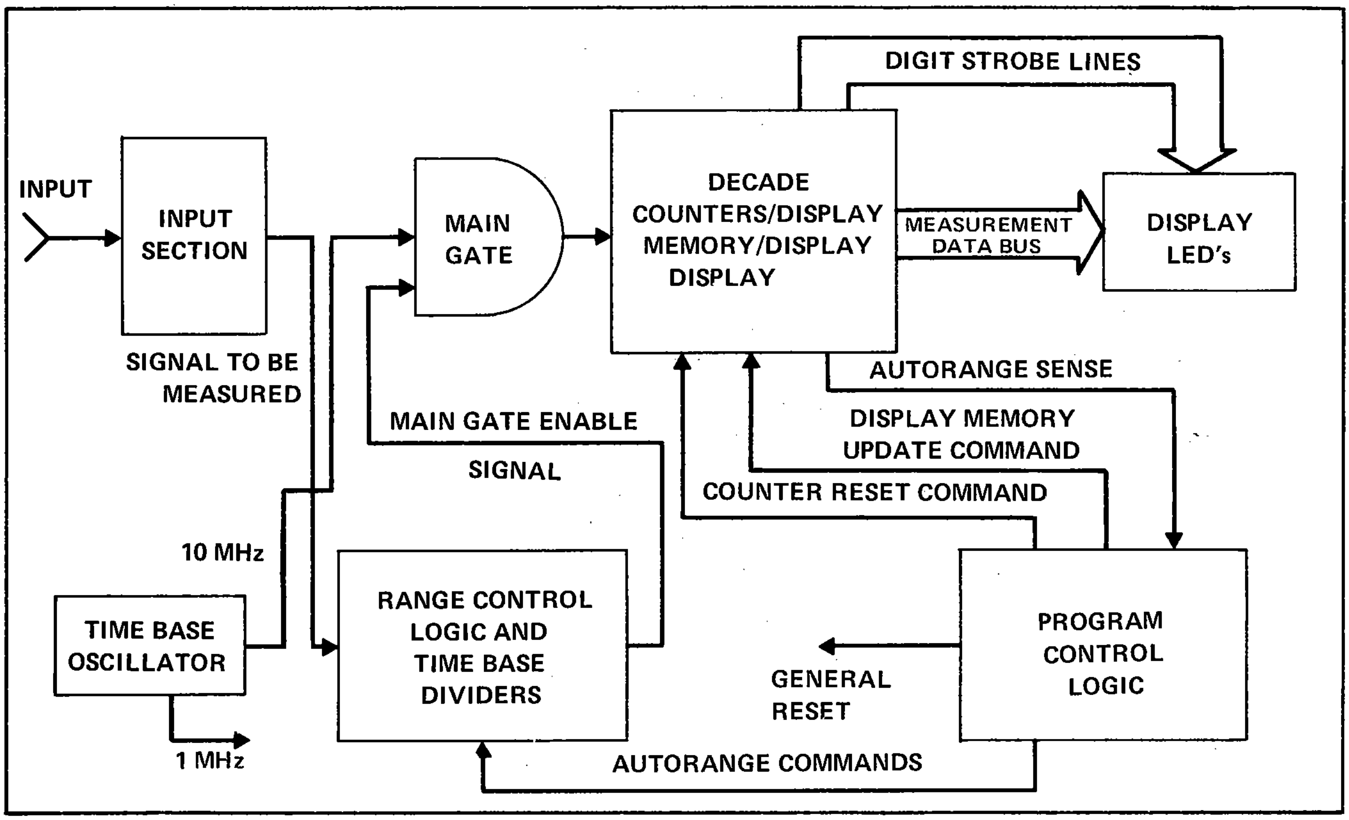


Figure 3-3. MODEL 1900A, SIMPLIFIED BLOCK DIAGRAM – PERIOD MODE

Refer to figure 3-3. Range control is programmed differently so that smaller division factors of ten are used in the period ranges. A 10MHz signal from the time base section is counted to determine how long the period is. The sequence of events is the same as in the frequency mode.

3-14. Totalize Mode

3-15. All range and program control functions are bypassed in the totalize mode. Refer to figure 3-4. The signal from the input section is applied to the first counter as in the frequency mode. However, the gate time is manually

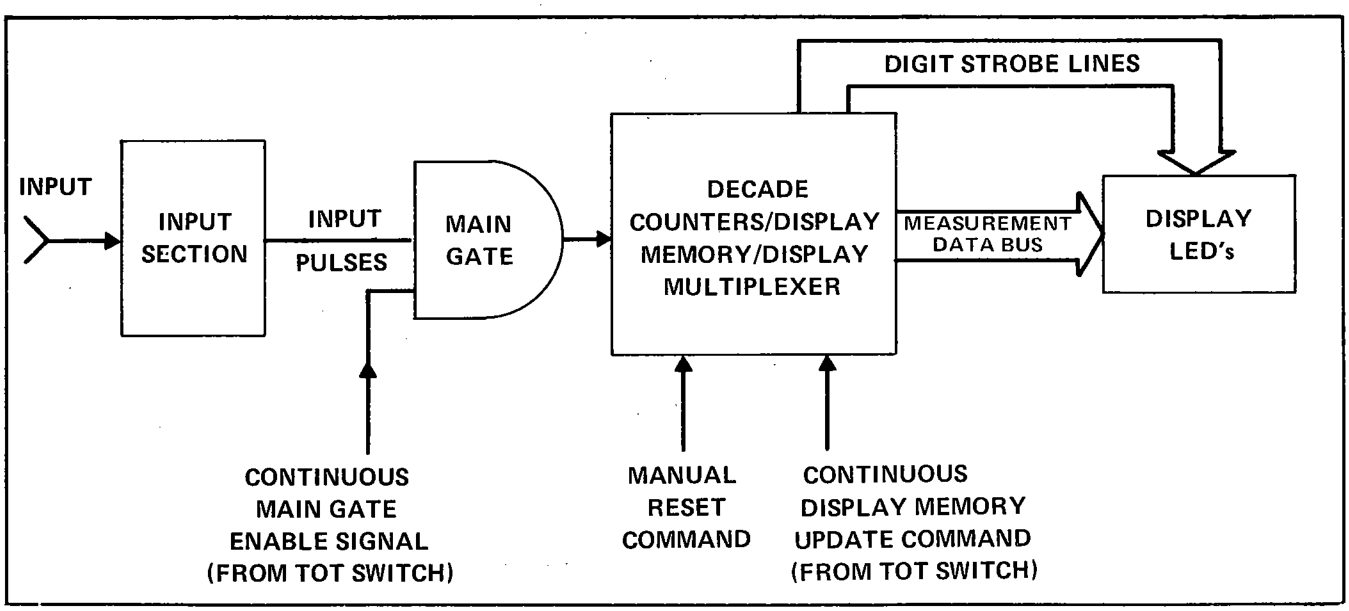


Figure 3-4. MODEL 1900A, SIMPLIFIED BLOCK DIAGRAM – TOTALIZE MODE

controlled. MUP is continuously enabled and the count is displayed as it is counted. The counter will count to 999999, when the overflow indicator lights and the count starts over. A new count may be initiated by depressing the reset switch.

3-16. Self Check Mode

3-17. In the self check mode the 1 MHz output from the time base section is used both as the derivation of the gate time and as the frequency to be counted. Refer to figure 3-5. In this mode the functioning of all parts of the instrument may be checked except the input section, the accuracy of the time base, and the time base dividers used in the period mode. The sequence of events and the operation of the circuitry is the same as in the frequency mode.

3-18. CIRCUIT DESCRIPTION

3-19. Introduction

3-20. Analysis of circuit blocks are contained in this section of the manual. Simplified schematic block diagrams are referred to by figure number. Information presented in tabular form is referred to by table number. Complete schematic diagrams are located in section 8. Circuit blocks must be analysed not only with respect to their internal operation but in relation to the sequence of events as explained under Frequency Mode. Figure 3-2 is a flow chart of the sequence of events in the 1900A.

3-21. Sequencer

3-22. The sequencer consists of a relaxation oscillator (U1), a decade counter (U2), and a decoder (U3). Refer to figure 3-6. Two sections of U1 are used to form the relaxation oscillator. R3 and C1 determine the frequency, approximately 100 Hz. U2 counts the oscillator frequency and presents the count to U3 in BCD form. Outputs from U3 are used to command events in the 1900A sequence. In all cases the output of U3 goes low to select an event. Step 1 is general reset (GR). The output of U3 is applied to a two-input NAND gate, one section of U5. The other input to the NAND gate is from the front panel switches through U1. If either input goes low, GR is initiated. The output of U5 is inverted twice to obtain the required GR and $\overline{\text{GR}}$ signals.

3-23. During step 3 the main gate is enabled. The $\overline{\text{GATE}}$ signal applied to a section of U5 inhibits the sequencer. $\overline{\text{RMAX}}$ from U3 inhibits the relaxation oscillator through CR1 and sets its output high so that at the end of $\overline{\text{GATE}}$, the counter will be toggled to the next step. Step 5 is autorange sense, step 7 is the memory update, MUP, and step 9 is the iteration counter reset, $\overline{\text{ICR}}$.

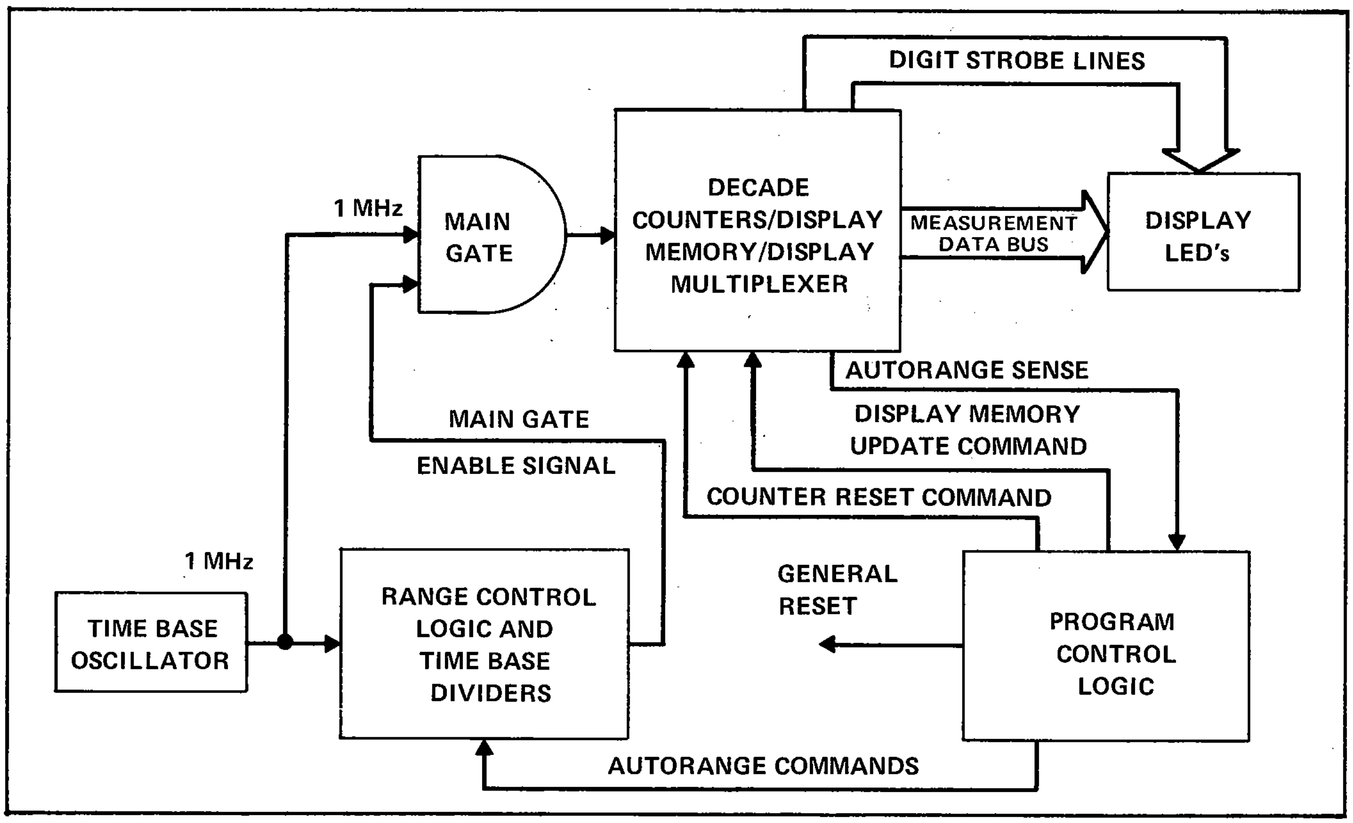


Figure 3-5. MODEL 1900A, SIMPLIFIED BLOCK DIAGRAM – SELF-CHECK MODE

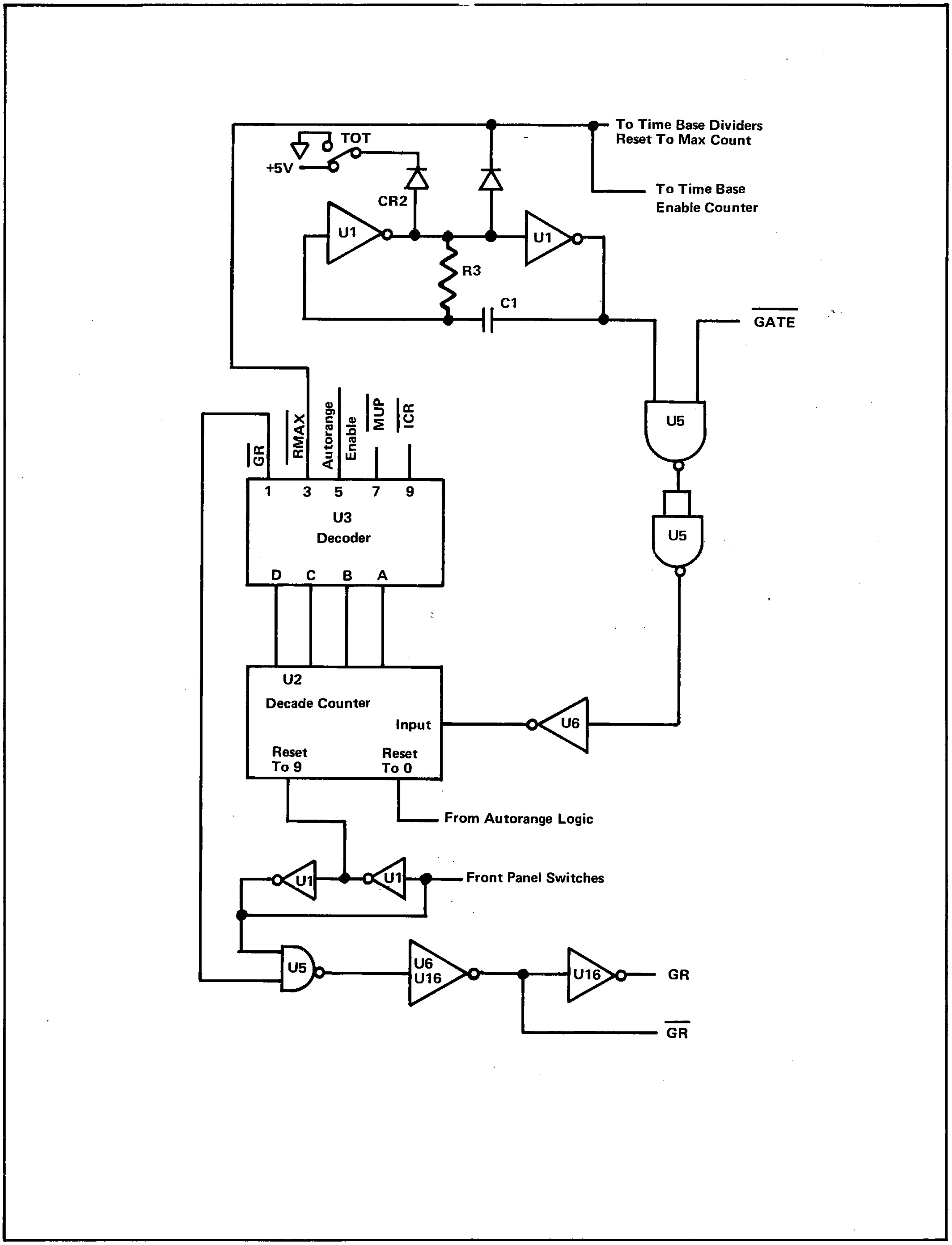


Figure 3-6. SEQUENCER

3-24. Input Section

3-25. An input signal from the BNC connector is coupled through C1 to buffer amplifier, Q1 and Q2. Refer to figure 3-7. The output of the buffer is applied to the emitters of Q3 and Q4. Attenuator switch, S1A, controls the biasing of Q3 and Q4. Q3 passes the signal unattenuated and Q4 passes the signal attenuated by R6 and R7. With the filter switch out, CR7 and CR8 are biased off and no filtering occurs. When CR7 and CR8 are biased on, C6 provides a low impedance path to ground for frequencies above 1 MHz. The first section of U1 is a comparator amplifier whose triggering sensitivity is controlled by R14. The second section of U1 is an amplifier which drives the third section, a schmitt trigger. The output amplifier consists of Q5, Q6, and Q7 which further squares the signal and converts it to TTL levels.

3-26. Main Gate/Decade Counters

3-27. At step 3 in the sequence, a gate pulse ($\overline{\text{GATE}}$) is generated by the range control logic. $\overline{\text{GATE}}$ is applied to one input of the main gate, U17. Refer to figure 3-8. The other main gate input is connected to the totalize (TOT) switch, S5C. If either input to U17 goes low, its output goes high. This presents a logic 1 to the J and K inputs of the first flip-flop in the LSD decade counter. The input signal is applied to the clock input of the decade counter and toggles the counter on the negative-going edge of the pulses. The output of the first counter is applied to U24 on

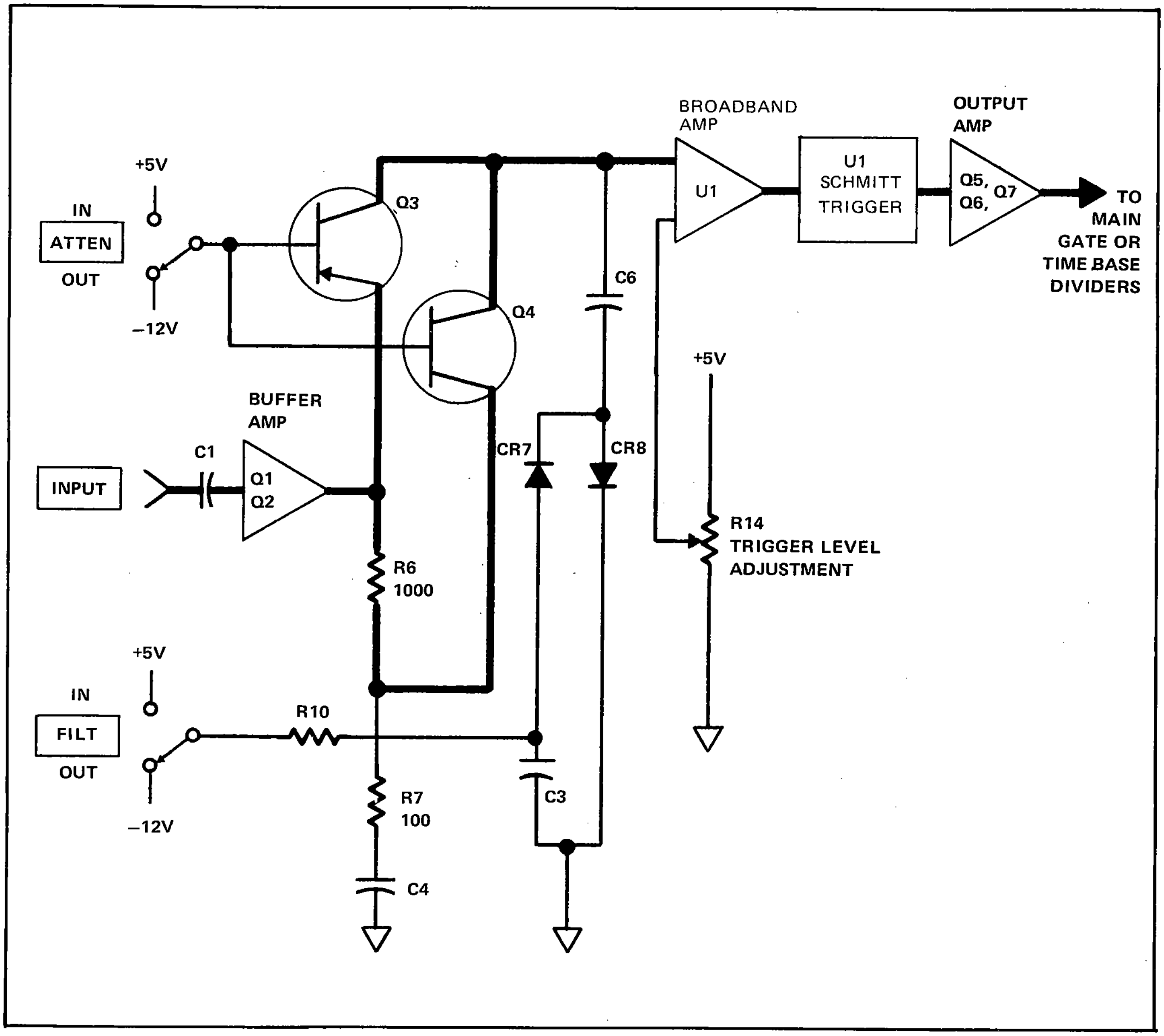


Figure 3-7 INPUT SECTION, BLOCK DIAGRAM

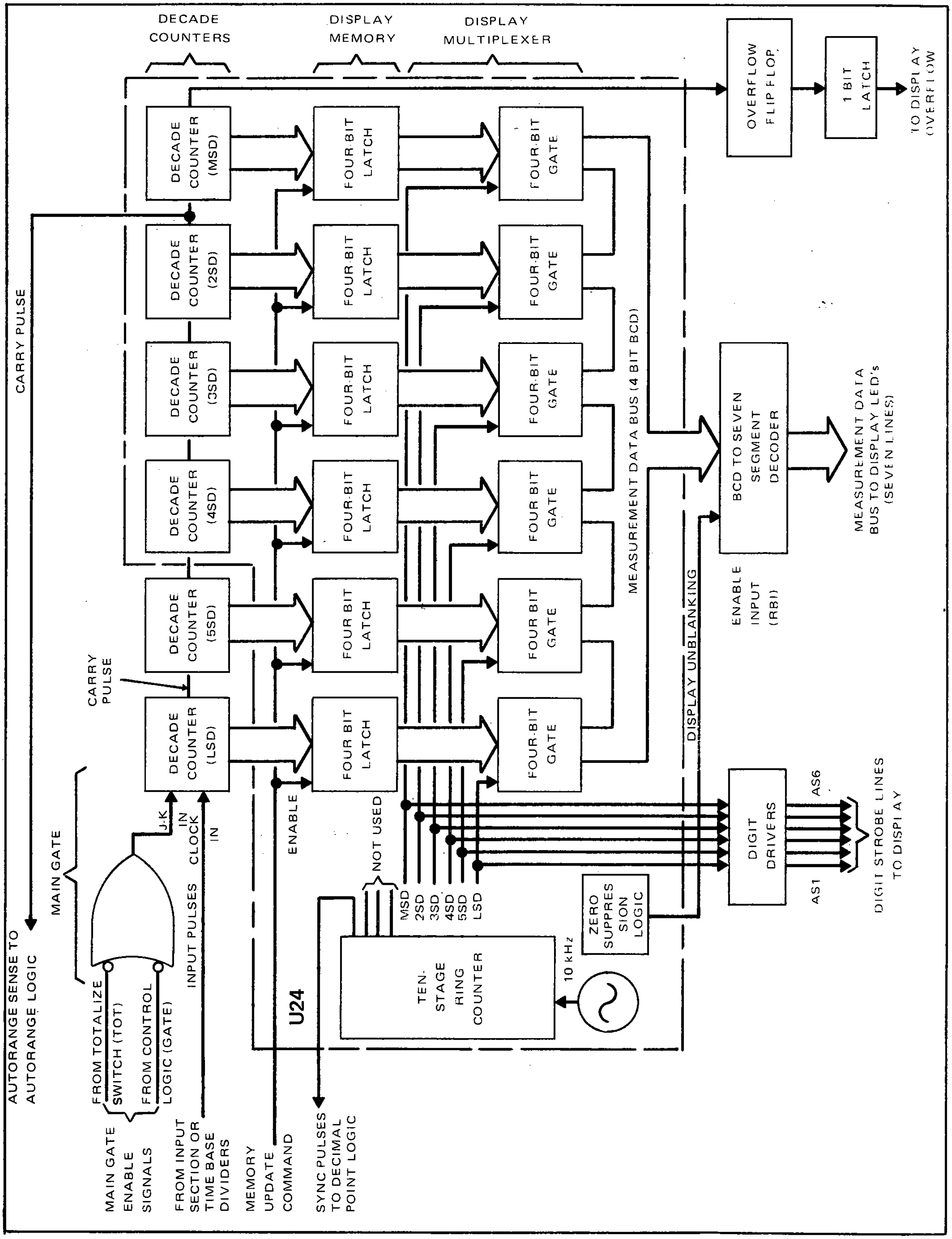


Figure 3-8. DECADE COUNTERS, DISPLAY MEMORY & DISPLAY MULTIPLEXER BLOCK DIAGRAM

four BCD lines, A, B, C, and D. The D output is also applied to the next counter (5SD). The LSD and 5SD counters are seperate ICs. The rest of the counters along with the display memory, display multiplexer, and a ring counter used to develop strobe signals are contained in U24. The fourth or D line from a counter, which is applied to the next counter, goes high when its count reaches 8 and falls low on the tenth count. The trailing edge so generated clocks the next counter. At the end of $\overline{GATE}$ both inputs to U17 are high and its output goes low. With a 0 applied to the J and K inputs of the first flip-flop, the clock input is ignored and counting ceases. The counters hold the count until GR during step 1.

3-28. Display Memory and Multiplexer

3-29. When step 7 is reached, the sequencer generates a memory update (MUP) signal. Refer to figure 3-8. At that time the contents of the decade counters are memorized in four-bit latches. A 10 kHz oscillator and 10 stage ring counter inside U24 generate strobe signals used by the display multiplexer. The multiplexer consists of a four-bit gate for each latch in the display memory. The gates are sequentially enabled by the strobe signals to apply the contents of the memory latches onto the common measurement data bus, four BCD lines. Information on the measurement data bus is decoded by a seven-segment decoder for application to the display.

3-30. Display

3-31. The display consists of six seven-segment LEDs and three annunciators. Refer to figure 3-9. Decimal LEDs are contained in the seven-segment LEDs. At the same time a strobe signal enables a gate in the display multiplexer, it enables the appropriate LED. Although the digit information is applied to all the LEDs, only one will light at a time. An LED will only be on, then, for a period of 90 µseconds, allowing a 10 µsecond guard space between digit strobes. Decimal information and signals for two of the annunciators come from the decimal point logic as will be explained later. The overload annunciator is lit by an inverted signal from U24 when the count exceeds the capacity of the display.

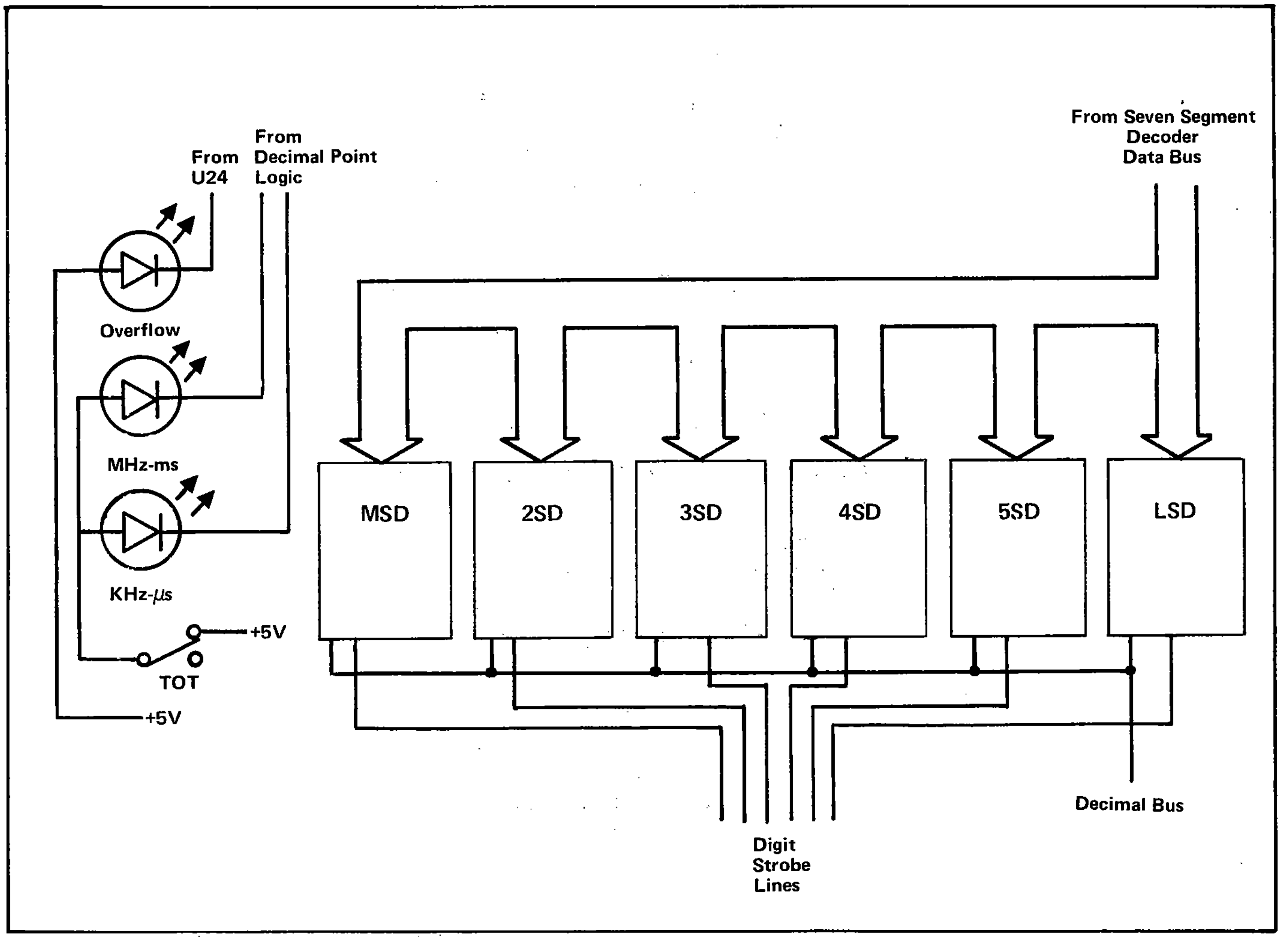


Figure 3-9. DISPLAY

3-32. Time Base

3-33. The time base section consists of a 10 MHz oscillator, a buffer amplifier (Q15), a NAND gate (U17), and a decade counter (U12). Refer to figure 3-10. Q16 is configured as a colpitts oscillator whose frequency is controlled by crystal Y1. Buffer amplifier, Q15, drives the NAND gate, U17, which provides further buffering. U12 divides the 10 MHz oscillator signal by ten to obtain the 1 MHz time base. U12 is held reset to 0 by the RMAX output from the sequencer being high. During step 3 of the sequence RMAX goes low and enables U12 to count. In the frequency and self-check modes the 1 MHz output from U12 is applied to the time base dividers of the range control logic. It is also the frequency counted in the self-check mode. In the period mode the 10 MHz output from the time base is the frequency counted. 10 MHz is used to optimize resolution when measuring short periods.

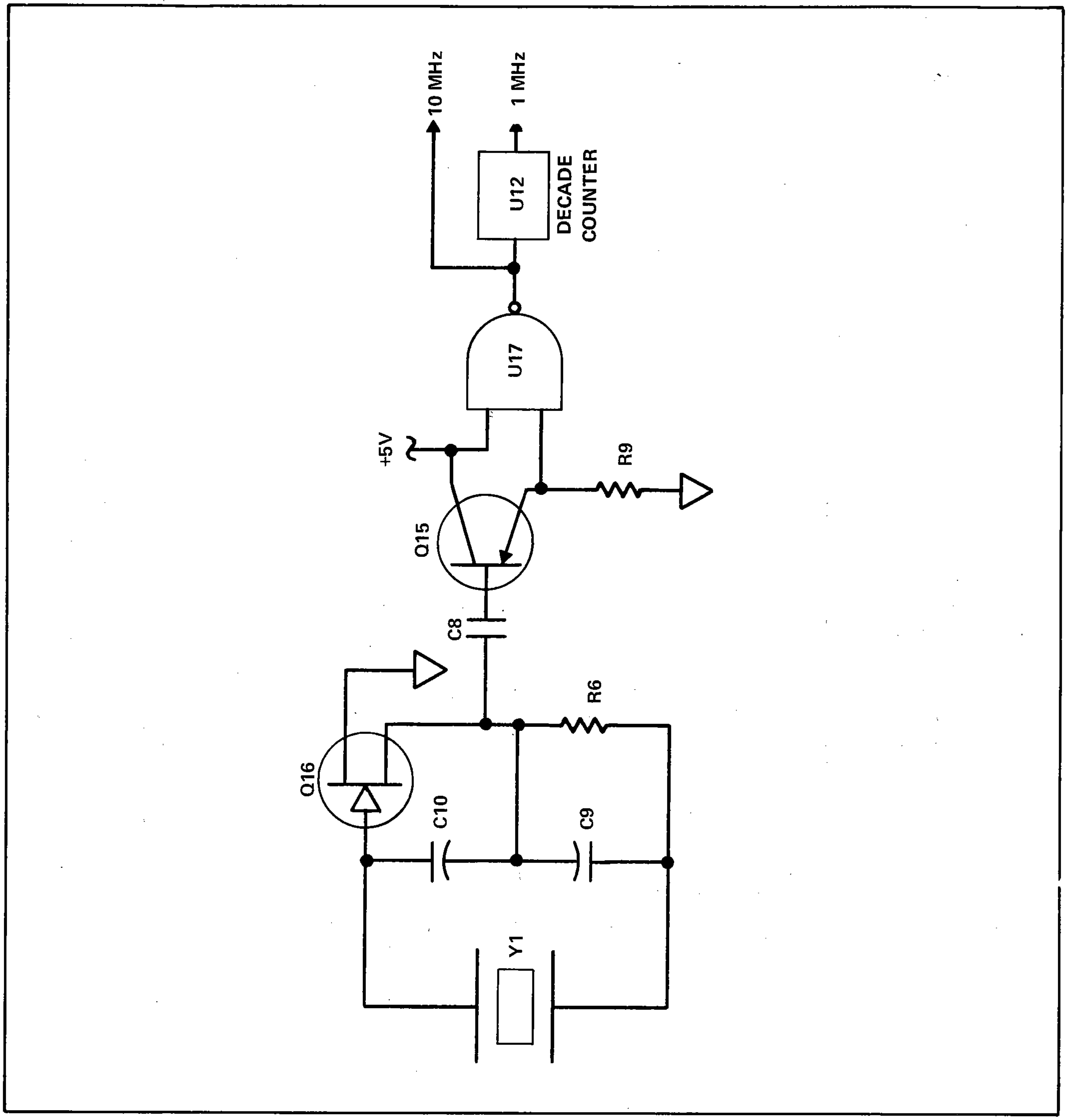


Figure 3-10 TIME BASE OSCILLATOR, BLOCK DIAGRAM

3-34. Range Control Logic

3-35. Range control logic consists of the range switches, an iteration counter (U13), time base dividers (U7), and a gate time flip-flop (U8). Refer to figure 3-11. The range switches program the iteration counter through four NAND gates (U18). The outputs of U18 are connected to the set and reset inputs of U13. When all inputs to U18 are high, all outputs are low, and the iteration counter will respond to a clock input from the autorange logic. For manual range programming, a range switch places a 0 on two inputs of

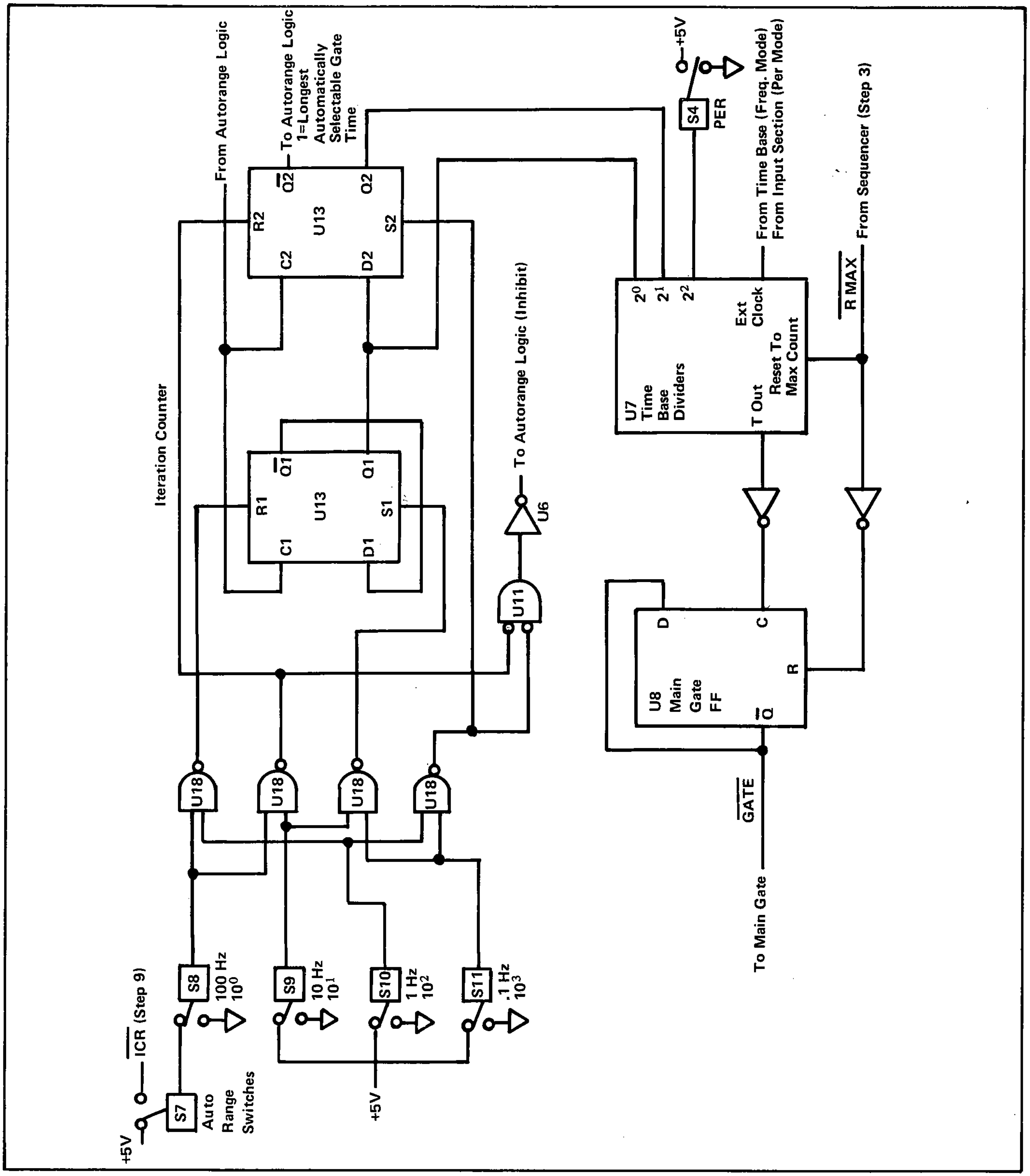


Figure 3-11. RANGE CONTROL LOGIC

U18. The iteration counter outputs are then set for that range. Autoranging is inhibited by a 1 output from one section of U6. When autorange is selected, two inputs to U18 are connected to the $\overline{ICR}$ output from the sequencer. At step 9 $\overline{ICR}$ goes low and resets the iteration counter to the shortest gate time. If at step 5 the autorange conditions are not satisfied, the autorange logic outputs a 1 to clock the iteration counter to the next longer gate time and to reset the sequence to step 1. When the third range has been automatically selected, the Q2 output from U13 will be high. Q2 then will be low and will inhibit the autorange logic from further increasing the gate time.

3-36. Outputs from the iteration counter are applied to the time base dividers, U7, and to the decimal point logic. Table 3-2 shows the programming of the time base dividers. External clocking, applied to U7, is divided to derive the gate time. In the frequency and self-check modes, 1 MHz from the time base is used. In the period mode, the signal from the input section is used. Note that the 2^2 input to U7 is from the PER switch. A 1 from the PER switch programs U7 for the three least division ratios (10^0, 10^1, 10^2) used in the period mode.

Table 3-2. TIME BASE DIVIDER RATIOS (U7)

RANGE CODE LINES TO U7			Division Factor Input/Output	Front-Panel Selected Resolution/ Periods Averaged
RNG2 (PIN 12)	RNG1 (PIN 13)	RNG0 (PIN 14)		
0	0	0	10^0	10^0
0	0	1	10^1	10^1
0	1	0	10^2	10^2
0	1	1	10^3	10^3
1	0	0	10^4	100Hz
1	0	1	10^5	10Hz
1	1	0	10^6	1Hz
1	1	1	10^7	0.1Hz

3-37. At step 3 in the sequence, the $\overline{RMAX}$ signal is applied to U7. All the counters in U7 have been set to maximum count (all nines) by $\overline{RMAX}$ having been high and the T Out output of U7 is high. As previously stated the $\overline{RMAX}$ signal enables the counter in the time base section. On the first pulse from the time base section (or from the input section in the period mode) T Out falls low. The trailing edge from T Out is inverted and applied to U8 as its clock. U8 flops and outputs the $\overline{GATE}$ signal. The counters in U7 are now counting. Just before the count reaches the desired division ratio, T Out goes high due to an 8 in the selected counter in U7. When the selected counter in U7 receives its tenth pulse, T Out again falls low and the trailing edge is inverted to clock U8. U8 flips to inhibit the $\overline{GATE}$ signal. RMAX then goes high and resets U7 to maximum count.

3-38. Decimal Point Logic

3-39. Outputs from the iteration counter (RNG1 and RNG0) are applied to the date inputs of two "D" type flip-flops in the decimal point logic. Refer to figure 3-12. During step 7 in the 1900A sequence, the MUP signal clocks the data into the flip-flops. The Q and $\overline{Q}$ outputs from the flip-flops are applied to five NAND gates. One of the NAND gates is used to select a unit annunciator (MHz-ms or kHz-μs). The outputs from four of the NAND gates are applied to a negated-input OR gate, U9. The desired output from U9 is a positive pulse or 1 during the strobe pulse which will corrently place the decimal point. Strobes 2, 3 and 4 (counting from the LSD) are applied to the four NAND gates used in decoding the range information. Range information is applied to the four gates in such a way that two ones (1s) will be on only one of the NAND gates for each range. This sets up the NAND gate so that when the strobe applied to its third input goes high, its output will go low. A low input to U9 will force its output to go high. The output of U9 is applied through the TOT switch (decimals are not used in the totalize mode) to U24 and the decimal driver (Q14). The decimal driver enables the decimal segment of the appropriate LED to light. U24 utilizes the decimal input to prevent zero blanking after the decimal point.

3-40. Autorange Logic

3-41. The autorange logic consists of three "D" type flip-flops and three logic gates. Refer to figure 3-13. The function of the autorange logic is to output a positive pulse to clock the iteration counter and to reset the sequencer to step 1 if optimum range conditions have not been met. Optimum range conditions are defined as the MSD greater than or equal to one. A hysteresis provision has been added so that if the MSD = 1 in a measurement, the 2SD of the succeeding measurement (if MSD < 1) must fall below 8 before a range change will be initiated.

3-42. A four-input NAND gate (U9) is the main control gate for the autorange logic. One of the inputs to U9 is from the sequencer. At step 5 the sequencer applies a 1 to U9, enabling it to sense the condition of the autorange logic. If any input to U9 is a 0, its output is a 1 which is inverted and no clock pulse exists. Another input to U9 is from the iteration counter, which goes to 0 in the 1 Hz-10^2 Periods range. A longer gate time cannot be selected, then, by the autorange logic. The other two inputs to U9 are derived from the state of the 2SD counter.

3-43. Autorange Sense is taken from U24: the output of the 2SD counter (D5D), which is high when the 2SD count equals 8 or 9. Autorange Sense is applied to a two-input NAND gate (U5), and after inversion to the MSD=1 flip-flop. On the tenth count of the 2SD counter (MSD=1), Autorange Sense falls low. After it is inverted, the trailing edge so produced clocks the MSD=1 flip-flop. The Q output from the MSD=1 flip-flop goes to 1 and the Q output goes to 0. Q from the MSD=1 flip-flop clocks the MSDM flip-flop so that its Q output equals 1. When Autorange Sense again goes from high to low (MSD > 1), the MSD=1 flip-flop is clocked again. Its Q output goes to 0 and its Q goes to 1, which clocks the MSD > 1 flip-flop. Since the data input to the MSD > 1 flip-flop is tied to +5V, its Q output will now remain equal to 1 no matter how many more times it is clocked.

3-44. Two of the inputs to the autorange control gate, U9, are from U5 and U11. U11, a NOR gate, outputs a 0 (producing satisfied range conditions) if either input is a 1. One input to U11 is from the MSD=1 flip-flop and the other input is from the MSD > 1 flip-flop. So if either flip-flop has been clocked, a 1 will be applied to U11 and the range conditions will be satisfied. U5 provides the hysteresis effect. Both its inputs must equal 1 to get a 0 out. One input to U5 is from the MSDM flip-flop. The other input is from Autorange Sense. At step 7 of the sequence, MUP will reset the MSDM flip-flop if the MSD of the measurement was greater than 1. The output of a negated-input NAND gate (U11) is used to reset the MSDM flip-flop. One input to U11 is the MUP signal. The other input is from the Q output of the MSD > 1 flip-flop. Therefore the MSDM flip-flop cannot be reset unless the MSD is greater than 1. If in the next measurement the MSD = 0, the MSDM will prevent a range change unless Autorange Sense is also 0, that is the 2SD is less than 8.

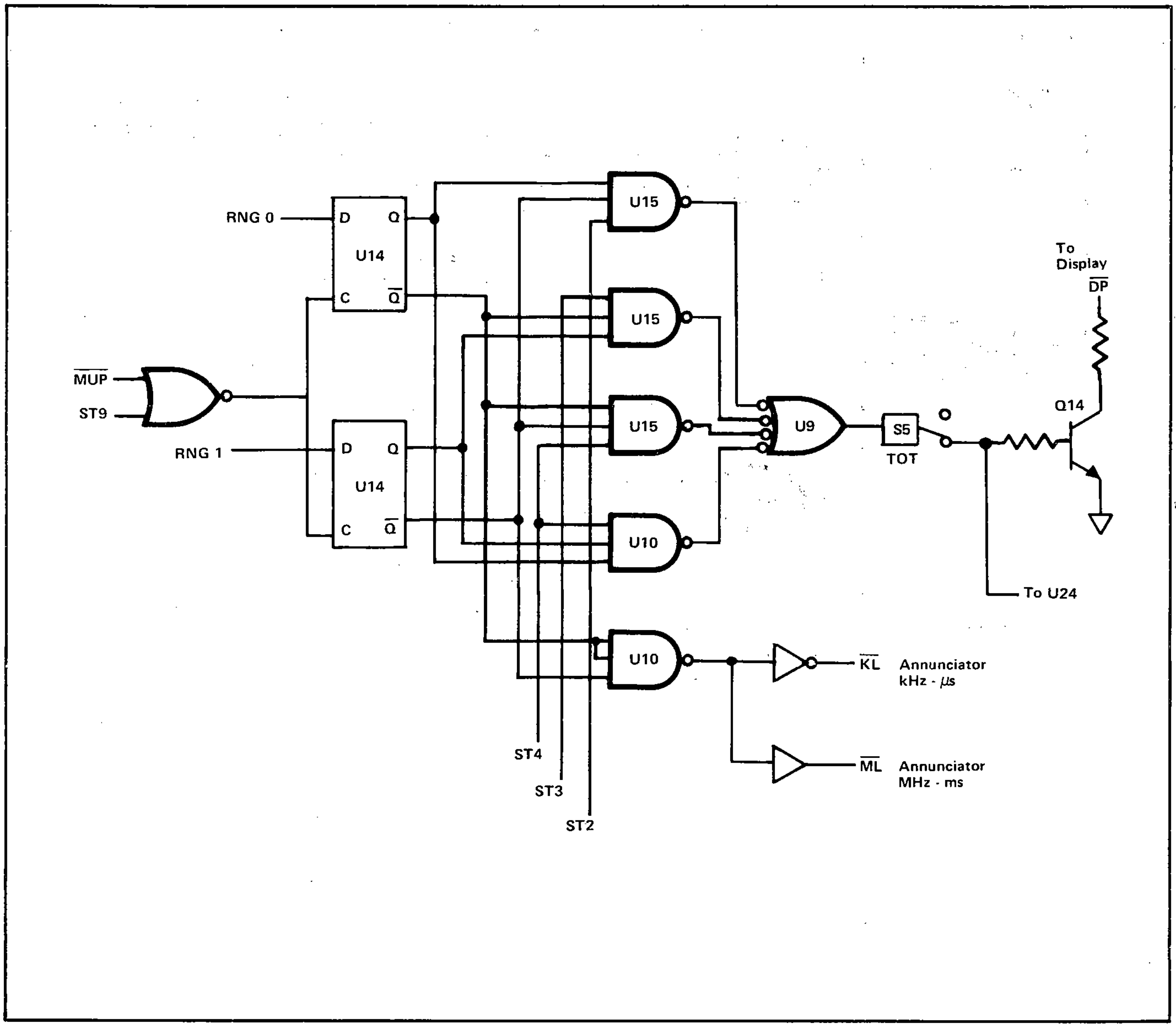


Figure 3-12. DECIMAL POINT LOGIC

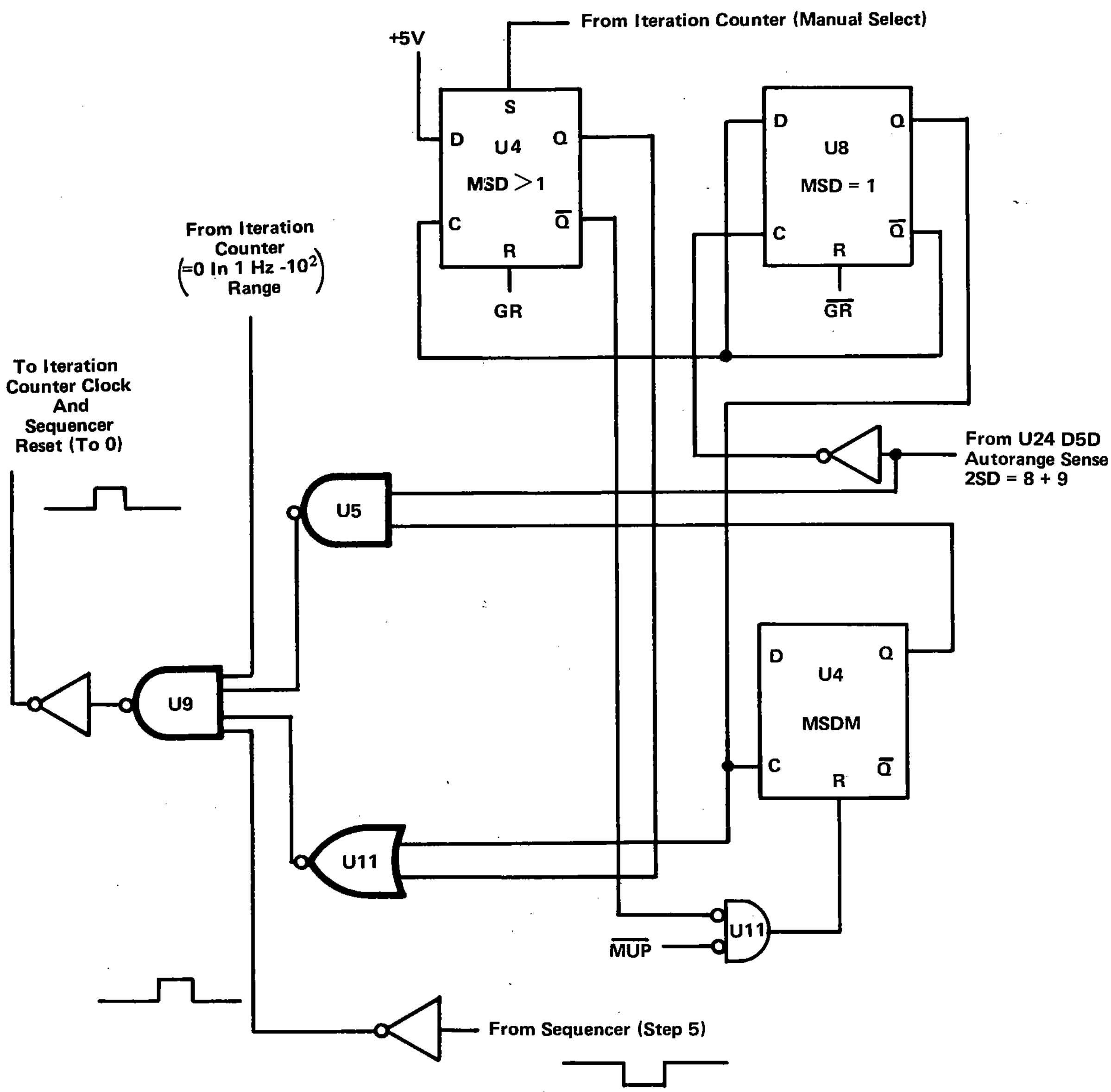


Figure 3-13. AUTORANGE LOGIC

Section 4

Maintenance

4-1. INTRODUCTION

4-2. This section contains information concerning preventive and corrective maintenance for the Model 1900A Multi-Counter. A maintenance interval of one year for calibration is recommended to ensure instrument operation within the one year specifications. Equipment for performing maintenance tests and adjustments is listed in Table 4-1. If this equipment is not available, other equipment having equivalent specifications may be used.

NOTE

When greater than one year accuracy is required, refer to specifications for timebase aging rate to determine the re-calibration interval required to maintain desired accuracy.

4-3. SERVICE INFORMATION

4-4. Should your instrument need repair, send it to the nearest factory authorized service center. A list of these authorized service centers is located in section 7. Located on the inside front cover is the WARRANTY which warrants the instrument for a period of one year. of one year.

4-5. GENERAL MAINTENANCE

4-6. Access

4-7. Use the following procedure to gain access to the interior of the Model 1900A.

a. With the power switch OFF, disconnect the line cord.

b. Remove the Phillips screw at the rear of the instrument case.

c. Remove the instrument from the case.

4-8. Cleaning

4-9. Clean the front panel and case with denatured alcohol or mild solution of detergent and water. Do not use aromatic hydrocarbons or chlorinated solvents because they will react with the plastic materials of the instrument.

4-10. Fuse Replacement

4-11. The input power fuse, F1, is located within the instrument in a fuse clip near the power transformer (T1). To gain access to the fuse, refer to paragraph 4-6. When replacement is required, install AGC 1/4A (fast acting) for line powered instruments. Use MDA ½A (slow blow) for battery powered instruments.

4-12. PERFORMANCE CHECKS

4-13. The performance checks provide a means of verifying overall operation of the Model 1900A. The checks can be used as an acceptance check during incoming inspection or as a periodic maintenance check. Refer to Table 4-1 for a list of required test equipment. Equivalent equipment may be used.

4-14. Functional Check

4-15. To perform a functional check of the Model 1900A, refer to the self-check described in Section 3.

4-16. Sensitivity Check

4-17. Perform the sensitivity checks as follows:

Table 4-1. TEST EQUIPMENT REQUIRED FOR PERFORMANCE TEST, CALIBRATION AND TROUBLESHOOTING

EQUIPMENT NOMENCLATURE	RECOMMENDED MODEL	WHERE USED
Quartz Oscillator Frequency Standard with 10 MHz Output	-	Timebase Oscillator Adjustment
Low-Frequency Oscillator	HP204D	
High-Frequency Oscillator	HP8654A	
RF millivoltmeter with 50Ω terminator	Boonton 91C	Sensitivity Check
Multimeter	Fluke 8000A	Troubleshooting
Oscilloscope	Tek 465	Troubleshooting

a. Connect the low frequency generator, set for 5 Hz at 25mV, to the 1900A input.

b. Energize the counter and depress the FREQ function switch and AUTO resolution switch.

c. Confirm that the counter display indicates .005 kHz ± 1 digit.

d. Disconnect the low frequency generator from the input.

e. Connect the high frequency generator, terminated into 50 ohms, to a T-connector on the 1900A input. Set the generator output for 10 MHz at approximately 25mV rms.

g. Connect the RF millivolt meter to the T-connector on the input of the 1900A.

h. Adjust the high frequency generator output for a reading of exactly 25mV on the RF millivolt meter.

i. Confirm that the counter display indicates 10.0000 MHz ± generator accuracy.

j. Change the generator output to 80 MHz at exactly 25mV.

k. Confirm that the counter display indicates 80.0000 MHz ± generator accuracy.

4-18. CALIBRATION

4-19. Calibration of the Model 1900A is limited to adjustment of the trigger level and time base oscillator frequency.

4-20. Trigger Level Adjustment

4-21. Trigger level adjustment should be performed whenever repairs have been made to the input section of the counter. The input section comprises that circuitry contained on the input printed circuit board assembly. Perform trigger level adjustment as follows:

a. Remove the counter from the case (paragraph 4-6).

b. Energize the counter and connect the high-frequency oscillator to the counter input.

c. Select an output of 25 mV rms at approximately 80 MHz on the oscillator.

d. Adjust the trigger level control (R14) to a mid-point which produces a stable display near 80 MHz.

e. Reduce the signal level until the display becomes unstable.

f. Re-adjust the trigger level control until the display is again stable.

g. Repeat steps e and f until no additional sensitivity increase is possible.

4-22. Time-Base Oscillator Adjustment

4-23. Time base oscillator adjustment should be made whenever the oscillator is repaired, or whenever it is determined that accuracy of the counter is not within the accuracy desired. Perform time base oscillator adjustment in an environment having an ambient temperature of +22°C to +25°C (72°F to 77°F). Allow the instrument to warm up at least 30 minutes with the case on before adjusting the time base.

4-24. Timebase Adjustment Using A Frequency Standard

a. Remove the counter from the case (paragraph 4-6)

b. Energize the counter and select the FREQ function and 10 Hz resolution.

c. Select a 10 MHz output on the quartz oscillator and connect the 10 MHz signal to the counter input.

d. While observing the counter display, adjust the time base oscillator control (C11 located on the main pcb directly behind the reset switch) to obtain a reading of 000000 ± 1 digit.

4-25. TROUBLESHOOTING

4-26. Introduction

4-27. The following information is designed as an aid in troubleshooting the 1900A multi-counter. Figures 4-2 to 4-6 are flow charts directed toward specific problems. Figure 4-1 shows the location of test points and table 4-2 gives the electrical location of the test points and what to expect at each point. Theory of Operation, section 3, and repair techniques, later in section 4, should be read and understood before attempting to troubleshoot the instrument.

4-28. Initial Troubleshooting

4-29. Thoroughly inspect the unit for physical damage such as broken parts, shorted leads, or other visually discernible problems. Recheck input connections and switch settings to be sure the problem actually is in the 1900A.

4-30. Power Supply

4-31. The power supplies should be checked first in the event of a 1900A malfunction. Remove the case as described in paragraph 4-6. Apply ac power. Test point 1 is the +5V regulated supply. Its limits for the line version are +4.75V to 5.25V with no more than 100mV p-p ripple. With the battery option the limits are +4.5V to 5.5V with no more than 500mV p-p ripple. Test point 2 is the -12V supply whose limits are -10.5V to -12.0V with no more than 100mV p-p ripple for either version.

4-32. Fault Isolation

4-33. Perform the self-check as described in section 2. Observation of the symptoms evident in the self-check mode should provide clues as to the location of the problem. If the unit performs the self-check satisfactorily the problem is probably in the input section. If the problem is decimal point related, the operation of the iteration counter and decimal point logic should be checked. No display or a missing digit probably indicates U23 or U24. Missing segments in the display probably indicates U23 or one or more faulty LEDs. No counting action or an erroneous count probably indicates program control, time base, or main gate/decade counter problems.

4-34. Input Section

4-35. Apply a 1V p-p signal to the 1900A BNC connector. Choose a frequency which has good waveform resolution on the oscilloscope. At the gate of Q1 the signal should be .5V p-p with no distortion (the voltage levels given are approximate). Distortion of the input, visible at the gate of Q1, begins at about 4V p-p input level. The emitter of Q3 should have 1.5V p-p as should pin 10 of U1. Depressing the FILT switch (looking at pin 10 of U1) should diminish the level slightly even at low frequencies. The roll-off of the filter is gradual. Succeeding waveforms are square waves with a spike on the leading edge. Outputs from U10 (pins 7, 3, 15) are approximately 1.25V p-p. The output of the input section (TP4) should be a square wave with spikes on the leading edge going positive from near OV to +5V.

4-36. Time Base

4-37. The voltage on the base of buffer Q15 should be about 9V p-p. TP3 should have 6V p-p of a moderately distorted sine wave. The output of U12 is a square wave with a spike on the trailing edge and ripple on the top of the waveform.

4-38. Sequencer

4-39. The output of the relaxation oscillator should be a 5V square wave. A differentiated square wave, about 10V in amplitude should be at pins 5 and 6 of U1. TP8 is a 5V square wave. The frequency of the relaxation oscillator should be around 100 Hz, interrupted by the duration of the gate signal. The outputs of U3 are normally at +5V and go low to near OV to select an event.

4-40. Control Logic and Counters.

4-41. To check the iteration counter, manually select the ranges and check the outputs against table 3-2. Troubleshooting the rest of the circuitry is best accomplished by checking for output pulses from the circuitry sections, keeping in mind the oscillator which governs the duration of the pulse and the place of the pulse in the sequence.

4-42. REPAIR TECHNIQUES

4-43. Battery-Powered Instruments

4-44. In battery-powered instruments, one of the batteries should be removed before attempting any repair. This is necessary to eliminate the danger of shorting portions of the circuitry which carry the battery voltage. Remove the battery as described in Section 6.

4-45. Integrated Circuit Replacement

4-46. Three types of integrated circuits are used in the Model 1900A, as listed in Table 4-3. The handling of TTL types require no special handling. However, the CMOS and PMOS types can be destroyed by a static electricity discharge. To prevent damage due to static discharge, the following precautions should be taken whenever this type of integrated circuit is handled:

a. The PMOS or CMOS integrated circuit is packed in conductive foam. Do not remove the conductive foam from the integrated circuit until ready for installation into the unit.

b. Be sure the repairing personnel and the unit under repair are commonly grounded.

c. Be sure the soldering iron used is grounded to the common ground.

Table 4-2. TEST POINT DESCRIPTIONS

TEST POINTS	ELECTRICAL LOCATION	DESCRIPTION
1	+5V reg.	+4.75V to +5.25V (⩽100mV ripple) line. +4.5V to +5.5V (⩽500mV ripple) –01 Option
2	–12V	–10.5V to –12.0V (⩽100mV ripple)
3	U17	Timebase 10 MHz Sine, moderately distorted
4	Output of Input PCB	OV to +5V Square wave
5	U6 & U16	$\overline{GR}$ +5V to OV pulse
6	U19	GR OV to +5V pulse
7	U8 (1)	Gate time flip-flop $\overline{(GATE)}$ +5V to OV pulse
8	U2	Clock input to sequencer OV to +5V pulses
9	U4 (1)	MSDM flip-flop OV to +5V when MSD ⩾1
10	U23	Display LED segment test ground to test all segments (except decimals)

Table 4-3. MODEL 1900A INTEGRATED CIRCUIT TYPES.

REFERENCE DESIGNATOR	TYPE	REFERENCE DESIGNATOR	TYPE	REFERENCE DESIGNATOR	TYPE
U1	CMOS	U10	CMOS	U19*	TTL
U2*	TTL	U11	CMOS	U20*	TTL
U3*	TTL	U12*	TTL	U21*	TTL
U4	CMOS	U13	CMOS	U22	CMOS
U5	CMOS	U14	CMOS	U23*	TTL
U6	CMOS	U15	CMOS	U24	PMOS
U7	PMOS	U16	CMOS	U25	R
U8*	TTL	U17*	TTL		
U9	CMOS	U18	CMOS		

* For -01 Battery Option, low power TTL devices are being used and consistency should be maintained. See Section 5 for part numbers and serial number effectivity.