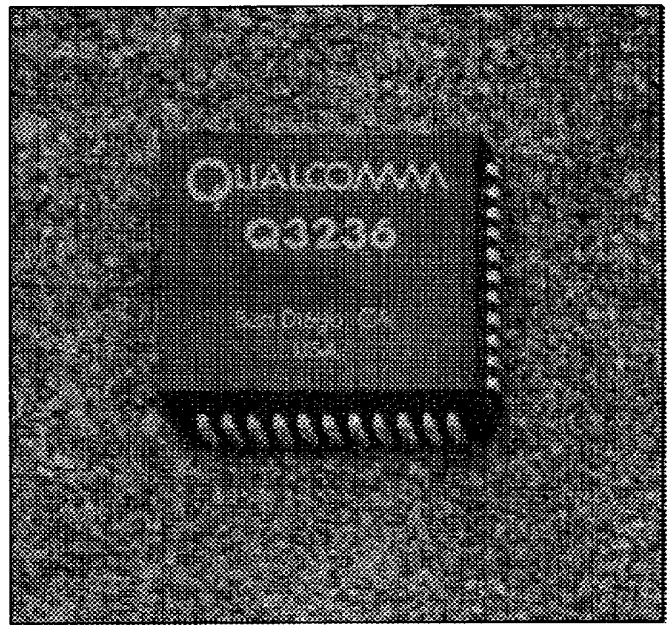
Q3236

PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER



FEATURES

- Backwards Compatible with the Q3036 and Q3216 PLL Chips
- Phase Noise Contributions as Low as -154 dBc/Hz at 100 Hz from Carrier
- < 0.6 W Power Consumption Nominal
- On-chip +10/11 Prescaler
- Single +5 V Supply Operation
- Wide Input Sensitivity Range: -10 to +3.5 dBm
- Programmable via 16 TTL/CMOS-Compatible Parallel Inputs, 8-Bit Data Bus, or Serial Loading
- 100 MHz Phase/Frequency Detector
- High Gain Linearized Phase/Frequency Detector (No Dead Zone): 302 mV/Rad
- Out-of-Lock Indication
- VCO Division Ratios in Unit Steps:
  For Serial and 8-bit Bus Mode:
  2 to 5135 up to 300 MHz or
  90 to 5135 to 2.0 GHz
  For Direct Parallel Mode:
  2 to 1295 up to 300 MHz or
  90 to 1295 to 2.0 GHz
- Reference Division Ratios of 1 to 16 in Direct Parallel Mode, or 1 to 64 in Serial and 8-bit Bus Mode
- Programmability for Faster Multiplexing between Two Pre-loaded Frequencies
- Evaluation Board Available - Q0420

APPLICATIONS

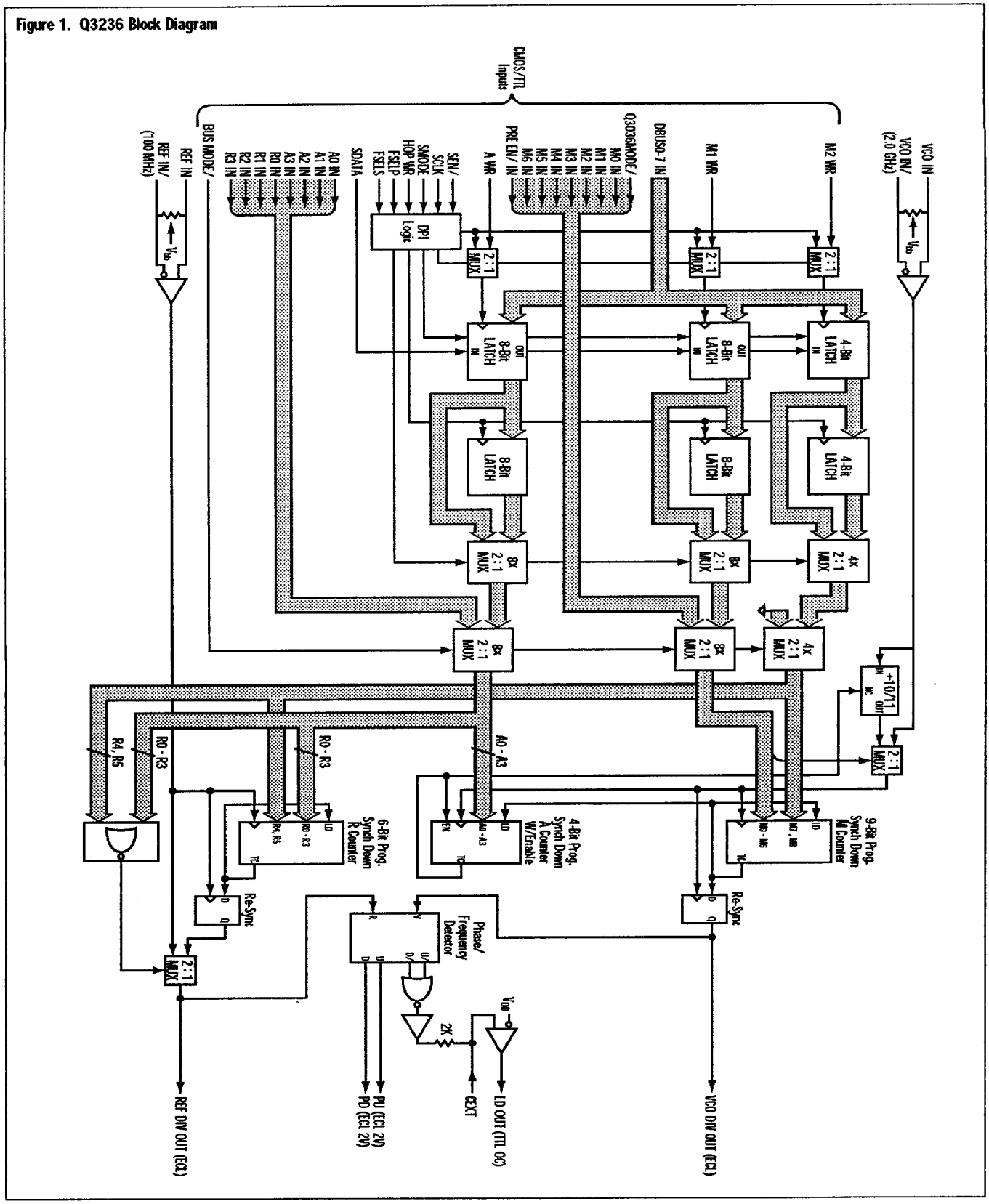
- Cellular Base Stations
- Mobile/Airborne Communications
- Frequency Hopping Systems
- Digital Radios and Modems
- High Performance Test Equipment
- Local Oscillator Generation for VSAT, DBS, and GPS Applications
- RADAR and Missile Local Oscillators
- Paging Systems

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

CONTENTS

Figure 1. Q3236 Block Diagram



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

GENERAL DESCRIPTION

The Q3236 is a low power, single chip solution for Phase-Locked Loop (PLL) Frequency Synthesizers. Requiring only a single +5 V supply, the Q3236 contains all the necessary elements – with the exception of the VCO and loop filter components – to build a PLL frequency synthesizer operating from UHF through L-Band, and is also backwards compatible with the Q3036 and Q3216 devices as a replaceable part.

The block diagram for the Q3236 is shown in Figure 1. Its major components, listed below, are described in detail in the *Functional Overview* section.

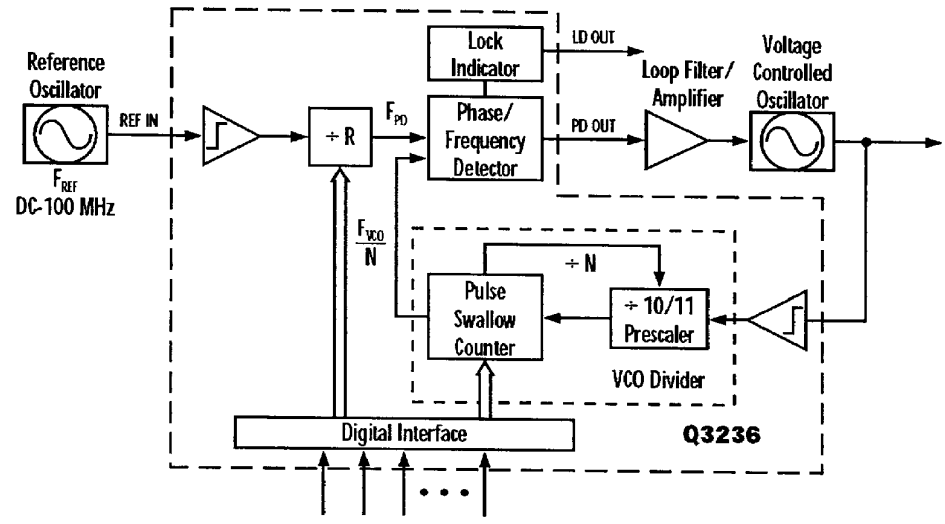
- High Speed Line Receivers
- ÷10/11 Dual Modulus Prescaler
- 9-bit M and 4-bit A Pulse Swallow Counters
- 6-bit Reference Counter
- Digital Phase/Frequency Comparator
- Out-of-Lock Detection Circuitry
- TTL/+5 V CMOS-Compatible Parallel, Serial, or 8-bit Data Bus Interface.

The Q3236 is fabricated using a three metalization layer, single polysilicon oxide-isolated Bi-CMOS process. Its architecture provides breakthrough prescaler performance for high frequency operation, permitting PLL designs with smaller VCO division ratios. The Q3236 design makes possible wider loop bandwidths yielding faster settling times and lower VCO phase noise contributions.

The parallel interface permits hardwiring the Q3236 for applications without the requirement of a processor. The ÷10/11 prescaler can be bypassed selectively to make two divide modes possible. When the ÷10/11 prescaler is enabled, frequency divide ratios can be achieved from 90 to 5135, in unit steps, from DC to 2.0 GHz when operating in Serial or 8-bit Bus Interface Modes. Direct Parallel interface allows divide ratios from 90 to 1295 in unit steps up to 2.0 GHz. In the Non-prescaler Mode, it is possible to divide inputs directly up to 300 MHz by 2 to 512, in unit steps when operating in Serial or 8-bit Bus interface and from 2 to 128 using Direct Parallel interface.

Similarly, the reference counter allows the reference input frequency to be divided directly in ratios of 1 to 64 with the Serial or 8-bit Bus interface and from 1 to 16 using Direct Parallel interface. As shown in Figure 2, the Q3236's highly integrated architecture greatly simplifies the design of UHF through L-Band synthesizers.

Figure 2. Q3236 in a PLL Frequency Synthesizer System



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

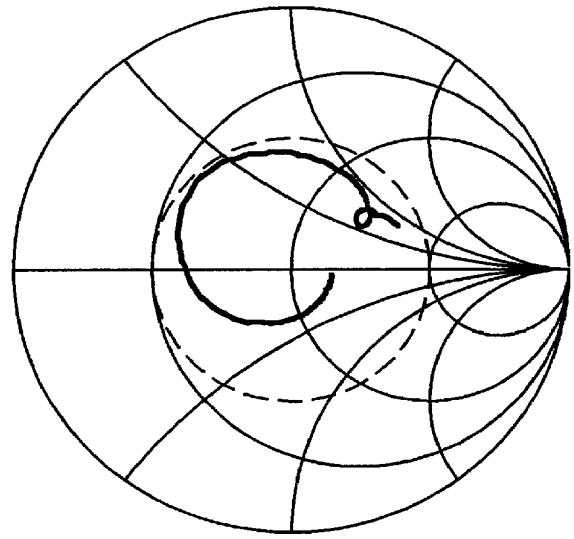
FUNCTIONAL OVERVIEW

DIFFERENTIAL LINE RECEIVERS

The VCO and reference frequency divider chains are clocked by their respective input clock signals, which have been processed by their differential line receivers. The line receiver inputs are externally AC coupled and can be driven differentially or single ended, where the unused input is de-coupled to ground.

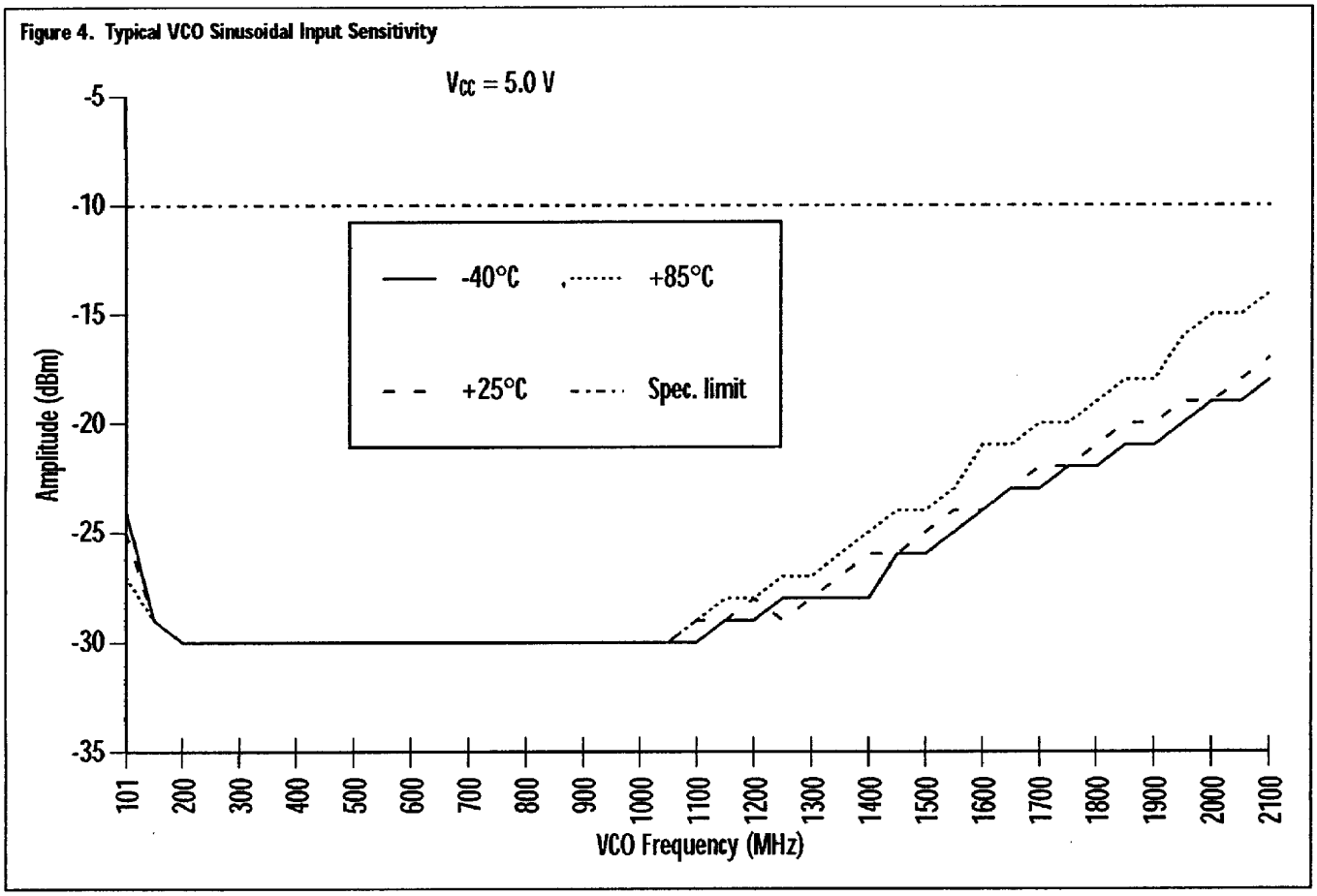
When configured this way, the VCO input has a guaranteed sinusoidal input sensitivity of -10 dBm (200 mV_{P-P} from a 50 Ω source) in the range 20 MHz to 2.0 GHz, and an input VSWR of less than 3:1. Typical VSWR and sensitivity measurements are shown in Figures 3 and 4. They were obtained using the test circuit in Figure 5a. The reference input operates in a similar manner in the range 20 MHz to 100 MHz. Below 20 MHz, square wave signals are recommended (see *Frequency Synthesizer Design Considerations with the Q3236* section).

Figure 3. VCO Sinusoidal Input Reflection Measurement



Note: The circle indicates a constant 3:1 VSWR.

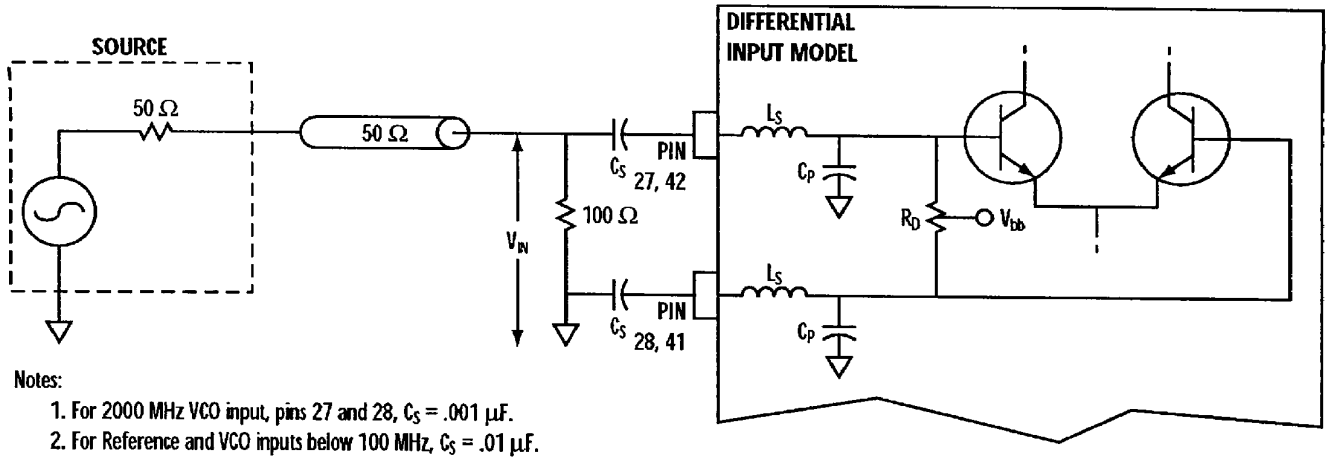
Figure 4. Typical VCO Sinusoidal Input Sensitivity



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

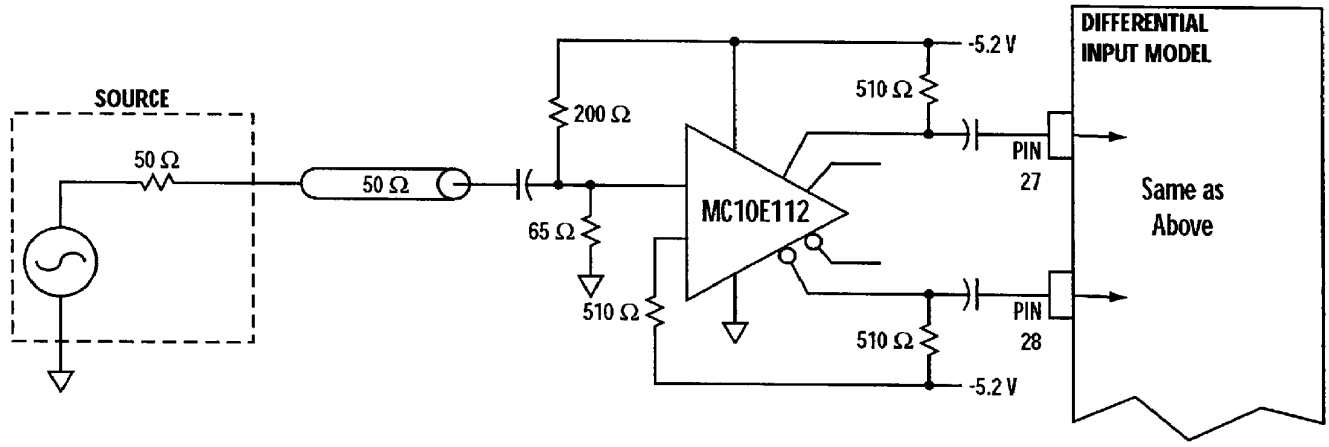
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Figure 5a. VCO Input Sensitivity Measurement Test Circuit - Single-Ended Input



Notes:
1. For 2000 MHz VCO input, pins 27 and 28, C_S = .001 µF.
2. For Reference and VCO inputs below 100 MHz, C_S = .01 µF.

Figure 5b. VCO Input Sensitivity Measurement Test Circuit - Differential (balanced) Input



VCO DIVIDER

The VCO frequency division chain is used to divide the VCO IN (pin 27) frequency, F_{VCO}, down to the phase detector frequency, F_{PD}. It operates in two modes. In the first mode, Prescaler Mode (PRE EN/ = "Low") up to 2.0 GHz, frequency division is accomplished with a pulse-swallow counter made up of the 10/11 front-end dual modulus prescaler (DMP), the 4-bit A counter and the 9-bit M counter. This mode, selected by the pulse-swallow counter, effectively implements a programmable divide-by N counter at the VCO frequency, even though only the DMP is operating at that frequency. The total VCO input frequency division ratio, N, obtained from programming the binary M and A counters is given by:

$$N = F_{VCO}/F_{PD}$$
$$= 10 * (M + 1) + A, \text{ for } A \leq M + 1, M \neq 0 \quad (1)$$

When operating in the Prescaler Mode, programming of control inputs via the 8-Bit Bus or Serial Bus interface utilizes access to all nine M counter bits, M0 - M8, and provides continuous integer divide ratios from 90 to 5135. Programming of control inputs via the Direct Parallel interface does not utilize the M7 and M8 counter bits since these are not provided from external inputs. Therefore, the Direct Parallel Mode allows the resulting 7-bit M counter to provide continuous integer divide ratios from 90 to 1295.

With the M counter set to a binary value of "0", the VCO input division chain is disabled; this, in turn, will cause the phase detector outputs, PD U and

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

PD D, to go to an ECL 2 V "High" and "Low' state, respectively. However, the following non-continuous division ratios in the Prescaler Mode are possible:

N = 20...22, 30...33, 40...44, 50...55, 60...66, 70...77, 80...88.

Given a value for N, the binary values, M and A, are determined as follows:

$$M = \text{integer}\{N/10\} - 1 \quad (2)$$

and

$$A = N - 10 * (M + 1) \quad (3)$$

In the alternate mode, Non-prescaler Mode, (PRE EN/ = "High"), the prescaler is bypassed so that the VCO input frequency is divided directly by the M counter. The counter operates at frequencies up to 300 MHz. In this mode, frequency division ratio is determined by:

$$(F_{VCO}/F_{PD}) = M + 1, M \neq 0 \quad (4)$$

Where M = 1,...,511 is the binary value programmed to the M0 - M8 inputs of the M counter and the values programmed to the A0 - A3 inputs of the A counter are ignored.

As in the previous mode, programming via the 8-Bit Bus or Serial Bus interface will allow divide ratios of 2 to 512, while programming via the Direct Parallel interface will allow divide ratios of 2 to 128. Finally, the output of the VCO frequency division chain is available as the VCO DIV OUT signal (pin 30). It is a pseudo ECL-level emitter follower output, which requires a pull down resistor (between 500 and 1000 Ω typical) and directly interfaces to ECL logic. It is referenced to +5 V and GND. The waveform is a digital pulse with a frequency of F_{PD} and duty cycle of 10/N in Prescaler Mode, and 1/N in Non-prescaler Mode.

REFERENCE DIVIDER

The reference frequency division chain is used to divide the REF IN (pin 42) frequency, F_{REF}, down to the phase detector frequency, F_{PD}, using the 6-bit R counter. The counter operates at frequencies up to 100 MHz and frequency division ratio is determined by

$$(F_{REF}/F_{PD}) = R + 1 \quad (5)$$

Where R = 0,..., 63 is the binary value programmed to the R0 - R5 inputs of the R counter.

As in the case with the VCO Divider, programming of control inputs via the 8-Bit Bus or Serial Bus interface utilizes access to all six R counter bits and permits divide ratios of 1 to 64. Programming of control inputs via the Direct Parallel interface does not utilize the R4 and R5 counter bits since these are not provided from external inputs. Therefore, this allows the resulting 4-bit R counter to provide divide ratios from 1 to 16. The divided result is available at REF DIV OUT (pin 39), and is similar to VCO DIV OUT.

DIGITAL PHASE/FREQUENCY DETECTOR

The Q3236 has a digital phase/frequency detector capable of up to 100 MHz operation and a phase detector gain constant of 302 mV/Rad. This high gain suppresses the active loop filter noise floor. Additionally, the high phase detector gain permits wider loop bandwidths, which yield faster settling times and lower VCO phase noise contributions. The outputs of the VCO and reference frequency divider chains are connected to an internal digital phase/ frequency detector (PFD). The PFD is triggered by the rising edges of these signals and has three outputs. (Refer to Figure 6.)

Two of these outputs make up a double-ended PFD output. The two signals corresponding to this output are PD U OUT (Phase Detector Pulse Up) and PD D OUT (Phase Detector Pulse Down). The first output, PD U OUT (pin 36), pulses "High" approximately 1.9 V when the divided VCO lags behind the divided reference in phase or frequency. The pulse begins at the rising edge of the REF DIV input and is terminated on the rising edge of the divided VCO signal, VCO DIV. Conversely, PD D OUT (pin 37) pulses "High" in the same manner when the divided VCO leads the divided reference in phase of frequency. The pulse begins at the rising edge of the VCO DIV input and terminates on the rising edge of the divided reference signal, REF DIV. Thus, the phase error is encoded as a

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

pulse-width modulated waveform, whose DC average is proportional to its duty cycle which equals the phase error. In typical differential phase detector output applications, PD U OUT is subtracted from PD D OUT in a differential OP-AMP active loop integrator filter, as shown in Figure 13. Therefore, it is only necessary that the differential output power between the two phase detector outputs, PU and PD, be linearly proportionate to the phase difference between the VCO DIV and REF DIV input rising edges. A residual pulse width, t_{RP}, is also added onto both phase detector outputs after the rising edge of the lagging input to mitigate the usual "dead zone" nonlinearity. This works as follows: as long as this residual pulse is kept above a minimum duration, then the phase detector outputs will always reach full amplitude all the way down to zero phase difference, thereby maintaining output power which stays linearly proportionate to the time skew between the phase detector inputs.

The third output, LD OUT (pin 43), is used for an out-of-lock indication. It pulses "Low" when either PD U OUT or PD D OUT is pulsing "High". Lock detection is performed by NORing the phase detector PD U and PD D output signals. The result is a signal which pulses for a duration equal to the time skew between the VCO DIV and REF DIV rising edges. These pulses are integrated with an internal 2K series resistor, and a shunt capacitor connected to the CEXT output (pin 34). When the PLL is out of lock and there is pulsing on the PFD outputs sufficient to bring the voltage on CEXT above an internal comparator threshold, then the open collector output, LD OUT, will turn on, sinking up to 25mA. LD OUT can be wired to an open-collector fault bus or used to drive an LED, indicating an out-of-lock condition. The phase/frequency detector waveforms are shown in Figure 6.

Certain conditions may produce electrical overstress (EOS) to pin 43 and damage the LD OUT. Such an occurance would typically be the result of capacitive discharge with insufficient current limiting resistance with respect to LD OUT and how out-of-lock conditions are indicated within a particular system design. Careful attention to proper current limiting will eliminate any EOS potential.

DIGITAL PROCESSOR INTERFACE (DPI) MODES

The Q3236 can be programmed using one of three operating modes including a Direct Parallel Input Mode, 8-bit Bus Mode, or Serial Bus Mode. All of the DPI data and control inputs operate at either static or low speeds relative to the rest of the device and are to be compatible with CMOS/TTL levels, whose characteristics are described in Table 6. The DPI outputs consist of twenty counter programming bits, M0 - M8, A0 - A3, R0 - R5 as well as the prescaler enable control input, PRE EN/. An Enhanced Operation Mode option for the 8-bit Bus and Serial Bus Modes is provided to enable access to all of these counter programming bits and is described below. A Frequency Multiplexing Mode option for the 8-bit Bus and Serial Bus Modes is also provided to allow rapid toggling between stored programmed frequencies and is described below the following sections of these two respective interface modes.

The interface modes are selected in the following manner: when the external DPI control signal, BUSMODE/(pin 22), is "High", the DPI is in the Direct Parallel Mode. When the BUSMODE/ input is "Low", the DPI is in either the 8-bit Bus or Serial Bus Mode, depending on the "Low" or "High" state, respectively, of the SMODE input (pin 21). Serial Mode addressing is accomplished in a standard fashion using three signals: SDATA, SCLK, and SEN/. DPI Mode selection is summarized in Table 1. In order to consolidate the utility of as many of the package pins as possible, most of the CMOS/TTL inputs are multi-functional as denoted in Figure 10. This is possible because some of the DPI Modes and the inputs are mutually exclusive. Internally, these differing control signal inputs are logically OR'ed to avoid contention.

Table 1. Digital Processor Interface (DPI) Mode Selection

BUSMODE/ INPUT	SMODE INPUT	DPI MODE
LOW	LOW	8-BIT BUS
LOW	HIGH	SERIAL BUS
HIGH	X	DIRECT PARALLEL INPUT

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

ENHANCED OPERATION or Q3036 MODE

An enhanced operation mode control signal, Q3036 MODE/(pin 44), is referenced after QUALCOMM's original single-chip PLL, the Q3036. It allows the Q3236 to maintain identical DPI Modes and divider ratios as the Q3036 for backwards compatibility, or be set for expanded divider capability and DPI operation. When the Q3036 MODE/ input is "High", this enables access to all twenty counter programming bits for operation only in the 8-bit Bus or Serial Bus Modes if the additional M7, M8 or R4, R5 counter bits are required for larger division ratios. This allows for programmability to the full range of divider ratios as described in the *Functional Overview* section under the *VCO Divider* and *Reference Divider* subsections.

When the Q3036 MODE/ input is "Low", all of the counter programming bits except M7, M8, R4, and R5 are available in all three interface modes, with a corresponding reduction in the available range of divider ratios as mentioned in the previous section. When operating with Q3036 MODE/ set "Low", the M7, M8, R4, and R5 inputs are set internally to the "Low" state. This allows any previously designed synthesizer circuits using the Q3036 to be directly replaced with the Q3236 device.

Additionally, all external CMOS/TTL inputs will register as a "High" or "Low" state when left floating, according to the "Low" or "High" state of the Q3036 MODE/ input, respectively. This however, means that when operating in 8-bit Bus Mode or Serial Bus Mode when pin 44 is tied "Low", the FSELP and FSELS inputs (pins 18 and 16, respectively) must also be tied "Low" so that the data loaded into the primary registers can remain inactive until after the HOP WR input is asserted. (See section under *8-bit Bus or Serial Bus Frequency Multiplexing: Ping-Pong Mode* for further details.)

DIRECT PARALLEL INPUT MODE

With the BUSMODE/ input set "High" and the Q3036 MODE/ input set "Low", all of the DPI outputs except M7, M8, R4, and R5 are taken directly from external inputs, as listed in the pin assignment/ descriptions in Table 8J. Referring to the Q3236 Block Diagram (Figure 1), BUSMODE/ is really the select input to a row of 20 x 2:1 MUXes. Each of the inputs are connected to the external inputs, with the exception of the M7, M8, R4, and R5 signals. This mode allows the device to be hardwired for fixed frequency phase-locked oscillators as well as parallel-loaded fast frequency hopping applications.

8-BIT BUS MODE

With the BUSMODE/ input "Low" and the SMODE input "Low", the 8-bit Bus Mode is selected and the external DBUS0-7 inputs are latched into one of the three primary registers, with the A WR, M1 WR, or M2 WR external control inputs according to the timing requirements shown in Figure 8. In the 8-bit Bus Mode, the interface is double-buffered consisting of a set of primary registers and secondary registers. The primary registers are programmed in parallel fashion without affecting the inputs to the counters. The contents from the primary registers are loaded into the secondary registers on the rising edge of the HOP WR input and are then immediately available to the counters and prescaler as DPI outputs. The DPI outputs are simply the secondary register outputs. A mapping of the DBUS0-7 inputs to the primary registers for all twenty counter programming bits is shown in Table 2, and listed in the pin assignment/ descriptions in Table 8H. Note however, that when operating in the 8-bit Bus Mode and the Q3036 Mode (pin 44 tied "Low"), it is necessary to also tie "Low" the R2 and R3 external reference counter inputs (pins 4 and 5, respectively) in order for the 8-bit bus to program correctly. This requirement is due to the DBUS0-1 inputs sharing the R2-3 input pads which automatically register to the opposite logic state of pin 44 when left floating. A failure to set pins 4 and 5 "Low" when operating this way will result in the internal M0-1 and A0-1 programming counter bits being stuck in a logic "High" condition.

SERIAL BUS MODE

With the BUSMODE/ input "Low" and the SMODE input "High", the Serial Bus Mode is selected and data is shifted serially into the SDATA input on the

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Table 2. 8-bit Bus Mode Primary Register Map

EXTERNAL INPUT	INTERNAL PRIMARY REGISTER MAPPING		
	A WR RISING EDGE	M1 WR RISING EDGE	M2 WR RISING EDGE
DBUS0	A0	M0	M7
DBUS1	A1	M1	M8
DBUS2	A2	M2	R4
DBUS3	A3	M3	R5
DBUS4	R0	M4	N/A
DBUS5	R1	M5	N/A
DBUS6	R2	M6	N/A
DBUS7	R3	PRE EN/	N/A

rising edge of the SCLK input, while the active "Low" shift enable control input, SEN/, is "Low". In the same manner as the 8-bit Bus Mode, the interface is double-buffered consisting of a set of primary registers and secondary registers. The data for all twenty counter programming bits is shifted into the primary registers in accordance to the sequence shown in Table 3, starting with R5 and ending with A0. When operating in the Q3036 Mode (pin 44 tied "Low"), all twenty serial data bits still need to be shifted into the SDATA input even though the M7-8 and R4-5 counter bits cannot be utilized. In this case, a logic "0" should be used for the first four data bits of the SDATA input. The contents from the primary registers are shifted into the secondary registers on the rising edge of either the SEN/ input or the HOP WR input asserted according to the timing requirements shown in Figure 9, and are then immediately available to the counters and prescaler as DPI outputs. A list of the respective Serial Bus Mode pin assignment/ descriptions is shown in Table 8I.

8-BIT BUS OR SERIAL BUS FREQUENCY MULTIPLEXING: PING-PONG MODE

The Ping-Pong Mode is a subset of both the 8-bit Bus and Serial Bus Modes which enables the Q3236 to be multiplexed between two pre-loaded frequencies for applications involving random frequency hopping, low-data-rate FSK modulation, or half-duplex transceiving operation using a single synthesizer. ATE system environments requiring multiple frequencies also use fast switching synthesizers to greatly increase system throughput, and they are increasingly being used as the reference oscillator in commercial Magnetic Resonance Imaging (MRI) systems. In either interface mode, this is carried out by toggling between two different VCO division ratios in the primary and secondary registers, since the counter programming bits in the primary registers may be updated while the ones in the secondary registers are controlling the programmable divider.

The so-called "ping-pong" frequency selection is controlled by the external input signal, FSELP in the 8-bit Bus Mode, and FSELS in the Serial Mode.

As noted in the 8-bit Bus Mode subsection, after the DBUS0-7 inputs are latched into the three primary registers, they are then only loaded into the secondary registers after the HOP WR input is asserted. This means that the contents of the primary registers can be updated with a new frequency word while the

Table 3. Serial Mode Data Programming Sequence

BIT NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SDATA INPUT	R5	R4	M8	M7	PRE EN/	M6	M5	M4	M3	M2	M1	M0	R3	R2	R1	R0	A3	A2	A1	A0

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

secondary registers retain control of the DPI outputs with the previously loaded data. An external frequency multiplexing control input, FSELP (pin 18), enables the device to be toggled between these two pre-loaded frequencies as noted in the pin assignment/ descriptions, Table 8H. When the FSELP input is "High", the synthesizer output frequency is obtained from the frequency word stored in the primary registers, and when the FSELP input is "Low", the output frequency is obtained from the frequency word stored in the secondary registers. The DPI outputs are simply the multiplexed output of either the primary or secondary register outputs selected by the control signal FSELP.

As noted in the *Serial Bus Mode* subsection, after the data for all twenty counter programming bits is shifted into the primary registers, they are then only loaded into the secondary registers after the SEN/ and HOP WR inputs are asserted. In the same manner as in the 8-bit Bus Mode, an external frequency multiplexing control input, FSELS (pin 16), enables the device to be toggled between these two pre-loaded frequencies as noted in the pin assignment/ descriptions in Table 8I. The synthesizer output frequency is simply the multiplexed output of either the primary or secondary register outputs selected by the "High" or "Low" state, respectively, of the control signal FSELS.

For Q3236 implementation using the Ping-Pong Mode for FSK modulation of the synthesizer's output, the data rate limitation of the loop will be a function of the natural frequency, ω_n, since a second-order PLL is able to track for phase and frequency modulations of the reference signal as long as the modulation frequencies remain within an angular frequency band roughly between zero and ω_n. When using the Ping-Pong Mode for a frequency hopping synthesizer, or as a transmit and receive synthesizer for half-duplex operation, the synthesizer's switching speed performance, otherwise known as it's settling time characteristics, will essentially govern the achievable switching or hop rate, although the 20-bit load period for the respective interface mode used should also be taken into account.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

TECHNICAL SPECIFICATIONS

Tables 1 through 4 contain technical specifications for the Q3236 PLL. Figures 6, 8 and 9 contain timing specifications for the Q3236. Figure 7 shows the typical Q3236 supply current as a function of V_{CC} and temperature.

Stresses above those listed in this Absolute Maximum Ratings table may cause permanent and functional damage to the Q3236 device. This is a stress rating only. Functional operation of the Q3236 at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect Q3236 reliability.

Table 4. Absolute Maximum Ratings: Q3236I-20N

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	T_{STO}	- 55	+ 150	°C	–
Junction Temperature	T_J	- 55	+ 150	°C	–
Supply Voltage (Relative to V_{EE})	V_{CC}	–	+ 7.0	V	–
Voltage on Any Non Differential Input Pin (Relative to V_{EE})	V_{IN}	- 0.5	V_{CC} + 0.5	V	–
Continuous Output Current	I_{OUT}	25	–	mA	1
Surge Output Current	I_{OUT}	200	–	mA	1
AC Coupled Voltage on Any Differential Input	V_{IN}	–	1275	mV_{PP}	–
Bipolar Latchup Insensitivity	I_{TRIG}	± 100	–	mA	2
ESD Protection	V_{ESD}	± 2000	–	V	3

Notes:

1. ECL and ECL 2V outputs terminated with 510 Ω to V_{EE}.
2. Method meets the intent of JEDEC STD 17 Publication. This is the maximum allowable current flow through the input and output protection diodes.
3. Method meets the intent of MIL-STD-883, Method 3015.

Table 5. Operating Conditions

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Operating Ambient Temperature	T_A	-40	–	+85	°C	–
Operating Voltage (Relative to V_{EE})	V_{CC}	+4.5	–	+5.5	V	–
Junction to Case Resistance	θ_{JC}	–	19	–	°C/W	1
Junction to Ambient Resistance	θ_{JA}	–	51	–	°C/W	2

Notes:

1. θ_{JC} measured with package held against an "infinite" heatsink test condition.
2. θ_{JA} measured in still-air, room temperature test condition.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

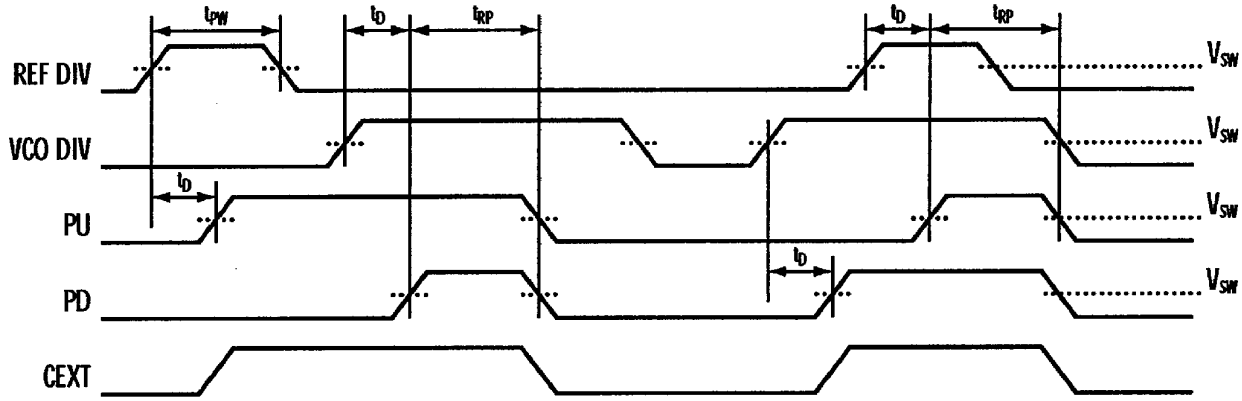
Table 6. DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
ECL "High" Output Voltage	V_{OH}	V_{CC} - 1150	V_{CC} - 850	mV	1
ECL "Low" Output Voltage	V_{OL}	V_{CC} - 2030	V_{CC} - 1620	mV	1
ECL 2V "High" Output Voltage	V_{OH}	V_{CC} - 1150	V_{CC} - 650	mV	1
ECL 2V "Low" Output Voltage	V_{OL}	V_{CC} - 3250	V_{CC} - 2610	mV	1
CEXT "High" Output Voltage	V_{OH}	V_{CC} - 1150	V_{CC} - 700	mV	2
CEXT "Low" Output Voltage	V_{OL}	V_{CC} - 2100	V_{CC} - 1500	mV	2
Open Collector "Low" Output Voltage	V_{OL}	–	500	mV	3
Open Collector "High" Output Current	I_{OL}	-2	+2	µA	4
CMOS/TTL "High" Input Current	TTL I_{IH}	+225	+400	µA	5
CMOS/TTL "Low" Input Current	TTL I_{IL}	-100	0	µA	6
CMOS/TTL "High" Input Voltage	V_{IH}	2.0	–	V	7
CMOS/TTL "Low" Input Voltage	V_{IL}	–	0.800	V	7
Q3036 MODE/ "High" Input Current	Q3036/ I_{IH}	+400	+800	µA	8
Q3036 MODE/ "Low" Input Current	Q3036/ I_{IL}	-400	-200	µA	9
Supply Current (V_{CC} - V_{EE})	I_{CC}	–	160	mA	10

Notes:

1. Outputs terminated through 510 Ω to V_{EE}.
2. Outputs measured directly with no termination resistance.
3. While open collector output is sinking 20 mA.
4. V_{CC}* = +5.5 V, V_{OUT} = V_{CC} - 10 mV.
5. V_{CC}* = +5.5 V, V_{IN} = V_{CC} - 10 mV, Input Q3036 MODE/ = "V_{EE}".
6. V_{CC}* = +5.5 V, V_{IN} = V_{EE} + 10 mV, Input Q3036 MODE/ = "V_{EE}".
7. All CMOS/TTL inputs will register as a "High" or "Low" state when left floating, according to the "Low" or "High" state of the Q3036 MODE/ input, respectively.
8. V_{CC}* = +5.5 V, V_{IN} = V_{CC} - 10 mV.
9. V_{CC}* = +5.5 V, V_{IN} = V_{EE} + 10 mV.
10. V_{CC}* = +5.5 V (ECL, ECL 2 V Outputs terminated through 510 Ω to V_{EE}.
    *All V_{CC} values relative to V_{EE}.

Figure 6. Phase/Frequency Detector Waveforms

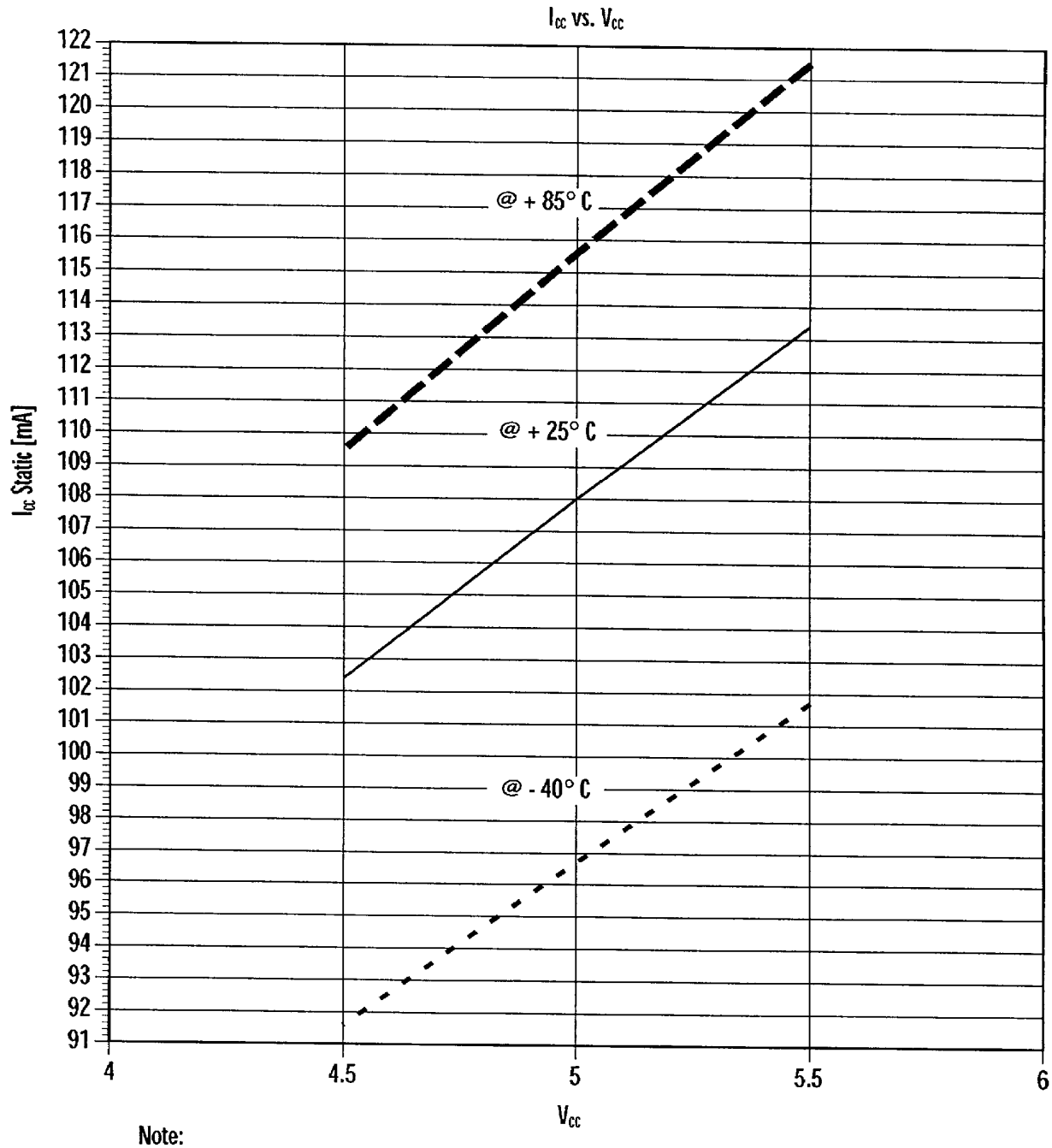


Note: V_{SW} is the CML logic voltage located at the 50% level between V_{OH} and V_{OL}.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 7. Typical I_{CC} (Static) vs. V_{CC}



Note:

All measurements conducted with Q3036 MODE/ (pin 44) tied "High", no termination resistance on any outputs, and all inputs left open (internally pulled down).

Table 7. AC Electrical Specifications

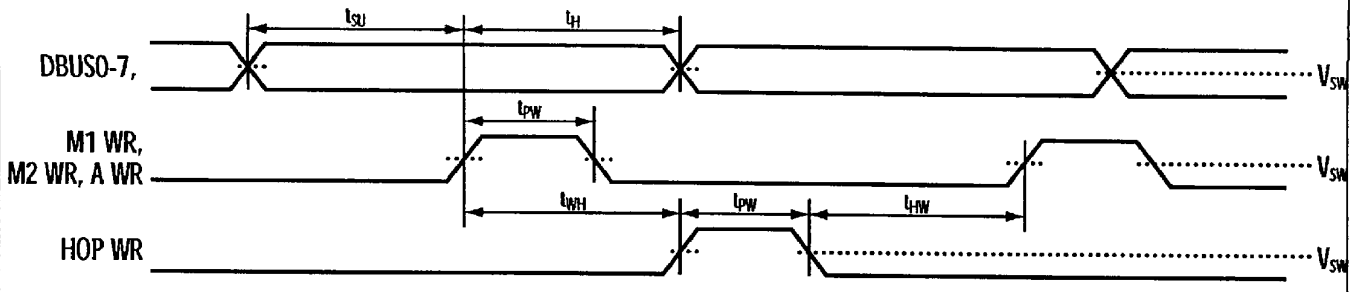
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
VCO IN, REF IN Differential Inputs Sinusoidal or Square Wave Input Sensitivity Input VSWR	V_{IN}	200 (-10)	950 (+3.5) 3:1	mVpp dBm	
VCO IN Frequency Range	F_{VCO}	20	2000	MHz	1, 2, 3
REF IN Frequency Range	F_{REF}	20	100	MHz	1, 2
10/11 Prescaler Frequency	F_P	20	2000	MHz	1, 2
M Counter Frequency	F_M	20	300	MHz	1, 2
A Counter Frequency	F_A	20	182	MHz	1, 2
R Counter Frequency	F_R	20	100	MHz	1, 2
Phase Detector Input Pulse Width, REF DIV, VCO DIV	t_{PW}	4	–	ns	6
Phase Detector Output Residual Pulse Width	t_{RP}	3.2	–	ns	5, 6
Phase Detector Propogation Delay	t_D	–	2.5	ns	5, 6
DBUS0-7 Valid to M1 WR, M2 WR, A WR Rising	t_{SU}	50	–	ns	4
DBUS0-7 Valid after M1 WR, M2 WR, A WR Rising	t_H	50	–	ns	4
SDATA Valid to SCLK Rising	t_{SU}	50	–	ns	4
SDATA Valid after SCLK Rising	t_H	50	–	ns	4
SEN/ Setup to SCLK Rising	t_{SU}	50	–	ns	4
SEN/ Hold after SCLK Rising	t_H	50	–	ns	4
SCLK, M1 WR, M2 WR, A WR Rising to HOP WR, SEN/ Rising	t_{WH}	50	–	ns	4
Pulse Width SCLK, M1 WR, M2 WR, A WR, HOP WR, and SEN/	t_{PW}	50	–	ns	4
HOP WR Rising to SCLK, M1 WR, M2 WR, A WR Rising	t_{HW}	0	–	ns	4
CMOS/TTL Input Capacitance	C_{IN}	–	2	pF	7

Notes:

1. For square wave inputs with edge rates of at least 200mV/25ns, there shall be no lower frequency limit.
2. Per input loading of Figure 5a.
3. The Q3236I-20N will operate up to 2200 MHz typical with $0 \leq T_A \leq 70°C$ and $4.75 \leq V_{CC} \leq 5.25$ V.
4. Timing is referenced at the CMOS/TTL input logic voltage switching threshold.
5. Outputs PD D, PD U loaded per Figure 21.
6. Timing is referenced at the 50% level between V_{OH} and V_{OL}.
7. Guaranteed by design; not tested in production.

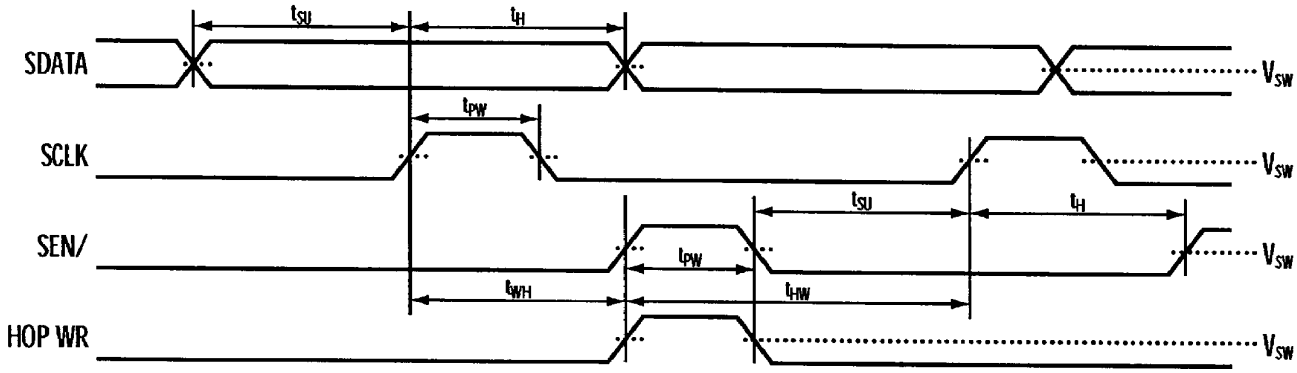
QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Figure 8. Bus Mode Interface AC Timing Waveforms



Note: V_{SW} is the CMOS/TTL INPUT logic voltage switching threshold.

Figure 9. Serial Mode Interface AC Timing Waveforms



Note: V_{SW} is the CMOS/TTL INPUT logic voltage switching threshold.

INPUT/OUTPUT SIGNALS

Figure 10 provides the pin configuration of the Q3236 PLL package and Tables 8-17 provide summaries of the input/output signal pin assignments.

Figure 10. Q3236 44-pin Configuration

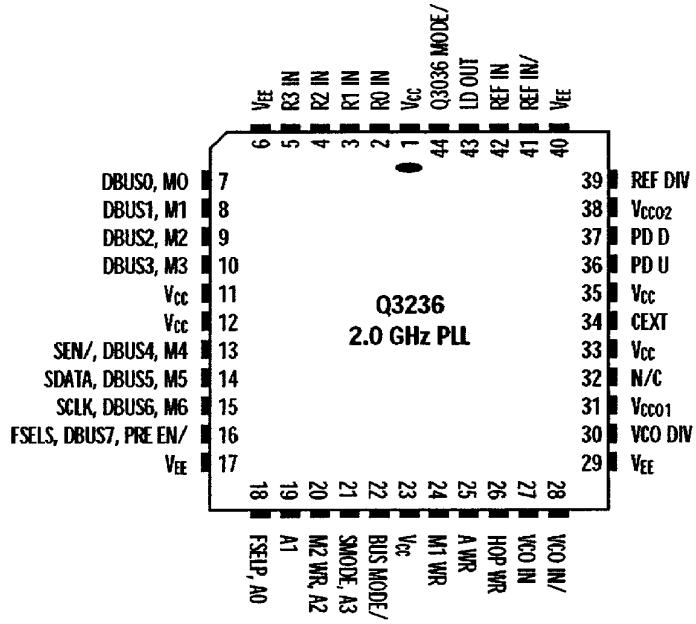


Table 8. Differential Line Receiver Input Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
VCO IN	27	Differential INPUT	VCO Driven Differential Input
VCO IN/	28	Differential INPUT	VCO Driven Complimentary Differential Input
REF IN	42	Differential INPUT	Reference Driven Differential Input
REF IN/	41	Differential INPUT	Reference Driven Complimentary Differential Input

Table 9. Enhanced Operation Mode Control Input Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
Q3236 MODE/	44	V_{CC}/V_{EE} INPUT	Q3036 MODE. When configured "Low" (V_{EE}), internal M-Counter Bits [8:7] and R-Counter Bits [5:4] set to logic "0". External CMOS/TTL inputs "pulled up" internally through > 50 kΩ resistors. When configured "High" (V_{CC}), internal M-Counter Bits [8:7] and R-Counter bits [5:4] programmable in Serial or 8-bit Bus Mode. External CMOS/TTL inputs "pulled down" internally through > 50 kΩ resistors.

Table 10. Divider Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
VCO DIV	30	ECL 100 k OUTPUT	VCO Divided Output. Provides output with frequency equal to VCO IN frequency divided by VCO IN division ratio.
REF DIV	39	ECL 100 k OUTPUT	Reference Divided Output. Provides output with frequency equal to REF IN frequency divided by REF IN division ratio.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Table 11. Phase Detector Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
PD U	36	ECL 2 V 100 k OUTPUT	Phase Detect Pulse "Up". Pulses "High" when VCO DIV lags REF DIV.
PD D	37	ECL 2 V 100 k OUTPUT	Phase Detect Pulse "Down". Pulsed "High" when VCO DIV leads REF DIV.

Table 12. Phase Lock Detect Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
LD OUT	43	TTL Open Collector	Lock Detect. High impedance during phase-locked operation, low impedance during phase unlocked operation.
CEXT	34	Series 2 k ECL OUTPUT	C EXTERNAL. OR'd output of PD and PU provided by 100 k ECL emitter follower terminated through 2 k, on chip, series resistance. External attachment of 0.1 µF capacitor acts to low pass filter OR'd output of PD and PU signals. Output drives inverting differential input of on-chip comparator used for switching LD OUT.

Table 13. Unconnected Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
–	32	N/C	Unconnected Pin

Table 14. Voltage Supply Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
V_{CC}	1, 11, 12, 23, 33, 35	Power	Core Circuitry V_{CC} POWER SUPPLY
V_{CCO1}	31	Power	Output Drivers V_{CC} POWER SUPPLY for VCO DIV OUT and CEXT
V_{CCO2}	38	Power	Output Drivers V_{CC} POWER SUPPLY for PD U OUT, PD D OUT and REF DIV OUT
V_{EE}	6, 17, 29, 40	Power	V_{EE} POWER SUPPLY

Table 15. Digital Processor Interface (DPI) 8-bit Bus Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
BUSMODE/	22	CMOS/TTL INPUT	BUSMODE. Used with SMODE to select one of three possible DPI modes of operation.
SMODE	21	CMOS/TTL INPUT	SMODE. Selects SERIAL BUS MODE (BUSMODE/ "Low", SMODE "High") or 8-bit BUS MODE (BUSMODE/ "Low", SMODE "Low")
DBUS7-DBUS0	16 (MSB), 15, 14, 13, 10, 9, 8, 7 (LSB)	CMOS/TTL INPUT	DATA BUS bit 7 (MSB) - DATA bus bit 0 (LSB)
M1 WR	24	CMOS/TTL INPUT	M1 WRITE. Rising edge active. Latches DATA BUS bits [7:0] (PRE EN/ and M[6:0]) to primary register.
M2 WR	20	CMOS/TTL INPUT	M2 WRITE. Rising edge active. Latches DATA BUS bits [3:0] (R[5:4] and M[8:7]) to primary register.
A WR	25	CMOS/TTL INPUT	A WRITE. Rising edge active. Latches DATA BUS bits [7:0] (R[3:0] and A[3:0]) to primary register.
HOP WR	26	CMOS/TTL INPUT	HOP WRITE. Rising edge active. Latches primary register data previously latched with M1 WR, M2 WR, and A WR, to secondary register.
FSELP	18	CMOS/TTL INPUT	Provides option of selecting DPI information stored in primary registers (FSLEP = "1") or secondary registers (FSELP = "0").

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Table 16. Digital Processor Interface (DPI) Serial Bus Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
SDATA	14	CMOS/TTL INPUT	SERIAL DATA. Data is shifted serially into input SDATA on rising edge of SCLK signal.
SEN/	13	CMOS/TTL INPUT	SHIFT ENABLE. Active "Low" for SERIAL DATA loading with input SDATA. Also latches primary registers SERIAL DATA into secondary registers. SEN/ or HOP WR must be asserted "High" when loading SERIAL DATA to secondary registers.
SCLK	15	CMOS/TTL INPUT	SHIFT CLOCK. Rising edge active. Shifts serial data into input SDATA with each rising edge (SEN/ = "Low").
HOP WR	26	CMOS/TTL INPUT	HOP WRITE. Rising edge active. Latches primary registers SERIAL DATA into secondary registers. SEN/ or HOP WR must be asserted "High" when loading SERIAL DATA to secondary registers.
FSELS	16	CMOS/TTL INPUT	Provides option of selecting DPI information stored in primary registers (FSELS = "1") or secondary registers (FSELS = "0").

Table 17. Digital Processor Interface (DPI) Direct Parallel Input Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
M[6:0]	15 (MSB), 14, 13, 10, 9, 8, 7 (LSB)	CMOS/TTL INPUT	M-COUNTER BITS 6 (MSB) - 0 (LSB)
A[3:0]	21 (MSB), 20, 19, 18 (LSB)	CMOS/TTL INPUT	A-COUNTER BITS 3 (MSB) - 0 (LSB)
R[3:0]	5 (MSB), 4, 3, 2 (LSB)	CMOS/TTL INPUT	R-COUNTER BITS 3 (MSB) - 0 (LSB)
PRE EN/	16	CMOS/TTL INPUT	PRESCALER ENABLE. Enables Divide-by 10/11 Prescaler (Active "Low")

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Figure 11a. Output Spectrum - Spurious

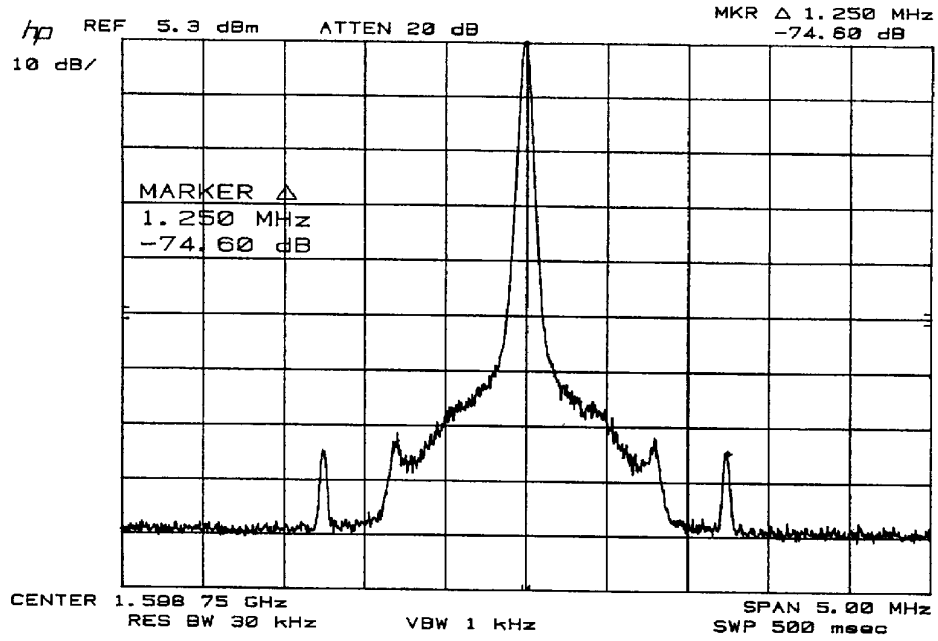
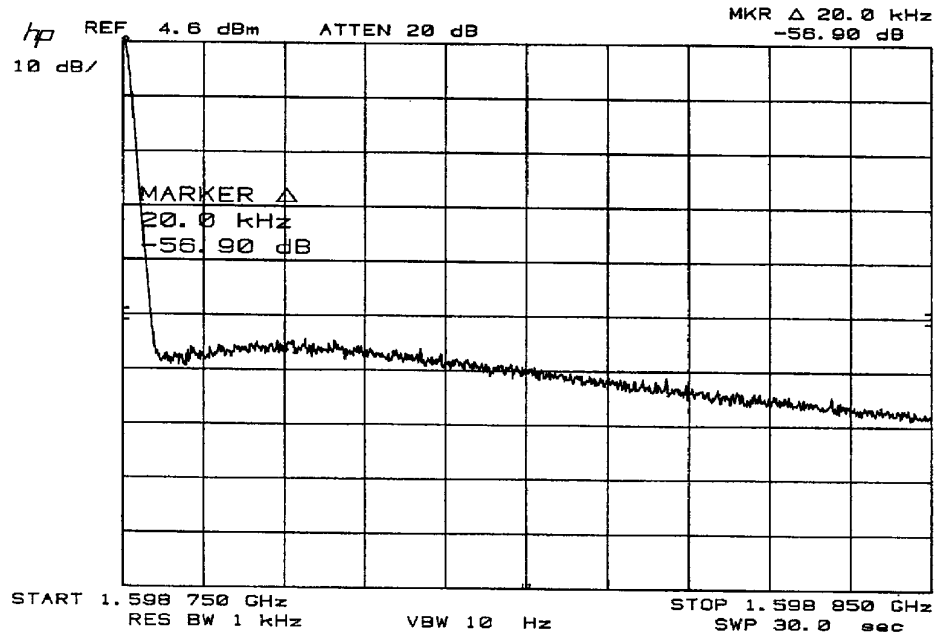


Figure 11b. Output Spectrum - Phase Noise



APPLICATION INFORMATION

GENERAL

A high performance frequency synthesizer can be designed by connecting loop filter components, a VCO and reference oscillator to the Q3236.

As a sample application, a PLL frequency synthesizer can be designed to generate output frequencies from 900 to 1600 MHz in 1.25 MHz steps while phase locked to a 10 MHz reference oscillator input. The 1.25 MHz frequency step size requires a phase detector comparison frequency, F_{PD} = 1.25 MHz. See Figure 11 for output spectrum.

The following sections describe how to connect the Q3236 for this application, calculate the R, M and A values for programming the Q3236, construct the active loop filter, and analyze loop stability. Refer to Figures 12, 13, and 14.

VCO/REFERENCE INPUT CONNECTIONS

When using a single-ended input signal, VCO IN (pin 27) is AC-coupled with a high frequency 1000 pF capacitor. The other input, VCO IN/(pin 28), is AC-coupled to ground in the same manner as shown in Figure 5a. Because the input impedance between the two is approximately 80 Ω plus reactance, an external shunt 100 Ω input termination resistor matches the input to a 50 Ω source as shown in the measured plot of Figure 3. If the VCO is in close proximity to the PLL chip, the 100 Ω terminating resistor may not be necessary if the connecting trace is short enough not to warrant transmission line design considerations. In a balanced 50 Ω configuration, both double-ended VCO outputs should be AC-coupled to pins 27 and 28. An example of implementing a differential input signal is shown in Figure 5b. Additionally, the output noise performance can sometimes be improved by experimenting with lower values for the AC-coupling capacitors to pins 27 and 28. The idea here is that smaller-value caps will effectively differentiate the signal into VCO IN thereby providing a modicum of high pass filtering and improved lower frequency noise immunity.

PROGRAMMING THE BINARY COUNTERS

For a synthesizer output frequency of F_{VCO} = 1598.75 MHz, the total divide ratio is:

$$N = F_{VCO}/F_{PD} = 1598.75/1.25 = 1279 \quad (6)$$

The binary values in which to program the binary R, M and A counters are given by:

$$R = (F_{REF}/F_{PD}) - 1 = 7$$
(R0 to R2 = "High"; R3 to R5 = "Low" (7)

$$M = \text{Integer}\{N/10\} - 1 = 126$$
(M0 = "Low"; M1 to M6 = "High"; M7, M8 = "Low" (8)

$$A = N - (10 * (M + 1)) = 9$$
(A1, A2 = "Low"; A0, A3 = "High") (9)

CALCULATING LOOP FILTER COMPONENT VALUES

Figure 12 shows a block diagram of a PLL feedback control system.

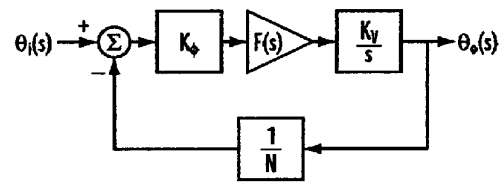
A second order type II PLL has two perfect integrators (poles on the imaginary axis). The tuning voltage-to-frequency conversion of the VCO implements integration with respect to phase, and the other integrator is obtained with the active loop filter shown in Figure 13 whose transfer function is given by:

$$F(s) = \frac{(1 + s * T_2)}{s * T_1} \quad (10)$$

The transfer function of output phase to input phase in terms of frequency is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{N * (1 + s * T_2)}{\frac{s^2 * N * T_1}{K_V * K_\phi} + s * T_2 + 1} \quad (11)$$

Figure 12. Second Order Type II PLL



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Where K_V (Rad/V) is the VCO tuning sensitivity, K_ϕ(V/Rad) is the phase detector gain constant, N is the VCO-to-phase detector comparison frequency divide ratio and:

$T_1 = R_1 * C$ and $T_2 = R_2 * C$

are time constants based on the active loop filter components.

Using standard control theory, this can be rewritten as:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{N * (1 + s * T_2)}{\frac{s^2}{\omega_n^2} + \frac{2 * s * \zeta}{\omega_n} + 1} \quad (12)$$

Where the "natural frequency", ωn and damping factor, ζ are given by:

$$\omega_n = \sqrt{\frac{K_V * K_\phi}{N * T_1}} \quad (13)$$

and

$$\zeta = \frac{\omega_n * T_2}{2} \quad (14)$$

For this application,

$K_V = 2 * \pi$ (80 MHz/V), VCO specification

$K\phi$ = 0.302 V/Rad

ω_n and ζ are usually constrained by the noise performance, stability, and settling time requirements of the loop.

In this example,

$\omega_n = 2 * \pi *$ 20kRad/s (F_n = 20 kHz)

and

ζ = 0.85.

These values correspond to the synthesizer output at 1600 MHz, or N = 1280.

If C is chosen to be 4700 pF, then R_1 and R_2 are left to be calculated from:

$$R_1 = \frac{K_V * K_\phi}{\omega_n^2 * N * C} = 1598\ \Omega \quad (15)$$

and

$$R_2 = \frac{2 * \zeta}{\omega_n * C} = 2878\ \Omega \quad (16)$$

Figure 13a. Active Loop Filter Circuit - Loop Filter

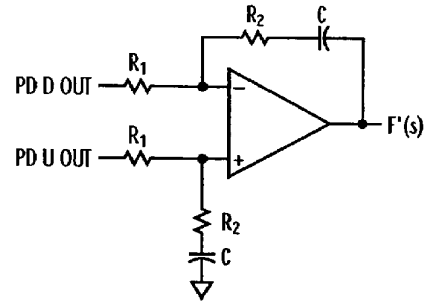


Figure 13b. Active Loop Filter Circuit - Modified Loop Filter with Pre-Integrator

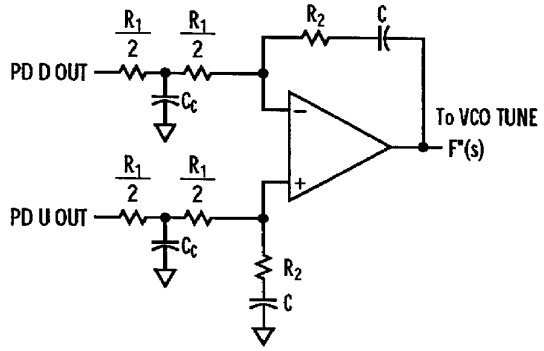
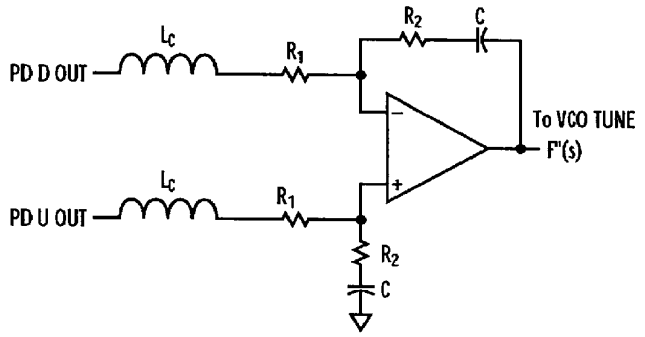


Figure 13c. Active Loop Filter Circuit - Alternative Loop Filter with Pre-Integrator



LOOP STABILITY ANALYSIS

There are many different methods of analyzing the stability of feedback control networks. The approach used here is to derive the total open loop transfer function of the network and perform a Bode analysis. The open loop transfer function of the PLL with an ideal loop filter with no other delays, T(s), is given by:

$$T(s) = \frac{K_V * K_\phi * F(s)}{N * s} \quad (17)$$

Substituting (10) for F(s), $s = j\omega$ and converting to magnitude and phase,

$$|T(j\omega)|^2 = \frac{(K_V * K_\phi/\omega * N)^2 * (1 + \omega^2 * T_2^2)}{\omega^2 * T_1^2} \quad (18)$$

and

$$\angle T(j\omega) = -180 + \tan^{-1}(\omega * T_2) \quad (19)$$

In a Bode analysis, the phase margin is the difference between -180 degrees and the phase angle of $T(j\omega)$ at the frequency where $|T(j\omega)|$ is equal to unity. Although a phase margin greater than zero theoretically yields a stable loop, it is desirable to have at least 40° of phase margin to limit "peaking" in the frequency response and "ringing" in the transient response of the loop. In the example, evaluating (18) and (19) yields a phase margin of 71.6° at a unity magnitude frequency of 35.5 kHz.

It is important to note that the above results apply strictly to the ideal second order type 2 loop. However, a practical design has op-amp finite gain/bandwidth effects, additional poles and zeros for filtering, and other delays in the loop. If these additional effects are neglected during the analysis, the consequences can be severe.

Therefore, the following sections have been included to describe many of these additional effects, to re-analyze loop stability and to analyze closed loop frequency response.

OP AMP FINITE GAIN/BANDWIDTH

The open loop transfer function, (17), includes an ideal loop filter with a perfect integrator, which implies an op-amp with infinitely large signal voltage gain and bandwidth. The open-loop response of a typical op-amp is predominantly described by:

$$A_0(s) = \frac{A_0}{1 + s * T_0} \quad (20)$$

Where T_0, the dominant pole, is given by:

$$T_0 = \frac{A_0}{2 * \pi * GBW} \quad (21)$$

The large signal voltage gain, A_o, and the gain-bandwidth product, GBW, are specified in the op-amp manufacturer's data sheets. For this implementation, we use OP-27 whose A_0 and GBW specifications are $2 * 10^6$ and 8 MHz respectively.

With the op-amp response taken into account, the loop filter transfer function becomes:

$$F''(s) = \frac{(1+s * T_2)}{s * T_1 + [1+s(T_1+T_2)](1+s * T_0)/A_0} \quad (22)$$

Further evaluation of (22) reveals that the finite gain and bandwidth of the op-amp effectively add another pole to the loop filter response (the PLL overall open loop transfer function). The frequency of this pole is reduced by the amount of gain required of the op-amp (R_2/R_1 feedback ratio). However, for a given amount of gain, the pole is farther out for an op-amp with a higher GBW. Depending on the gain of the loop filter and the op-amp GBW, this significantly impacts the phase margin of the loop and (22) should be used in the stability analysis. In some very wide loop bandwidth applications, it may be necessary to take the higher order op-amp poles into account.

PRE-INTEGRATOR FILTERING

The Q3236 digital phase detector supplies error information by generating pulses at the reference frequency with a duty cycle proportional to the phase error. Voltage offsets between the phase detector and VCO – caused by component mismatches, op-amp input offsets, or other imbalances – are transformed into a steady state phase-error. This results in error pulses of large amplitude and short duration that contain high power at many harmonics of F_{PD}. The active loop filter is being relied on to filter linearly the DC averages of these pulses. However, high frequency, large amplitude signals on the inputs of an op-amp can cause non-linear saturation in the amplifier, greatly reducing its GBW. This effect can be devastating to wide-bandwidth PLLs.

One solution is to pre-filter the error pulses before they reach the active filter by inserting an RC lowpass section by splitting R_1. The modified loop filter with the "pre-integrator" filter is shown in Figure 13b. The addition of this circuit adds another pole, which can potentially degrade the phase margin. The time

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

constant, T_C, and frequency, F_C, of the pole are given by:

$$T_C = \frac{R_1 * C_C}{4} \quad (23)$$

and

$$F_C = \frac{1}{2 * \pi * T_C} \quad (24)$$

The loop filter transfer function with the pre-integrator pole included is given by

$$F''(s) = \frac{(1 + s * T_2)/(1 + s * T_C)}{s * T_1 + 2[1 + s(T_1/2 + T_2)](1 + s * T_0)/A_0} \quad (25)$$

The pole should be placed far enough below the reference frequency to pre-filter the phase detector pulses enough to keep the op-amp response linear and attenuate the reference spurs on the synthesizer output, while keeping it far enough above ω_n so as not to degrade the phase margin. A rule of thumb is to place F_C greater than 10 times F_n. Accordingly, we set C_C = 2000pF. However, this imposes a degradation in phase margin.

Another possible solution for pre-integrator filtering is to use a series LR section in place of the RC type previously described. This alternative scheme is shown in Figure 13c. Like with the RC type pre-integrator filter, the addition of this circuit adds a pole which can potentially degrade the phase margin. The time constant, $T_{C'}$, and frequency, $F_{C'}$, of the pole are given by:

$$T_{C'} = \frac{L_C}{R_1} \quad (26)$$

and

$$F_{C'} = \frac{1}{2 * \pi * T_{C'}} \quad (27)$$

The loop filter transfer function with the series LR pre-integrator pole included is given as follows:

$$F''(s) = \frac{(1+s * T_2)/(1+s * T_{C'})}{s * T_1+[1 + s(T_1+T_2)]*(1 + s * T_0)/A_0} \quad (28)$$

All related design guidelines apply as with the RC type pre-integrator filter scheme.

DIGITAL PHASE DETECTOR SAMPLING DELAY

In the above analysis, the frequency divider and phase detector were treated as constant, linear gain elements (1/N and K_ϕ, respectively) with no frequency response. In fact, there is a finite propagation delay through the counters that implement the frequency divider. In the frequency domain, this fixed time delay corresponds to a phase shift which increases linearly with frequency.

Similarly, the digital phase detector responds to the edges of the frequency-divided reference and VCO signals. Thus, it cannot be treated in a continuous-time fashion. There is an inherent sampling delay of one-half the period of the phase comparison frequency. Generally, this delay is at least an order of magnitude greater than the frequency divider delay. Therefore, the divider delay may be neglected.

Because the phase error is encoded using pulse-width modulation, there is an associated output spectrum, with a DC component equal to the duty cycle of the pulse or phase error. If the higher frequency components of the output are neglected, the phase detector is modeled with a linear transfer function of

$$K_\phi'(s) = K_\phi * e^{-|s/(2 * F_{PD})|} \quad (29)$$

Which contributes a phase delay of:

$$\angle K_\phi'(\omega) = \frac{\omega}{2 * F_{PD}} \quad (30)$$

Where F_{PD} is the phase detector comparison frequency and K_ϕ is the phase detector gain constant.

ADDITIONAL REFERENCE SUPPRESSION FILTERING

The higher frequency components of the phase detector output pulses have the effect of modulating the VCO at the harmonics of F_{PD}, creating sidebands on the synthesizer output known as "reference spurs". The pre-integrator filtering can help reduce these spurs to meet very low spurious requirements. But it may be necessary to include a higher degree of filtering. This increases attenuation at the phase comparison frequency, F_{PD}, while maintaining low insertion phase and loss down inside the loop bandwidth so as not to degrade the phase margin.

One example is the LC low-pass filter network, shown in Figure 14.

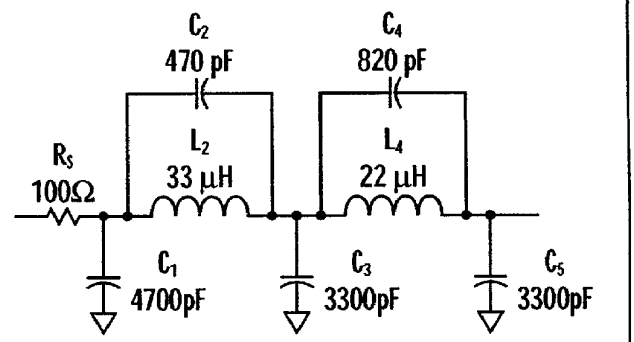
The voltage transfer function of this network is:

$$F_R(s)^{-1} = \left(1 + \frac{s^2 * L_4 * C_5}{1 + s^2 * L_4 * C_4}\right) * \left(1 + \frac{s^2 * L_2 * C_3}{1 + s^2 * L_2 * C_2}\right) * (1 + s * C_1 * R_S) + \left(\frac{s^2 * L_2 * C_5}{1 + s^2 * L_2 * C_2}\right) * (1 + s * C_1 * R_S) + \left(1 + \frac{s^2 * L_4 * C_5}{1 + s^2 * L_4 * C_4}\right) * (s * C_3 * R_S) + (s * C_5 * R_S) \quad (31)$$

A series 100Ω resistor at the output of the op-amp establishes the source resistance. The filter drives the varactor tuning network of the VCO, which is modeled as a low value shunt capacitance. The filter is singly terminated, driving a high impedance.

A high ripple (reflection coefficient = 50%) Cauer-Chebyshev response is selected from a filter design handbook (e.g., Handbook of Filter Synthesis) to yield a steep rolloff. This allows placement of the cutoff frequency very near F_{PD} to keep the poles far away from the loop bandwidth and to minimize their impact on the phase margin. The high ripple is not detrimental as long as the response is flat down in the PLL loop bandwidth.

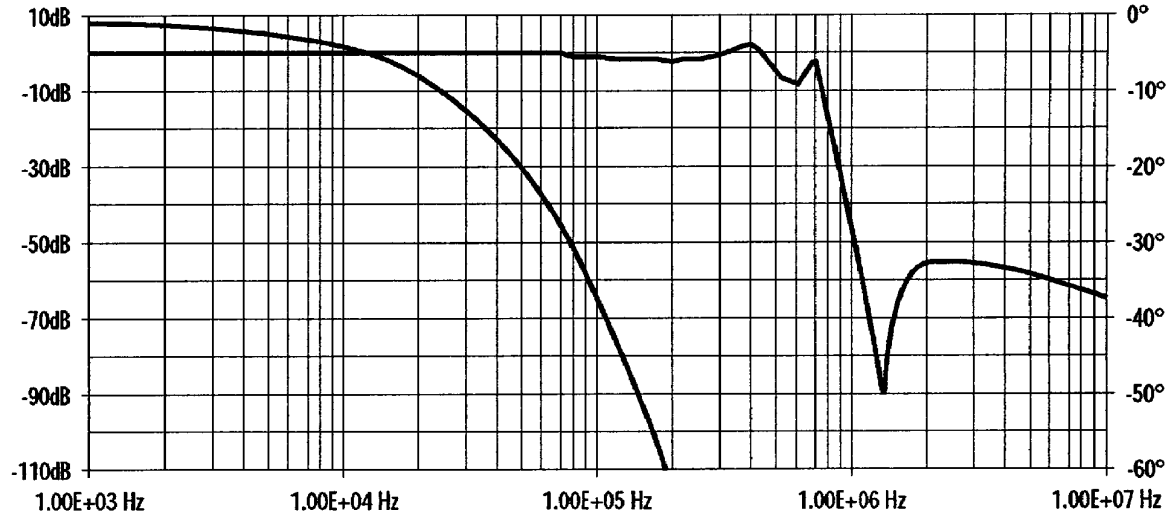
Figure 14. Reference Suppression Filter



Finally, the frequency of the transmission zeros are adjusted (by changing C_2 and C_4) in such a way as to create a wide "notch" response at F_{PD} = 1.25 MHz and the rest of the filter was optimized to use standard component values.

The filter's resulting voltage transfer function magnitude and phase response vs. frequency, shown in Figure 15, indicate an insertion phase of -14° at 35.5 kHz, and a -90 dB notch at 1.25 MHz. In practice, the filter achieves about 60 dB of attenuation, due to limitation of the Q-value of the practical filter

Figure 15. 1.25 MHz Reference Suppression Filter Voltage Transfer Characteristics



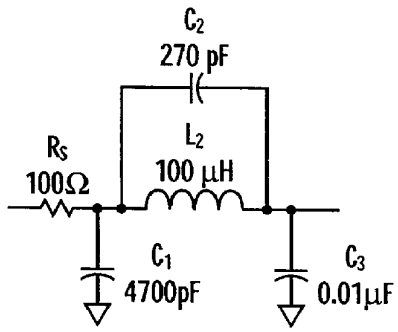
QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

components and physical layout.

The parallel-resonant LC tanks, which make the transmission zeros, are inherently high impedances at the notch frequency and without proper shielding, can actually pick up switching noise at the notch frequency via RF-coupling.

A 3-pole elliptic filter designed to suppress reference energy from an F_{PD} = 1 MHz is shown in Figure 16. Using the same source and termination impedance as in the previous example, this simpler topology allows direct scaling of component values to accommodate sideband suppression for different phase comparison frequencies, albeit with somewhat less attenuation effect and reduced phase margin than the 5-pole design.

Figure 16. 1 MHz 3-pole Reference Suppression Filter



STABILITY ANALYSIS (REVISITED) AND CLOSED LOOP RESPONSE

The stability analysis is repeated, calculating the unity gain frequency, F_0 dB, of the open loop transfer function, T(s), and evaluating the phase margin, ϕ_m, at that frequency for loops which include the effects described above. Also evaluated is the closed loop frequency response in terms of the total open loop gain and loop divisor, N, given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{T(s)}{[1 + T(s)/N]} \quad (32)$$

Peaking in the closed loop response is defined as the ratio of its maximum magnitude to its magnitude at DC. However, the DC value of the open loop response is equal to N:

$$\frac{\theta_o(DC)}{\theta_i(DC)} = N \quad (33)$$

Thus,

$$\text{Peaking} = 20 * \log \left[\frac{\max \left\{ \frac{\theta_o(s)}{\theta_i(s)} \right\}}{N} \right] \quad (34)$$

In general, as the phase margin decreases, the peaking in the closed loop response increases.

The phase margin and closed loop frequency response are evaluated for five different cases. These cases begin with the ideal second order type II loop, $T_1(s)$, then cumulatively add the effects to the op-amp finite gain/bandwidth, $T_2(s)$, pre-integrator filter pole, $T_3(s)$, phase detector sampling delay, $T_4(s)$, and reference suppression filter, $T_5(s)$.

The results are shown in Table 18 and plotted in Figures 17 and 18 for two cases of loop divisors:

N = 1280 (F_{VCO} = 1600 MHz)

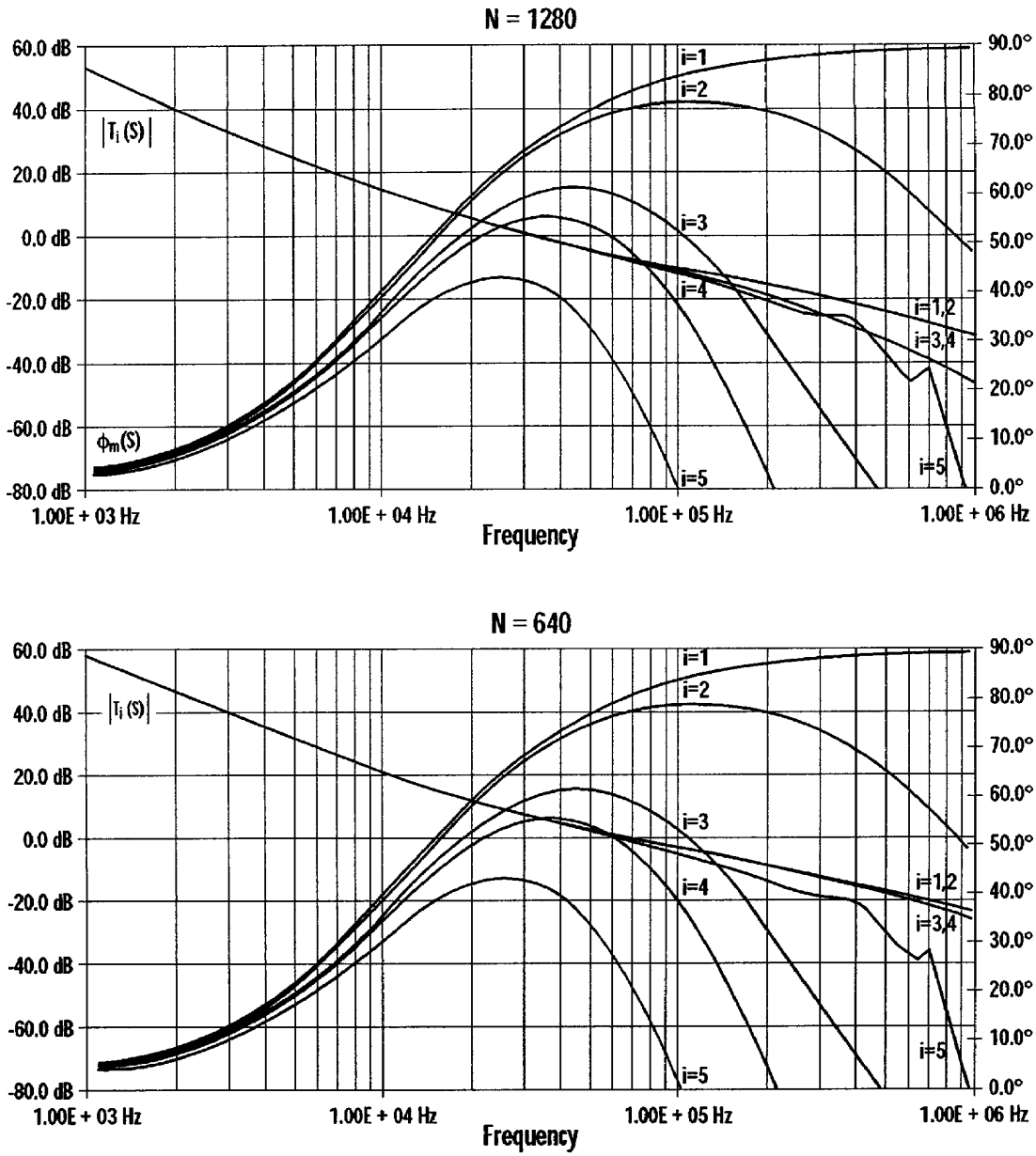
Table 18. Phase Margin vs. Loop Configuration

EXPRESSION	DESCRIPTION	N	F_0 dB	ϕ_m	PEAKING
$T_1(s) = \frac{K_V * K_\phi * F(s)}{N * s}$	Standard 2nd Order Type II Loop	1280	35.6 kHz	71.7°	1.5 dB
	$\omega_n = 2\pi * 20$ kRad/s, $\zeta = 0.85$	640	69.0 kHz	80.3°	1.0 dB
$T_2(s) = \frac{K_V * K_\phi * F'(s)}{N * s}$	Adds Op-amp Characteristics	1280	35.6 kHz	70.0°	1.6 dB
	$A_o = 2\times10^6$, GBW = 8 MHz	640	68.5 kHz	77.0°	1.1 dB
$T_3(s) = \frac{K_V * K_\phi * F''(s)}{N * s}$	Adds Pre-integrator Capacitor	1280	35.0 kHz	60.4°	1.9 dB
	C_C = 2000 pF	640	65.0 kHz	59.35°	1.3 dB
$T_4(s) = \frac{K_V * K'_\phi(s) * F''(s)}{N * s}$	Adds PFD Sample Delay	1280	35.0 kHz	55.3°	2.1 dB
	$K'_\phi(s)$	640	65.0 kHz	50.1°	1.7 dB
$T_5(s) = \frac{K_V * K'_\phi(s) * F''(s) * F_R(s)}{N * s}$	Adds Reference Suppression Filter	1280	34.5 kHz	41.5°	3.2 dB
	Response, $F_R(s)$	640	62.5 kHz	26.5°	7.4 dB

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 17. Bode Analysis - Open Loop Gain and Phase Margin



and, N = 640 (F_{VCO} = 800 MHz)

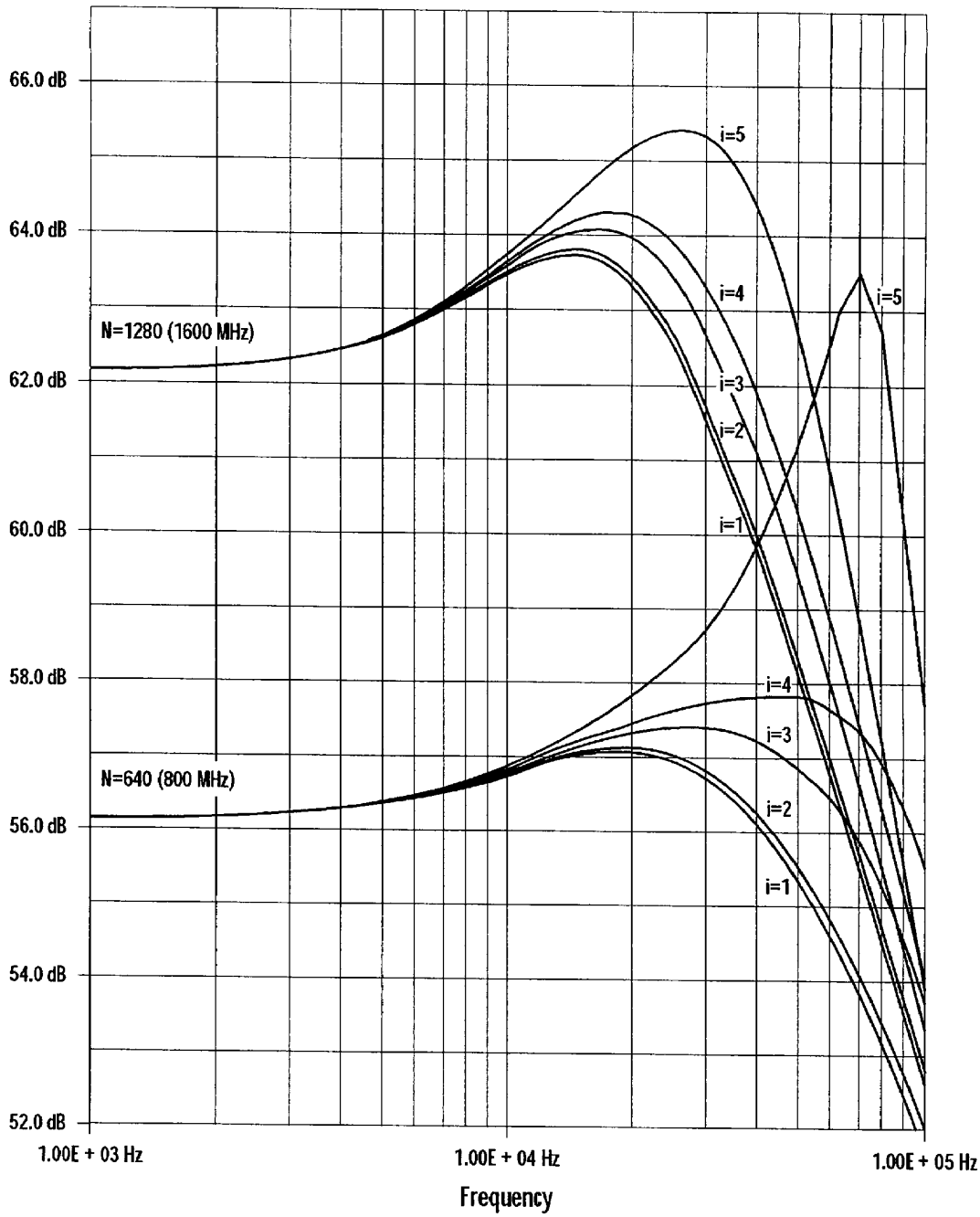
First, at the lower end of the synthesizer output frequency range, 800 MHz, N decreases by a factor of 2 to 640. On inspecting (13) and (14) it is clear that both ω_n and ζ increase by a factor of $\sqrt{2}$. A recollection of servo theory on a second type II loop suggests that an increase in damping always improves the phase margin and, hence, the stability of the loop. The results show that for this ideal case the phase margin increases from ϕ_m = 71.7° at F_0 dB = 35.6 kHz at N = 1280 to ϕ_m = 80.3° at F_0 dB = 69.0 kHz at N = 640. As expected, the peaking drops from 1.5 dB to 1.0 dB.

For the case of $T_2(s)$, the op-amp finite gain/bandwidth effects degrade the phase margin by 1.7°, where ϕ_m = 70.0° for N = 1280. Where N = 640, the phase margin is degraded by 3.3° with ϕ_m = 77.0°.

With the incorporation of the pre-integrator filter,

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 18. Closed Loop Frequency Response



the results for $T_3(s)$ show a more pronounced impact on the phase margin and peaking.

When the phase detector sampling delay is added, it is evident that although it does not effect the magnitude of the open loop gain, $|T_4(s)|$, the phase margin is degraded by the added phase delay of 9.4° at the unity gain frequency, F_0 dB = 65.0 kHz, for N = 640, and 5.1° at F_0 dB = 35.0 kHz, for N = 1280.

Up to this point, the results of this example have indicated that although the added poles and delays have begun to impact the phase margin and induce peaking in the closed-loop frequency response, the loop is still behaving approximately like the second order loop in that for the larger ω_n and ζ in the N = 640 case,

the phase margin and peaking are less. This is due to the fact that up to this point, the pole and zero of the loop filter, $R_1 * C$ and $R_2 * C$, are still dominating the response.

However, this is not the general case. For example, if the loop bandwidth were higher, it would require more gain out of the op-amp (larger R_2/R_1 ratio), and the op-amp pole would be more dominant. Also, the pre-integrator pole and detector sampling delays would be relatively higher and thus have more impact.

Finally, the results show that by adding the reference suppression filter in T_5 (s), the impact on the phase margin and peaking is quite severe in both cases, $\phi_m = 41.5°$ for N = 1280, and $\phi_m = 26.5°$ for N = 640.

It is extremely important to note that the impact is more pronounced for the case N = 640 (see Figure 18). This is significant in that it contradicts the results of the second loop theory. This is caused by the loop no longer approximating the second order loop. In fact, the higher order effects cause the natural loop bandwidth and damping to lose their meaning in terms of loop stability.

Although the phase margin of 41.5° at F_{VCO} = 1600 MHz (N = 1280) is still acceptable, the results at N = 640 pose a few problems when operating at the frequency F_{VCO} = 800 MHz.

First, the low phase margin of 26.5° is not enough to allow for component tolerances and drift due to age, temperature, etc. Therefore, under some conditions the loop could become unstable and lose lock completely.

Also, the high amount of peaking (7.4 dB) in the closed loop response corresponds to a higher "overshoot" in the transient response of the loop. For the loop to remain linear in operation, the VCO must have a wider tuning range, and the loop amplifier must have a wider dynamic range in order to accommodate for this overshoot.

Finally, this excessive peaking in the loop frequency response amplifies both the VCO and reference phase noise contributions at frequency offsets where the peaking occurs. Therefore, it can heavily degrade the expected phase noise performance at those frequencies.

In summary, the results show that the cumulative effects of all these additional factors greatly degrades the stability when compared with an ideal second order loop. Therefore, a different design approach is in order when operating over the entire frequency range F_{VCO} = 800 -1600 MHz. For example, using a reference suppression filter technique which has less insertion phase, such as a third order LC, or a twin T notch at 1.25 MHz would reduce its insertion phase delay, although it may require in-circuit tuning to achieve adequate rejection. Alternatively, the effect of decreasing N in the loop gain could be equalized by non-linearizing the VCO tuning sensitivity over the frequency range.

SYNTHESIZER OUTPUT SPECTRUM

Figure 11a shows the output spectrum of a synthesizer programmed to 1598.75 MHz (N = 1279) at a span of 5 MHz, indicating the 1.25 MHz reference spurious outputs are less than -74 dBc.

At frequency offsets less than the loop bandwidth, the synthesizer output phase noise consists of the reference phase noise, the Q3236 frequency divider/ phase detector noise floor and the op-amp active loop filter's noise, all multiplied up by the loop divisor:

$$N = 1279 \text{ or } 20 * \log10(N) = 62 \text{ dB}$$

Figure 11b shows the synthesizer output phase noise measured in a 1 kHz bandwidth at frequency offsets up to 100 kHz. The plot shows that at a 20 kHz offset, the output phase noise is about -87 dBc/Hz. The Q3236 phase noise contribution at that offset is less than or equal to :

$$-87 - 62 = -149 \text{ dBc/Hz @ 20 kHz}$$

The Q3236 PLL is an ECL device. This calculation substantiates a phase noise floor of an ECL device to be > -150 dBc.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

FREQUENCY SYNTHESIZER DESIGN CONSIDERATIONS WITH THE Q3236

GENERAL ELECTROMAGNETIC ISSUES

Proper power supply biasing and grounding are critical to the design of frequency synthesizers for high performance communications systems. Power supply and digital bus noise can couple into the PLL circuitry and degrade phase noise performance. Additionally, PLL divider switching noise and phase detector pulses coupling onto power supply lines can create EMI problems and couple into high-gain/wideband IF amplifier chains.

The Q3236 offers some key advantages in these areas due to its highly integrated architecture. In the Q3236 synthesizer, all the high speed digital circuitry is confined to a small area and the internal logic is implemented with lower bias currents due to a high f_t process, and uses fully differential CML circuits. Both of these features reduce the amount of switching noise on the power supply inputs. This can be compared with a discrete, distributed design which has long circuit traces carrying fast switching logic signals requiring special terminations. The discrete approach also allows a greater opportunity for picking up external noise which can degrade the synthesizer's phase noise performance. The Q3236 architecture and pinout are optimized for simple and compact external circuit layout which aids in these issues. However, there are still some important guidelines to follow.

When programming a PLL synthesizer using a digital microprocessor bus, it is desirable to isolate the bus from the frequency divider/phase detector circuitry because it is usually switching all the time and can add noise to the synthesizer. If, for instance, the HOP WR, M1 WR, M2 WR, and AWR signals are being controlled by logic that is very noisy or perhaps goes to a high impedance state when the signals are de-selected, the connecting traces can easily pick up extraneous signals which RF-couple to the output and become another component of low-level additive phase noise. The data bus inputs can also be susceptible in this way. One way to mitigate this so called noise feedthru effect is to put high-frequency bypass capacitors, such as 100 pF value, right at the PLL control interface pins in question. In this way, maximizing the noise immunity will help in achieving optimum phase noise results. The Q3236 bus interface is double-buffered, which aids in this isolation. Also, the device pinout is configured so that all the digital inputs are on one side of the package, allowing partitioning between the digital *and* analog portions of the printed circuit board layout.

Additionally, the Q3236 contains on-chip bandgap voltage referencing which is effective for filtering noise below approximately 30 kHz when the power supply requirement of V_{CC} = +5.0 ± 0.5 V is met. To limit the AM to PM conversion phase noise at higher frequencies, it is essential to add external power supply filtering.

First, the V_{CC} inputs should each be bypassed to ground with about a 0.01 µF capacitor. To simplify circuit layout, these pins can be connected together underneath the Q3236 package on the PWB. The +5 V can run off of the same +5 V logic supply; but depending on the level and frequencies of switching noise on that supply, it may be desirable to insert a series RF choke before the V_{CC} inputs, which can handle 75 mA.

For optimal synthesizer noise performance, it is recommended to use a linear regulated power supply to eliminate any contribution of extraneous noise coupling through the power bus lines to the synthesizer's output.

The phase detector outputs should be considered separately. There are five emitter follower outputs on the Q3236: the VCO divider output, VCO DIV OUT, the Lock Detect integrated output, CEXT, the double-ended phase detector outputs, PD U OUT and PD D OUT, and the reference divider output REF DIV OUT. The outputs have separate supply rails brought off of the Q3236. Specifically, V_{CCO1} is the VCO DIV OUT and CEXT supply rail and V_{CCO2} is the supply rail for PD U OUT, PD D OUT and REF DIV OUT. These outputs are each externally terminated to ground with 510 Ω (except CEXT) and therefore draw 9 mA from its supply rail. Since REF DIV OUT and VCO DIV OUT are brought off-chip with their own output drivers, they can be used to drive AC-coupled 50 Ω test and measurement equipment or, of course, into other ECL

logic. It is sometimes useful to shift CEXT's internal out-of-lock threshold closer to either the ECL 2 V "High" or "Low" state in order to establish a more consistent threshold to trigger LD OUT between unlocked and locked conditions, depending on the response of the integrated waveform on CEXT. This is done by connecting a resistor (typical values between 20 kΩ to 50 kΩ) from the CEXT output to either +5 Volts or ground, depending on which direction of bias is desired.

Because emitter follower outputs are always "On", any power supply ripple or switching noise on the supply rail goes directly through to the phase detector output and therefore can increase the phase noise and spurious output of the synthesizer. Furthermore, the phase detector outputs convey phase error information in the form of very narrow 2 V pulses. If not dealt with, these pulses bleed into the power supply and corrupt the system. If REF DIV OUT or VCO DIV OUT are only going to be used as a test point for high impedance probing, such as for monitoring the pulse-train waveform with an oscilloscope probe, then these outputs can be externally terminated with a higher value resistor, such as 10 KΩ. This can benefit in a couple of ways, especially for very densely populated circuit layout conditions. First, it reduces the current draw of either output from 9 mA to under 0.5 mA Secondly, it will cause a lower level of signal current to radiate which reduces another additive component to potentially degrade the output phase noise.

Therefore, it may be necessary to connect the phase detector supply rail, V_{CCO2}, to a separate, well-filtered supply. The filtering should consist of a 0.01 µF bypass capacitor followed by a ladder of series inductor and shunt capacitor elements whose values can effectively filter the frequencies. For instance, inductors of 100 µH combined with 47 µF electrolytic capacitors effectively filter noise in the tens of kHz but are not effective at higher frequencies. At these higher frequencies, 0.01 µF capacitors along with ferrite beads are effective.

Finally, ground plane construction is very important. Its quality directly impacts the effectiveness of the filtering/bypassing techniques. By taking advantage of the Q3236 pinout arrangement, and using surface mount components on a two-layer printed circuit board, it is possible to achieve a virtually solid ground plane under the device. The ground plane can also be utilized to act as a coaxial-like shield to prevent parallel-line coupling between the VCO input and the digital input traces. Coupling of this kind can degrade VCO input VSWR and EMI immunity which can be detrimental to the synthesizer's noise performance. Surrounding the VCO input trace with a "shield plane" of copper on the top layer, connected to the ground plane with a row of vias, should provide such a shielding effect.

VCO AND REFERENCE LINE RECEIVER INPUT MINIMUM EDGE RATES

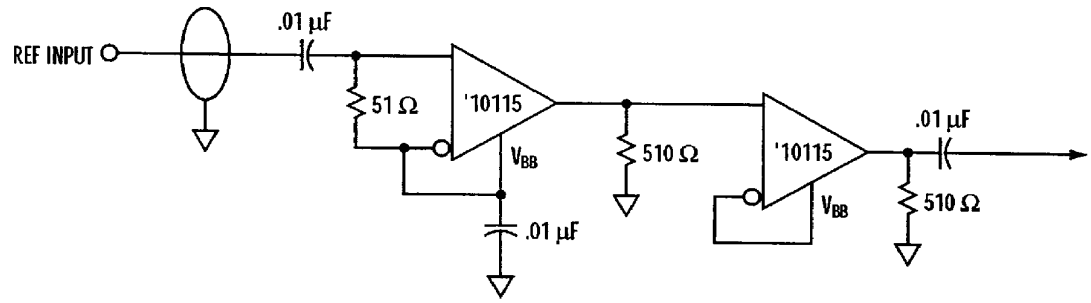
Although the device operates for sinusoidal VCO and reference input signals below 20 MHz, the sensitivity is reduced. There is a minimum edge-rate, which corresponds to about 200 mV in one half cycle of a 20 MHz sinusoid (25 ns). Therefore, the input frequency range extends down to DC with input waveforms whose amplitudes are at least 200 mVpp and rise/fall times are less than 25 ns. For larger amplitudes, the rise/fall times can be slower as long as they correspond to about 200 mV/25 ns.

This is easily understood considering that the frequency divider is an edge-triggered circuit, which depends on the transition of the clock signal through a certain level threshold (also known as a zero-crossing). There is an inherent amplitude-to-phase noise conversion process associated with edge-triggered circuits. Amplitude noise on the clock signal during this transition causes an uncertainty when the zero-crossing occurred, resulting in clock edge jitter. Random jitter on the clock edges converts to phase noise in the synthesizer. Furthermore, a given amount of AM noise will cause more edge jitter on a clock which has slower edges (rise/fall times). The longer it takes to pass through the zero-crossing threshold, the more influence the AM noise will have on the zero crossing.

For applications in which phase noise performance is critical, the circuit in Figure 19 is recommended for

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 19. Optional Reference Input Line Receiver Circuit (V_{CC} = + 5 V, V_{EE} = 0)



squaring up sinusoidal divider inputs below 20 MHz. (See #3 under References.)

PHASE/FREQUENCY DETECTOR CONSIDERATIONS

Ideally, the phase detector's behavior is such that as the skew between REF DIV and VCO DIV signals goes to zero, the output pulse should become smaller and smaller in duration, while maintaining its full 2 V amplitude. However, in real operation there would be some minimum pulse width below which the amplitude would start to decrease and create a non-linearity due to the pulse changing in two dimensions, amplitude and time. With the addition of the offset pulse, t_{RP}, to both PD conditions, this so called "dead zone" non-linearity is alleviated. This situation can be exploited to optimize the common-mode rejection of the phase detector output pulses as they are subtracted from one another in the differential active loop filter. By implementing a circuit that biases the phase detector outputs and introduces a tuneable phase error offset, as in Figure 20, the residual reference frequency energy that is seen as sideband spurs around the synthesizer's output frequency, can be significantly attenuated or even nulled out completely. One precaution that should be taken into account is to ensure that the phase detector output levels are well within the common-mode input voltage range for the particular op-amp used in the differential active loop filter. Since the phase detector outputs are positive-going pulses which start at a DC operating level of ≈ 2 V, the op-amp will have to permit a common-mode input voltage down to at least 2 VDC plus some added headroom for good measure. This condition may not be met if the op-amp is biased between V_{CC} and Ground, and may require connecting the minus supply pin to some negative V_{EE} voltage like - 5 VDC. The Q3236 phase detector outputs are designed to track each other over the operating temperature range, although enough phase offset to allow for mismatches in the temperature coefficients of the components in the differential active loop filter should be accommodated. If this approach is unacceptable, the Q3236 reference and VCO divider outputs may be used to drive an external phase/frequency detector.

Another important consideration is the use of pre-integrator filter capacitors as shown in Figure 13b. In normal operation between phase detector output pulses, the voltage on capacitor Cc charges up to the V_{OL} level (2.1 V). During an output pulse, the voltage then jumps to V_{OH} (4 V) and the capacitor starts to charge through $R_1/2$. The actual voltage at the output of the phase detector is the voltage divider of $R_1/2$ and the shunt bias resistor, R_T. These outputs are driven by ECL 2 V output drivers which maintain an approximately 2 V swing at the pin while driving the shunt bias resistor, R_T, followed by a series resistor, R_S, terminated by a shunt capacitor, C_S, as shown in the Phase Detector Output Termination Model, Figure 21. The minimum bias resistor, R_T, is 240 ohms, the minimum series resistance, R_S, is 100 ohms, and the maximum shunt capacitance, C_S, is 0.1 µF, in order to maintain the AC timing parameters as given in Table 7.

Figure 20. Phase Offset Adjust Circuit

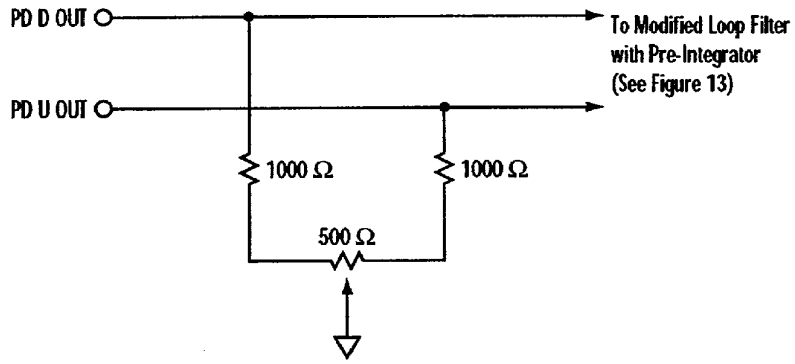
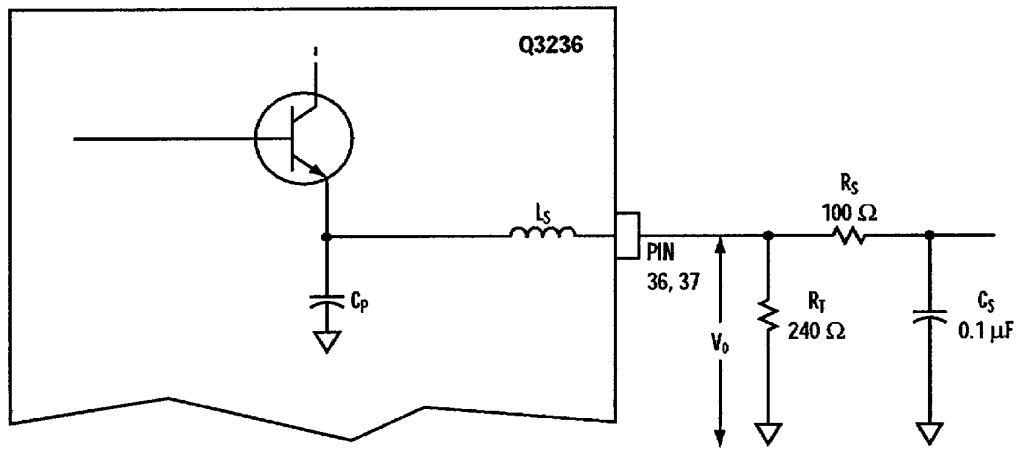


Figure 21. PD D, PD U Output Maximum Loading



PHASE NOISE PERFORMANCE CONSIDERATIONS

A general definition for the term "phase noise" is: the unwanted frequency or noise energy which modulates the output frequency (carrier) thereby determining the overall noise floor characteristic of the synthesizer's output. Respectively, phase noise is a small angle random phase modulation of the synthesized signal itself. More specifically, it is the single sideband power level relative to the level of the carrier, measured at specified offset frequencies from the carrier, in a 1 Hz bandwidth (dBc/Hz). Phase noise performance is a key criteria in qualifying a synthesizer's spectral purity. From a practical standpoint, the random PM process responsible for phase noise spreads the signal energy and therefore reduces the signal power from which useful information is carried.

In general, the phase noise contributions of synthesizer components are sufficiently well understood to be theoretically and suitably combined to predict the measured phase noise of (competently designed) synthesizers with adequate accuracy for engineering purposes. A key exception to this statement is the phase jitter contributions from the logic gates of the PLL's frequency divider and phase detector, but for now let's only consider the general case. The noise performance of the PLL within it's closed-loop bandwidth is that of the reference frequency source multiplied by $(N_{TOT})^2$, where $N_{TOT} = (N * P)/R$ is the total divisor of the loop including external prescaler (P) and reference frequency divisor (R), if used. (See *Using External Prescalers for Higher Frequency Translation* section for additional reference.) The noise response is then low pass filtered by the closed-loop transfer function at ≈ 6 dB/octave outside the loop bandwidth. That is to say, the output

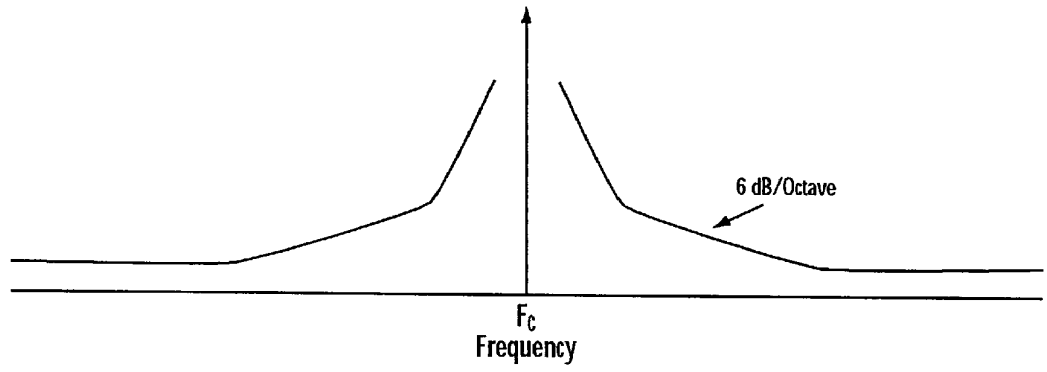
QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

phase noise within the loop bandwidth is the divided-down reference phase noise + 20 LOG (N * P) dB. Note: the VCO noise is not multiplied by $(N_{TOT})^2$ and is high pass filtered by the loop; the synthesizer's output phase noise beyond the closed-loop bandwidth is basically determined by the VCO's phase noise from this respective frequency offset. This typically results in only the VCO noise and PLL's noise floor being considered in determining the final phase noise of the synthesizer. For optimum phase noise performance, the loop bandwidth would be chosen where the noise level within the closed-loop bandwidth intersects the phase noise of the VCO. As a quick evaluation of where to place the loop bandwidth, this procedure is quite valid.

Phase noise may be specified either in the frequency or the time domain. Evaluating the stability of ultra-stable oscillators often requires sampling data in the time domain by taking fractional frequency measurements (Allan variance). Conversions between the time domain data and frequency domain data are possible but very tedious (see Chapter 2 of #6 in the *References* section). In evaluating a synthesizer's output noise performance, it becomes obvious that the phase noise density decreases with carrier offset frequency so most of the power, and hence jitter contribution, are from the components closest to the carrier frequency. The nominal predicted noise slope as you approach closer to the carrier changes from flat to 6 dB/octave, and even steeper to around 9 dB/octave as you move very close-in on the carrier, as depicted in Figure 22. This response is due to the aggregate effect of shot noise, thermal noise, and flicker noise (1/f) from the PLL's process technology and reference oscillator compounding together with varying frequency characteristics.

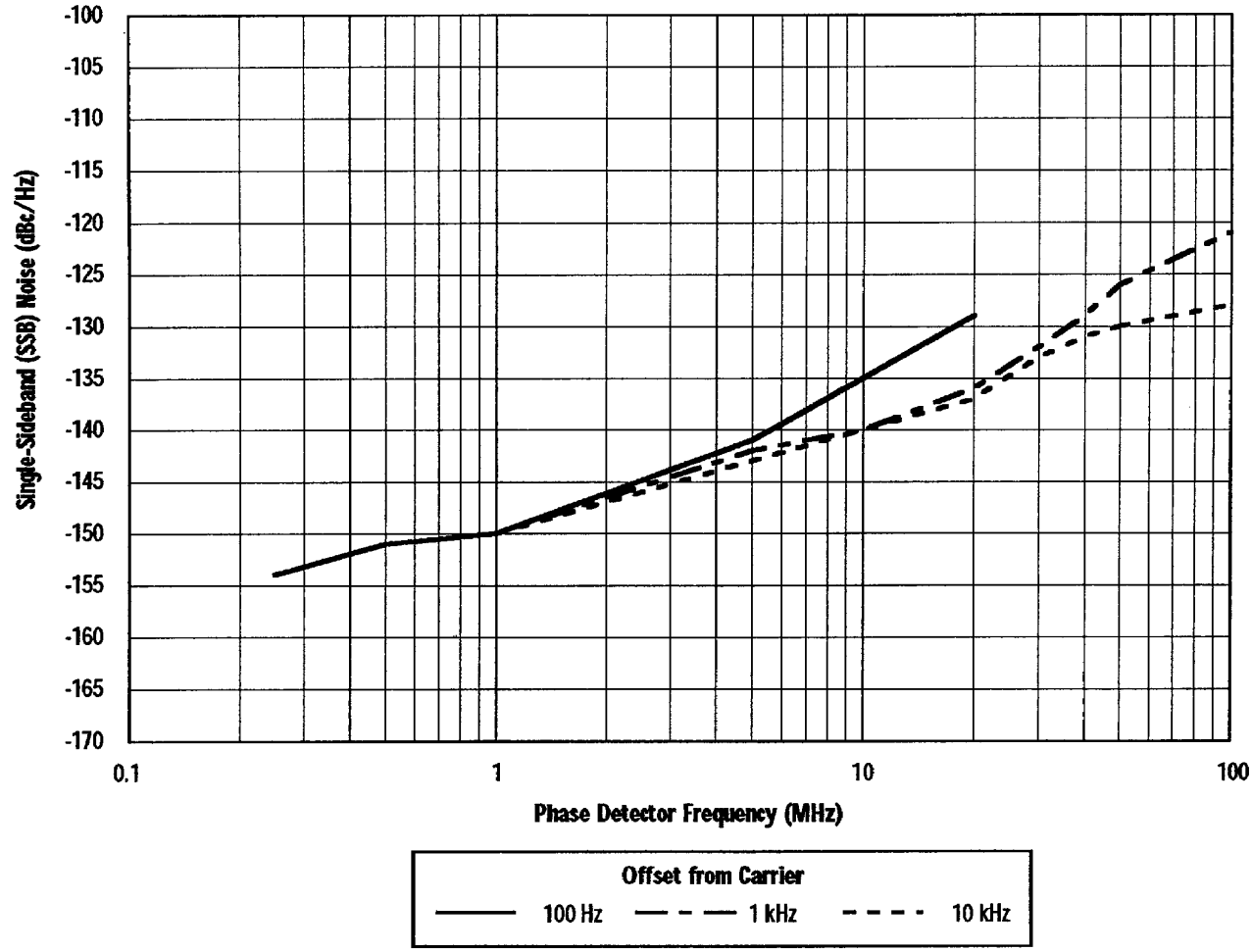
As will be shown, the phase noise performance of digital PLLs is inversely proportional to the operating frequency of it's digital phase/frequency detector (PFD). This noise would be independent of the PFD's operating frequency if the phase detector were ideal. In considering PLLs designed with a digital PFD, it is sometimes assumed that all noise contributions from the associated logic are less than those of the filter amplifier. This assumption is barely true for "good" digital circuitry operating at low to moderate frequencies and seriously in error at higher operating frequencies due to the phase jitter contribution of the PFD logic. Since the PFD contributes more noise than the filter amplifier at high operating frequencies, only empirical methods are recommended to validate performance and assess the magnitudes of these contributions. It is also known that the quality of the integration capacitor within the loop filter section can have an affect on the residual-FM noise at the synthesizer's output. This effect translates to degraded phase noise and settling time performance (see *Settling Time Considerations*section). This may be worth investigating if the same design varies in performance when different type caps or different manufacturer's caps are used in the loop filter circuit. It cannot be too strongly emphasized that careless engineering design, particularly in respect to power supply noise, inadequate shielding and earth loop coupling, can

Figure 22. Predicted Noise Spectrum around Output Carrier (F_C)



result in a measured performance many orders worse than expected. A graph showing the phase noise floor of the Q3236 vs. phase detector frequency is shown in Figure 23. These phase noise measurements were performed on Q3236-based synthesizer designs consisting of phase comparison frequencies of 0.25, 0.5, 1, 5, 10, 20, 50 and 100 MHz. In all cases, as the Q3236 feedback divider value was changed to adjust for a new PFD frequency, the loop bandwidth was compensated to maintain loop stability and kept deliberately extra-wide so the phase noise of the VCO would not be a contributing factor. A very low-noise reference frequency oscillator source was also used to ensure that the measured phase noise at the 100 Hz, 1 kHz and 10 kHz offsets for each phase comparison frequency was always dominated by the noise floor limit of the Q3236. This data was measured with an HP 3048A Phase Noise Test Set and the corresponding noise multiplication factor inside the loop bandwidth was subtracted out to determine the noise limits of the Q3236. As Figure 23 shows, the Q3236's phase noise floor is not independent of the operating frequency of the phase detector, i.e. it is not solely dependent on the divider ratio N_{TOT} as previously generalized. One interesting point that should be noted however, is the relatively shallow slope of the phase noise floor as a function of phase detector comparison frequency, for each of the given offset positions. Owing to a quite innovative design of it's PFD circuitry, the Q3236 also maintains a remarkable noise floor flatness very close-in on the carrier as compared to a typical digital PLL's performance. The Q3236's phase noise floor measured

Figure 23. Typical Q3236 Phase Noise as a Function of Phase Detector Frequency



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

at -154 dBc/Hz operating it's phase detector at 0.25 MHz, and degrades gradually to -122 dBc/Hz at 100 MHz operation.

SETTLING TIME CONSIDERATIONS

In many applications the channel switching speed is critical. This requires accurately knowing the time it takes the PLL synthesizer to settle for a given frequency step to within a certain tolerance. The Q3236's architecture is conducive to having relatively wide loop bandwidths which result in a faster switching speed, although the design criteria always means balancing tradeoffs between noise performance, spurious rejection and step size. Various techniques of measuring synthesizer switching time can be employed which generally involve the cancellation of two frequency carriers through a mixer/detector with some degree of frequency offset employed to relate the resulting beat note amplitude to the settling of a transient phase or frequency error at the filtered output. A more thorough treatment pertaining to "Synthesizer Switching Time" can be found in Chapters 2 and 5 of #2 in the *References* section.

$$F_{3dB} = F_n \left[2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}\right]^{1/2} \quad (35)$$

Equation 35 gives the relationship between the loop natural frequency and the closed-loop 3 dB frequency. The closed loop transfer function 3 dB point is a function of both the natural frequency F_n and the damping ζ and is always greater than 2ζ times the natural frequency. Table 19 is provided as a convenient chart for estimating the closed-loop 3 dB bandwidth as a function of F_n and varying ζ values.

The speed at which a PLL can sweep over a certain frequency range is mainly determined by the loop integrator. Thus, it is important to understand this mechanism when fast frequency changes are required.

In designing sythesizers with very critical settling time requirements, it is important to note that sometimes the non-ideal behavior of the loop integrator capacitors can cause significant settling time errors. This is more often than not related to a rather subtle phenomenon called "dielectric absorption", and its' effects on sensitive settling time requirements can be devastating. An example will help illustrate the effect: a synthesizer's settling time is being measured for a given step size with a procedure similar to the technique stated above. As the transient phase or frequency error output from the detector is being carefully observed and measured, an abrupt shift occurs which causes the normal decay period to become greatly exaggerated until the transient decay stabilizes once again, thereby increasing the net settling time result. This phenomenon is believed to be related to remnant polarization trapped on the dielectric interfaces within the capacitor which effectively allows the capacitor to recharge somewhat after discharging. From a circuit point of view, this extra polarization behaves like additional RCs kicking in spontaneously across the loop integrator capacitor which extend the voltage % vs. time characteristics.

Different type capacitors have dielectrics which vary widely in their susceptibility to dielectric absorption, with the lower-grade variety usually being the most unsuitable. When stringent settling time accuracy is demanded, the best approach is to choose your capacitors carefully, designing with higher-grade teflon or polystyrene types for instance, over mica or lower quality ceramic types.

Table 19. Closed-Loop Bandwidth vs. Natural Loop Frequency

ζ	F_{3dB}
0.6	1.92 F_n
0.7	2 F_n
0.8	2.18 F_n
0.9	2.33 F_n
1	2.48 F_n

USING EXTERNAL PRESCALERS FOR HIGHER FREQUENCY TRANSLATION

To use the Q3236 to generate a higher output frequency (or frequencies) than it's rated 2.0 GHz capability, external prescalers can be employed within the synthesizer's feedback loop to bring the VCO frequency into the Q3236's VCO input range. Prescalers are essentially frequency dividers that are implemented between the synthesized output carrier

and the programmable divider inputs of the PLL device for suitable processing to the phase/frequency detector. A block diagram illustrating a single-loop synthesizer topology incorporating an external prescaler is shown in Figure 24. The prescaler, which can operate at frequencies of several gigahertz or more, first reduces the output frequency by the factor P before it is applied to the programmable divider. When the loop is in lock,

$$F_{PD} = \frac{F_{OUT}}{P * N}$$

or

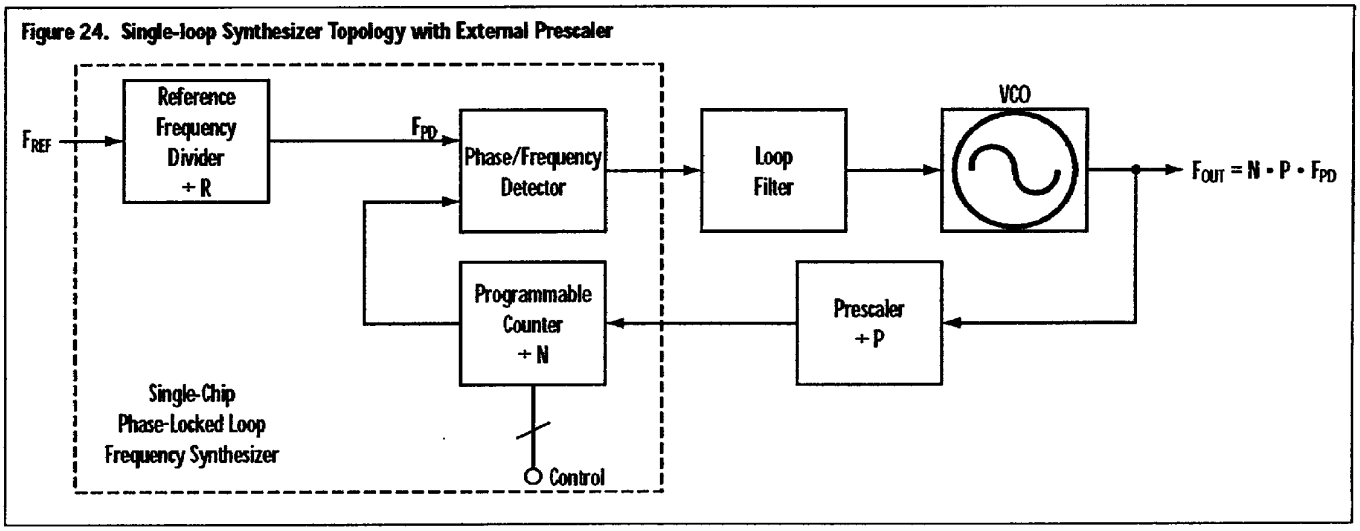
$$F_{OUT} = N * (P * F_{PD})$$

Although the use of a prescaler, which divides the VCO output frequency by P, allows the loop to operate with higher output frequencies, the frequency resolution of the PLL is limited to multiples of $P * F_{PD}$ rather than F_{PD}. In order to obtain the same resolution, the reference frequency must be decreased by the prescaler factor P. That is to say, the frequency step size of the synthesizer is as follows:

$$\text{Step Size} = P * F_{PD}$$

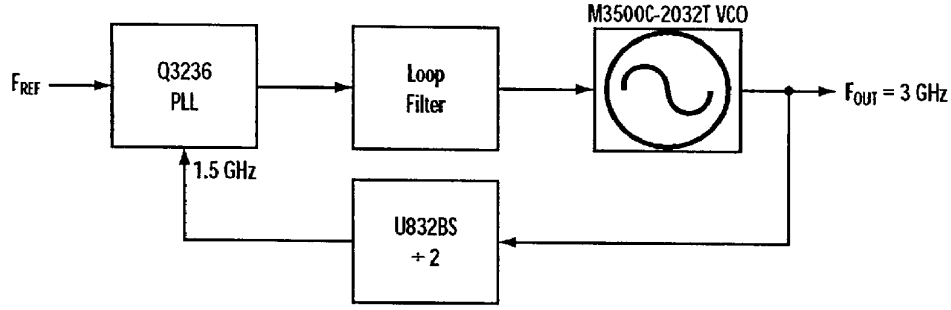
In loops where the total phase noise must be minimized, the closed-loop bandwidth is set equal to the intersection of the VCO noise and multiplied reference source noise. Additionally, if the output frequency step size is desired to be sustained at it's original resolution of F_{PD} by reducing the phase detector comparison frequency by the prescaler factor, P, then this will affect the ability to optimize the phase noise and/or switching speed that can be achieved. That is, the lower phase detect frequency will require a narrower loop bandwidth to get reasonable suppression of the reference sideband spurs around the output carrier; this will in turn mean slower switching speed due to the longer settling time of the loop. An example of a synthesizer designed to output up to 3.0 GHz with the Q3236 PLL and a divide-by-2 external prescaler in its feedback is given in Figure 25 with some basic circuit analysis to illustrate the above comments. With regards to designing with high-frequency prescalers, guarding against any parasitic oscillations means paying careful attention to true RF grounding, and RF coupling and decoupling to the device. Basically, the ground leads to the device should reach to the back plane of the circuit as soon as possible to achieve near-zero parasitic reactance at the common ground point. RF bypassing is done with a combination of capacitors positioned as close as possible to the V_{CC} terminal of the device. The coupling capacitors used for dc blocking at the input and output must provide a low impedance path over the desired operating range. Designers should note that with high division prescalers, the output frequency may be too low for the same value output capacitor as the input capacitor.

Figure 24. Single-loop Synthesizer Topology with External Prescaler



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Figure 25. Q3236 PLL with External Prescaler Example



Reference Frequency, F_{REF} (MHz)	N_{TOT}*	dB Degradation to Reference Phase Noise	Step Size ** (MHz) to F_{OUT} = 3 GHz
100	N/A***	–	–
50	60	36	Non-Continuous
25	120	42	Non-Continuous
20	150	44	Non-Continuous
10	300	50	20
5	600	56	10
2	1500	64	4
1	3000	70	2
0.6	5000	74	1.2

Notes:

* Assumes a reference frequency division ratio, R = 1.

** In the Q3236's Prescaler Mode, N_{MIN} = 90 for continuous frequency steps.

*** Q3236 cannot achieve feedback division ratio of 15 in Prescaler Mode.

Q3036 TO Q3236 MIGRATION

Table 20 is a quick reference guide for circuit design considerations that should be taken when migrating from the Q3036 PLL to the Q3236 PLL. If you are not sure if your particular design can be migrated to the Q3236, please contact QUALCOMM ASIC Products at (619) 658-5005 or fax your questions to (619) 658-1556.

Table 20. Quick Reference for Q3036 to Q3236 Migration

Circuit Design Considerations
Phase Detector Outputs Pins 36 and 37 are the opposite polarity (positive going pulses) compared to the Q3036. To account for this, the Q3236's phase/frequency detector has been modified to provide the same tuning characteristics to the synthesizer's feedback loop. This should be transparent to the customer's design of their synthesizer.
OP-AMP for Loop Filter The OP-AMP used in the differential loop filter needs to accommodate the common-mode input voltage range for the phase detector outputs since they pulse positive from a DC operating level of approximately 2 V. This condition may not be met if the OP-AMP is biased between V_{CC} and Ground. This may require connecting the OP-AMP's minus supply pin to a negative V_{EE} like -5 VDC.
Dead Zone A residual pulse of 3 nsec minimum has been internally added onto both phase detector outputs to eliminate any dead zone nonlinearity which causes output phase noise degradation. There is no requirement to offset the phase detector with a trimpot or use asymmetrical termination resistors on the outputs of the phase detector for mitigating this effect. The Q3236 has no output phase noise degradation, even with zero phase error detection.
Programming For programming control via the 8-bit Bus Mode, both the BUSMODE Input (pin 22) and the SMODE Input (pin 21) must be set to a logic "Low" state. This differentiates the digital processor interface from programming control in Serial Mode, which is not applicable to the Q3036. The FSELP Input (pin 18) should also be tied "Low" so that data can be updated without affecting the secondary register until the HOP WR Input (pin 26) is asserted. (Reference *Ping-Pong Mode* under the *Digital Processor Interface Modes* section.) Additionally, the external reference counter inputs R2 IN and R3 IN (pins 4 and 5) must be set to a logic "Low" state in order for the DATA BUS Inputs to program the correct values (specifically the corresponding DBUS0 and DBUS1 bits). The revised specifications for the 8-bit Bus Mode AC timing , located in this data book, should be reviewed to ensure adequate timing compatability with the existing interface.
Power Since the nominal power dissipation of the Q3236 is between 0.5 and 0.6 watts, there is no need for special thermal management techniques. Most designs will not require particular heatsinking or other heat dissipation methods to sustain the rated operating junction temperature of less than +150 °C.

*Migrating from Q3216 to Q3236 does not require circuit design changes.

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

Q0420 PLO EVALUATION SYSTEM

The Q0420 Phase-Locked Oscillator (PLO) Evaluation System is a complete evaluation board designed on a compact 5" x 7.5" printed circuit card for the Q3236 PLL. The actual evaluation platform includes a fixed demonstration as well as a custom prototyping design. A block diagram is shown in Figure 26. The Q0420 demonstration platform consists of a phase-locked oscillator system which generates output frequencies from 2 GHz to 3 GHz with a minimum step size of 5 MHz over the full output range (÷2 prescaler included on-board). The custom prototyping option allows the designer to rapidly configure a custom synthesizer by adding the VCO, loop filter and reference suppression filter components to the alternative circuit sections of the board. The user can easily select between the demonstration platform and the custom prototyping design via on-board jumper options. Additional input and output connectors are also provided to easily support the use of off-board VCOs and prescalers to quickly evaluate the performance tradeoffs between alternative components.

The Q0420 can be computer-controlled for remote operation, or alternatively controlled through the on-board frequency control switches for stand-alone operation. The menu-driven software will automatically compute all desired frequency programming and can exercise the following Q3236 modes of operation:

- 16-bit Direct Parallel Control
- 8-bit Data Bus Control
- 20-bit Serial Control
- 8-bit Data Ping-Pong Control
- 20-bit Serial Ping-Pong Control

Stand-alone operation with the Q0420 requires only the + 15 VDC power supply voltage, but can only utilize the Q3236's direct parallel interface for frequency programming using on-board DIP switches.

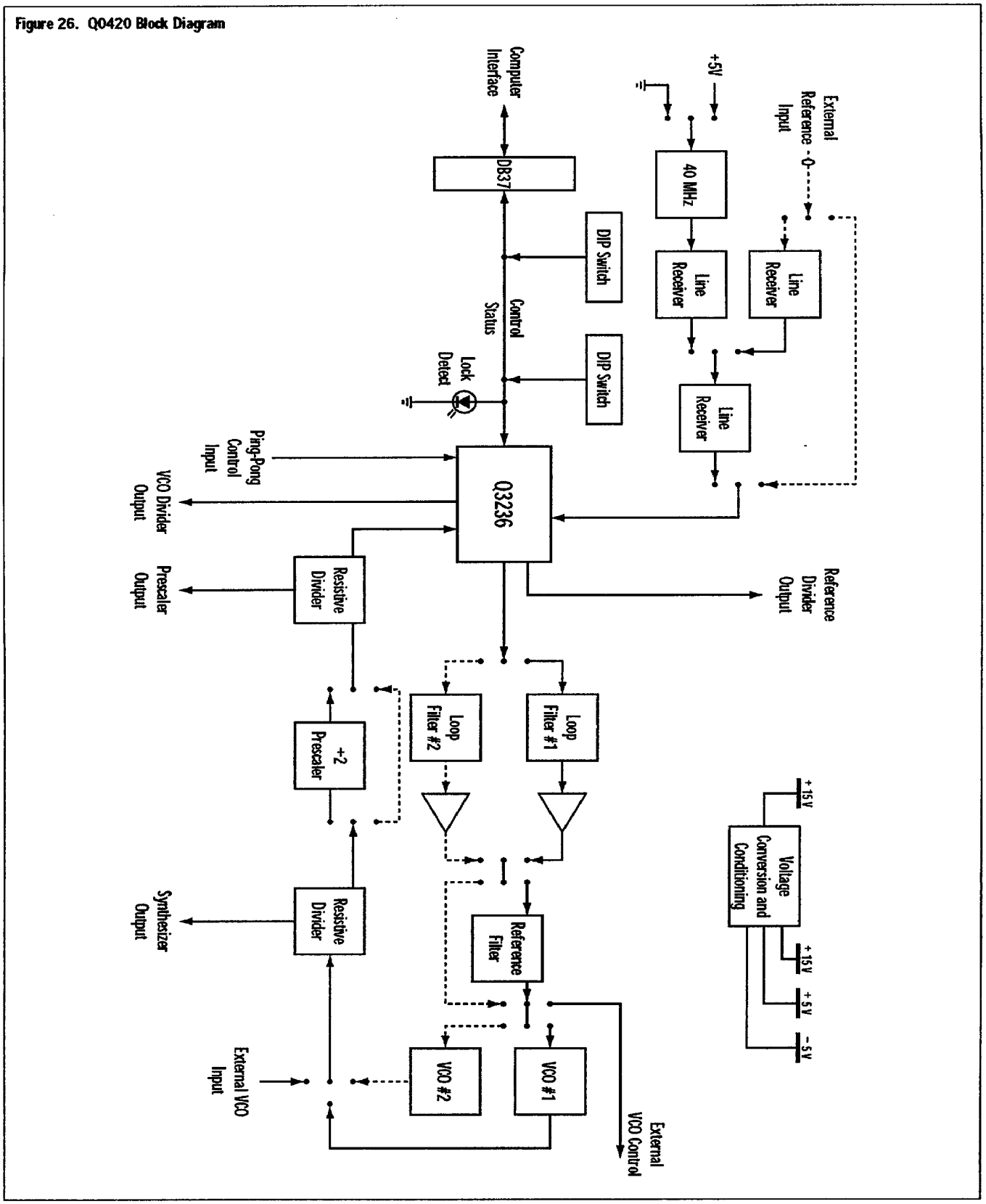
The User's Guide provides all the information required to operate the Q0420 and exercise all built-in functionality of the Q3236. Appendices are also provided which contain the schematics, layout and complete parts list. The Q0420 consists of a PLL Evaluation Board, Control Software, Control Cable, Digital I/O (DIO) Board and DIO Board Installation Software. In order to operate the PLL Evaluation Board, the DIO Board needs to be installed in a PC. The DIO Driver Software and the Q0420 Control Software need to be installed on the hard drive of the PC. The Q0420 PLL Evaluation System requires the following computer hardware as a minimum to operate in Remote Mode:

- PC 80386 or Better
- 4 MB RAM
- Math Co-processor
- Hard Drive
- Mouse
- Windows™ Version 3.1 or Windows '95™
- SVGA Video Card (1024 X 768 Resolution, Small Fonts)

Note: Windows™ is a trademark of Microsoft ® Corporation

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

Figure 26. Q0420 Block Diagram

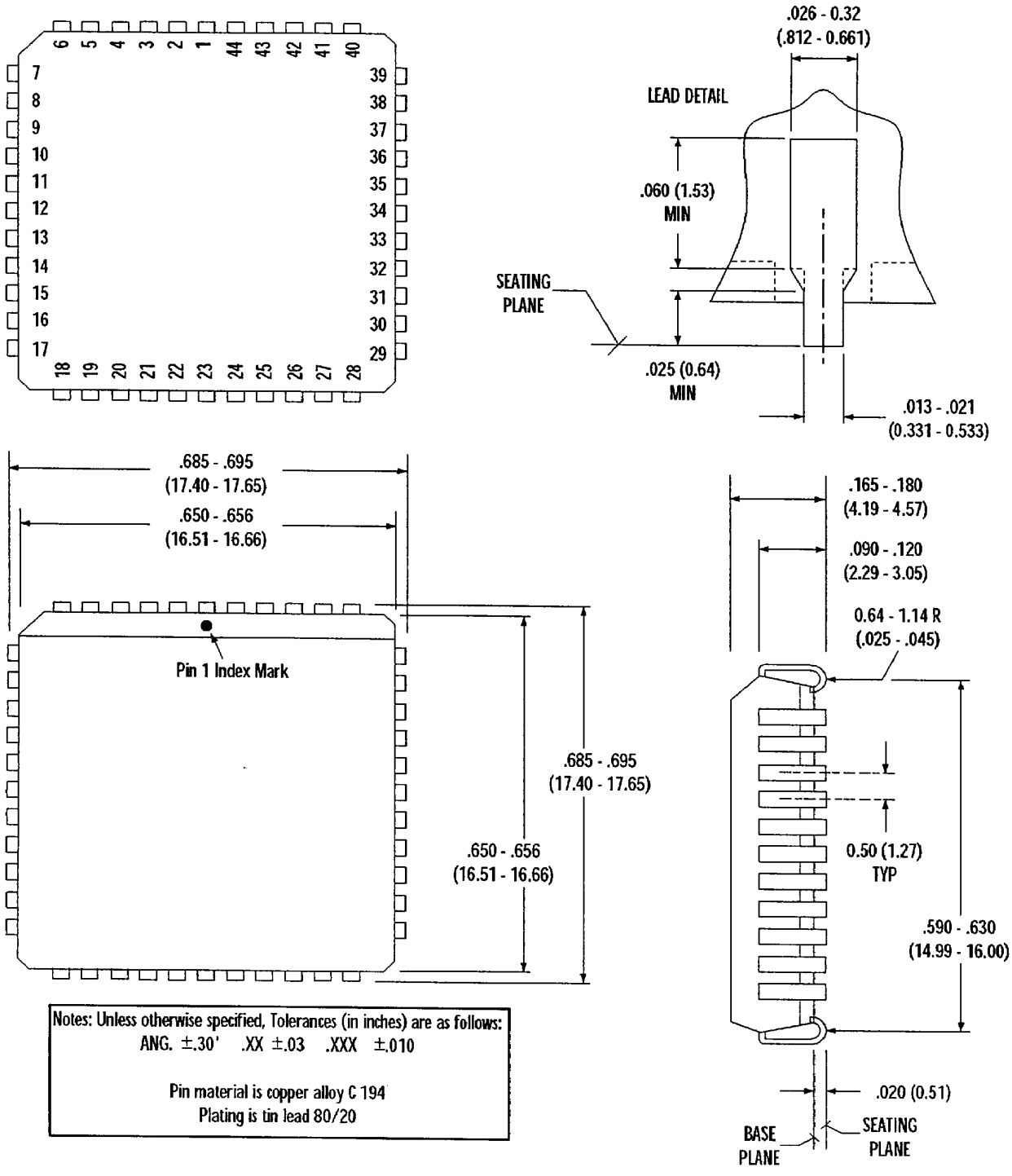


QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

PLCC PACKAGING

The Q3236I-20N is packaged in the 44-pin plastic leaded chip carrier (PLCC) shown in Figure 27. The dimensions are given in inches and (mm).

Figure 27. Q3236I-20N 44-pin PLCC Packaging



QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

RECOMMENDED SOCKETS

We recommend the low profile surface mount 44-pin PLCC socket from Methode Electronic, Inc. P/N 213-044-602. This socket is available from QUALCOMM. Another recommended socket is the AMP P/N 821575-1 thru-hole 44-pin carrier socket.

REFERENCES

1.) F. M. Gardner, PhD, Phaselock Techniques, Second Edition, John Wiley & Sons, Inc., New York, NY 1979

2.) V. Manassewitsch, *Frequency Synthesizers* , Theory and Design, John Wiley & Sons, Inc., New York, NY, 1987

3.) *MECL Device Data*,Motorola databook, 1989

4.) P. Gray, R. Paul, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, Second Edition, John Wiley & Sons, Inc., New York, NY, 1977, 1984

5.) Anatol I. Zverev, *Handbook of Filter Synthesis* , John Wiley & Sons, Inc., New York, NY , 1967

6.) Rohde, Ulrich L., *Digital PLL Frequency Synthesizers* , Prentice-Hall, Inc., 1983

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA

Synthesizer Products Data Book, 80-24127-1 A, 8/97
Data Subject to Change Without Notice

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556