where g_m = transconductance at operating E_c, and g_{m0} = transconductance at E_c = 0 V.

These characteristics give the solid-state device a true square-law characteristic and, because of this, very low harmonic distortion. Higher-than-second-order harmonics are virtually nonexistent.

In contrast, the vacuum tubes have a "three-halves-power" characteristic, and can generate substantially higher-order harmonics and intermodulation products. Interestingly enough, bipolar transistors have even more harmonics than the tube.

The Fetron's very high output impedance, analogous to a vacuum tube's plate resistance r_p, maximizes the voltage gain for a given load R_L. The voltage gain of an amplifier (see Fig. 4) can be expressed as:

$$A_v = \frac{\mu R_L}{r_p + R_L} = \frac{g_m r_p R_L}{r_p + R_L}$$

where $\mu = g_m r_p$ (μ is the tube amplification factor). But since r_p is much higher than R_L, the equation is simply

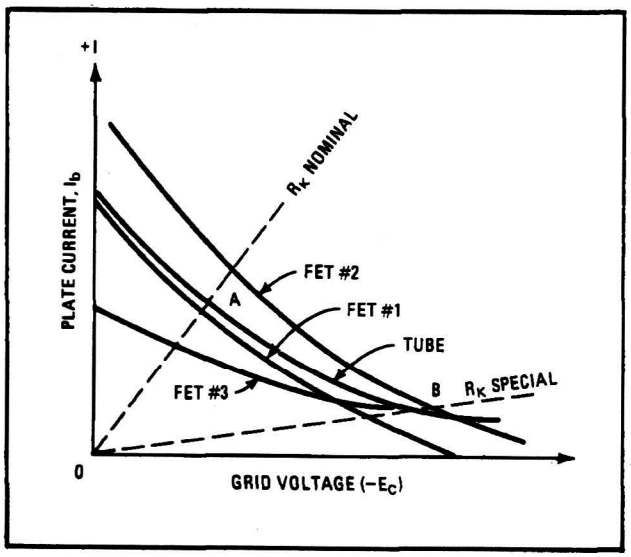
$$A_v \approx g_m R_L$$

At lower frequencies—less than a few megahertz—the simplified equation is more than 99% accurate for a Fetron.

Fitting the FETs

Versions of the device can be made for both amplifier and oscillator service. (The package for oscillator applications may include a small resistor or RC network for feedback and neutralization.) In practice, many FET characteristics are available, and single or JFET cascode pairs can be made to match the tube's current-voltage curves as shown in Fig. 5.

Although several approaches are available, about 80% of the general-purpose applications considered to date are satisfied by the simple FET #1 approach. This type of JFET is chosen if the application is unknown or if the device must operate around some nominal operating point A (in which case, the JFET curve closely approximates the tube curve over most of the control voltage range). In large-volume applications, where the exact operating point is known, FET #1 can be selected at the factory to coincide exactly with a point anywhere near A on the tube's curve.



5. Choosing a Fetron. Several Fetron types are available to match a tube's application. If the tube operates around a fixed point, such as A, a JFET, such as FET #1, is chosen. To match a tube that operates beyond a FET's cutoff, FET #2 or FET #3 is chosen: FET #2 for high current before cutoff, FET #3 for low, flat current.

An operating point such as B beyond the normal FET cutoff can be matched by FET #2 or FET #3. FET #2 would provide a higher current for the same control voltage, so it passes through B before cutoff. FET #3 would have to be specially tailored for low, flat current characteristics, or for a narrow range of operation beyond the normal FET's cutoff. It would be a lower-transconductance, higher-cutoff JFET.

In simulating a tube, the dynamic characteristics as well as the operating point must be considered. Depending on the particular application, special attention must be given to transconductance, phase shift, phase margin, operating range, and neutralization requirements.

For amplifier operation, neutralization and operating range are the principle concerns. In most tube circuits, neutralization is used to nullify the effects of feedback capacitance during higher-frequency operation.

When used as an oscillator, the Fetron must provide for positive feedback between the output and input. An internal RC network within the device headers (Fig. 6) acts as a screen grid which is connected to the plate to assure direct replacement.

In Fetrons designed for amplifier operations, how-

Building the high-voltage JFETs

JFETs with breakdown voltages over 300 volts can be made by standard planar processing. But to achieve this high voltage, it is essential to attain the maximum breakdown field for silicon, about 30 volts per micron. Also critical is the epitaxial layer thickness and resistivity.

The channel is formed by the n-type epitaxial layer, which has a resistivity exceeding 5 ohm-cm. Since the channel region where pinchoff occurs is directly under the gate, doping levels in that region must be precisely controlled to limit spreading of the depletion region into the channel. The channel height depends on what final pinchoff voltage is desired.

The voltage from gate to source, V_{GS}, may be as large as –50 V. This V_{DG} value is required to enable the drain to withstand a voltage of up to 400 V. However, this high drain-to-gate voltage can only be achieved if the spacing of the gate, source and drain is held to very close tolerances.

Another difficulty is the need to shape the diffusions so as to minimize any surface field concentrations at the chip. Breakdown should occur in the bulk silicon, not at the surface. The substrate resistivity must be fairly high for good control of depletion spreading, as well. Otherwise, the channel might get pinched off with a very small charge in V_{GS}. At high operating voltages, V_{DS} can vary widely without any change in signal voltage, due to normal supply tolerances.